Unidirectional High-Frequency-Link DC to Three-Phase AC Conversion: Topology, Modulation and Converter Design

A Thesis
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by

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Dedication

This thesis is dedicated to my parents,
uncle and aunt for their endless love,
support and encouragement
to follow my dreams.

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Abstract

In recent years, stringent restrictions on greenhouse gas emission due to the present global warming scenario is driving governments and power utilities worldwide behind electricity generation using renewable energy sources. Conventionally, for grid integration of a large scale photovoltaic (PV) system, a three-phase voltage source inverter followed by a line frequency transformer (LFT) is used. The inverter generates line frequency (50/60 Hz) AC from the DC output of PV. The LFT provides galvanic isolation and thus reduces the circulation of leakage current, and ensures safety. Few limitations with the conventional system are a) huge volume as the LFT is bulky, (b) quite expensive due to large amount of iron and copper used in LFT and (c) the inverter is hard switched. The converter topologies with high-frequency galvanic isolation have attractive features like high power density and are less expensive. Hence these converters are promising alternatives to the conventional solution.

The three-phase inverter topologies with high-frequency transformer are generally of two types- a) multi-stage and b) single-stage. In multi-stage, interstage DC link is voltage stiff as filter capacitor is used. In a single-stage solution, the intermediate DC link is pulsating as filter capacitor is avoided to improve reliability. Though these converters have high power density, they employ large number of active switches on both the sides of the transformer to process power and hence have relatively lower efficiency compared to the conventional solution. The active switch count can be reduced in case of unidirectional applications like grid integration of PV, fuel-cell where the active power flows from DC source to AC grid. The converter efficiency can be further improved by reducing the switching loss. In this work, we have investigated four new unidirectional single-stage three-phase inverter topologies with low or negligible switching loss.

To reduce the switching loss, the active switches of the introduced topologies are either line frequency switched or high-frequency soft-switched. The soft-switching is achieved without additional snubber circuit. The pulse width modulation is implemented on the input DC side converters which are soft-switched. The active switches of the grid interfaced converter are low frequency switched and thus enabling the use of high voltage blocking inherently slow semiconductor devices for direct medium voltage grid integration. The topologies are gradually improved to achieve soft-switching of the DC side converters throughout the line cycle. The conditions on dead time to ensure soft-switching are derived through detailed circuit analysis. The operations of these topologies are experimentally verified on hardware prototypes with power range 2-6kW. Out of four introduced topologies, three topologies can support only unity power factor operation. An additional shunt compensator is needed for any reactive power support. The fourth topology can support up to $\pm$ 0.866 power factor operation though it

has relatively higher conduction loss. The performances of the introduced topologies are compared with multi-stage and conventional solutions. Though the new topologies have relatively higher switch counts, the converter power losses, filter requirements are comparable with the conventional solution with line frequency transformer, and have high power density.

Contents

List of Tables

List of Figures

Acronyms

ac or AC	: Alternating current
dc or DC	: Direct current
PV	: Photovoltaics
PEC	: Power electronic converter
MPPT	: Maximum power point tracking
THD	: Total harmonic distortion
VSI	: Voltage source inverter
LFT	: Line frequency transformer
HFT	: High frequency transformer
HFL	: High frequency link
PMSG	: Permanent magnet synchronous generator
PSFB	: Phase-shifted full bride
ESR	: Equivalent series resistance
CHFL	: Cyclo-converter type high frequency link
RHFL	: Rectifier type high frequency link
HFAC	: High frequency AC
LFAC	: Line frequency AC
DSC	: DC side converter
PWM	: Pulse width modulation
ZVS	: Zero voltage switching
ZCS	: Zero current switching
NPC	: Neutral point clamp
THD	: Total harmonic distortion
ASC	: AC side converter
DT	: Dead time
IGBT	: Insulated gate bipolar transistor
THD_V	: Voltage total harmonic distortion
THD_I	: Current total harmonic distortion
SoC	: System on chip
PF	: Power factor
UPF	: Unity power factor

Nomenclature

1ϕ	: Single phase
3ϕ	: Three phase
f_s	: Switching frequency of the DSC
T_s	: Switching period of the DSC
$m(t)$	: Modulation signal of the 1ϕ inverter
M	: Modulation index
ω_o	: Angular frequency of the line cycle quantities
T_o	: Period of the line cycle quantities
θ	: Time angle of the line cycle quantities
V_{dc}	: Input DC bus voltage
$t_0 - t_{10}$	: Instances over a switching period of the DSC
n	: Transformer primary to secondary turns ratio
v_{PQ}	: Pulsating intermediate DC link voltage of the 1ϕ inverter
i_a, i_b, i_c	: Line currents of the converter
i_{pa}, i_{pb}, i_{pc}	: Transformer primary currents of the topology 1-3
I_{pk}	: Peak value of the line currents
$v_{m_1m_2}$	: Pole voltage of the 1ϕ inverter
V_{pk}	: Peak value of the average pole voltage
L_f	: Line filter inductor
X_f	: Line filter impedance
$m_a(t), m_b(t), m_c(t)$	: Modulation signals of the 3ϕ inverter
v_{aN}, v_{bN}, v_{cN}	: Pole voltages of the 3ϕ inverter w.r.t transformer neutral
v_{an_t}, v_{bn_t}, v_{cn_t}	: Pole voltages of the 3ϕ inverter w.r.t load neutral
v_{ga}, v_{gb}, v_{gc}	: Grid voltage or voltage across the load
v_{po}, v_{oq}	: Pulsating DC link voltages of topology 4
V_{gpk}	: Peak value of the grid voltage
C_s	: Capacitance across a device of the DSC
L_{lk}	: Leakage and additional series inductance seen from primary of the HFT
I_a, I_b, I_c	: Line current magnitudes over a switching cycle
ω_p	: L_{lk}, C_s resonant frequency
I_{RMS}	: RMS current through a semiconductor
I_{avg}	: Average current through a semiconductor

$I_{RMS,p}$: RMS current of the transformer primary
$I_{RMS,s}$: RMS current of the transformer secondary
R_p : Transformer primary winding resistance
R_s : Transformer secondary winding resistance
P_C : Conduction loss in a semiconductor
P_S : Switching loss in a semiconductor
$P_{cu,HFT}$: Copper loss in HFT
V_{CE} : Device collector-emitter drop during conduction
R_{CE} : On state resistance of the device during conduction
V_D : Diode drop during conduction
R_D : On state resistance of the diode during conduction
E_{ON_R}, E_{OFF_R} : Turn-on and Turn-off energy loss in an IGBT at rated condition (V_{CC}, I_C)
C_f : Input capacitive filter
$\tilde{i}$: RMS of the current ripple
$\tilde{v}$: RMS of the voltage ripple
μ, λ : Percentage of voltage and current ripple w.r.t fundamental component
Z_b, Y_b : Base impedance and admittance
$Z_{p.u}, Y_{p.u}$: Per unit impedance and admittance
$i_{dc,rms}$: RMS of the DC link current
$i_{dc,avg}$: DC component of the DC link current
$v_{an_t,rms}$: RMS of the pole voltage, v_{an_t}
$v_{an_t,rms1}$: RMS of the fundamental component of the pole voltage, v_{an_t}
ψ : Phase angle between grid voltage and average pole voltage
P : Three phase power output
$P_{1\phi}$: Single phase power output
A_c : Transformer core area
A_w : Transformer window area
K_w : Window fill factor
B_{max} : Peak flux density
J : Conductor current density

Chapter 1

Introduction

1.1 Background and Motivation

The modern human civilization is facing a great challenge of climate change due to global warming. To limit the increase in global average temperature to 1.5° C above the pre-industrial era levels as per the Paris Agreement on April, 2016 under the United Nations Framework Convention on Climate Change (UNFCCC) [2], the nations worldwide are taking effective steps to cut down the emission of greenhouse gases by increasing the energy generations from renewable sources and by improving the energy conversion efficiency. By the end of 2017, renewable energy based power generation capacity has reached 2179 GW worldwide with a yearly growth of around 8.3% [3]. Out of which the solar photovoltaics (PV) is 390.6 GW and has seen a growth rate 32% in 2017. With steeply declining cost curve, the solar and wind power are becoming competitive on price with the fossil fuel based conventionally generated power [4].

Power electronic converters (PEC) are the integral parts of a renewable energy based power generation system to process, conversion and control of the harvested power [5,6]. For example, DC output of photovoltaic (PV) cells needs to be converted to AC through a PEC before connecting to the utility grid. Additionally, the control of the PEC ensures obtaining maximum power output from the PV cell by using maximum power point tracking (MPPT) algorithm. The PEC maintains the power quality particularly voltage magnitude, frequency, current THD to conform with the grid regulation.

Conventionally, for grid integration of a large scale PV system, a three phase voltage source inverter (VSI) followed by a line frequency transformer (LFT) is used [7]. The VSI generates the controllable magnitude and line frequency (50/60 Hz) AC from the DC output of the PV. The LFT provides galvanic isolation and thus reduces circulation of leakage or common mode current, and ensures safety [8, 9]. The major problem with the conventional system is that the VSI is hard switched which affects the converter efficiency and the LFT is bulky, heavy and quite expensive due to large amount of iron and copper used. The LFT requires a significant amount of real estate of the complete system. The transformer size (product of the window and core area) is inversely proportional to the frequency of operation [10]. A high frequency transformer (HFT), handling same amount of power, is much smaller in size hence less expensive.

The converter system with such high frequency isolation has some attractive features like high power density, low cost etc, hence are promising alternatives to the conventional solution.

This has influenced the researchers of power electronics community to come up with different high frequency link (HFL) inverter topologies and modulation strategies to provide compact, efficient, low cost converter solution.

1.2 Grid integration of photovoltaics: State-of-the-art

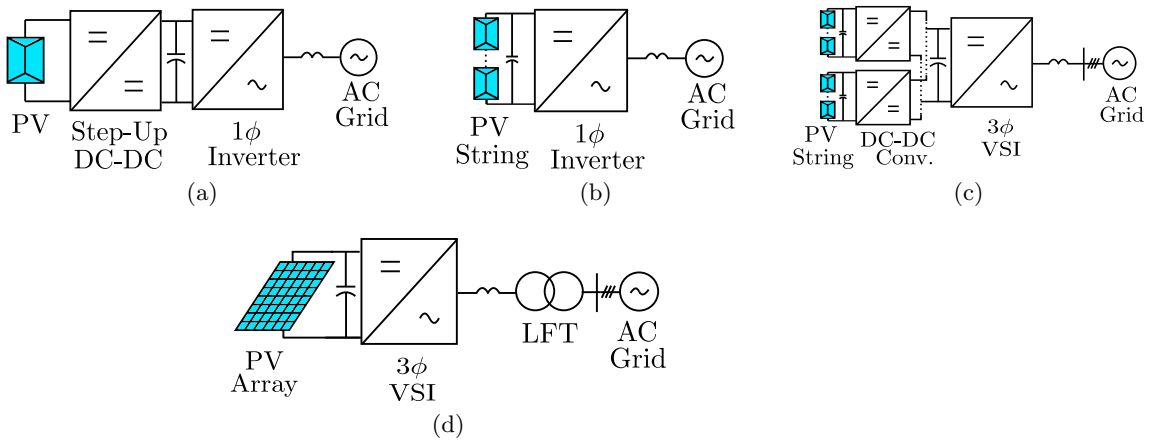


Figure 1.1: Inverters for grid integration of PV. (a) Micro-inverter, (b) String inverter, (c) Multi-string inverter and (d) Central inverter [1].

Depending on applications, the grid connected PV system can be of few watts to hundreds of kilo-watts. Based on power levels, inverters in the PV systems are classified in four major groups (Fig. 1.1)- a) micro-inverter, (b) string inverter, (c) multi-string inverter and (d) central inverter [1].

Micro-inverter

Micro-inverters are employed for small scale roof-top solar applications with power rating upto 500 W. Due to small size, the PEC is directly attached to the PV module. The output of the PV module is around 30-40 V DC. As seen in Fig. 1.1a, DC output of the PV module is fed to a step-up DC-DC converter and output of which is connected to the single phase (1ϕ) AC grid through a 1ϕ VSI. These converters have efficiency around 96%. But such system has highest MPPT accuracy due to the dedicated converter connected to each PV module. Siemens SMIINV215R60 is an commercially available micro inverter system [11].

String inverter

In small- to medium scale PV systems like residential rooftop PV plants, the string inverters are employed. Multiple PV modules are connected in series to form a PV string which gives a DC output of 400-600V. A single phase VSI connects the PV to the single phase utility grid (Fig.1.1b). Typical power rating of such systems is few KWs (<10kW). Many a times a DC-DC stage is introduced before the VSI which decouples the MPPT control from the grid side

control. Such a system has typical efficiency approximately 97%. ABB PVS 300 is an example of commercially available string inverter system [12].

Multi-string inverter

In medium to large scale PV application multi-string configuration is adopted. Small PV strings are connected through DC-DC converters to a common DC bus as shown in Fig. 1.1c. A three phase (3ϕ) VSI is employed to connect DC bus to the AC grid. Such a system has improved MPPT performance and has typical efficiency 97.5%. Typical power rating of such a system is few hundreds of KW and can go upto 500 KW. SATCON Solstice is a commercially available multi-string inverter solution [13].

Central inverter

Central inverters are common in utility scale PV power plants. Several PV strings are connected in parallel through reverse blocking diodes to form PV arrays. Output of the PV array is 500-800V DC. The PV array is connected to the 400V AC grid through a 3ϕ VSI followed by a LFT as shown in Fig. 1.1d. The LFT provides isolation to reduce leakage current circulation. Typical power rating of such system goes upto 800kW with converter efficiency 98%. Siemens SINVERT PVS630 is a commercially available central inverter solution [14].

In our work, the converter topologies are investigated for the central inverter system. Hence the target application of this work is grid integration of utility scale PV plants. The state-of-the-art central inverter system has following limitations.

Limitations of Central inverter system

- The VSI is hard-switched which impacts the efficiency of the system.
- The LFT is one of the largest component of the overall system which occupies significant amount of real-estate.
- The LFT is also one of the expensive component as it needs lots of iron and copper to manufacture.

Though we are mainly focusing on central inverter of PV application but similar system structures are also seen in case of grid integration of fuel cell [15] or PMSG based wind power [16]. Fig. 1.2a shows a scheme of commercially available fuel cell based inverter (ES5-AA2AAA,

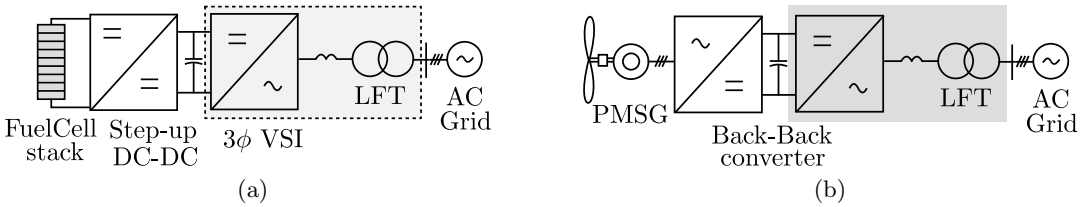


Figure 1.2: Grid integration of (a) fuel-cell, (b) PMSG based wind system.

Bloomenergy) of power rating 100-200kW which has a 3ϕ VSI followed by LFT. ABB PCS 6000 is a inverter system to connect PMSG based wind to grid as shown in Fig. 1.2b. These systems also have similar limitations as seen in case of the central inverter. The proposed topologies in this work can be an alternative solutions to these conventional inverter systems.

1.3 High-frequency-link based solutions

To eliminate the LFT of the conventional 3ϕ inverter system and also to provide galvanic isolation between input and output stage, HFL based converter solutions are widely discussed in literature. In a HFL inverter system high frequency transformers provide required galvanic isolation. As the operating frequency of these transformers are high (mostly switching frequency of the converter) compared to the line frequency outputs, the size (which can be indicated by the area product of window and core) of the transformer is one order of magnitude lower than the similarly rated LFT which results in compact-high power density, low cost converter solution. Several HFL inverter topologies and their modulation strategies are discussed in literature. These topologies can be broadly classified in two major categories - (a) multi-stage high frequency link inverter solution and (b) single-stage high frequency link inverter solution.

1.3.1 Multi-stage high frequency link inverter

Multi-stage inverters are most widely used HFL inverter solution [17–19]. Fig. 1.3 shows the schematic of a multi-stage HFL inverter. As seen in the figure, the converter has two stages.

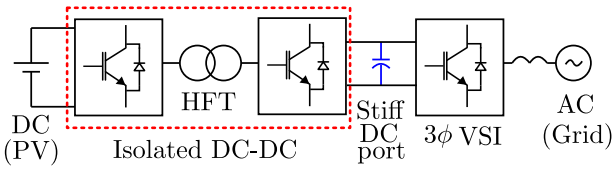


Figure 1.3: Multi-stage HFL inverter

First an isolated DC-DC converter provides the required galvanic isolation using a HFT. The DC-DC converter can be a most popular phase-shifted full bride (PSFB) or a dual active bride where the active switches can be soft-switched. The output of the DC-DC converter is passed through a capacitive filter which bypasses the high frequency ripple and creates a stiff DC port. A 3ϕ VSI inverter is connected to the stiff DC port which generates required magnitude line frequency AC. Here the control of the VSI and the DC-DC converter can be decoupled. This topology has few limitations as follows.

Limitations of the multi-stage topology

- Like the conventional inverter system, the 3ϕ VSI is hard-switched which affects the converter efficiency.
- Such a scheme requires additional filtering to make interstage stiff DC link. Hence, additional components like inductors and capacitors are used. Which increases converter

component count and has impact on power density.

- To have stiff interstage DC link, electrolytic capacitors are employed in most applications. Due to high ESR, the electrolytic capacitors have long term reliability issue which affects the long term performance of the converter.

1.3.2 Single-stage high frequency link inverter

The single stage HFL inverter does not use any interstage DC link filter [20–25]. The converters in the secondary side of the HFT are controlled in synchronized with the primary side converter hence such topologies are called single-stage. Based on the secondary side converter structure the single stage topologies are broadly classified into two categories- a) cyclo converter type (CHFL) and (b) rectifier type (RHFL).

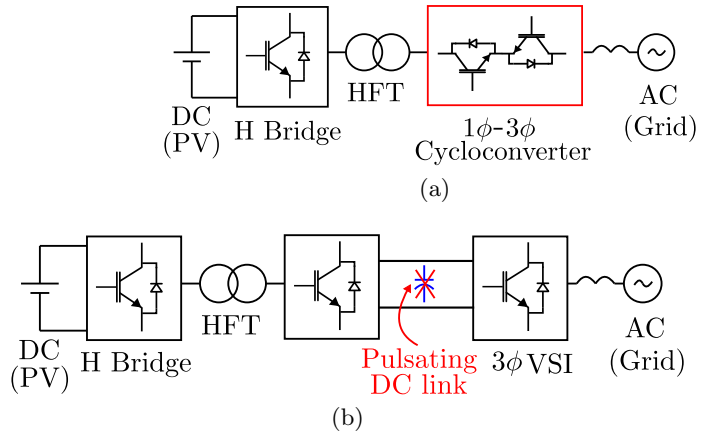


Figure 1.4: Single-stage high frequency link inverter. (a) Cyclo-converter type (CHFL), (b) Rectifier type (RHFL).

Cyclo-converter type HFL (CHFL) inverter

In a CHFL topology [20,21], a H-bridge is employed in the DC side of the converter to generate high frequency AC (HFAC) from the input DC and is fed to a HFT. In the secondary of the HFT a 1ϕ-3ϕ cyclo-converter is employed to generate line frequency AC (LFAC) output from the HFAC. Fig. 1.4a shows the CHFL topology. As the cyclo-converter is used to directly convert HFAC to LFAC, intermediate DC link is not present and hence no need of additional filtering. In [22], three $1\phi-1\phi$ cyclo-converters along with three HFTs are used. The limitation with a CHFL topology is that it employs four quadrant AC switches which many a times are not commercially available and have implementation and control complexities.

Rectifier type HFL (RHFL) inverter

The operation of the cyclo-converter in a CHFL topology can be viewed in two parts-first rectification and then inversion [26]. The concept is used in a RHFL topology [23–25] as shown in Fig. 1.4b. In the secondary of the HFT an active rectifier followed by a 3ϕ VSI are used.

The rectifier output is pulsating as it is not filtered. The control of the rectifier and the VSI are synchronised. Here all the switches are two quadrant.

The converters discussed so-far have the ability of bidirectional power flow. But there are quite a few applications like grid integration of PV, fuel-cell or PMSG based wind generator, where the power flow is unidirectional i.e. from input to output side. In such applications, the bidirectional converters with so many active switches and associated control circuits are redundant. For such applications, unidirectional RHFL topologies can be used.

1.4 Unidirectional RHFL DC-3ϕ AC converters

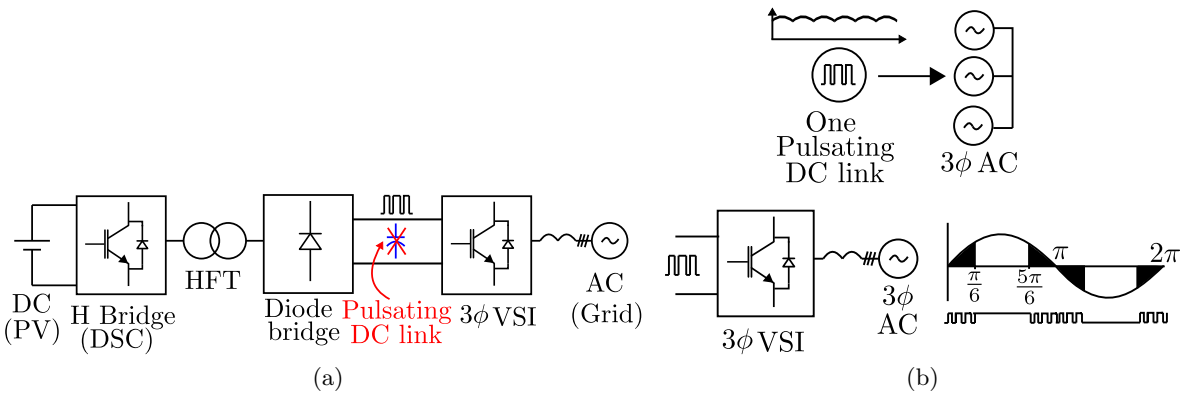


Figure 1.5: (a) Unidirectional RHFL DC-3ϕ AC converters, (b) Hybrid-modulation of the 3ϕ VSI.

In literature, several unidirectional RHFL topologies are reported [27–30]. In these topologies, in the secondary of the HFT, instead of active rectifier, diode bridge rectifier is used as shown in Fig. 1.5a. Thus the number of active switches and associated control circuits are reduced. These converters employ a special synchronised modulation strategy between the DC side converter (DSC) (1.5a) and the secondary side 3ϕ VSI, which is termed as hybrid modulation strategy. The hybrid modulation strategy reduces the high frequency switching of the 3ϕ VSI required for pulse width modulation (PWM). The 3ϕ VSI is high frequency switched only for one third of the line cycle thus improves the overall converter efficiency. Fig. 1.5b shows the conceptual diagram of the hybrid modulation. In these topologies the 3ϕ AC is generated from a single pulsating DC link. The pulsating DC link has an average of six-pulse rectified line voltages. At a given instant of time two legs of the 3ϕ VSI are clamped to the positive and negative of the pulsating DC link and the remaining leg is high frequency switched for modulation. The gating signal of a VSI switch over a line cycle is shown in Fig. 1.5b. Dark zones shown in the line cycle are where the switch is high frequency switched. Generally the VSI and the DSC are hard-switched. These converters support loads upto $\pm$0.866 PF.

1.5 Aim of the work

This work investigates unidirectional RHFL topologies to overcome the limitations of already existing unidirectional topologies. The topologies are explored and their modulation strategies are designed to achieve following objectives-

- Complete line frequency switching of all active switches of the grid interfaced converter. This scheme has following advantages-
  - Negligible switching loss of the grid interfaced converter, hence improved efficiency.
  - Efficiency can be improved further by using conduction loss optimized switches in the grid interfaced converter.
  - Due to line frequency switching, control complexity of the active switches are reduced.
  - In case of direct medium voltage grid integration, inherently slow high voltage blocking active devices can be used. This devices can not be switched at high frequency due to excessive switching loss.
- Soft commutation of the diode bridge which results in reduced diode loss.
- Ensuring soft-switching (either zero voltage switching (ZVS) or zero current switching (ZCS)) of high frequency switched active devices without additional snubber circuit.
- The active switches are either soft-switched or line frequency switched. So, the converters will have negligible switching loss. Thus the converter power loss is decoupled from the switching frequency of the converter. Hence converter can be switched at high frequency which results in smaller magnetics. The power density of the converter can be improved further.

1.6 Contribution

The objective of this work is to explore unidirectional RHFL topologies in line with the aims listed above. Four new unidirectional RHFL topologies along-with their modulation strategies and the working principle are investigated. These new topologies can be classified into two major categories based on number of pulsating DC-links present in a converter.

Topologies with three pulsating DC-links

Three such topologies have been explored. In these topologies all the active switches of the grid interfaced converter are line frequency switched. The topology 1 has six half-bridge legs on the DSC which are soft-switched over some part of a line cycle. The topology 2 has four half-bridge legs on the DSC. Where one leg is zero voltage switched (ZVS) over complete line cycle but the remaining three legs are partially soft-switched like topology 1. The topology 3 has three half-bridge legs on the DSC which and are soft-switched over complete line cycle. These topologies can support only UPF operation.

Topology with two pulsating DC-links

One such topology has been explored. This topology can support operation upto ±0.866 PF. In this topology, the active switches of the grid side converter are switched either at line frequency or twice of the line frequency. The topology has three soft-switched half-bridge legs on the DSC. On the ASC it employs a three level unfolder circuit.

The operation of the converters are discussed in details and the conditions for soft-switching are derived using detailed circuit analysis. The operations of these topologies are experimentally validated using laboratory scale hardware prototypes of power rating 2-6 kW.

1.7 Organization of the thesis

This chapter presents an overview of the converter topologies for the application of grid integration of utility scale PV. The limitations of the conventional state-of-the-art converter topology also known as central inverter, are described. As an alternative solution, the HFL based converter topologies are discussed along with their respective advantages and limitations. Finally research objectives are identified and the contributions are discussed in brief. Brief chapter-wise summaries are presented below.

Chapter 2- Unidirectional HFL DC-3ϕ AC Conversion with Three Pulsating DC Links: Topology-1 presents the basic principle of generating balanced three-phase line frequency AC voltage from three pulsating DC links using line frequency switched half-bridge legs. To generate three pulsating DC links, three isolated DC-DC converters are used. The converters are modulated like three phase-shifted full bridges (PSFB) with sinusoidally varying duty ratios. Like a PSFB, these DC-DC converters are soft-switched (ZVS) with the help of device capacitances and transformer leakage inductances. But as the transformer current magnitudes also vary sinusoidally over a line cycle, the DSC legs are soft-switched over a zone of the line cycle where the current magnitude is sufficiently high. A detailed circuit analysis is presented to show the converter operation over a switching cycle and to derive the soft-switching condition of the DSC. The converter is designed for a target application and the losses are computed analytically. The converter operation is validated in a 6.2 kW hardware prototype.

Chapter 3- Unidirectional HFL DC-3ϕ AC Conversion with Three Pulsating DC Links: Topology-2 presents an improvement over topology 1 with reduced active switches and improved soft-switching performance. The generation of balanced 3ϕ AC from the three pulsating DC links is similar to topology 1. But, the converter uses lower number of active switches in the DSC. The modulation strategy and detailed circuit analysis are described. The operation shows that one DSC leg can be soft-switched over complete line cycle while others are partially soft-switched like topology 1. The converter design and loss analysis are provided for a target application. Key experimental results are presented to validate the converter operation.

Chapter 4- Unidirectional HFL DC-3ϕ AC Conversion with Three Pulsating DC Links: Topology-3 describes how to generate three pulsating DC links, each with an

average of the rectified phase voltage, using only three half-bridge legs in the DSC using phase-shift modulation. The topology is an improvement over topology 2 with minimum number of active switches used and also ensures soft-switching of all the DSC legs over complete line cycle. A detailed circuit analysis is presented to show the converter operation over a line cycle and to derive soft-switching conditions. The design of the converter is given in details. The operation is verified in a 4kW hardware prototype.

Chapter 5- Unidirectional HFL DC-3ϕ AC Conversion with Two Pulsating DC Links: Topology-4 presents the basic principle of generating balanced three-phase line frequency AC voltage from two pulsating DC links using a low frequency switched active switch network. This chapter also describes the generation of two pulsating DC links with three half-bridge legs in the DSC using phase-shift modulation. It is shown that the DSC legs can be soft-switched over complete line cycle. The converter design and loss analysis are provided. The operation is verified in a 2kW hardware prototype.

Chapter 6- Topology Comparison presents a detailed comparison of all four proposed topologies with an existing multi-stage HFL inverter for a 200kW target application. The comparison in terms of number of semiconductors, voltage and current stress, power loss, transformer area product and filtering requirements of each topology are presented.

Chapter 8- Conclusion summarizes the overall contribution of the presented work in this thesis. An outline of the future work is also given.

Chapter 2

Unidirectional HFL DC-3ϕ AC Conversion with Three Pulsating DC Links: Topology-1

2.1 Introduction

Unidirectional single-stage HFL inverter topologies are popular for applications like grid integration of solar-photovoltaic, fuel cell etc. where the power flow is unidirectional, from source to load. As explained in the Chapter-1, these topologies employ uncontrolled diode bridge rectifiers to rectify the HFAC and hence have reduced number of active switches with reduced control complexity. As these topologies do not use any interstage filter capacitor, the rectifier output is pulsating. The topologies in [27–30] have one pulsating DC link and from the pulsating DC to generate line frequency AC, a 3ϕ VSI is used. As the 3ϕ VSI is hard-switched, the efficiency can be improved by reducing the high frequency switching of the VSI. But high frequency switching is essential from modulation perspective. In [27–30], a hybrid modulation strategy is adopted which reduces the high frequency switching of the VSI to only one third of line cycle thus improving the converter efficiency.

In this chapter, a new unidirectional HFL inverter topology is introduced which has three pulsating DC links and all the active switches in the secondary of the HFTs are completely line frequency switched. The derivation of the three phase topology is discussed in details. The high frequency switched DSC of the new converter is partially soft-switched and soft-switching is achieved without additional snubber circuit. Detailed circuit operation and soft-switching process are presented in this chapter. The converter power loss is obtained analytically. The filtering requirements in terms of input current and output voltage THDs are derived. Design and implementation aspects of a 6kW hardware prototype is first discussed followed by experimental results are presented to verify the converter operation. The content of this chapter is reported in [31].

2.2 Converter Configuration and Modulation Strategy

In this section a detailed discussion is presented on the derivation of the three phase converter configuration. First, the modulation strategy to achieve complete line frequency switching of the secondary side grid interfaced inverter of a single phase configuration is discussed. Then

the idea is extended to the three phase case.

Fig. 2.1 shows a single phase configuration of the unidirectional HFL inverter. The modulation strategy of the converter is shown in Fig. 2.2. From now on, the DC side converter which consists of four switches $S_{A1} - S_{A4}$ is called as DSC and the secondary diode bridge $(D_{a1} - D_{a4})$ along with the full bridge configuration $(Q_{a1} - Q_{a4})$ is termed as AC side converter or ASC. The DSC switches $S_{A1} - S_{A4}$ are switched at high frequency $(f_s = \frac{1}{T_s})$ with 50% duty ratio as shown in Fig. 2.2a. As the switch pairs (S_{A1}, S_{A2}) and (S_{A3}, S_{A4}) are across the DC source, these are complementary switched with a dead time between the switching signals. To generate pulse width modulated high frequency AC across the transformer primary terminals X_1Y_1, a phase shift is introduced between the gating signals of S_{A1} and S_{A3} and the phase shift varies sinusoidally with time. The phase shift is given by the controller as the modulation signal $m(t)$.

$$m(t) = M \mid \sin(\omega_o t) \mid = M \mid \sin\theta \mid \tag{2.1}$$

where M is modulation index and $M \in [0, 1]$. $\omega_o = \frac{2\pi}{T_o}$ is the angular frequency of the average

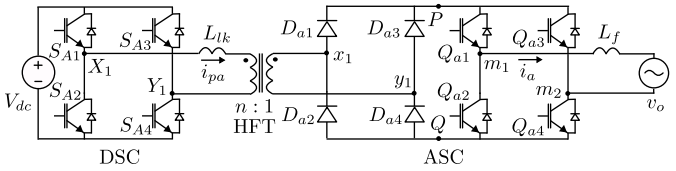


Figure 2.1: 1ϕ configuration of the unidirectional HFL topology

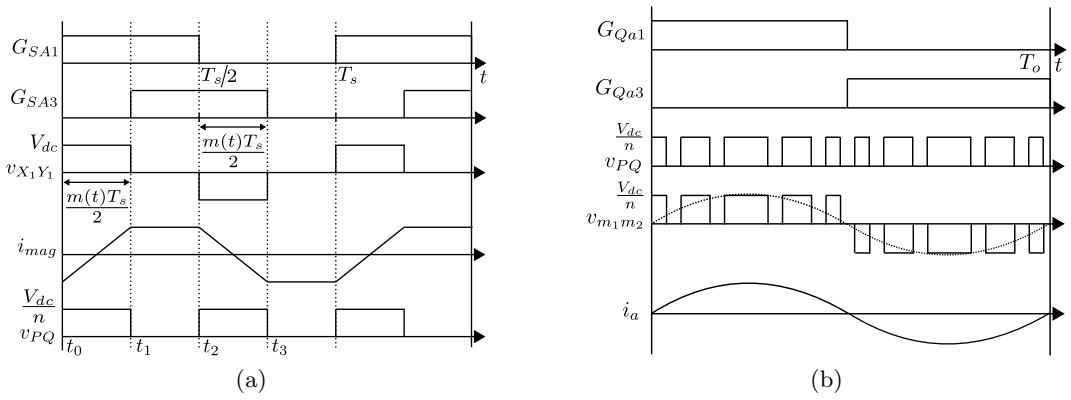


Figure 2.2: Modulation strategy. (a) DSC, (b) ASC.

output voltage $\overline{v}_{m_1m_2}$. The applied voltage across the transformer terminal X_1Y_1 is such that average volt-second over a switching period (T_s) is zero (Fig. 2.2a). The condition is expressed as-

$$\mid +V_{dc} \cdot (t_1 - t_0) \mid = \mid -V_{dc} \cdot (t_3 - t_2) \mid \tag{2.2}$$

where V_{dc} is input DC voltage. The magnetising current i_{mag} of the transformer is shown in Fig. 2.2a. PWM high frequency AC is step up/down by the high frequency transformer and is

applied to the ASC diode bridge rectifier. The average rectifier output is given as-

$$\overline{v}_{PQ} = \frac{m(t)V_{dc}}{n} \tag{2.3}$$

where n is primary to secondary turns ratio of the transformer. Rectified pulse width modulated pulsating DC (v_{PQ}) is then line frequency inverted (in Fig. 2.2b) by the line frequency switched inverter $Q_{a1} - Q_{a4}$. The switch pairs (Q_{a1}, Q_{a2}) and (Q_{a3}, Q_{a4}) are complementary switched. Q_{a1}, Q_{a4} are kept ON when the line current $i_a > 0$. Q_{a2}, Q_{a3} are ON when i_a is negative as is shown in Fig. 2.2b. Average pole voltage ($\overline{v}_{m_1m_2}$) over a line cycle is given as-

$$\overline{v}_{m_1m_2} = \frac{MV_{dc}}{n}\sin\theta \tag{2.4}$$

If the desired average output voltage is $\overline{v}_{m_1m_2} = V_{pk}\sin\theta$, the modulation index $M = \dfrac{nV_{pk}}{V_{dc}}$. Where V_{pk} is the peak of the average output voltage. $v_{m_1m_2}$ is passed through a line filter L_f to filter out switching frequency component. Due to ASC diode bridges, the converter is only capable of handling unidirectional power flow. Hence, the average pole voltage is in phase with the pole current i_a.

The above modulation strategy results in complete line frequency switching of the ASC active switches $Q_{a1} - Q_{a4}$. The idea is extended to the three phase case. Fig. 2.3 shows the

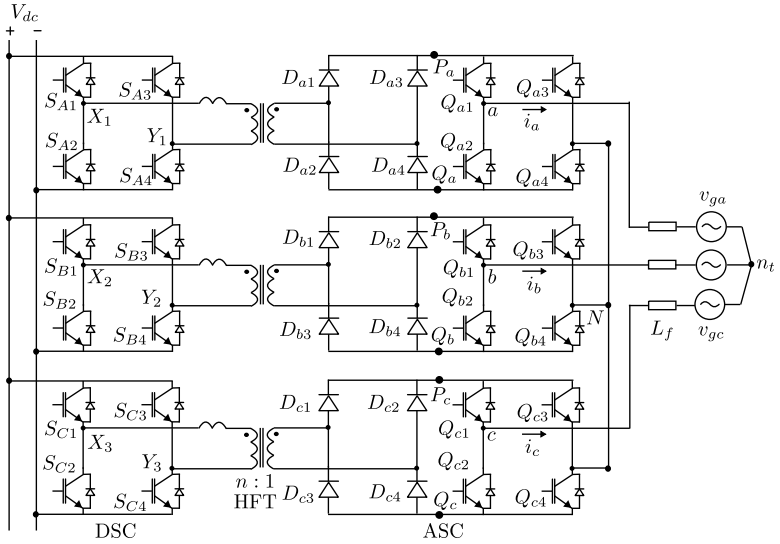


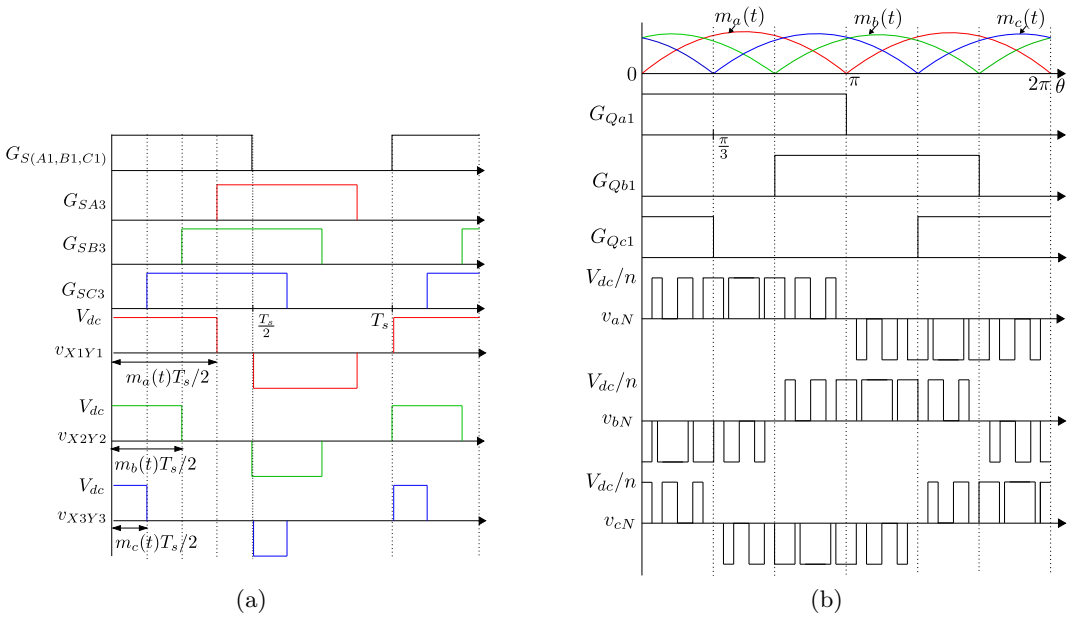
Figure 2.3: 3ϕ single stage unidirectional HFL topology

three phase configuration of the single stage unidirectional HFL topology. The modulation strategy of the 3ϕ converter is same as the 1ϕ topology shown in Fig. 2.1. Here for 3ϕ, three

single phase modules are integrated together. The three phase modulation signals are given as

$$\begin{aligned} m_a(t) &= M|\sin\theta| \\ m_b(t) &= M|\sin\left(\theta - \frac{2\pi}{3}\right)| \\ m_c(t) &= M|\sin\left(\theta + \frac{2\pi}{3}\right)| \end{aligned} \tag{2.5}$$

The modulation signals are shown in Fig. 2.4. Fig. 2.4a shows the modulation of DSC over a



(a) (b)

Figure 2.4: Modulation strategy of the 3ϕ converter. (a) DSC, (b) ASC.

switching cycle. Similar to the 1ϕ case, all the DSC active switches have gating signals with period T_s and 50% duty ratio. Following the modulation strategy of the 1ϕ topology, the gating signals of the switches S_{J3} are phase shifted by $\frac{m_j(t)T_s}{2}$ with respect to the gating signals of the switches S_{J1} respectively as shown in Fig. 2.4a. Where $J \in \{A, B, C\}$ and $j \in \{a, b, c\}$. The modulation strategy applies PWM HFAC voltages across the transformer primary terminals. In the secondary, the diode bridge rectifiers of the ASC rectify the HFAC voltages and generate **three pulsating DC links,** P_jQ_j. The three pulsating DC voltages containing three phase informations are then line frequency inverted by the ASC inverter switches $Q_{j1} - Q_{j4}$. Fig. 2.4b shows the modulation strategy of the ASC. Applied 3ϕ pole voltages v_{aN}, v_{bN} and v_{cN} with respect to neutral N are shown in Fig. 2.4b. Average pole voltages are given as-

$$\begin{aligned} \overline{v}_{aN} &= \frac{MV_{dc}}{n}\sin\theta \\ \overline{v}_{bN} &= \frac{MV_{dc}}{n}\sin\left(\theta - \frac{2\pi}{3}\right) \\ \overline{v}_{cN} &= \frac{MV_{dc}}{n}\sin\left(\theta + \frac{2\pi}{3}\right) \end{aligned} \tag{2.6}$$

Where $V_{pk} = \frac{MV_{dc}}{n}$. As M can have maximum value of 1, $V_{pk,max} = \frac{V_{dc}}{n}$.

As the AC port is connected to a balanced three-phase system and the sum of the switching cycle average of the pole voltages ($\sum_{j=a,b,c} \overline{v}_{jN} = 0$) are zero, the average line to neutral voltages are same as the pole voltages, $\overline{v}_{jn_t} = \overline{v}_{jN}$.

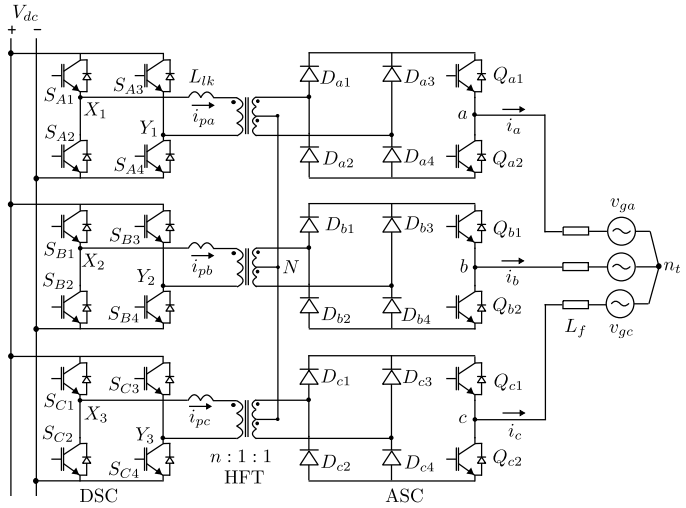


Figure 2.5: 3ϕ single stage unidirectional HFL topology with reduced active switches in ASC

The topology in Fig. 2.3 employs 12 active switches in the ASC. It is possible to have a 3ϕ topology with 6 active switches in the ASC as shown in Fig. 2.5. Here the secondary of each high frequency transformer has two identical windings. The starting of one secondary winding is connected to the finishing end of the other winding and three such points of the three HFTs are connected to form neutral point N. The modulation strategy of this converter is exactly same as the converter in Fig. 2.3. Though the number of active devices and associate control circuits are reduced but the blocking voltage of the ASC switches and diodes is twice of the topology in Fig. 2.3. In the thesis, the topology in Fig. 2.5 is considered for further discussion. Any future reference of topology 1 with three pulsating DC links indicates the topology in Fig. 2.5.

A multilevel variation of the topology in Fig. 2.3 is shown in Fig. 2.6. It is a single-stage cascaded multilevel topology that supports unidirectional power flow with line frequency switching of all the active switches of the ASC. The HFTs used in this topology have multiple secondary windings to form the multi-levels. The topology can be symmetric or asymmetric depending on whether the number of turns of all the secondary windings of a HFT is same or not. But in this discussion symmetric arrangement is considered. The multilevel topology enables direct medium voltage (11kV/33kV) grid integration of photovoltaic sources. Direct medium voltage grid integration eliminates requirement of intermediate line frequency step up transformer stages, thus improving system power density and cost [32–35]. What follows is a discussion on the modulation strategy of the multilevel topology shown in Fig. 2.6. The switching scheme of DSC is same as topology in Fig. 2.3. The generation of the output voltage v_{aN} of phase a is discussed in detail. Phase b and c have similar switching scheme. The output of the multi-winding HFTs are fed to diode bridge rectifiers. Output voltage of k^{th} rectifier module

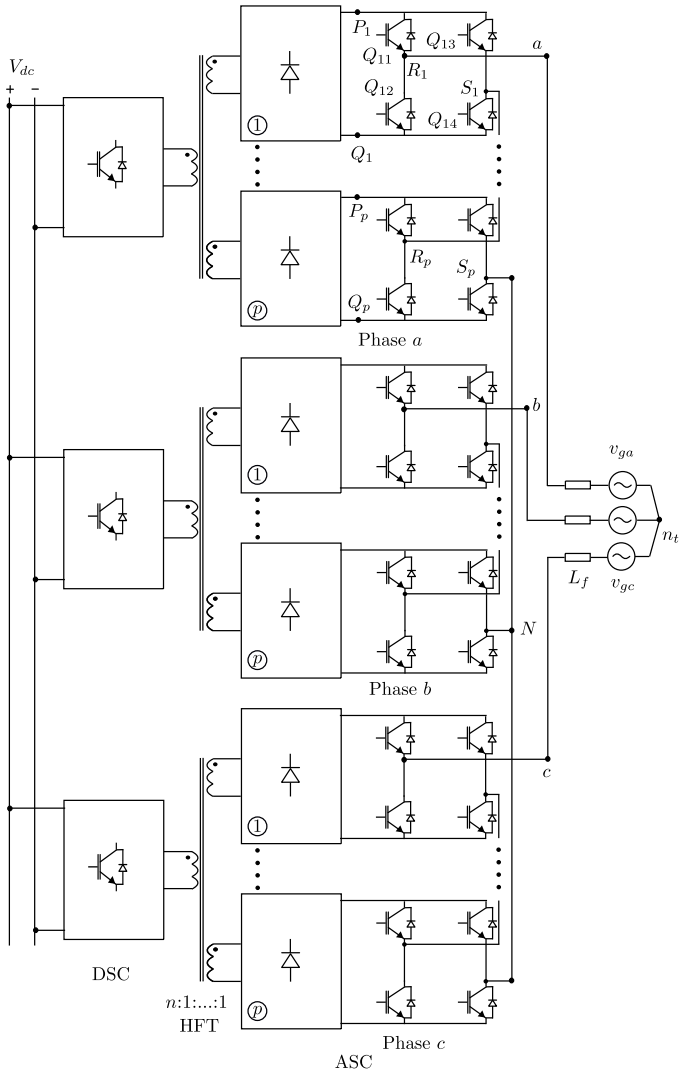


Figure 2.6: 3ϕ single stage unidirectional cascaded multilevel HFL topology

averaged over a switching cycle is expressed as-

$$\overline{v}_{PQ(k)} = \frac{M}{n} V_{dc} \mid \sin\theta \mid \tag{2.7}$$

Where $k \in (1, 2, .., p)$ and p is the total number of secondary modules in phase a (Fig. 2.6). Output of these rectifiers are fed to line frequency inverters to obtain bipolar output voltage. The gating signals of k^{th} line frequency inverter are given as-

$$G_{Qk1} = G_{Qk4} = \begin{cases} 1, & m_a(t) \geq 0 \\ 0, & Otherwise \end{cases} \tag{2.8}$$

$$G_{Qk2} = G_{Qk3} = \overline{G}_{Qk1} \tag{2.9}$$

Due to cascade connection, output of these line frequency inverters are summed up to build total output phase voltage. The average output voltage of phase a is given $\overline{v}_{aN}$ is given as-

$$\overline{v}_{aN} = \begin{cases} +\sum_{k=1}^{p} \overline{v}_{PQ(k)}, & 0 < \omega_o t < \pi \\ -\sum_{k=1}^{p} \overline{v}_{PQ(k)}, & \pi \leq \omega_o t \leq 2\pi \end{cases} \tag{2.10}$$

Using (2.10) the average output voltage can be expressed as-

$$\overline{v}_{aN} = \frac{pM}{n} V_{dc} \sin\theta \tag{2.11}$$

2.3 Steady-state Operation of the Converter

In this section, the operation of the 3ϕ topology (in Fig. 2.5) is described over a switching cycle (T_s). As stated earlier, the active switches of the ASC are line frequency switched. In the following discussion, it is considered that ASC active switches do not change the switching states over the switching cycle (T_s) under consideration. Hence the circuit dynamics due to the switching of the DSC is discussed in details. As mentioned before, the DSC is partially soft-switched. The switching process described here reveals the conditions for zero voltage switching of the DSC switches. As the switching strategy is similar in all the three phases, the circuit operation corresponding to phase a is only discussed here in details.

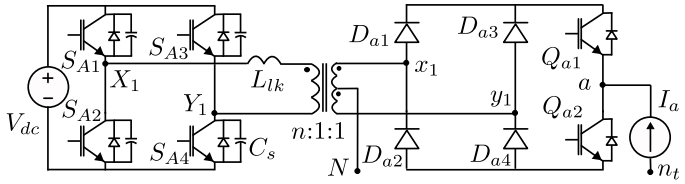


Figure 2.7: Simplified circuit diagram for switching analysis of phase a

The soft-switching of the DSC is achieved using device parasitic capacitance (C_s) and transformer leakage and additional series inductance (L_{lk}). For the ease of analysis, the slowly

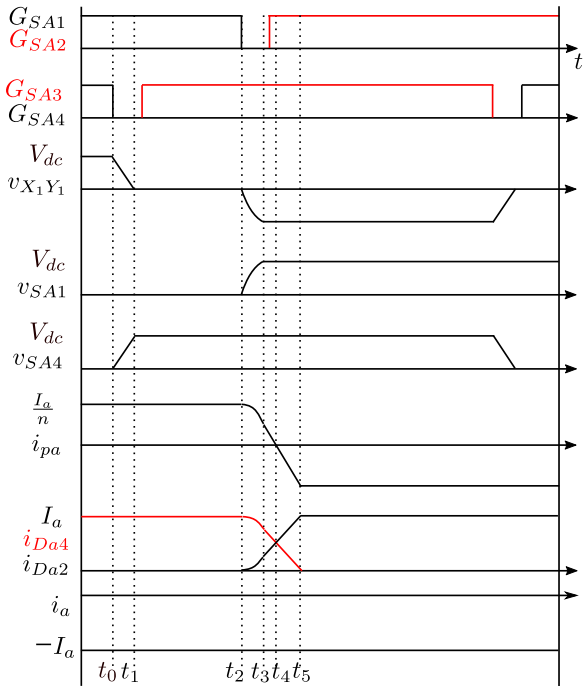


Figure 2.8: Switching waveforms showing zero to active and active to zero state transitions

varying, properly filtered line current (i_a) is considered as constant current (I_a) sink over T_s. The circuit is shown in Fig. 2.7. The switching process is described in the negative half cycle of the line current i_a. The switching transitions of the DC side converter are broadly classified as *active* to *zero state* transition and *zero* to *active state* transition. Where the *active state* is referred to the converter switching state when the applied voltage across the transformer terminals X_1Y_1 is V_{dc} or $-V_{dc}$. *Zero state* is the switching state when $v_{X_1Y_1} = 0$. Switching transition waveforms are shown in Fig. 2.8.

2.3.1 Active State ($t < t_0$: Fig. 2.8)

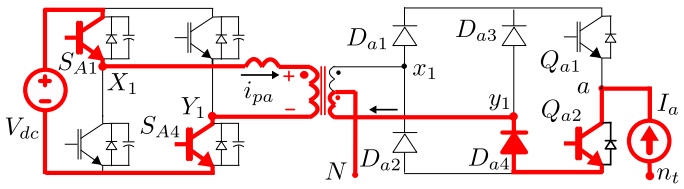


Figure 2.9: Simplified circuit diagram during active state

In this state switches S_{A1} and S_{A4} are ON (in Fig. 2.9) and are conducting a current, $i_{pa} = \dfrac{I_a}{n}$. The switches S_{A2} and S_{A3} are blocking the DC voltage V_{dc}. A positive voltage V_{dc} is applied across the transformer terminals X_1Y_1. In AC side, the diode D_{a4} and the switch Q_{a2} are conducting the load current I_a whereas D_{a2} is blocking a voltage $\dfrac{2V_{dc}}{n}$. The polarities of transformer voltage and current indicate the active power flow from DC to AC side.

2.3.2 Active State ⇒ Zero State ($t_0 < t < t_1$: Fig. 2.8)

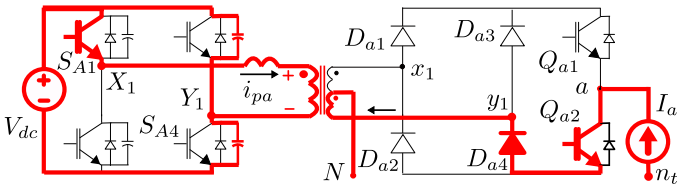


Figure 2.10: Circuit diagram during active to zero state transition

At the beginning of this transition, the switch S_{A4} is turned OFF. Due to presence of switch capacitance C_s voltage across the device changes slowly which helps to reduce the turn OFF loss of the outgoing device, S_{A4}. The current i_{pa} starts charging the device capacitance of S_{A4} and discharging the capacitance of S_{A3}. This causes the transformer voltage $v_{X_1Y_1}$ to fall linearly from V_{dc}. In the AC side, D_{a4} and Q_{a2} are conducting. The equivalent circuit in this mode is shown in Fig. 2.11. The initial conditions are given as: $v_{X_1Y_1}(t_0) = V_{dc}$, $i_{pa}(t_0) = \frac{I_a}{n}$.

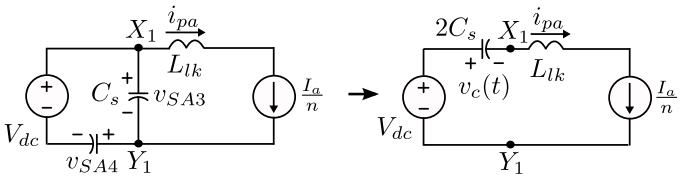


Figure 2.11: Equivalent circuit during active to zero state transition

Relevant circuit equations are given as-

$$\begin{aligned} V_{dc} &= v_{SA3}(t) + v_{SA4}(t) \\ i_{pa}(t) &= \frac{I_a}{n} \\ i_{pa}(t) &= C_s\left(\frac{dv_{SA4}}{dt} - \frac{dv_{SA3}}{dt}\right) \\ v_{X_1Y_1}(t) &= v_{SA3}(t) \end{aligned} \tag{2.12}$$

Where v_{SA3} and v_{SA4} are voltages across the devices S_{A3} and S_{A4} respectively. Solving equation (2.12),

$$v_{X_1Y_1}(t) = V_{dc} - \left(\frac{I_a}{nC_T}\right)t \tag{2.13}$$

where $C_T = 2C_s$.

The transition ends at t_1 when $v_{X_1Y_1}$ reaches 0 i.e the device capacitance across S_{A3} is completely discharged and the body diode of S_{A3} is forward biased and starts conducting. After t_1, S_{A4} is blocking V_{DC}. The time $t_{az} = (t_1 - t_0)$ is estimated by solving (2.13)

$$t_{az} = \frac{nC_TV_{dc}}{I_a} \tag{2.14}$$

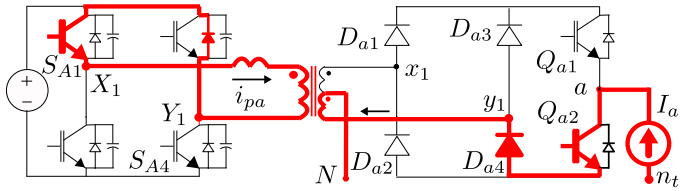


Figure 2.12: Simplified circuit in zero state

2.3.3 Zero State ($t_1 < t < t_2$: Fig. 2.8)

After t_1, the transformer terminals X_1Y_1 are shorted through switch S_{A1} and the body diode of S_{A3}. To ensure *zero voltage turn ON* of S_{A_3}, the gating signal is applied after t_1 when the body diode of S_{A3} is conducting. Simplified circuit diagram is shown in Fig. 2.12. No active power is transferred from DC to AC side in this state.

2.3.4 Zero State ⇒ Active State

The transition starts at t_2, when the switch S_{A1} is turned OFF. This transition is divided into three sub-modes.

Sub-mode I ($t_2 < t < t_3$: Fig. 2.8)

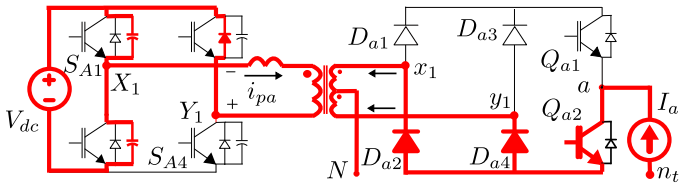


Figure 2.13: Simplified circuit in zero to active state transition in Sub-mode I

Simplified circuit diagram is shown in Fig. 2.13. Like S_{A4}, the turn OFF loss of S_{A1} is reduced due to the presence of device capacitor as explained earlier. The current i_{pa} starts charging the device capacitance of S_{A1} and discharging the device capacitance of S_{A2}. A negative voltage is applied across X_1Y_1 which forward biases D_{a2}. D_{a2} starts conducting. The HFT secondary winding is shorted through D_{a2} and D_{a4}. The equivalent circuit is shown in Fig. 2.14a. Initial conditions are given as: $v_{SA1}(t_2) = 0$, $v_{SA2}(t_2) = V_{dc}$ and $i_{pa}(t_2) = \dfrac{I_a}{n}$. Relevant circuit equations are

$$\begin{aligned} C_s\frac{dv_{SA1}(t)}{dt} &= C_s\frac{dv_{SA2}(t)}{dt} + i_{pa}(t) \\ L_{lk}\frac{di_{pa}(t)}{dt} &= -v_{SA1}(t) \\ V_{dc} &= v_{SA1}(t) + v_{SA2}(t) \end{aligned} \tag{2.15}$$

Solving (2.15) following expressions are obtained-

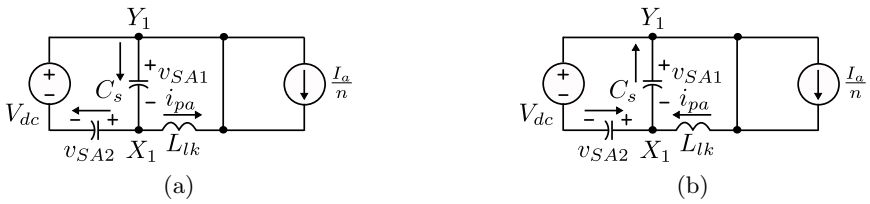


Figure 2.14: Equivalent circuit of zero to active state transition- (a) in Sub-mode I, (b) during resonant oscillation in Sub-mode I.

$$\begin{aligned} i_{pa}(t) &= \frac{I_a}{n}\cos\omega_p t + \frac{i'_{pa}(t_2)}{\omega_p}\sin\omega_p t \\ v_{SA1}(t) &= \frac{\omega_p L_{lk} I_a}{n}\sin\omega_p t - L_{lk} i'_{pa}(t_2)\cos\omega_p t \end{aligned} \tag{2.16}$$

Where $\omega_p = \dfrac{1}{\sqrt{L_{lk}C_T}}$, and $i'_{pa}(t_2) = \dfrac{di_{pa}(t)}{dt}|_{t_2}$
Here $i'_{pa}(t_2) = 0$ as $v_{SA1}(t_2) = 0$. At t_3, $v_{SA1}(t)$ reaches V_{dc}. The capacitor across S_{A2} is completely discharged and the body diode is forward biased. The time interval $t_{za1} = (t_3 - t_2)$ is estimated as-

$$t_{za1} = \frac{1}{\omega_p}\sin^{-1}\left(\frac{nV_{dc}}{\omega_p L_{lk} I_a}\right) \tag{2.17}$$

The capacitor across S_{A2} will be completely discharged and the circuit will move to next sub mode only if

$$\omega_p L_{lk} I_a \geq nV_{dc} \tag{2.18}$$

Else the circuit will experience resonant oscillation with angular frequency ω_p i.e. before v_{SA2} becomes zero i_{pa} will be negative and starts charging and discharging the capacitances across S_{A2} and S_{A1} respectively. The circuit moves back and forth between Fig. 2.14a and Fig. 2.14b till next switching transition i.e till the gating pulse of S_{A2} is applied. And this turn ON of S_{A2} will be hard switching, as capacitance across the device is not completely discharged. If (2.18) is satisfied, at t_3 $i_{pa}(t)$ is given as

$$i_{pa}(t_3) = \frac{\sqrt{(\omega_p L_{lk} i_{pa}(t_2))^2 - (V_{dc})^2}}{\omega_p L_{lk}} \tag{2.19}$$

Sub mode II ($t_3 < t < t_4$: Fig. 2.8)

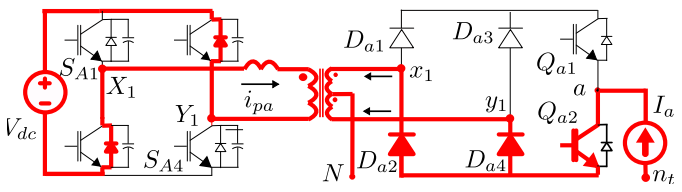


Figure 2.15: Simplified circuit in zero to active state transition in Sub-mode II

In this sub mode, body diodes of S_{A2} and S_{A3} conduct $i_{pa}(t)$. Simplified circuit diagram is

shown in Fig. 2.15. As $-V_{dc}$ is applied across L_{lk} (in Fig. 2.16a), i_{pa} falls linearly-

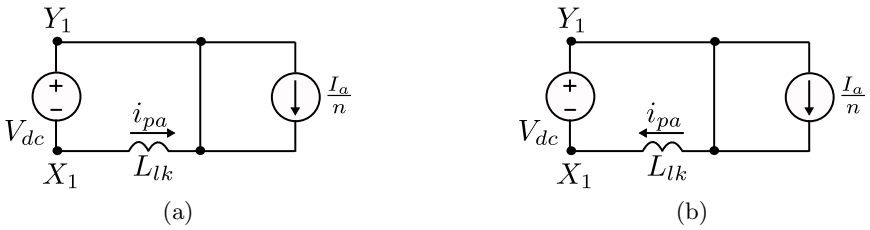


Figure 2.16: Equivalent circuit of zero to active state transition - (a) in sub-mode II, (b) in sub-mode III.

$$i_{pa}(t) = i_{pa}(t_3) - \frac{V_{dc}}{L_{lk}}t \tag{2.20}$$

This mode ends when i_{pa} reaches zero at t_4. The interval $t_{za2} = (t_4 - t_3)$ is given as

$$t_{za2} = i_{pa}(t_3)\frac{L_{lk}}{V_{dc}} \tag{2.21}$$

To ensure ZVS turn ON of S_{A_2} gating signal is applied during this interval. *Dead time* (DT) between the gating signals of S_{A_1} and S_{A_2} must be-

$$t_{za1} \leq DT \leq (t_{za1} + t_{za2}) \tag{2.22}$$

From (2.17) and (2.21), due to dependence on the initial conditions of $i_{pa}(t)$, t_{za1} and t_{za2} varies over a line cycle. With fixed dead time switching signals and for a given load, (2.22) will not be satisfied in some part of the line cycle. Which will result hard switching of S_{A2}. It is seen that near zero crossing of the line current when I_a is small and (2.22) is not satisfied. But as the current magnitude is small, resulting switching loss is less.

Sub mode III ($t_4 < t < t_5$: Fig. 2.8)

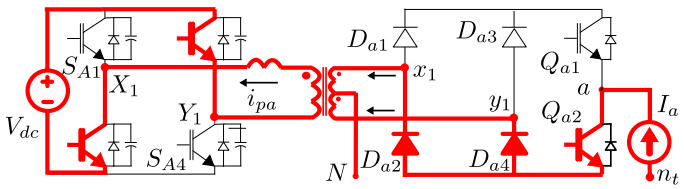


Figure 2.17: Simplified circuit in zero to active state transition in Sub-mode III

Simplified circuit diagram in this sub-mode is shown in Fig. 2.17. After t_4, i_{pa} starts flowing in the opposite direction as the switches S_{A_2} and S_{A3} are ON and $-V_{dc}$ is still applied across L_{lk} (see equivalent circuit in Fig. 2.16b).
i_{pa} can be expressed as-

$$i_{pa}(t) = -\frac{V_{dc}}{L_{lk}}t \tag{2.23}$$

Table 2.1: Target design specification

Parameter	Value
Output power (P)	200 kW
Operation power factor	UPF
Input DC (V_{dc})	800V
Output phase AC peak (V_{pk})	339V (415V L-L RMS)
Switching frequency (f_s)	20kHz
Line frequency (f_o)	50Hz

This mode ends at t_5 when $i_{pa} = -\frac{I_a}{n}$.

2.3.5 Active state ($t > t_5$: Fig. 2.8)

At t_5, current through D_{a4} becomes zero. The applied voltage polarity across the transformer terminal X_1Y_1 reverse biases the diode D_{a4}. Simplified circuit schematic is shown in Fig. 2.18.

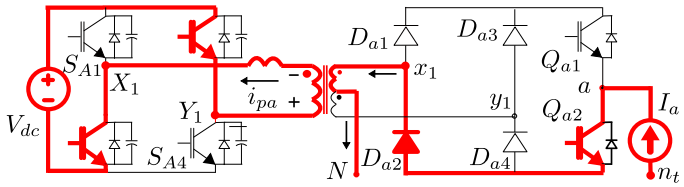


Figure 2.18: Simplified circuit in next active state

The circuit is in next active state.

The above discussion shows the polarity reversal of transformer primary voltage and current in one half of the switching cycle. In remaining half of the switching cycle another two state transitions take place- *active to zero state* transition (S_{A3} is turned OFF and S_{A4} is turned ON) followed by *zero to active state* transition (S_{A2} is turned OFF and S_{A1} is turned ON). In these switching transitions, similar switching process as discussed above are followed. In positive half cycle of the line current i_a the diodes D_{a1}, D_{a3} and the switch Q_{a1} take part in conduction and switching process. The operation of the primary DSC remains same.

2.4 Converter design

We have designed the converter for a target application of grid integration of utility scale solar photo-voltaic. The specification of the design is given in Table 2.1. At rated condition the inverter is supplying 200kW of active power at unity power factor (UPF) to a 415V (line to line RMS), 50Hz three-phase utility from an 800V DC source. The topology is modulated at the 85% of its maximum possible modulation index. Hence the modulation index $M = \frac{nV_{pk}}{V_{dc}} = 0.85$. Thus the high frequency transformer (HFT) primary to secondary turns ratio is $n = 2.0$.

2.4.1 Device blocking voltage and RMS current

From input-output power balance, at UPF operation following equation can be written

$$P = \frac{3}{2} V_{pk} I_{pk} = V_{dc} I_{dc} \tag{2.24}$$

Again in case of Topology 1, $V_{pk} = \frac{MV_{dc}}{n}$. Using this expression of V_{pk} in (2.24), I_{pk} can be expressed as

$$\begin{aligned} \frac{I_{pk}}{n} &= \frac{2}{3M} \frac{P}{V_{dc}} \\ I_{pk} &= \frac{2P}{3V_{pk}} \end{aligned} \tag{2.25}$$

The RMS current in switch pair $S_{X1} - S_{X2}$ ($X \in A, B, C$) is given below.

$$I_{RMS,S_{X1}-S_{X2}} = 0.5 \frac{I_{pk}}{n} = \frac{1}{3M} \frac{P}{V_{dc}} \tag{2.26}$$

The peak current through $S_{X1} - S_{X2}$ is $I_{pk,S_{X1}-S_{X2}} = \frac{I_{pk}}{n} = \frac{2}{3M} \frac{P}{V_{dc}}$. With $M = 0.85$, $I_{RMS,S_{X1}-S_{X2}} = 0.39 \frac{P}{V_{dc}}$ and $I_{pk,S_{X1}-S_{X2}} = 0.78 \frac{P}{V_{dc}}$.
The RMS current in $S_{X3} - S_{X4}$ is expressed as follows.

$$I_{RMS,S_{X3}-S_{X4}} = \frac{I_{pk}}{n} \sqrt{\frac{2M}{3\pi}} = \frac{2\sqrt{2}}{3\sqrt{3M\pi}} \frac{P}{V_{dc}} \tag{2.27}$$

The peak current of $S_{X3}-S_{X4}$ is $I_{pk,S_{X3}-S_{X4}} = \frac{I_{pk}}{n} = \frac{2}{3M} \frac{P}{V_{dc}}$. With $M = 0.85$, $I_{RMS,S_{X3}-S_{X4}} = 0.33 \frac{P}{V_{dc}}$ and $I_{pk,S_{X3}-S_{X4}} = 0.78 \frac{P}{V_{dc}}$.
The Blocking voltage of the DSC switches are V_{dc}.
The RMS current of secondary diodes $D_{a1} - D_{c4}$ is given as follows.

$$I_{RMS,D_{a1}-D_{c4}} = \frac{I_{pk}}{2\sqrt{2}} = 0.236 \frac{P}{V_{pk}} \tag{2.28}$$

The RMS current of secondary devices $Q_{a1} - Q_{c2}$ is expressed as-

$$I_{RMS,Q_{a1}-Q_{c2}} = \frac{I_{pk}}{2} = 0.33 \frac{P}{V_{pk}} \tag{2.29}$$

Peak current of secondary diodes and devices are given as $I_{pk,D_{a1}-D_{c4}} = I_{pk,Q_{a1}-Q_{c2}} = I_{pk} = 0.67 \frac{P}{V_{pk}}$. The blocking voltage of secondary diodes and devices is given as- $\frac{2V_{dc}}{n} = \frac{2}{M} V_{pk}$. With $M = 0.85$, blocking voltage $\frac{2}{M} V_{pk} = 2.35 V_{pk}$.

The detailed derivation steps of the RMS currents are given in Appendix A.

2.4.2 Estimation of Converter Power Loss

Closed form expressions of power losses in active switches and diodes of the converter are given in this section. The conduction loss in a switch is given as

$$P_C = V_{CE} I_{avg} + R_{CE} I_{RMS}^2 \tag{2.30}$$

where, V_{CE} and R_{CE} is the device voltage drop and on state resistance respectively obtained from the device data-sheet. In case of diode these parameters are V_D and R_D respectively. I_{avg} and I_{RMS} are the average and RMS currents through the device. The expressions of I_{avg} and I_{RMS} are derived first to obtain the conduction loss expression. The loss expression of phase a devices and diodes are presented here.Phase b and c switches have similar loss expressions. The detailed derivation steps of the conduction loss are given in Appendix A.

Loss estimation of DSC switches and diodes

Over a switching cycle the switches S_{A1}-S_{A4} and the anti-parallel diodes of S_{A3} and S_{A4} take part in conduction. The anti-parallel diodes of S_{A1} and S_{A2} conducts for very small durations during switching transitions. Hence the conduction losses in these diodes are neglected. Using (2.30) the conduction loss of these switches and their anti-parallel diodes are expressed in (2.31)-(2.33).

$$P_{C_{SA1}} = P_{C_{SA2}} = \frac{V_{CE} I_{pk}}{n\pi} + \frac{R_{CE} I_{pk}^2}{4n^2} \tag{2.31}$$

$$P_{C_{SA3}} = P_{C_{SA4}} = \frac{M V_{CE} I_{pk}}{4n} + \frac{M R_{CE} I_{pk}^2}{1.5\pi n^2} \tag{2.32}$$

$$P_{C_{D,SA3}} = P_{C_{D,SA4}} = \frac{V_D I_{pk}}{\pi n} + \frac{R_D I_{pk}^2}{4n^2} - \frac{M V_D I_{pk}}{4n} - \frac{M R_D I_{pk}^2}{1.5\pi n^2} \tag{2.33}$$

V_D and R_D are forward voltage drop and on state resistance of the anti-parallel diodes of S_{A3} and S_{A4} respectively.

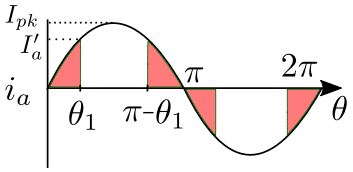


Figure 2.19: Shaded area showing hard-switching region of DSC switches over a line cycle

As discussed in the last section, the soft-switching of the DSC switches depends on the current magnitude (I_a) (see equations (2.14) and (2.22)). Again the current magnitude varies sinusoidally over a line cycle. Near zero crossing of the line current, I_a is small which results in hard-switching of the DSC. The range of soft turn ON of $S_{A1} - S_{A4}$ in one half of line cycle is indicated as $(\theta_1, \pi - \theta_1)$, as shown in Fig. 2.19. The shaded region indicates hard turn ON zone of the DSC over a line cycle for a given load. For a given dead time DT, the range of soft turn ON over a line cycle is obtained in Appendix B. The analytical expression of θ_1 for switch

pairs $S_{A1} - S_{A2}$ and $S_{A3} - S_{A4}$ is given in (B.4) and (B.7) respectively.

The turn OFF of $S_{A1} - S_{A4}$ are capacitor assisted soft transition. In this work the range of soft-turn OFF is not derived. In loss calculation the zone of soft turn ON is also considered as zone of soft turn OFF of the DC bridge. The switching loss of the DC bridge switches is expressed in (2.34).

$$P_{S_{S_{Ai}}} = \frac{2V_{dc}I_{pk}}{n\pi T_s}\left(\frac{E_{ON_R} + E_{OFF_R}}{V_{CC}I_C}\right)\left(1 - \cos\theta_{1_{S_{Ai}}}\right) \tag{2.34}$$

Where $i \in \{1, 2, 3, 4\}$. $E_{ON,R}$, $E_{OFF,R}$ are the turn ON and turn OFF energy losses of IGBT at rated condition- V_{CC}, I_C given in device datasheet.

Loss estimation of ASC switches and diodes

Conduction loss expressions of the switches $Q_{a1} - Q_{a2}$ and diodes $D_{a1} - D_{a4}$ are given in (2.35) and (2.36).

$$P_{C_{Qa1}} = P_{C_{Qa2}} = \frac{V_{CE}I_{pk}}{\pi} + \frac{R_{CE}I_{pk}^2}{4} \tag{2.35}$$

$$P_{C_{Da(1-4)}} = \frac{V_D I_{pk}}{2\pi} + \frac{R_D I_{pk}^2}{8} \tag{2.36}$$

As the switches are line frequency switched, switching loss is negligible. The diodes are commutated softly as the rate of change of the current during commutation is low, $\left(\frac{V_{dc}}{L_{lk}}\right)$. Hence the diodes have very low reverse recovery loss.

2.4.3 Design of high frequency transformers

The RMS current of HFT primary winding is $I_{RMS,p} = \frac{nI_{pk}}{\sqrt{2}} = \frac{\sqrt{2}}{3M}\frac{P}{V_{dc}}$. For $M = 0.85$, $I_{RMS,p} = 0.55\frac{P}{V_{dc}}$. The RMS current of HFT secondary winding is $I_{RMS,s} = \frac{I_{pk}}{2} = 0.33\frac{P}{V_{pk}}$.

Next we will find the area product of the HFTs. The area product which is the product of the core and window area of the HFT, indicates the transformer size.

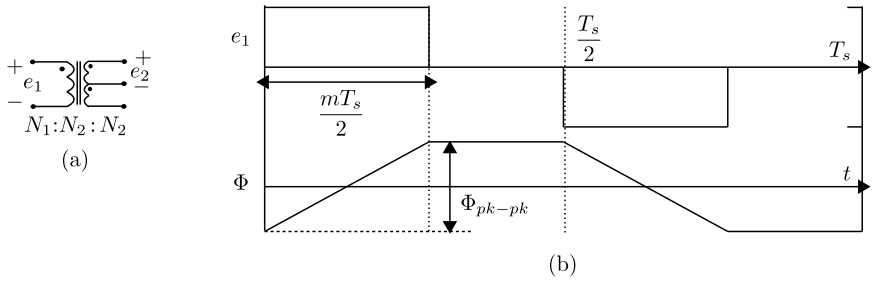


Figure 2.20: (a) Three winding HFT (b) HFT voltage and flux waveforms over a switching cycle

Area product of HFTs used in topology 1

These topologies employ three winding HFTs as shown in Fig. 2.20a. The applied HFT primary voltage (e_1) is duty cycle modulated square wave with magnitude V_{dc}. The duty cycle is maximum at $\theta = \frac{\pi}{2}$ in one half of a line cycle and when the modulation signal reaches its maxima ($M = 0.85$). The maximum peak-peak flux (see Fig. 2.20b) is estimated as follows.

$$\Phi_{pk-pk,max} = \frac{1}{N_1}\int_0^{\frac{MT_s}{2}} e_1 dt = \frac{MV_{dc}T_s}{2N_1} \tag{2.37}$$

Where N_1 and N_2 are HFT primary and secondary turns and $n = \frac{N_1}{N_2}$. The peak flux density (B_{max}) is related to $\Phi_{pk-pk,max}$ through HFT core area A_c.

$$A_c B_{max} = \frac{\Phi_{pk-pk,max}}{2} = \frac{MV_{dc}}{4N_1 f_s} \tag{2.38}$$

The switching frequency $f_s = \frac{1}{T_s}$. HFT window area (A_w) is estimated as follows.

$$A_w K_w = \frac{N_1 I_{RMS,p}}{J} + \frac{2N_2 I_{RMS,s}}{J} = \frac{N_1 I_{RMS,p}}{J}(1+\sqrt{2}) \tag{2.39}$$

where K_w is the window fill factor and J is the current density. The primary and secondary winding RMS currents are $I_{RMS,p} = \frac{N_2 I_{pk}}{\sqrt{2}N_1}$, $I_{RMS,s} = \frac{I_{pk}}{2}$ respectively. The product of window and core area is estimated as follows.

$$A_c A_w = \frac{MV_{dc}}{4N_1 f_s B_{max}} \frac{N_1 I_{RMS,p}}{JK_w}(1+\sqrt{2}) = 0.242\frac{P}{K_w J B_{max} f_s} \tag{2.40}$$

Where output power is $P = \frac{3V_{pk}I_{pk}}{2} = \frac{3MN_2 V_{dc} I_{pk}}{2N_1}$.

Estimation of copper Loss of the HFTs

Copper loss of the HFT is given as-

$$P_{cu,HFT} = R_p I^2_{RMS,p} + (2R_s) I^2_{RMS,s} \tag{2.41}$$

$I_{RMS,p} = \frac{I_{pk}}{n\sqrt{2}}$ and $I_{RMS,s} = \frac{I_{pk}}{2}$ are the RMS currents of primary and secondary windings of the HFT respectively. R_p and R_s are the primary and secondary winding resistances of the HFT at the operating frequency.
At the switching frequency below 40kHz, the HFT core (EPCOS ferrite) loss is negligible.

2.4.4 Input and Output Filter Requirement of the Converter

At the DC input of the converter, a capacitor is required to support the high frequency switching ripple current. Similarly, at the output port, inductors are required to filter out the high frequency voltage ripple.

The filtering requirements and THD

At the output of the converter, filter inductor L_f is used to limit harmonics in the grid current. Let the rms of harmonics present in line current is $\tilde{i}$ where as harmonics present in pole voltage is $\tilde{v}$. The current harmonics $\tilde{i}$ should be restricted to a certain percentage (say λ) of the fundamental component (I_{rms_1}) of line current. Considering all harmonics are concentrated at switching frequency (f_s) (which leads to slight over design of the filter), $\tilde{i} = \dfrac{\tilde{v}}{2\pi f_s L_f} = \lambda I_{rms_1}$. If V_{rms_1} is the rms of the fundamental component of phase voltage, voltage THD can be expressed as $THD_V = \dfrac{\tilde{v}}{V_{rms_1}}$. Considering base impedance $Z_b = \dfrac{V_{rms_1}}{I_{rms_1}}$, the per unit inductive filter impedance $Z_{p.u}$ can be expressed as-

$$Z_{p.u} = \frac{2\pi f_s L_f}{Z_b} = \frac{THD_V}{\lambda} \tag{2.42}$$

Similarly, in case of a capacitive filter, if the ripple voltage ($\tilde{v}$) is restricted to μV_{rms_1} and the current THD is given by $THD_I = \dfrac{\tilde{i}}{I_{rms_1}}$, per unit capacitive admittance is given as-

$$Y_{p.u} = \frac{2\pi f_s C_f}{Y_b} = \frac{THD_I}{\mu} \tag{2.43}$$

where $Y_b = \dfrac{I_{rms_1}}{V_{rms_1}}$ and C_f is the filter capacitance. **Thus THD is a direct measurement of filtering requirement independent of converter power for given μ and λ.** THD depends on modulation strategy and the modulation index of the converter. Next, THD_V and THD_I of the converter are derived.

Filter capacitance requirement at the input of the converter

Input DC filter capacitors provide high frequency switching ripple current to the converter. In this section, input ripple current RMS is found out. The gating signals of the DSC switches and the DC link currents are shown in Fig. 2.21 when $\theta \in (0, \dfrac{\pi}{3})$. In Fig. 2.21, i_{dc_A} is the DC link current drawn due to switching operation of $S_{A1} - S_{A4}$. Similarly i_{dc_B} and i_{dc_C} are defined. Net DC link current is given by $i_{dc} = i_{dc_A} + i_{dc_B} + i_{dc_C}$. The waveform of i_{dc} has a periodicity of $\frac{\pi}{3}$. As seen from Fig. 2.4b, over $\theta \in (0, \frac{\pi}{3})$, the modulation signals are given as

$$\begin{aligned} m_a(t) &= M \sin\theta \\ m_b(t) &= M \sin\left(\theta + \frac{\pi}{3}\right) \\ m_c(t) &= M \sin\left(\theta + \frac{2\pi}{3}\right) \end{aligned} \tag{2.44}$$

Over $\theta \in (0, \frac{\pi}{3})$ the magnitudes of i_{dc_A}, i_{dc_B} and i_{dc_C} (which are $I'_{A,B,C}$ respectively) vary sinusoidally as given in (2.45).

$$\begin{aligned} I'_A(t) &= \frac{I_{pk}}{n}\sin\theta \\ I'_B(t) &= \frac{I_{pk}}{n}\sin\left(\theta + \frac{\pi}{3}\right) \\ I'_C(t) &= \frac{I_{pk}}{n}\sin\left(\theta + \frac{2\pi}{3}\right) \end{aligned} \tag{2.45}$$

The RMS of DC link current can be derived as follows.

$$\begin{aligned} i^2_{dc,rms} =& \frac{3}{\pi}\int_0^{\frac{\pi}{3}} \left[(I'_A + I'_B + I'_C)^2 m_a + (I'_B + I'_C)^2(m_c - m_a) + I'^2_B(m_b - m_c)\right] d\theta \\ =& 2.492M\left(\frac{I_{pk}}{n}\right)^2 \end{aligned} \tag{2.46}$$

The average DC link current $i_{dc,avg}$ can be derived from input and output power balance and

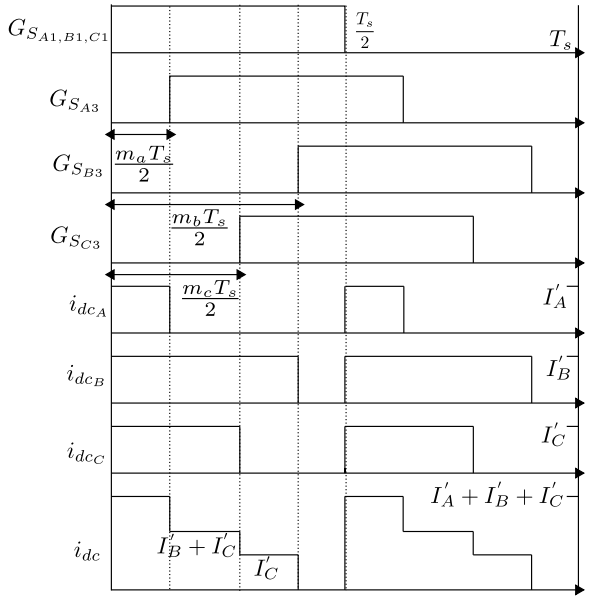


Figure 2.21: Input DC link current of the converter when $\theta \in (0, \frac{\pi}{3})$

is given as $i_{dc,avg} = \dfrac{3MI_{pk}}{2n}$. The ripple current RMS, $\tilde{i}$ is given as

$$\begin{aligned} \tilde{i} =& \sqrt{i^2_{dc,rms} - i^2_{dc,avg}} \\ =& \frac{I_{pk}}{n}\sqrt{(2.492M - 2.25M^2)} \end{aligned} \tag{2.47}$$

THD_I is given as

$$THD_I = \frac{\tilde{i}}{i_{dc,avg}} = \frac{\sqrt{(2.492M - 2.25M^2)}}{1.5M} \tag{2.48}$$

For $M = 0.85$, THD_I is 0.55.

Filter inductance requirement at the output of the converter

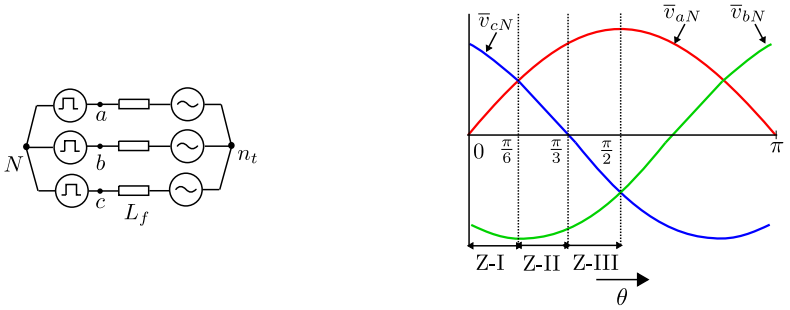
The filter inductors filter out the switching voltage ripple present in the pole voltages. The switching voltage ripple present in the pole voltage v_{an_t} is estimated in this section. In Fig. 2.22a, an equivalent circuit configuration of the converter is shown. By applying KVL, following circuit equations can be written-

$$\begin{aligned} v_{aN} &= v_{an_t} + v_{n_tN} \\ v_{bN} &= v_{bn_t} + v_{n_tN} \\ v_{cN} &= v_{cn_t} + v_{n_tN} \end{aligned} \tag{2.49}$$

For a balanced 3ϕ load, $v_{an_t} + v_{bn_t} + v_{cn_t} = 0$. Hence v_{n_tN} is given as

$$v_{n_tN} = \frac{v_{aN} + v_{bN} + v_{cN}}{3} \tag{2.50}$$

The average pole voltages, $\overline{v}_{jN} = \overline{v}_{jn_t} = V_{pk}\sin(\theta + M_j\frac{2\pi}{3})$ (where $M_a = 0$, $M_b = -1$ and $M_c = +1$ and $j \in \{a, b, c\}$) are shown in Fig. 2.22b. In this figure, following three zones are marked- zone-I (Z-I: $\theta \in (0, \frac{\pi}{6})$), zone-II (Z-II: $\theta \in (\frac{\pi}{6}, \frac{\pi}{3})$) and zone-III (Z-III: $\theta \in (\frac{\pi}{3}, \frac{\pi}{2})$).



(a) (b)

Figure 2.22: (a) Equivalent circuit of the converter, (b) Average pole voltages shown over one half of a line cycle

Using (2.49) and (2.50), applied pole voltages v_{jn_t} can be estimated. Fig. 2.23 shows the pole voltage v_{an_t}. It is found that the waveform of v_{an_t} has quarter symmetry.

In Z-I, the RMS of v_{an_t} is expressed as (see Fig. 2.23a)-

$$\begin{aligned} V^2_{an_{tZ-I}} &= \left(\frac{2V_{dc}}{3n}\right)^2 m_a + \left(\frac{V_{dc}}{3n}\right)^2 m_a \\ &= \frac{5M}{9}\left(\frac{V_{dc}}{n}\right)^2 \sin\theta \end{aligned} \tag{2.51}$$

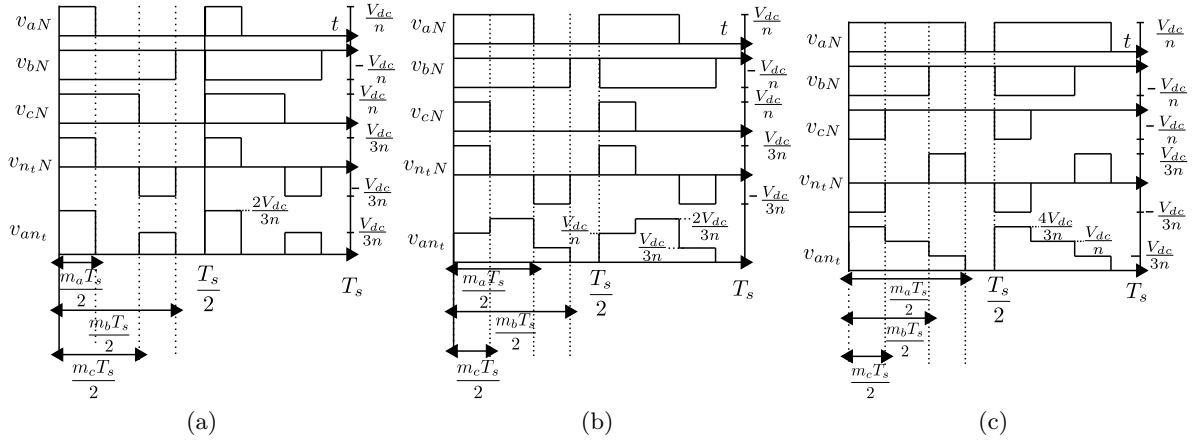


Figure 2.23: Pole voltage waveforms-(a) in zone I (Z-I) (b) in zone II (Z-II) and (c) in zone III (Z-III). Zones are marked in Fig. 2.22b

In zone II, v_{an_t} RMS is given by (see Fig. 2.23b)-

$$\begin{aligned} V^2_{an_t{}_{Z-II}} =& \left(\frac{2V_{dc}}{3n}\right)^2 m_c + \left(\frac{V_{dc}}{n}\right)^2 (m_a - m_c) + \left(\frac{V_{dc}}{3n}\right)^2 m_c \\ =& \frac{M}{9}\left(\frac{V_{dc}}{n}\right)^2 (11\sin\theta - 2\sqrt{3}\cos\theta) \end{aligned} \tag{2.52}$$

In Z-III, the RMS of v_{an_t} is expressed as (see Fig. 2.23c).

$$\begin{aligned} V^2_{an_t{}_{Z-III}} =& \left(\frac{4V_{dc}}{3n}\right)^2 m_c + \left(\frac{V_{dc}}{n}\right)^2 (m_b - m_c) + \left(\frac{2V_{dc}}{3n}\right)^2 m_c \\ =& \frac{M}{9}\left(\frac{V_{dc}}{n}\right)^2 (10\sin\theta - \sqrt{3}\cos\theta) \end{aligned} \tag{2.53}$$

As the waveform of v_{an_t} has quarter wave symmetry, the line cycle RMS of v_{an_t} can be expressed as-

$$\begin{aligned} v^2_{an_t,rms} =& \frac{2}{\pi}\left(\int_0^{\frac{\pi}{6}} V^2_{an_t{}_{Z-I}} + \int_{\frac{\pi}{6}}^{\frac{\pi}{3}} V^2_{an_t{}_{Z-II}} + \int_{\frac{\pi}{3}}^{\frac{\pi}{2}} V^2_{an_t{}_{Z-III}}\right) d\theta \\ =& 0.5798M\left(\frac{V_{dc}}{n}\right)^2 \end{aligned} \tag{2.54}$$

The RMS of fundamental component of v_{an_t} is $v_{an_t,rms1} = \dfrac{V_{pk}}{\sqrt{2}} = \dfrac{MV_{dc}}{\sqrt{2}n}$. The ripple voltage RMS of v_{an_t} can be expressed as-

$$\tilde{v} = \frac{V_{dc}}{n}\sqrt{[0.5798M - 0.5M^2]} \tag{2.55}$$

The voltage THD is given as-

$$THD_V = \frac{\tilde{v}}{v_{an_t,rms1}} = \frac{\sqrt{[1.16M - M^2]}}{M} \tag{2.56}$$

For $M = 0.85$, THD_V is 0.6.

2.5 Experimental Results

The modulation strategy and switching techniques of the converter discussed so far are experimentally verified on laboratory prototype (see Fig. 2.24). Fig. 2.24a shows a silicon IGBT module (SEMIKRON SKM75GB123D) based half-bridge leg which is the basic building block of the converter. Six such modules are integrated to implement the DSC as shown in Fig. 2.24b. The ASC diode bridges are implemented with IXYS fast recovery diodes MEE 75-12 DA. For

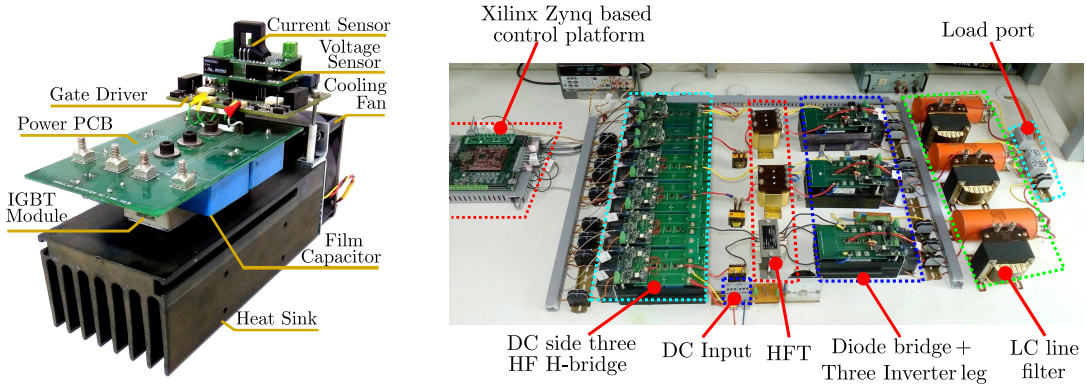


Figure 2.24: (a) Basic building block: the half-bridge IGBT module, (b) 3ϕ converter Hardware prototype

the active switches in ASC, SEMIKRON SKM75GB123D IGBT modules are employed. Table 2.2 summaries the component details of the hardware prototype. The switching frequency of the DSC is 20kHz, whereas ASC active switches are switched at 50Hz. A DSP-FPGA based System on Chip (SoC) controller platform (Xilinx Zynq-7000) is used to generate required PWM signals of the converter. Optically isolated intelligent gate driver ICs (ACPL-339J) with voltage levels $\pm$15V are used to drive the IGBT devices. 15Ω gate resistance is used externally. An effective dead time of 600 ns is provided between the gating signals of top and bottom IGBT devices of an IGBT module. For three winding high frequency transformers ferrite E core (E80/38/20) from EPCOS are used. Details of the transformer in given in Table 2.2.

The converter is modulated in open loop at the operating conditions given in Table 2.3. As described in the modulation section, in order to generate the AC output voltage one requires reference signals $m_{(a,b,c)}(t)$. These reference voltages are generated from three-phase balanced internal sinusoidal signals at frequency f_o. In order to compute modulation index M, given the turns ratio n and V_{dc}, we need to find the value of V_{pk}.

Table 2.2: Hardware details

Component	Particulars
Active switches	SKM75GB123D (1200V,75A)
Diode	MEE 75-12 DA (1200V,75A)
HFT	Turns ratio (N1:N2:N2)- 51:34:34, Enamelled copper wire-21 SWG, Core material- ferrite E80/38/20, $L_m = 23mH$, $L_{lkT} = 6 - 8\mu H$
Series inductor with HFT	$36\mu H$
Filter inductor	L_f =2.3mH
Filter capacitor	$10\mu F$
Controller	Xilinx Zynq-7000 based SoC platform

Table 2.3: Operating Condition of the topology 1

Parameter	Values
Output Power, P (kW)	6.2
DC input, V_{dc} (V)	440
Grid voltage peak , V_{gpk} (V)	252
Output frequency, f_o (Hz)	50

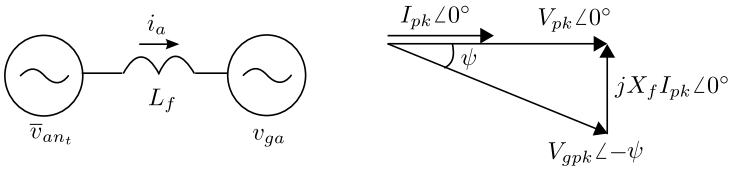


Figure 2.25: Equivalent circuit showing grid connection of the converter and phasor diagram corresponding to phase a

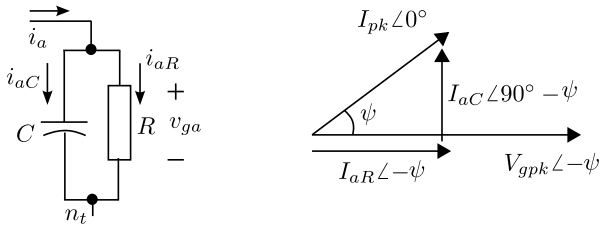


Figure 2.26: Grid is modelled as parallel RC branch for a particular operating point

The converter can support only instantaneous unidirectional power flow. So, $\overline{v}_{in_t}$ and line currents $i_{a,b,c}$ must be in phase. Fig. 2.25 shows per phase equivalent circuit (here for phase a) of the converter connected to the grid along with the phasor diagram for the line frequency (f_o) components. Equation (2.57) represents the phasor diagram and can be solved along with the fact that $P = 1.5V_{pk}I_{pk}$, to find V_{pk} in terms of the parameters given in Table 2.2 and Table 2.3, (2.58). Once, V_{pk} is known one can determine I_{pk} from P.

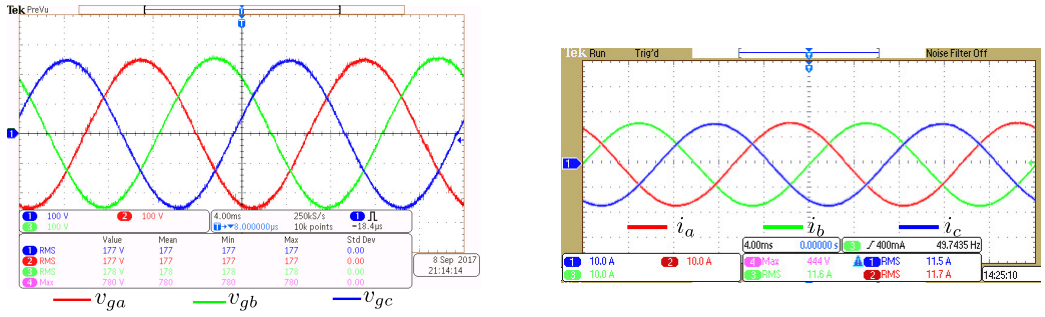
$$V_{pk}\angle 0^\circ = V_{gpk}\angle -\psi + jX_f I_{pk}\angle 0^\circ \tag{2.57}$$

$$V_{pk} = \left(\frac{V_{gpk}^2}{2} + \sqrt{\frac{V_{gpk}^4}{4} - \left(\frac{X_f P}{1.5}\right)^2}\right)^{1/2} \tag{2.58}$$

where $X_f = \omega_o L_f$. The line current leads the grid voltage by $\psi = \cos^{-1}\left(\frac{V_{pk}}{V_{gpk}}\right)$. The line current has an in phase ($I_{aR} = I_{pk}\cos\psi$) and a leading quadrature ($I_{aC} = I_{pk}\sin\psi$) components with respect to the grid voltage (Fig. 2.26). Because the power is unidirectional, the grid can be modelled as parallel RC network for a particular operating point, V_{gpk} and P (Fig. 2.26). Where, The value of $R = \frac{V_{gpk}}{I_{aR}}$ and $C = \frac{I_{aC}}{\omega_o V_{gpk}}$.

2.5.1 Experimental validation of modulation strategy

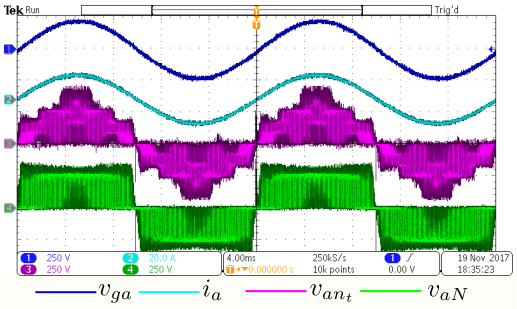
This section presents key experimental results to validate the modulation strategy of the 3ϕ converter (Fig. 2.5).



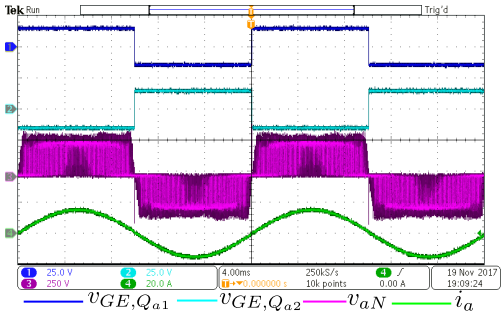
(a) (b)

Figure 2.27: (a) Output phase voltages: [CH1] c phase voltage (100V/div.), [CH2] a phase voltage (100V/div.), [CH3] b phase voltage (100V/div.). Time scale 4ms/div. (b) Output current waveforms: [CH1] c phase current (10A/div.), [CH2] a phase current (10A/div.), [CH3] b phase current (10A/div.). Time scale 4ms/div.

Fig. 2.27a shows the output voltage waveforms $v_{g-a,b,c}$. The waveforms have a peak of approximately 250V. The high frequency switching ripple in the pole voltages is filtered by the line inductors L_f. The line currents shown in Fig. 2.27b have a peak 16.4A. Fig. 2.28a shows grid voltage, line current and pole voltage with respect to load neutral (n_t) and pole voltage with respect to the transformer neutral point (N) of phase a. The line current i_a leads the load voltage v_{ga} by an angle 2.77°. Due to the presence of switching frequency common-mode

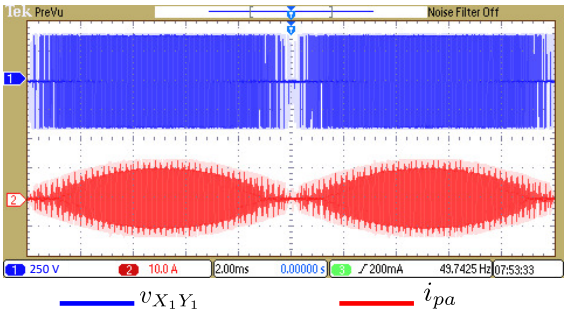


(a)

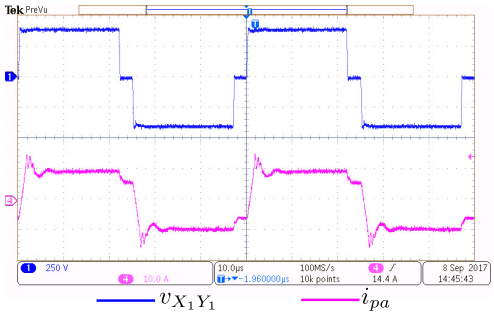


(b)

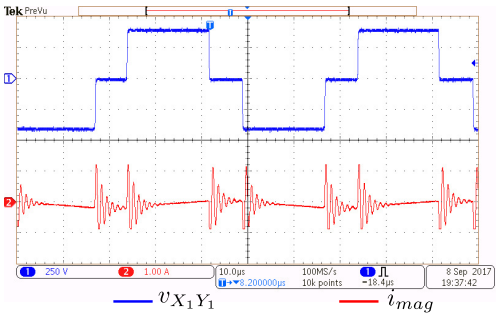
Figure 2.28: (a) Pole voltage waveforms-[CH1] Load voltage (250V/div.), [CH2] line current (20A/div.), [CH3] pole voltage w.r.t load neutral (250V/div.), [CH4] pole voltage w.r.t transformer neutral (250V/div.) of phase a. Time scale 4ms/div. (b) Line frequency switching-[CH1] Gate-emitter voltage of Q_{a1} (25V/div.), [CH2] gate-emitter voltage of Q_{a2} (25V/div.), [CH3] pole voltage w.r.t transformer neutral (250V/div.), [CH4] line current (20A/div.) of phase a. Time scale 4ms/div.



(a)



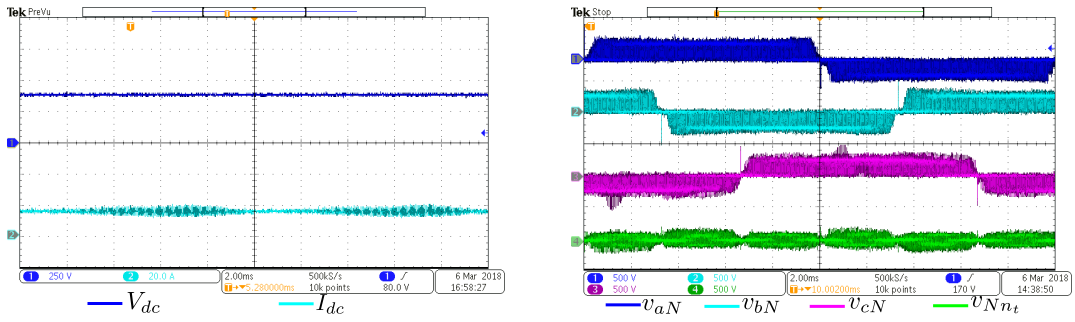
(b)



(c)

Figure 2.29: (a) Over a line cycle- HFT [CH1] input voltage (250V/div.) and [CH2] input current (10A/div.). Time scale 2ms/div. (b) Over a switching cycle- HFT [CH1] input voltage (250V/div.) and [CH4] input current (10A/div.). Time scale 10μs/div. (c) HFT [CH1] input voltage (250V/div.) and [CH2] magnetising current (1A/div.). Time scale 10μs/div.

voltage the instantaneous waveforms of v_{aN} and v_{an_t} are not same. Fig. 2.28b present the gate-emitter voltages of Q_{a1} and Q_{a2} along with the pole voltages w.r.t N and line current of phase a. These figures show that, Q_{a1} and Q_{a2} are complementary switched at line frequency and Q_{a1} is conducting when the line current i_a is positive. The primary voltage of the transformer

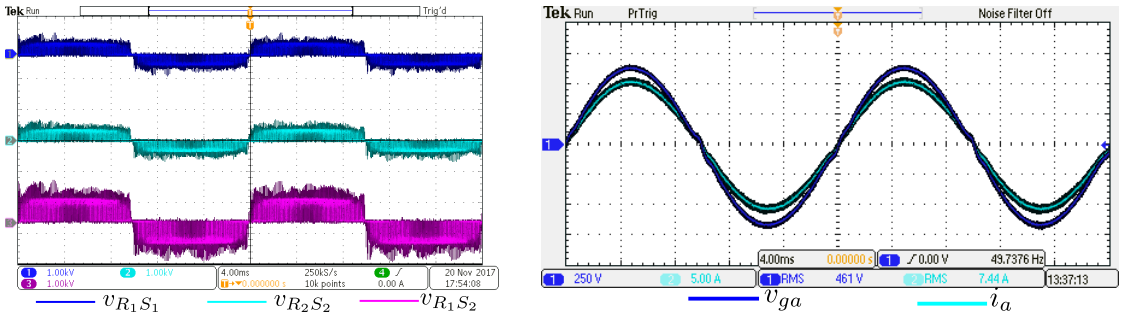


(a) (b)

Figure 2.30: (a) DC input- [CH1] Input DC voltage (250V/div.), [CH2] Input DC current (20A/div.). Time scale 2ms/div. (b) Common mode voltage- [CH1] v_{aN} (500V/div.), [CH2] v_{bN} (500V/div.), [CH3] v_{cN} (500V/div.), [CH4] v_{Nn_t} (500V/div.). Time scale 2ms/div.

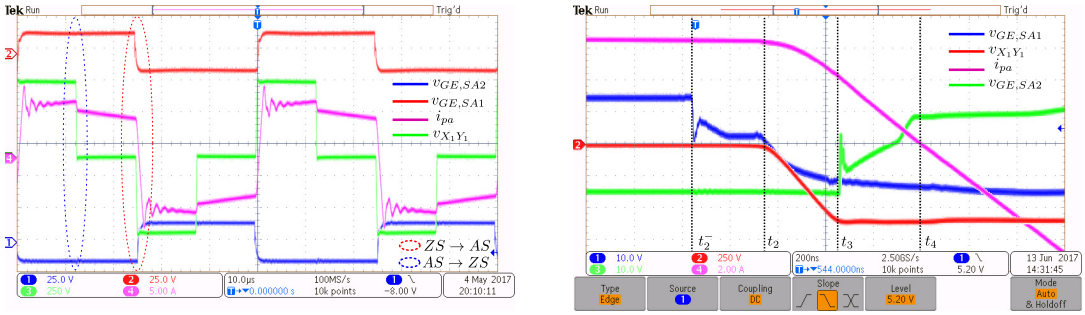
along with the primary current corresponding to phase a is shown in Fig. 2.29a over a line cycle. An expanded view of Fig. 2.29a over two switching cycles ($2T_s$) is shown in Fig. 2.29b. The figure shows applied volt-second across the transformer primary over a switching cycle (T_s) is zero. The primary current has high frequency oscillation due to parasitic capacitance of the diode bridge which is not considered in the analysis. The input voltage and the magnetising current waveform of the HFT of phase a are presented in Fig. 2.29c. The magnetising current is obtained by exciting the system at no load. The experimental result of the magnetising current contains high frequency oscillation at switching transitions. This oscillation appears mainly due to leakage inductance and inter-turn and inter- winding parasitic capacitances of the transformer. High frequency flux balance is clearly observed from the experimental result. Fig. 2.30a present input DC bus voltage and input DC current. The current has high frequency switching ripple. Fig. 2.30b shows the experimental results of the pole voltages with respect to HFT neutral i.e. $v_{(a,b,c)N}$ and v_{Nn_t}. The high frequency v_{Nn_t} cause the common mode current to circulate in the secondary of the converter which can be limited by using common mode choke.

To verify modulation strategy of the multilevel converter in Fig. 2.6, a prototype is used with two cascaded modules ($p = 2$) in the AC side per phase. The experimental results are presented corresponding to phase a. Experiments are done with $V_{dc} = 600V$, $V_{gpk} = 650V$ and per phase output power $P_\phi = 3.5kW$. Fig. 2.31a shows the output voltage of module-1 ($v_{R_1S_1}$), module-2 ($v_{R_2S_2}$) and the resultant output voltage ($v_{R_1S_2}$). The output phase voltage and line current waveforms are shown in Fig. 2.31b. The observed line current peak is 11A.



(a) (b)

Figure 2.31: (a) Pole voltages of multilevel topology (Fig. 2.6): [CH1] pole voltage of module-1 (250V/div.), [CH2] pole voltage of module-2 (250V/div.), [CH3] combined pole voltage of two modules (500V/div.). Time scale $4ms$/div. (b) Load voltage and current waveform of the multilevel topology corresponding to phase a: [CH1] load voltage (250V/div.), [CH3] load current (5A/div.). Time scale $4ms$/div.



(a) (b)

Figure 2.32: (a) Switching transition waveforms: [CH1] Gate-emitter voltage of S_{A2}(25V/div.), [CH2] gate-emitter voltage of S_{A1}(25V/div.), [CH3] HFT input voltage(250V/div.), and [CH4] HFT input current (5A/div). Time $10\mu s$/div. (b) Zero to active state transition: [CH1] gate-emitter voltage of S_{A1}(10V/div.), [CH2] HFT input voltage(250V/div.), [CH3] gate-emitter voltage of S_{A2}(10V/div.) and [CH4] HFT input current (2A/div). Time 200ns/div.

2.5.2 Experimental verification of switching transitions of the DSC

In this section results corresponding to switching transitions of the DSC are shown to validate soft-switching of the converter. Switching transitions of the DSC legs corresponding to phase a is considered for discussion. Fig. 2.32a, shows the gating signals of the switches S_{A1} and S_{A2} along with primary voltage and current waveforms over two switching cycles.

Zero to active state transition

Fig. 2.32b shows the enlarged picture of zero to active state transition. In Fig. 2.32a this transition is marked using red dotted circle. Before the transition, S_{A1} and body diode of S_{A3} are conducting (in Fig. 2.12). A zero voltage is applied across the transformer terminals X_1Y_1. The experimental result shows the switching transition from S_{A1} to S_{A2}. At the end of this transition $-V_{dc}$ is applied across X_1Y_1. At t_2^- the gating signal of S_{A1} is removed. After sometime at t_2, when gate-emitter voltage of S_{A1}, $v_{GE,SA1}$ is almost zero, the voltage across S_{A1} starts rising resulting change in voltage $v_{X_1Y_1}$ seen in Fig. 2.32b. The slow rise of the voltage across the device is due to the device capacitance across the collector-emitter terminals of S_{A1}. This results in reduced turn OFF loss of S_{A1} as discussed previously. In between t_2 and t_3 (in Fig. 2.32b) the transformer current i_{pa} charges the capacitance across S_{A1} and discharges capacitor across S_{A2}. The LC dynamics given by (2.16) are clearly visible from the non-linear change of i_{pa} and $v_{X_1Y_1}$ in Fig. 2.32b. At t_3 when $v_{X_1Y_1}$ is $-V_{dc}$, the capacitor across S_{A2} is completely discharged and the body diode of S_{A2} comes into conduction. Between t_3 to t_4 (Fig. 2.32b) a linear fall i_{pa} verifies equation (2.20). To achieve ZVS turn ON of S_{A2}, gating pulse is applied in between t_3 and t_4 (when the body diode is conducting) as seen from $v_{GE,SA2}$ in Fig. 2.32b. At t_4, the primary current i_{pa} becomes zero. After t_4 linear fall of i_{pa} continues as per (2.23) and is seen in Fig. 2.32b, i_{pa} becomes negative. Switches S_{A2} and S_{A3} start conducting i_{pa}.

At the end of zero to active state transition a high frequency ringing is observed in transformer current i_{pa} (in Fig. 2.32a). Diode parasitic capacitance and transformer series inductance form the resonating circuit and cause this high frequency ringing.

Active to zero state transition

Fig. 2.33 shows the enlarged picture of active to zero state transition. In Fig. 2.32a the transition is marked in blue dotted circle. Before this transition, S_{A1} and S_{A4} were conducting and V_{dc} was applied across the transformer terminal X_1Y_1 (see Fig. 2.9). At t_0^-, gating signal of S_{A4} is withdrawn. After some time when gate-emitter voltage of S_{A4}, $v_{GE,SA4}$ is almost zero (below device threshold voltage 5.5V), the voltage across S_{A4} starts to rise (which is indicated by the fall in $v_{X_1Y_1}$). The slow change in voltage across S_{A4} is due to parasitic capacitance across the device (as the voltage can not change instantaneously across a capacitance). This helps to reduce turn OFF loss of S_{A4}. At t_1 when the voltage across S_{A4} reaches V_{dc}, the voltage across S_{A3} is zero and the body diode of S_{A_3} is forward biased. The transformer terminal X_1Y_1 is shorted through S_{A1} and body diode of S_{A3}. After some time, at t_1^+, gating signal of S_{A3} is

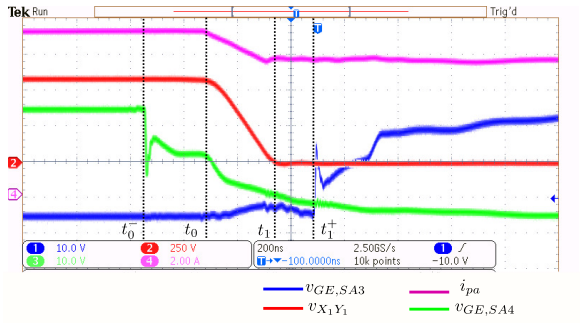


Figure 2.33: Active to zero state switching transition: [CH1] gate-emitter voltage of S_{A3}(10V/div.), [CH2] HFT input voltage(250V/div.), [CH3] gate-emitter voltage of S_{A4}(10V/div.) and [CH4] HFT input current (2A/div). Time 200ns/div.

applied to turn it ON. As the body diode is in conduction, this ensures ZVS turn ON of S_{A3}.

2.5.3 Estimation of circuit parameters

In this section the soft-switching parameters- device capacitance (C_s) and transformer inductance (L_{lk}) are estimated from the experimentally measured waveforms with the help of analytically obtained dynamic circuit equations. The estimated values are validated with actual measurement. Using (2.19) $\omega_p L_{lk}$ can be expressed as-

$$\omega_p L_{lk} = \frac{V_{dc}}{\sqrt{i_{pa}^2(t_2) - i_{pa}^2(t_3)}} \tag{2.59}$$

Again, from (2.21)

$$L_{lk} = \frac{V_{dc}}{i_{pa}(t_3)}(t_4 - t_3) \tag{2.60}$$

For different V_{dc} and load current i_a following parameters are experimentally obtained: $i_{pa}(t_2)$, $i_{pa}(t_3)$, $(t_3 - t_2)$ and $(t_4 - t_3)$. Using these values along with (2.59) and (2.60), L_{lk}, ω_p and C_T are estimated and tabulated in Table 2.4. The measured value of L_{lk} and C_T are given in

Table 2.4: Estimated L_{lk}, ω_p and C_T from experimental data

Experimentally observed					Estimated			
V_{dc}(V)	$i_{pa}(t_2)$(A)	$i_{pa}(t_3)$(A)	(t_3-t_2)(ns)	(t_4-t_3)(ns)	$\omega_p L_{lk}(\Omega)$	$\omega_p(rad/s)$	$L_{lk}(\mu H)$	$C_T(nF)$
200	1.85	1.05	330	250	131	2757435	47.6	2.76
300	3.2	2.3	280	360	134	2871592	46.9	2.58
400	4	2.5	320	330	128	2426184	52.8	3.2
500	6.1	4.5	280	440	121	2483401	48.9	3.3
600	6.4	4.4	300	360	129	2629803	49	2.94

Table 2.5. The measured and estimated values are closely matching. This verifies the switching analysis of the DSC converter presented previously in this chapter.

Table 2.5: Measured L_{lk} and C_T

$L_{lk}(\mu H)$	$C_T(nF)$
53	3.06

2.5.4 Measurement of converter power loss and efficiency

In Fig. 2.34a, experimentally obtained converter efficiency is plotted against the variation of output power from 1kW to 5.3kW. The DC voltage is kept fixed at 420V. The maximum efficiency of 90.6 % is observed at 3kW. The efficiency is relatively low as the experimental setup uses a general purpose hardware which is not optimally designed for the power rating of the experiment.

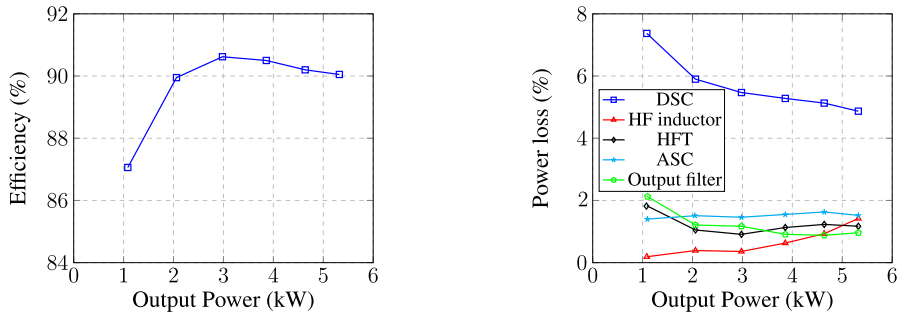


Figure 2.34: (a) Efficiency of the proposed 3ϕ HFL inverter, (b) Power loss at different stages of 3ϕ HFL inverter

Fig. 2.34b presents the variation of power losses of different stages of the converter with output power variation and these losses are obtained experimentally. The DSC has maximum power loss throughout the entire output power range. With increase in output power level, a significant reduction (2.5%) of the DSC power loss is observed. The switching loss contributes major portion of the DSC power loss. With the increase of output power level, the line current peak I_{pk} is increased. As seen in (B.4) and (B.7), θ_1 decreases with the increase of I_{pk}, results in increase of soft turn ON range $(\theta_1, \pi - \theta_1)$ over one half of the line cycle. The ASC has low (1.51%) and flat loss profile throughout the output power range. The flat loss profile indicates that major loss in the ASC is dominated by conduction loss of the diodes and active switches. The line frequency switching of the ASC active switches incurring negligible switching loss results in low loss in the ASC.

In Fig. 2.35a, power loss distribution of the converter is shown as bar diagram at 4.64kW output power. The analytically estimated power losses at the different stages of the converter are matched with the experimentally obtained losses. The DSC contributes around 260W out of 500W of total loss. In Fig. 2.35b, a pie chart is presented showing percentage loss contribution of the different stages of the converter at 4.64kW output power. The DSC incurs more than 50% of total power loss where as line frequency switched ASC contributes only 17%. The benefit of the proposed modulation strategy with line frequency switched ASC compared to

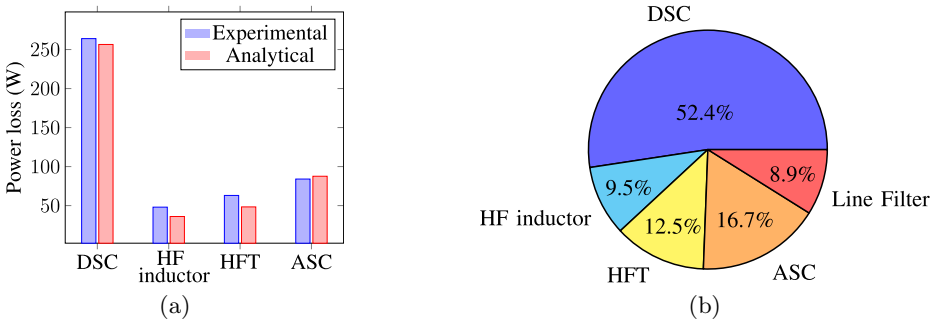


Figure 2.35: (a) Power loss break down at 4.64kW output power obtained experimentally and analytically, (b) Percentage loss distribution shown at 4.64kW output power obtained experimentally

conventional high frequency hard switched VSI of the ASC is clearly observed.

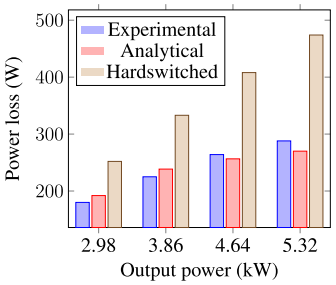


Figure 2.36: DSC power loss: experimental, analytical and complete hard-switched

Fig. 2.36 presents the DSC losses over a variation of output power 3kW-5kW. The figure shows that the analytically estimated DSC losses are closely matched with the experimentally obtained values. The figure also presents the losses corresponding to completely hard-switched DSC. Soft-switching results in 1.5 times reduction of the losses in the DSC of the proposed 3ϕ HFL inverter and thus improving the overall converter efficiency.

2.6 Compensation of line filter drop and reactive power support

The 3ϕ converter in Fig. 2.5 supports only instantaneous unidirectional power flow from DC to AC side due to presence of diode bridge rectifier. Due to line filter reactor grid side power factor will not be unity. Additionally, in case of utility scale PV to grid integration, the converter might need to support $\pm$ 0.9/0.95 PF operation at the grid end as per grid requirements [36]. Here a scheme is shown along with the converter which can support small amount reactive power at the grid end.

The compensation scheme is shown in Fig. 2.37a. A 3ϕ VSI is connected to the common coupling point through a small Line frequency transformer. This 3ϕ VSI supports the reactive power compensating the line filter drop. This can also support reactive power required from the grid end. Here, a computation is shown to compensate the reactive drop of the line filters.

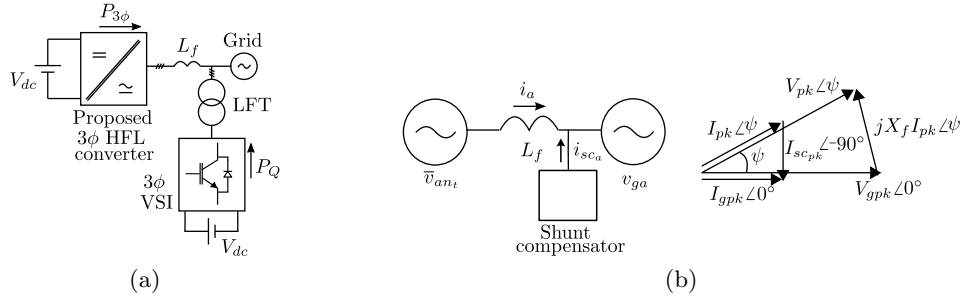


Figure 2.37: (a) Scheme to support reactive power, (b) Equivalent circuit and phasor diagram

The equivalent circuit and the phasor diagram is shown in Fig. 2.37b. The active power supplied to the grid at UPF is given as-

$$P = 1.5V_{gpk}I_{gpk} = 1.5V_{pk}I_{pk} \tag{2.61}$$

From the phasor diagram-

$$\begin{aligned} V_{pk}\angle\psi &= V_{gpk}\angle0° + j(2\pi f L_f)I_{gpk}\angle0° \\ I_{pk}\angle\psi &= I_{gpk}\angle0° - I_{sc_{pk}}\angle90° \end{aligned} \tag{2.62}$$

where L_f is combined line and filter inductance and $I_{sh_{pk}}$ is peak current supplied by the shunt compensator. Considering $V_{gpk} = 1$ p.u. and $I_{gpk} = 1$ p.u and line inductive reactance 0.05 p.u. using equations (2.61) and (2.62) the power rating of the 3ϕ shunt compensator can be shown as 4.5% of P, the power rating of the 3ϕ converter.

2.7 Conclusion

This chapter has introduced a single-stage unidirectional 3ϕ high-frequency link inverter topology with three pulsating DC links. A systematic approach to derive the 3ϕ converter topology from a 1ϕ version is presented. A single-stage unidirectional 3ϕ multilevel topology for direct medium voltage grid integration of the PV sources, is also reported in this chapter. The modulation strategy is discussed in details which ensures complete line frequency switching of the AC side converter active switches. The circuit analysis of the converter in all the switching modes over a switching cycle is presented in details. The analysis gives the conditions on dead times of the DSC half-bridge legs to achieve soft turn ON. In some parts of the line cycle (near the zero crossing of the line currents) where the line current magnitudes are small, the DC side converter half-bridge legs are hard-switched. The converter filtering requirements which are indicated by the input current and output voltage THDs are derived. The analytical loss estimation of the converter is provided. The converter operation, particularly, different aspects of the modulation strategy, ZVS transitions are experimentally verified on laboratory scale hardware prototype. The experimental results are presented with detailed discussions. The

converter efficiency and different stage power losses are experimentally measured. The analytically estimated power loss is verified with experimentally obtained values. The topology supporting unidirectional DC to AC power flow, is primarily targeted for grid integration of utility scale photovoltaic sources.

Chapter 3

Unidirectional HFL DC-3ϕ AC Conversion with Three Pulsating DC Links: Topology-2

3.1 Introduction

In chapter 2, the three phase HFL inverter topology shown in Fig. 2.5 achieves complete line frequency switching of the active switches of the ASC. The DSC is soft-switched in some parts of the line cycle. To generate three pulsating DC links, the DSC employs six half-bridge legs i.e 12 active switches. Per phase, two half-bridge legs are used. The number of active switches used in the DSC is relatively high compared to a standard multi-stage solution or single stage solutions reported in [17, 28–30]. It has an impact on converter cost, efficiency and reliability.

In this chapter a new converter topology is explored which reduces the number of half-bridge legs on the DSC and improves its soft-switching performance. The new topology is derived from the topology 1. The structure of the ASC remains same as Fig.2.5 and the adopted modulation strategy ensures line frequency switching of all the active switches in ASC like topology-1.

The derivation of the new topology along with the modulation strategy is discussed first. The circuit operation showing soft-switching process are presented in details. The improvement of the soft-switching performance compared to topology-1 is discussed. The analytical expressions of the converter power loss is given. The operation of the converter is experimentally verified in a 4kW hardware prototype. The content of this chapter is reported in [37].

3.2 Topology synthesis and modulation strategy

In this section, first we revisit the DSC structure of the topology-1 (see Fig. 2.5) and its modulation strategy. From the modulation strategy, the redundant half-bridge legs are identified. The new 3ϕ topology is derived by removing the redundant DSC legs. The modulation strategy of the converter is also discussed.

Fig. 3.1 shows the topology 1 presented in chapter 2 and its modulation strategy. To generate pulse width modulated high frequency AC across the HFT primary terminals, X_1Y_1, X_2Y_2 and X_3Y_3, three full-bridges are employed. To implement the phase-shift modulation, the half-bridge legs $S_{A1} - S_{A2}$, $S_{B1} - S_{B2}$ and $S_{C1} - S_{C2}$ are considered as reference legs. The gating signals of the other leg switches are phase shifted w.r.t the reference legs as discussed

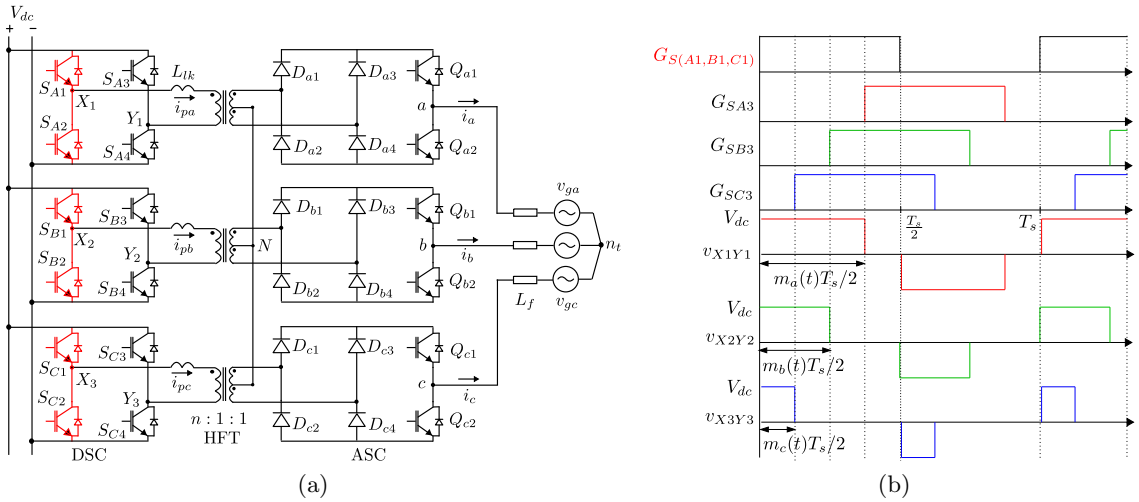


Figure 3.1: (a) 3ϕ HFL inverter with 3 pulsating DC link: topology 1, (b) Modulation strategy of the DSC topology 1.

in chapter 2. Though it is not necessary, the switches S_{A1}, S_{B1} and S_{C1} of the reference legs, can have same gating signals, $G_{S(A1,B1,C1)}$, as shown in Fig. 3.1b. The gating signals of S_{A3}, S_{B3} and S_{C3} are phase shifted by $\frac{m_aT_s}{2}$, $\frac{m_bT_s}{2}$ and $\frac{m_cT_s}{2}$ respectively w.r.t $G_{S(A1,B1,C1)}$. The applied voltages $v_{X_1Y_1}$, $v_{X_2Y_2}$ and $v_{X_3Y_3}$ are shown in Fig. 3.1b.

Following the above modulation strategy, the three reference half-bridge legs with same gating signals have redundancy. If the HFT primary terminals X_1, X_2 and X_3 are shorted, the above modulation strategy can be implemented with only one reference leg. This results in an improved HFL inverter topology which is referred as topology 2. The new topology has 8 active switches (4 half-bridge legs) on the DSC. The modified structure of the new converter has great impact on the soft-switching performance which will be discussed in section 3.3.10.

Fig. 3.2a shows the converter configuration of the topology 2. The reference leg $S_1 - S_2$ is highlighted in red. The HFT primary windings are connected in star and the star point (X), is connected to the pole of the reference leg. Fig. 3.2b shows the modulation strategy of the DSC. The gating pulse of the reference leg switch S_1, G_{S1} is shown. The gating signals of S_{A3}, S_{B3} and S_{C3} are phase shifted by $\frac{m_aT_s}{2}$, $\frac{m_bT_s}{2}$ and $\frac{m_cT_s}{2}$ respectively w.r.t G_{S1}. The applied PWM HFAC voltages v_{XY_1}, v_{XY_2} and v_{XY_3}, across the transformer terminals, XY_1, XY_2 and XY_3 are also shown in the figure. The modulation signals $m_{a,b,c}$ are same as defined in (2.5).

The ASC modulation strategy is same as the topology 1. The ASC diode bridge rectifiers rectify the three PWM HFAC voltages. The half-bridge legs of the ASC are line frequency switched based on the line current directions. For example, in case of phase a, when $i_a > 0$, Q_{a1} is turned ON and the top diodes D_{a1}, D_{a3} take part in high frequency rectification. Q_{a2} conducts and D_{a2}, D_{a4} rectify HFAC when $i_a < 0$. This results in generation of unipolar sine PWM pole voltages v_{aN} with voltage levels 0 and $\pm\left(\frac{V_{dc}}{n}\right)$ with respect to N. The average 3ϕ pole voltages with respect to HFT secondary neutral N are given in (2.6).

In the next section, the steady state operation of the converter is described. Modification

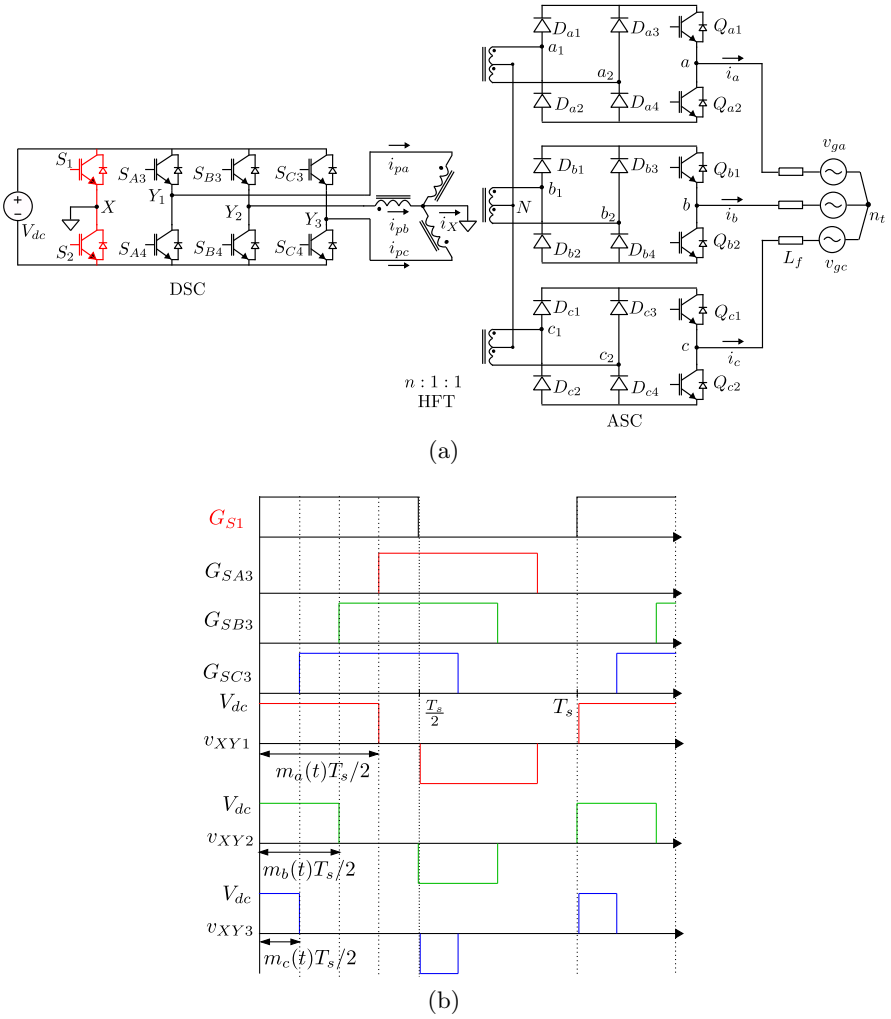


Figure 3.2: (a) 3ϕ HFL inverter with 3 pulsating DC link: topology 2, (b) Modulation strategy of the DSC of topology 2.

in the DSC structure has changed the circuit dynamics in comparison with topology 1.

3.3 Steady-state operation

The operation of the topology 2 is described over a switching cycle (T_s). The active switches of the ASC are line frequency switched. In the following discussion, it is considered that ASC active switches do not change the switching states over the switching cycle (T_s) under consideration. The circuit dynamics due to the switching of the DSC is discussed in details. The reference half-bridge leg $S_1 - S_2$ is soft-switched over complete line cycle and the other DSC legs, $S_{X3} - S_{X4}$ ($X \in \{A, B, C\}$), are soft-switched in some parts of the line cycle like topology 1. The soft-switching is achieved with the help of device parasitic capacitances (C_s) and transformer leakage and additional series inductance (L_{lk}). For ease of the analysis, slowly varying properly filtered line currents $i_{a,b,c}$ are considered as constant current sources with magnitude $I_{a,b,c}$ over a switching cycle T_s. The switching process of the converter is described

when $i_a = I_a$ and $i_b = I_b$ but $i_c = -I_c$ and $I_c > I_a > I_b$. In other regions similar switching process will be followed. Switching waveforms over T_s are shown in Fig. 3.3. The circuit dynamics in one half of the switching cycle (T_s) is divided into ten modes (1-10), other half evolves in an identical fashion.

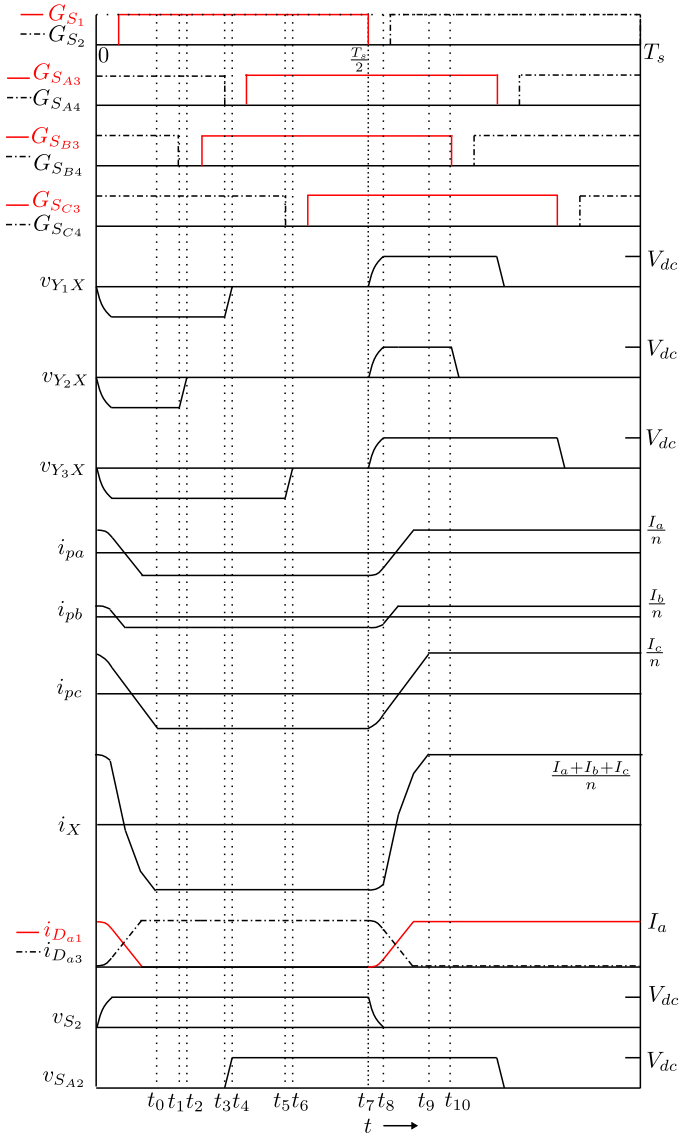


Figure 3.3: Switching waveforms over T_s

3.3.1 Mode 1 ($t_0 < t < t_1$)

In this mode the DSC switches S_1 and S_{X4} ($X \in \{A, B, C\}$) are conducting (Fig. 3.4). The equivalent circuit is shown in Fig. 3.5a. Negative voltage $-V_{dc}$ is applied across HFT primary terminals Y_1X, Y_2X and Y_3X. The HFT primary currents, $i_{pj} = -\dfrac{I_j}{n}$ where ($j \in \{a, b, c\}$) as shown in Fig. 3.3. The voltage polarity and direction of currents indicate active power flow from DC to AC side in all three phases (all three phases are in active state). In secondary D_{a3}, Q_{a1}; D_{b3}, Q_{b1} and D_{c2}, Q_{c2} are conducting.

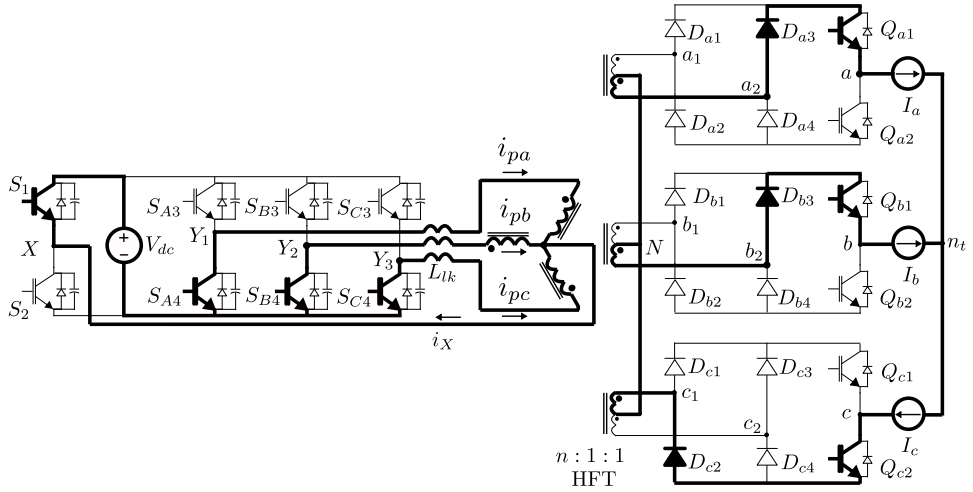


Figure 3.4: Simplified circuit diagram in *Mode 1* ($t_0 < t < t_1$ in Fig. 3.3)

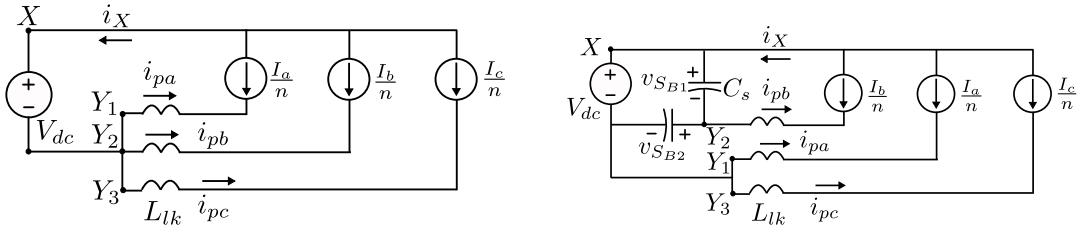


Figure 3.5: (a) Equivalent circuit diagram in *Mode 1*, (b) Equivalent circuit diagram in *Mode 2*.

3.3.2 Mode 2 ($t_1 < t < t_2$)

At t_1, S_{B4} is turned OFF (Fig. 3.6). Active to zero state transition of phase b starts at t_1. Due to device capacitance (C_s), the voltage across S_{B4} can not rise immediately. Voltage starts rising slowly across the device resulting in reduced turn OFF loss of S_{B4}. b phase primary current $-\frac{I_b}{n}$ starts charging the capacitance across S_{B4} and discharging the capacitance across S_{B3}. Equivalent circuit in this mode is shown in Fig. 3.5b. From the equivalent circuit it can be shown that the voltages across S_{B3}, $v_{S_{B3}}$ falls as per (3.1).

$$v_{S_{B3}}(t) = V_{dc} - \frac{I_b}{2nC_s}(t - t_1) \tag{3.1}$$

Phase a and c remain in active state during this duration.

3.3.3 Mode 3 ($t_2 < t < t_3$)

At t_2, the capacitor across S_{B3} is completely discharged. The anti-parallel diode of S_{B3} starts conducting (Fig. 3.7). After t_2, S_{B4} blocks V_{dc}. The duration $t_{az_b} = (t_2 - t_1)$ is given in (3.2).

$$t_{az_b} = \frac{2nC_sV_{dc}}{I_b} \tag{3.2}$$

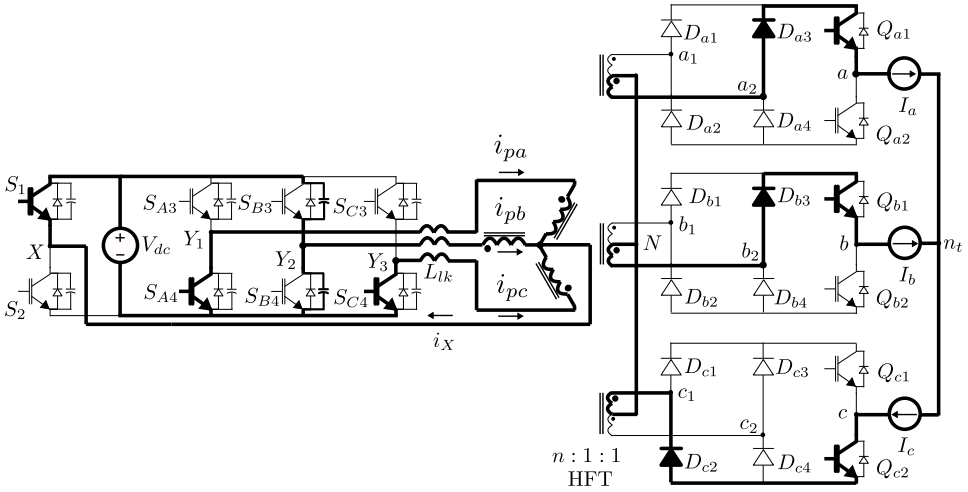


Figure 3.6: Simplified circuit diagram in *Mode 2* ($t_1 < t < t_2$ in Fig. 3.3)

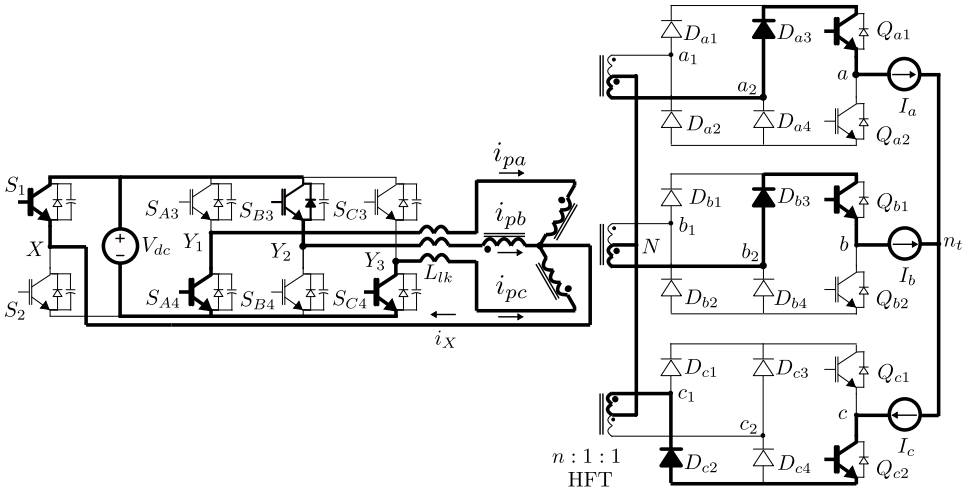


Figure 3.7: Simplified circuit diagram in *Mode 3* ($t_2 < t < t_3$ in Fig. 3.3)

The primary of b phase HFT is shorted through S_1 and anti-parallel diode of S_{B3}. To achieve ZVS transition, S_{B3} is turned ON in this mode (dead time between S_{B4} and S_{B3} must be greater than t_{az_b}). Equivalent circuit in this mode is shown in Fig. 3.8a. Phase b is in zero state i.e no active power is transferred from DC to AC side in phase b.

3.3.4 Mode 4-6

Similar active to zero state transitions occur in phase a in *Mode 4 ($t_3 < t < t_4$)* with reduced turn OFF loss of S_{A4} and in phase c in *Mode 6 ($t_5 < t < t_6$)* with reduced turn OFF loss of S_{C4} due to device capacitance. In *Mode 5 ($t_4 < t < t_5$)*, phase a, b are in zero states and phase c is in active state. S_{A3} is turned ON to ensure ZVS when its anti-parallel diode is conducting.

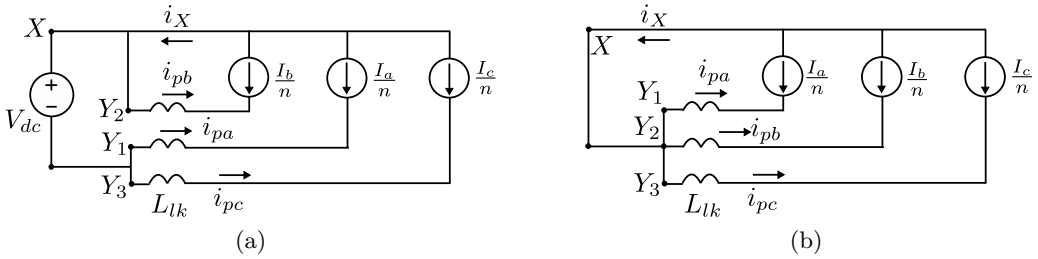


Figure 3.8: (a) Equivalent circuit diagram in *Mode 3*, (b) Equivalent circuit diagram in *Mode 7*.

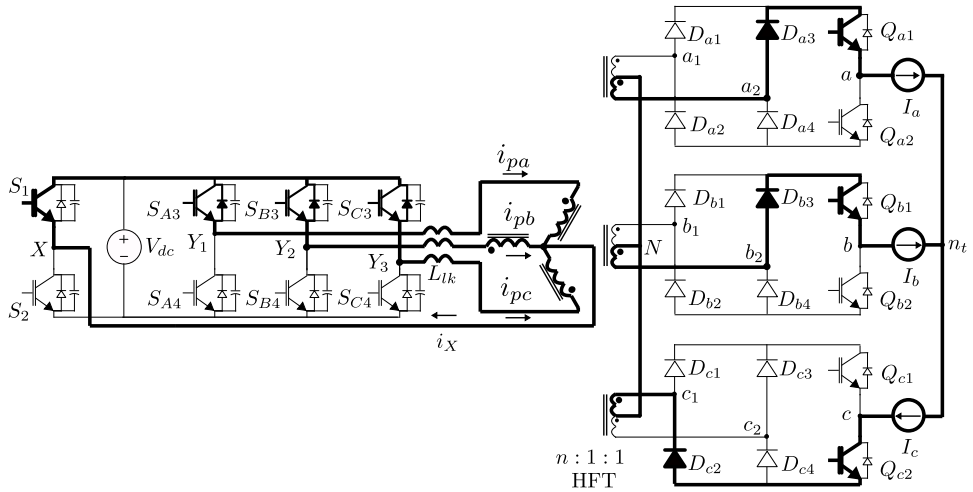


Figure 3.9: Simplified circuit diagram in *Mode 7* ($t_6 < t < t_7$ in Fig. 3.3)

3.3.5 Mode 7 ($t_6 < t < t_7$)

In this mode, all three phases are in zero state. HFT primary terminals Y_1X, Y_2X and Y_3X are shorted through S_1 and the anti-parallel diodes of S_{X3} (Fig. 3.9). ZVS turn ON of S_{C3} is achieved in this interval. No active power is transferred from DC to AC side. Equivalent circuit is shown in Fig. 3.8b.

3.3.6 Mode 8 ($t_7 < t < t_8$)

At t_7, S_1 is turned OFF. Due to device capacitance C_s, voltage across S_1, v_{S_1} can not rise immediately, resulting in reduced turn OFF loss of S_1. The neutral current i_X starts charging the capacitor (C_s) across S_1 and discharging the capacitor across S_2 (Fig. 3.10). Equivalent circuit in this mode is shown in Fig. 3.11a. A positive voltage appears across the HFT primaries (Y_1X, Y_2X and Y_3X). Secondary diodes D_{a1}, D_{b1} and D_{c4} are forward biased and start conducting. This results in shorting of HFT secondary windings (Fig. 3.11a) and the primary circuit dynamics become independent of secondary line currents. In primary, the voltage polarity is against the direction of currents through L_{lk} resulting in reduction of

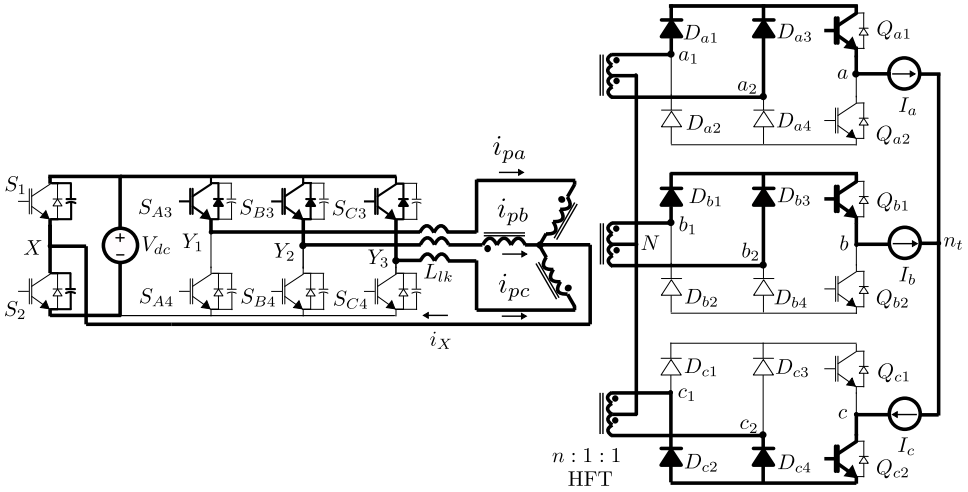


Figure 3.10: Simplified circuit diagram in *Mode 8* ($t_7 < t < t_8$ in Fig. 3.3)

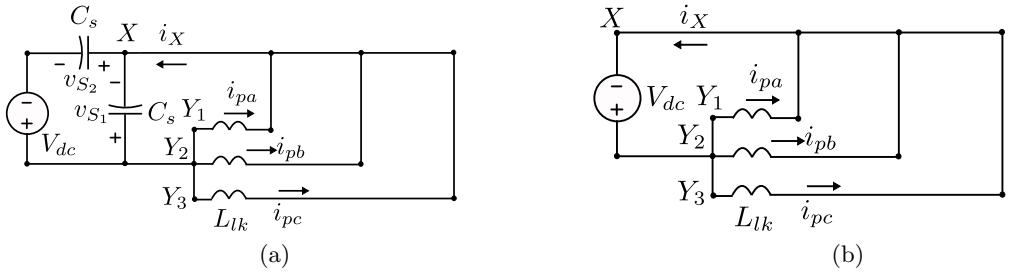


Figure 3.11: (a) Equivalent circuit diagram in *Mode 8*, (b) Equivalent circuit diagram in *Sub-mode 1* of *Mode 9*

magnitudes of primary currents (i_{pa}, i_{pb} and i_{pc}). Circuit equations are given in (3.3).

$$\begin{aligned} i_X &= i_{pa} + i_{pb} + i_{pc} \\ V_{dc} &= v_{S_1} + v_{S_2} \\ i_X(t) &= C_s \left(\frac{dv_{S_1}}{dt} - \frac{dv_{S_2}}{dt} \right) \\ \frac{di_{pa}}{dt} &= \frac{di_{pb}}{dt} = \frac{di_{pc}}{dt} = -\frac{v_{S_1}}{L_{lk}} \end{aligned} \tag{3.3}$$

Where v_{S_1} and v_{S_2} are the voltages across S_1 and S_2. Solving (3.3) following expressions of voltage and currents are obtained.

$$\begin{aligned} i_X(t) &= i_X(t_7) \cos \omega_r (t - t_7) \\ i_X(t_7) &= -\frac{I_a + I_b + I_c}{n} \\ i_{pj}(t) &= i_{pj}(t_7) - \frac{i_X(t_7)}{3} \left(1 - \cos \omega_r (t - t_7)\right) \\ v_{S_1}(t) &= \frac{\omega_r L_{lk} i_X(t_7)}{3} \sin \omega_r (t - t_7) \end{aligned} \tag{3.4}$$

Where $j \in \{a, b, c\}$ and $\omega_r = \sqrt{\frac{3}{2L_{lk}C_s}}$. At t_8, v_{S_1} reaches V_{dc} and $v_{S_2} = 0$. The anti-parallel diode of S_2 is forward biased and starts conducting. The duration of *Mode 8*, $t_{za_1} = (t_8 - t_7)$ is expressed as

$$t_{za_1} = \frac{1}{\omega_r} \sin^{-1}\left(\frac{3V_{dc}}{\omega_r L_{lk} i_X(t_7)}\right) \tag{3.5}$$

To avoid hard turn ON of S_2, the dead time between $S_1 - S_2$ should be greater than t_{za_1}. For the capacitor across S_2 to be completely discharged following condition must be satisfied

$$\omega_r L_{lk} i_X(t_7) \geq 3V_{dc} \tag{3.6}$$

Else the circuit will enter into resonant oscillation mode with angular frequency ω_r and will remain in this mode till the gating pulse of S_2 is being applied.

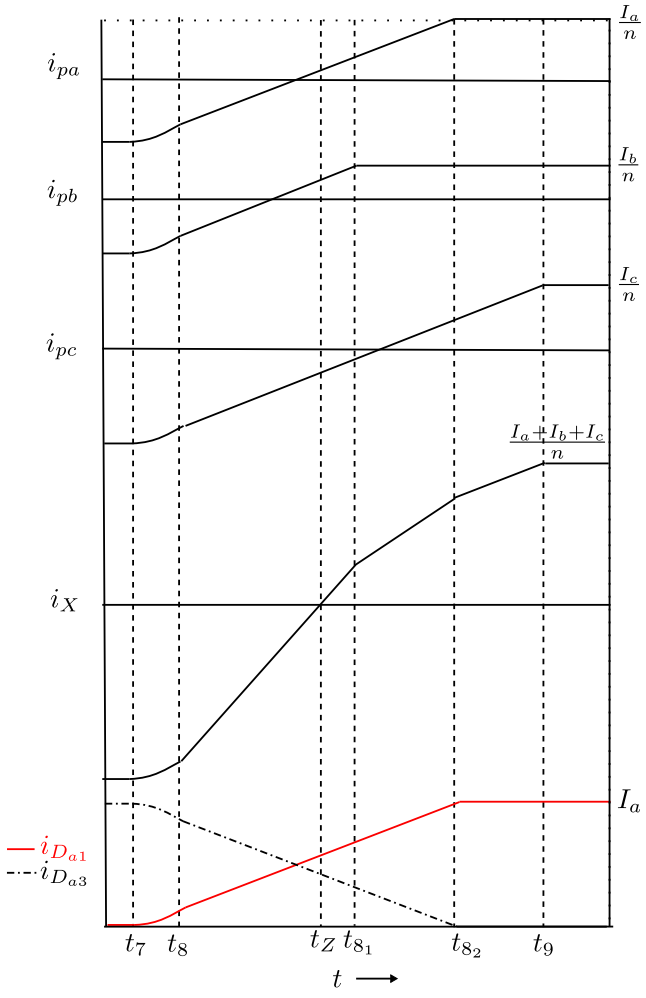


Figure 3.12: Enlarged current wave forms in *Mode 9*

3.3.7 Mode 9 ($t_8 < t < t_9$)

From (3.4), $|i_{pj}(t_7) - i_{pj}(t_8)|$ have same values for $j = a, b, c$. So, $|i_{pc}(t_8)| > |i_{pa}(t_8)| > |i_{pb}(t_8)|$ as $I_c > I_a > I_b$. In this mode, the primary currents i_{pj} change the direction linearly and

whenever i_{pj} reach $\frac{I_j}{n}$ the circuit dynamics of the corresponding phase is complete. Based on the magnitude at t_8, first b phase primary current reaches $\frac{I_b}{n}$ and then a and then c phase primary currents reach $\frac{I_a}{n}$ and $\frac{I_c}{n}$ respectively (see Fig. 3.12). *Mode 9* is divided into three sub-modes. As the DSC switches $S_{A3,B3,C3}$ are already ON (ZVS) before entering into this mode, in the sub-modes initially the anti-parallel diodes and then active switches ($S_{A3,B3,C3}$) take part in conduction based on the direction of i_{pj}.

Sub-mode 1 ($t_8 < t < t_{8_1}$)

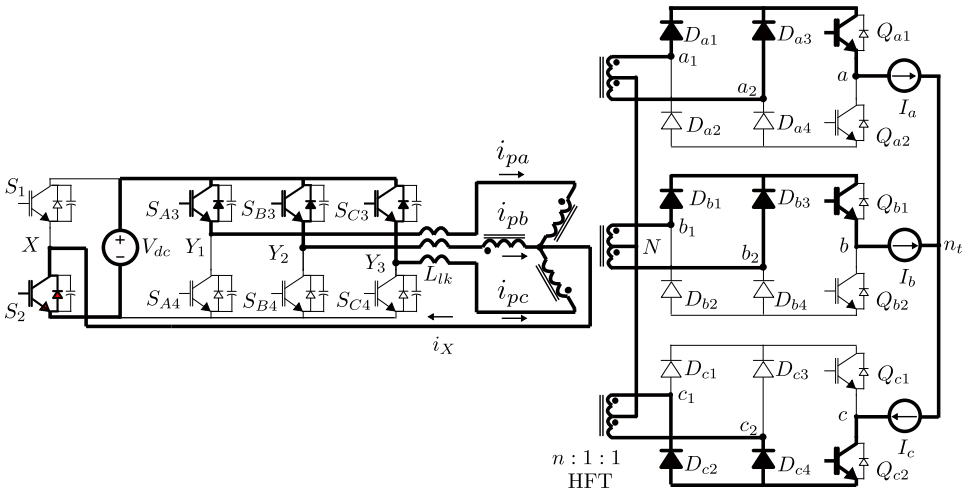


Figure 3.13: Simplified circuit diagram in *Sub-mode 1* ($t_8 < t < t_{8_1}$ in Fig. 3.12)

Simplified circuit in this sub-mode is shown in Fig. 3.13 and the equivalent circuit is shown in Fig. 3.11b. As the voltage polarity applied across the HFT primaries is against the direction of currents through L_{lk}, primary currents and i_X fall linearly as in (3.7).

$$\begin{aligned} i_X(t) &= i_X(t_8) - \frac{3V_{dc}}{L_{lk}}(t - t_8) \\ i_{pj}(t) &= i_{pj}(t_8) - \frac{V_{dc}}{L_{lk}}(t - t_8) \end{aligned} \tag{3.7}$$

In secondary, line currents are transferred linearly from D_{a3}, D_{b3} and D_{c2} to D_{a1}, D_{b1} and D_{c4} respectively. In Fig. 3.12, currents through D_{a1} and D_{a3} are shown. In this interval i_{pb} changes its direction.

Sub-mode 2 ($t_{8_1} < t < t_{8_2}$)

At t_{8_1}, i_{pb} reaches the active state value $\frac{I_b}{n}$. In secondary, I_b is completely transferred from D_{b3} to D_{b1} and D_{b3} is reverse biased (Fig. 3.15). Equivalent circuit is shown in Fig. 3.14a. As i_{pb} is clamped to $\frac{I_b}{n}$, the slope of i_X changes from $\frac{3V_{dc}}{L_{lk}}$ to $\frac{2V_{dc}}{L_{lk}}$ in this interval. Phase b has completed its zero to active state transition. Other two primary phase currents changes with same slope as in *Sub-mode 1*.

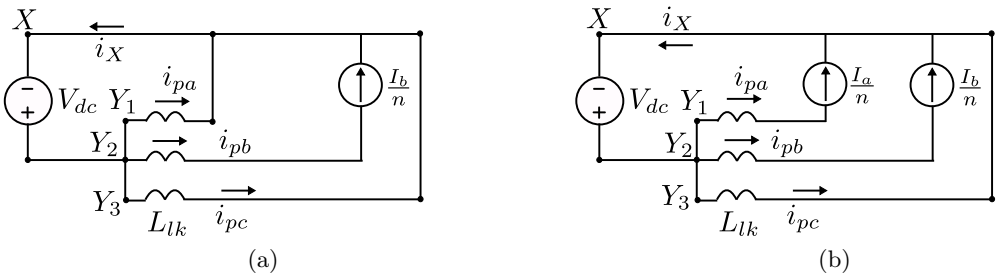


Figure 3.14: (a) Equivalent circuit diagram in *Sub-mode 2* of *Mode 9*, (b) Equivalent circuit diagram in *Sub-mode 3* of *Mode 9*

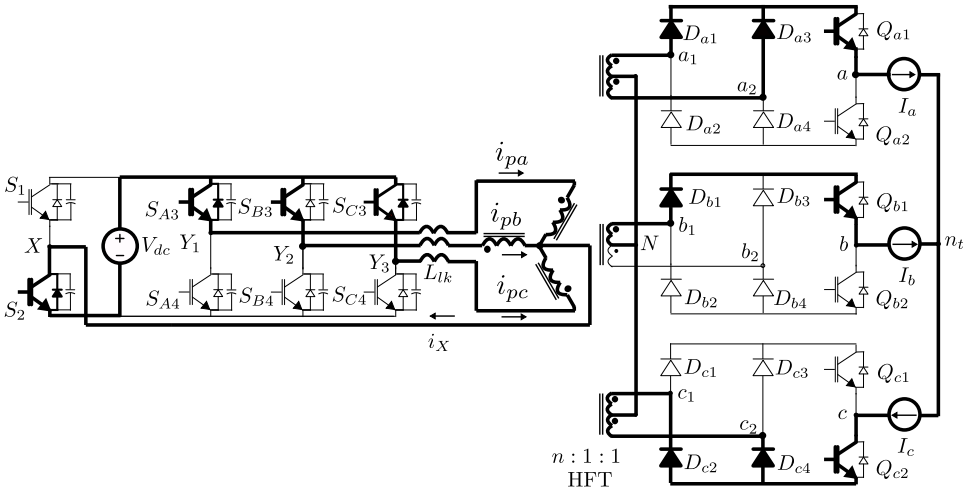


Figure 3.15: Simplified circuit diagram in *Sub-mode 2* ($t_{8_1} < t < t_{8_2}$ in Fig. 3.12)

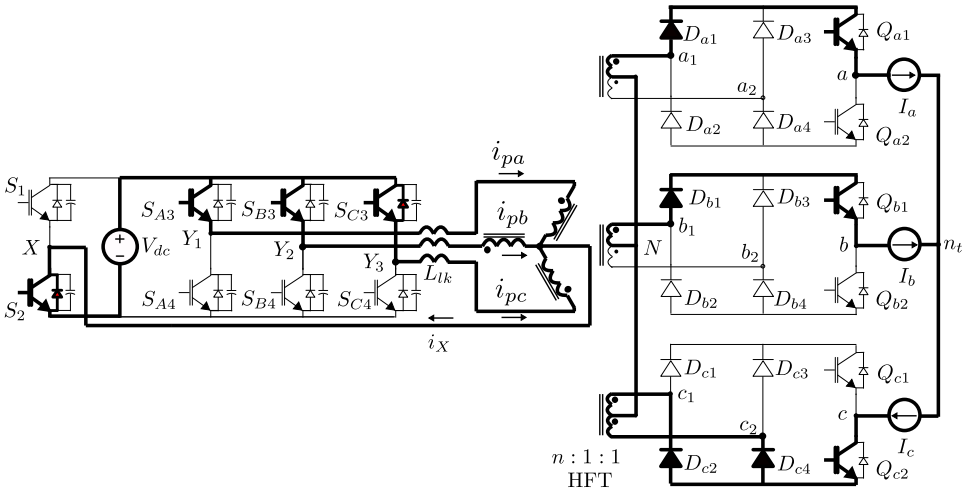


Figure 3.16: Simplified circuit diagram in *Sub-mode 3* ($t_{8_2} < t < t_9$ in Fig. 3.12)

Sub-mode 3 ($t_{8_2} < t < t_9$)

At t_{8_2}, i_{pa} reaches the active state value $\frac{I_a}{n}$. In secondary, I_a is transferred completely from D_{a3} to D_{a1} and D_{a3} is reverse biased (Fig. 3.16). Equivalent circuit is shown in Fig. 3.14b. As, i_{pb} and i_{pa} are clamped to $\frac{I_b}{n}$ and $\frac{I_a}{n}$ respectively, the slope of i_X changes from $\frac{2V_{dc}}{L_{lk}}$ to $\frac{V_{dc}}{L_{lk}}$ in this interval. Phase a has completed its zero to active state transition. Phase c current changes with same slope as in *Sub-mode 2*.

3.3.8 Mode 10 ($t_9 < t < t_{10}$)

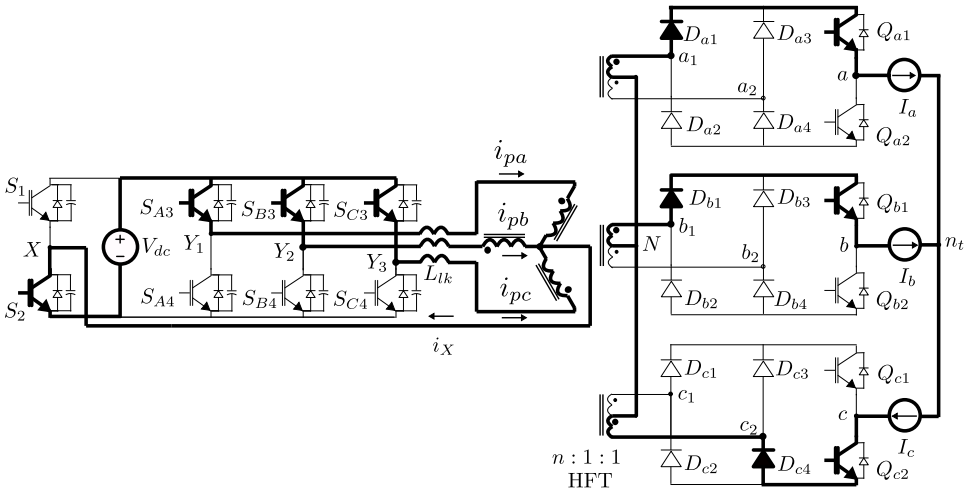


Figure 3.17: Simplified circuit diagram in *Mode 10* ($t_9 < t < t_{10}$ in Fig. 3.3)

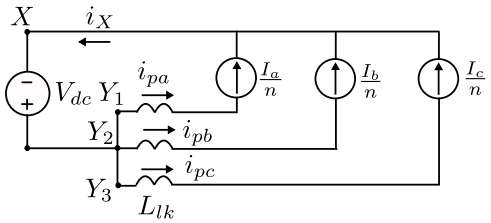


Figure 3.18: Equivalent circuit diagram in *Mode 10*

At t_9, i_{pc} reaches the active state value $\frac{I_c}{n}$. In secondary, I_c is transferred completely from D_{c2} to D_{c4} and D_{c2} is reverse biased (Fig. 3.17). Equivalent circuit is shown in Fig. 3.18. All the phases are in active state and transferring power. The circuit configuration is similar as in *Mode 1*.

In above discussion, polarity reversal of HFT primary voltages and currents are shown in one half of the switching cycle. Similar switching sequence will be followed in rest half of the switching cycle with other symmetrical switches. It is seen that the reference half-bridge leg ($S_1 - S_2$) is switched during zero to active state transition. During active to zero state transitions other three legs of the DSC are switched.

3.3.9 Soft-switching condition of the reference leg $S_1 - S_2$

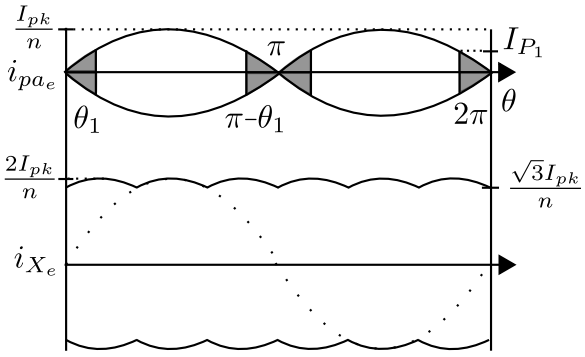


Figure 3.19: Figure showing envelopes of HFT primary and neutral currents

From the above discussion it is clear that, the pole current i_X changes its direction during the switching transition of leg $S_1 - S_2$ (in mode 9). The pole currents of the other DSC legs continue to flow in the same direction during the switching transitions of the legs. This fact pose a strict upper limit on dead time to achieve ZVS turn ON of the switches $S_1 - S_2$ unlike other three legs. Because to achieve ZVS turn ON of an incoming switch (either S_1 or S_2), the gating pulse should be applied when the anti-parallel diode is in conduction. The anti-parallel diode goes out of conduction when pole current i_X changes its direction. Here the upper limit of the dead time over a line cycle is derived.

The slope of i_X is $3S$ in *Sub-mode 1*, $2S$ in *Sub-mode 2* and S in *Sub-mode 3*, where $S = \frac{V_{dc}}{L_{lk}}$. In *mode 8-9*, i_X is changed from $-\frac{I_a + I_b + I_c}{n}$ to $\frac{I_a + I_b + I_c}{n}$. i_X reaches zero at t_Z (see Fig. 3.12). To achieve ZVS turn ON of S_2, it must be turned ON in some time between t_8 and t_Z when the anti-parallel diode of S_2 is in conduction. So, it is important to find $(t_Z - t_7) = (t_Z - t_8) + (t_8 - t_7)$. $(t_8 - t_7)$ is given in (3.5). $\triangle t_Z$ is defined as $\triangle t_Z = (t_Z - t_8)$. In this analysis, $(t_8 - t_7) \simeq 0$ and $i_X(t_7) \simeq i_X(t_8)$ are considered. Hence $(t_Z - t_7) \simeq \triangle t_Z$ and the value depends on the magnitude of i_X at t_8 (see (3.7)).

Let, i_{max} is maximum of I_a, I_b and I_c. Similarly, i_{mid} and i_{min} can be defined. As $i_a + i_b + i_c = 0$, $i_{max} = i_{min} + i_{mid}$. The magnitude of i_X can be given as $\frac{I_a + I_b + I_c}{n} = \frac{2i_{max}}{n}$. The waveform of i_X is square wave at switching frequency T_s and have envelope as i_{X_e} over a line cycle ($\theta = \omega_o t$) as shown in Fig. 3.19.

The objective of the following analysis is to find minimum value of $\triangle t_Z$, $\triangle t_{Z,min}$ over a line cycle. $\triangle t_Z$ depends on S, and the waveform of i_{max}. Here a variable $\alpha = (\theta - 90^\circ)$ is considered for computation. Due to symmetry in i_X envelope, the analysis of $\triangle t_{Z,min}$ is carried out for $0^\circ < \alpha < 30^\circ$. From above assumption, $i_X(t_7) \simeq i_X(t_8) \simeq -\frac{2i_{max}}{n}$ (see (3.4)). The variations of i_{max}, i_{mid} and i_{min} with α is shown in Fig. 3.20 and are given as

$$\begin{aligned} i_{max} &= I_{pk} \cos\alpha \\ i_{mid} &= I_{pk} \sin(\alpha + 30^\circ) \\ i_{min} &= -I_{pk} \sin(\alpha - 30^\circ) \end{aligned} \tag{3.8}$$

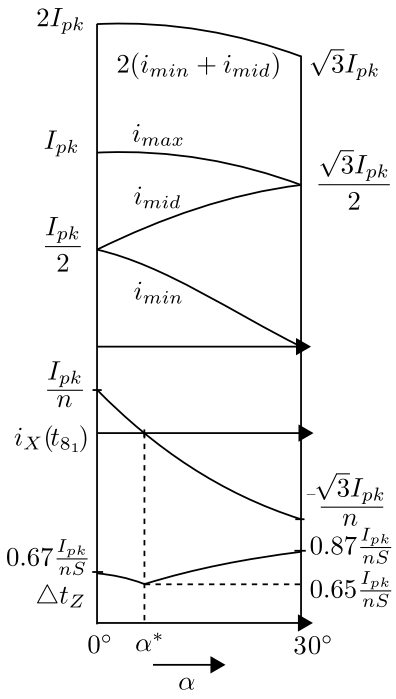


Figure 3.20: Variation of $\triangle t_Z$ over $0^\circ < \alpha < 30^\circ$

Following the operation of *Sub-mode 1*, the time interval $(t_{8_1} - t_8)$ can be expressed as- $(t_{8_1} - t_8) = \dfrac{2i_{min}}{nS}$. Using (3.7), at t_{8_1}, $i_X(t)$ can be expressed as in (3.9).

$$\begin{aligned} i_X(t_{8_1}) =& -\frac{2(i_{max})}{n} + 3S\left(\frac{2i_{min}}{nS}\right) \\ =& \frac{I_{pk}}{n}(\cos\alpha - 3\sqrt{3}\sin\alpha) \end{aligned} \tag{3.9}$$

$i_X(t_{8_1})$ is monotonic in α as shown in Fig. 3.20 and cross α axis at $\alpha^* = 10.89^\circ$. So, when $\alpha < \alpha^*$, the polarity of $i_X(t_8)$ and $i_X(t_{8_1})$ are opposite i.e. within the interval of *Sub-mode 1* $(t_{8_1} - t_8)$, i_X changes its polarity. Hence, $\triangle t_Z$ is given in (3.10).

$$\begin{aligned} \triangle t_Z =& \left(\frac{2i_{max}}{n}\right)\left(\frac{1}{3S}\right) \\ =& \frac{2I_{pk}}{3nS}\cos\alpha \qquad 0^\circ < \alpha < \alpha^* \end{aligned} \tag{3.10}$$

For $\alpha > \alpha^*$, it is possible to show i_X will reach zero in *Sub-mode 2*. i_X will take $\dfrac{i_X(t_{8_1})}{2S}$ amount of time to become zero in *Sub-mode 2*. $\triangle t_Z$ is given in (3.11).

$$\begin{aligned} \triangle t_Z =& \left(\frac{2i_{min}}{nS}\right) + \left(\frac{i_X(t_{8_1})}{2S}\right) \\ =& \frac{I_{pk}}{nS}\sin(\alpha + 30^\circ) \qquad \alpha^* < \alpha < 30^\circ \end{aligned} \tag{3.11}$$

From (3.10) and (3.11), $\triangle t_{Z,min}$ occurs at $\alpha = \alpha^*$ and $\triangle t_{Z,min} = 0.655\frac{I_{pk}}{nS}$. In Fig. 3.20, the variation of $\triangle t_Z$ with α is plotted. To achieve ZVS turn ON of the primary half-bridge leg $S_1 - S_2$ over the complete line cycle, the dead-time, DT should be less than $\triangle t_{Z,min}$. Using (3.5), complete soft-switching condition of $S_1 - S_2$ is given in (3.12).

$$\frac{1}{\omega_r}\sin^{-1}\left(\frac{\sqrt{3}nV_{dc}}{\omega_r L_{lk} I_{pk}}\right) \leq DT \leq 0.655\frac{I_{pk}L_{lk}}{nV_{dc}} \tag{3.12}$$

3.3.10 Comparison of soft-switching performance between topology 1 and 2

In topology 1 the pole currents of all six half-bridge legs have envelopes as i_{pa_e} shown in Fig. 3.19. The pole current magnitudes vary sinusoidally and become zero twice over a line cycle. As discussed in chapter 2, ZVS turn ON of the DSC legs depends on the pole current magnitudes. When the pole current magnitudes are small (near zero crossing of the line currents) all the DSC legs are hard switched. The shaded regions shown on the i_{pa_e} waveform are indicative of the hard-switching zones.

From the DSC operation it is seen that the pole current changes its direction when the corresponding reference leg is switched. This results in a very narrow duration when the anti-parallel diode of the incoming reference leg switch is in conduction. To achieve ZVS turn ON of the reference leg switch, the gating pulse should be applied within this short interval of time. This imposes a strict upper limit on the dead time of the reference leg. With constant dead time and varying magnitude of the pole current, the reference legs have narrow ZVS range compared to the other legs. This fact is also well known in PSFB DC-DC converter literature [38–41]. Hence, the three reference legs of the DSC are soft-switched over very short regions of the line cycle compared to the remaining three legs. The range of ZVS turn ON of the DSC legs are estimated in section 2.4.2 of the chapter 2.

In topology 2, the pole current envelope, i_{X_e} of the reference leg $S_1 - S_2$ is shown in Fig. 3.19. As seen from the figure the magnitude of i_{X_e} varies sinusoidally between $\frac{\sqrt{3}I_{pk}}{n}$ and $\frac{2I_{pk}}{n}$ over a line cycle and never becomes zero. This is due to the fact that now the reference leg pole current $i_X = \frac{I_a + I_b + I_c}{n}$, is the summation of all the three primary winding currents. A dead time can be set using (3.12), such that $S_1 - S_2$ is soft-switched over complete line cycle as discussed in subsection 3.3.9.

But the remaining three legs of the DSC have pole current waveforms as i_{pa_e}, shown in Fig. 3.19. Hence these legs are hard-switched in the shaded regions of Fig. 3.19 when the pole current magnitudes are small. The boundary of hard-switching zone, θ_1, is derived in appendix B and given in (B.7).

3.4 Converter design

We have designed the converter for a target application of grid integration of utility scale solar photo-voltaic. The specification of the design is given in Table 2.1. The topology is modulated at the 85% of its maximum possible modulation index. Hence the modulation

index $M = \frac{nV_{pk}}{V_{dc}} = 0.85$. Thus the high frequency transformer (HFT) primary to secondary turns ratio is $n = 2.0$.

3.4.1 Device blocking voltage and RMS currents

For UPF operation (2.24) and (2.25) are applicable here. The RMS current in switch pair $S_1 - S_2$ is given below.

$$I_{RMS,S_1-S_2} = \frac{I_{pk}}{n}\sqrt{\left[\frac{3}{\pi}\left(\frac{\pi}{3} + \frac{\sqrt{3}}{2}\right)\right]} = \frac{0.901}{M}\frac{P}{V_{dc}} \tag{3.13}$$

The peak current through $S_1 - S_2$ is $I_{pk,S_1-S_2} = \frac{2I_{pk}}{n} = \frac{4}{3M}\frac{P}{V_{dc}}$. With $M = 0.85$, $I_{RMS,S_1-S_2} = 1.06\frac{P}{V_{dc}}$ and $I_{pk,S_1-S_2} = 1.57\frac{P}{V_{dc}}$.
The RMS current in $S_{A3} - S_{C4}$ is expressed as follows.

$$I_{RMS,S_{A3}-S_{C4}} = \frac{I_{pk}}{n}\sqrt{\frac{2M}{3\pi}} = \frac{2\sqrt{2}}{3\sqrt{3M\pi}}\frac{P}{V_{dc}} \tag{3.14}$$

The peak current of $S_{A3} - S_{C4}$ is $I_{pk,S_{A3}-S_{C4}} = \frac{I_{pk}}{n} = \frac{2}{3M}\frac{P}{V_{dc}}$. With $M = 0.85$, $I_{RMS,S_{A1}-S_{C2}} = 0.33\frac{P}{V_{dc}}$ and $I_{pk,S_{A1}-S_{C2}} = 0.78\frac{P}{V_{dc}}$. The Blocking voltage of DC side switches are V_{dc}.
Due to structural similarity, the peak and RMS currents, blocking voltage of the ASC power devices are same as topology 1.

The detailed derivation steps of the RMS currents are given in Appendix A.

3.4.2 Estimation of Converter Power Loss

In this section, power loss expressions of the DSC of the topology 2 is analytically derived. The detailed derivation steps are given in Appendix A. As the switching strategy of the ASC and the current and voltage waveforms seen by the HFTs are same as topology 1, the power loss expressions of the ASC switches, diodes and HFTs are same as given in section 2.4.2 of chapter 2.

Loss estimation of DSC switches and diodes

To estimate the conduction loss of a switch, first the RMS and average currents through the switch are estimated. Using (2.30) the conduction loss expression of the switch is obtained. In a switching cycle, all the active switches and the anti-parallel diodes of the DSC take part in conduction except the anti-parallel diodes of S_1 and S_2. These diodes come in conduction for very small durations during switching transitions. Hence the conduction losses in these diodes are neglected.

The conduction loss in switch pair $S_1 - S_2$ is given as-

$$P_{C_{S_1}} = P_{C_{S_2}} = \frac{3V_{CE}I_{pk}}{n\pi} + 1.827\frac{R_{CE}I_{pk}^2}{n^2} \tag{3.15}$$

Where V_{CE} and R_{CE} are constant voltage drop and on state resistance respectively of the IGBT module. The conduction loss of a switch of $S_{A3} - S_{C4}$ are given as-

$$P_{C_{S_{A3}}} = \frac{MV_{CE}I_{pk}}{4n} + \frac{2M}{3\pi n^2}R_{CE}I_{pk}^2 \tag{3.16}$$

The conduction loss expression of an anti-parallel diodes of switches $S_{A3} - S_{C4}$ is given as

$$\begin{aligned} P_{C_{D,SA3}} =& \frac{V_D I_{pk}}{\pi n} + \frac{R_D I_{pk}^2}{4n^2} \\ & - \frac{MV_D I_{pk}}{4n} - \frac{MR_D I_{pk}^2}{1.5\pi n^2} \end{aligned} \tag{3.17}$$

The anti-parallel diodes have a voltage drop V_D and on state resistance R_D.
Complete ZVS turn ON of $S_1 - S_2$ can be ensured by proper choice of dead time. In Fig. 3.19, the shaded portions in i_{pa_e} indicate hard-switching zones of $S_{A3} - S_{A4}$. The range of soft turn ON of $S_{A3} - S_{A4}$ is given as $(\theta_1, \pi - \theta_1)$, as shown in Fig. 3.19. Details of derivation of θ_1 is given in Appendix B. θ_1 is given in (B.4). The turn OFF of all DSC switches are capacitor assisted soft transition. In this work the range of soft-turn OFF is not derived. In the switching loss calculation the zone of soft turn ON is also considered as zone of soft turn OFF of the DC bridge.

Switching loss in S_{A3} is given as in (3.18).

$$P_{S_{S_{A3}}} = \frac{2V_{dc}I_{pk}}{n\pi T_s}\left(\frac{E_{ON_R} + E_{OFF_R}}{V_{CC}I_C}\right)(1 - \cos\theta_1) \tag{3.18}$$

E_{ON_R} and E_{OFF_R} are the turn ON and OFF energy losses at rated condition (V_{CC}, I_C) given in device datasheet. The other two legs with switches $S_{B3} - S_{C4}$ have same switching loss expression.

3.4.3 Design of high frequency transformers

The ASC structure and HFTs of topology 2 remain same as topology 1. The applied voltage and the currents of the HFTs are also same as in topology 1. Hence the area product of the HFTs used in topology 2 is same as topology 1 and is given in subsection 2.4.3 of chapter 2.

3.4.4 Input and Output Filter Requirement of the Converter

Due to similarity in the modulation strategy, the input DC link current and the pole voltage waveforms of the new topology are similar to the topology 1. Hence the new converter has similar filtering requirements as topology 1 discussed in subsection 2.4.4 of chapter 2.

Table 3.1: Operating Condition of the topology 2

Parameter	Values
Output Power, P	4 kW
DC input, V_{dc}	350 V
output voltage peak , V_{gpk}	200 V
Output frequency, f_o	50 Hz
Switching frequency, f_s	20 kHz

3.5 Experimental verification

3.5.1 Setup and operating condition

The modulation strategy and switching process of the topology 2 are experimentally verified in a laboratory scale hardware prototype (Fig. 3.21). The setup is built using the silicon IGBT

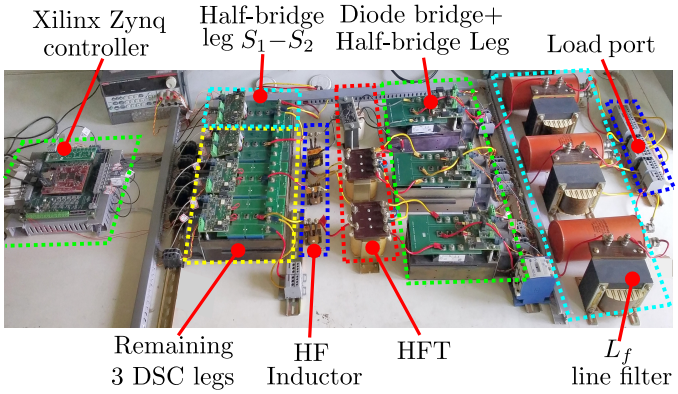


Figure 3.21: Laboratory prototype

module shown in Fig. 2.24a. In the hardware devices, diodes, HFTs, filters are used same as those of topology 1. Four DSC legs and three ASC legs are implemented using 1200 V, 75 A SEMIKRON IGBT modules SKM75GB123D. 1200 V, 75 A IXYS fast recovery diode modules MEE 75-12 DA are used to implement secondary diode bridges. The IGBT modules are driven with optically isolated gate driver IC, ACPL 339J with driving voltage level $\pm$15 V. The primary modules are switched at 20 kHz where as secondary modules are switched at 50 Hz. A 600 ns dead time (DT) is provided between the gating pulses of the top and the bottom IGBTs of an IGBT module. EPCOS ferrite E cores (E 80/38/20) are used for three winding HFTs. The turns ratio is selected as 51:34:34. The leakage inductance of HFTs are in the range of 6-8μH. A series inductance of 48μH is connected to each primary of the HFTs. To implement the modulation strategy and generate the gating signals a ARM-FPGA based System on Chip (SoC) controller platform (Xilinx Zynq-7000) is used. The operating condition of the converter is given in Table 3.1.

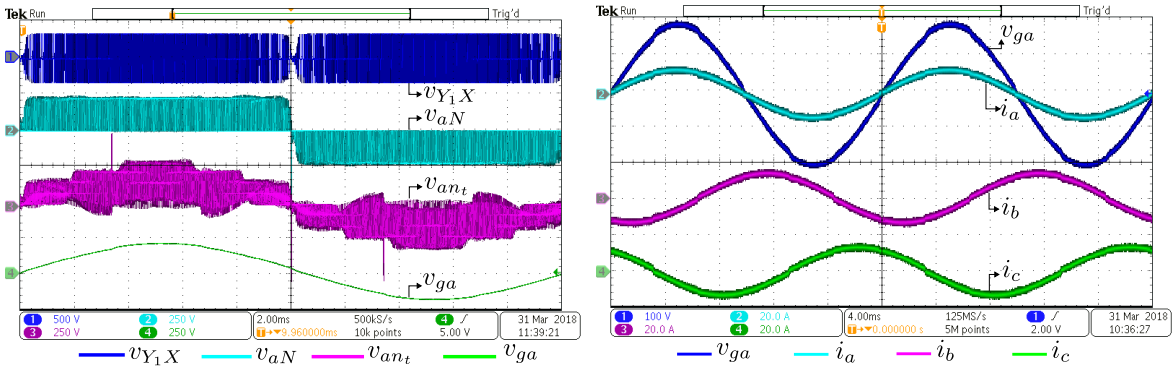


Figure 3.22: (a) Converter pole voltages- [CH1] v_{Y_1X} (500V/div.), [CH2] v_{aN} (250V/div.), [CH3] v_{an_t} (250V/div.), [CH4] v_{ga} (250V/div.). Time scale 2ms/div., (b) Converter output voltage and line currents- [CH1] v_{ga} (100V/div.), [CH2] i_a (20A/div.), [CH3] i_b (20A/div.), [CH4] i_c (20A/div.). Time scale 4ms/div.

3.5.2 Verification of modulation strategy

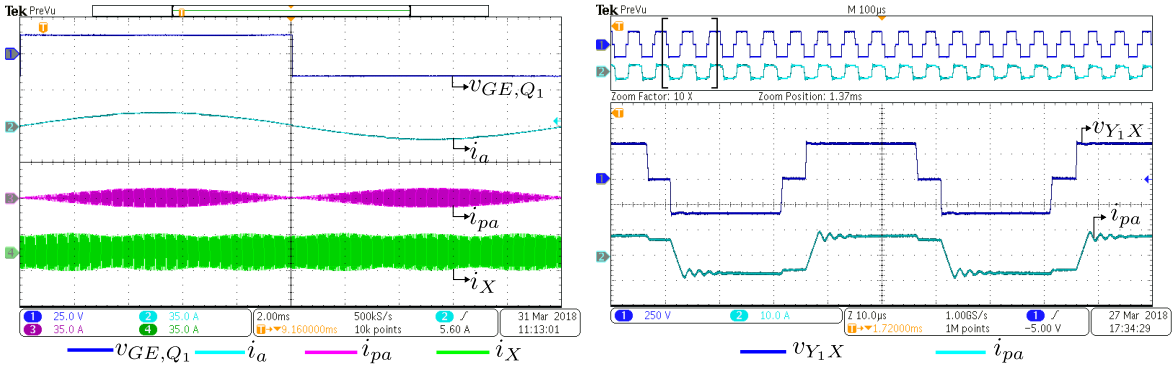
The output of the converter is connected to a balanced 3ϕ voltage source (v_{ga}, v_{gb} and v_{gc}) with phase peak (V_{gpk}) 200 V and frequency 50 Hz. The converter is modulated to generate balanced 3ϕ average output voltages ($\overline{v}_{an_t}$, $\overline{v}_{bn_t}$ and $\overline{v}_{cn_t}$) at 50 Hz following the strategy described in section 3.2 so that it supplies active power of 4 kW at unity power factor. $\overline{v}_{an_t}$ leads v_{ga}. As the impedance of $L_f = 2.5$mH at 50 Hz is relatively small, $\overline{v}_{an_t}$ approximately follows v_{ga}.

In Fig. 3.22a, the pulse width modulated HF AC across HFT primary of phase a (v_{Y_1X}) is shown. v_{Y_1X} has voltage levels of $\pm$350 V and zero. The unipolar PWM pole voltage (v_{aN}) with respect to HFT secondary neutral N is also shown in CH2. v_{aN} has voltage levels of $\pm$233 V and zero. The pole voltage (v_{an_t}) with respect to load neutral n_t is presented in CH3. Due to presence of HF common mode voltage, the waveforms of v_{aN} and v_{an_t} are different though they have same average component. The load voltage waveform (v_{ga}) after line filter L_f is shown in CH4. As in table 3.1, v_{ga} has a peak value (V_{gpk}) of 200 V.

Fig. 3.22b shows load voltage of phase a, v_{ga} and balanced 3ϕ line currents $i_{a,b,c}$ over two line cycles. v_{ga} is almost in phase with i_a and the line currents contain very low high frequency ripple due to filtering action of L_f. The line currents have an peak of I_{pk}=13.4 A. These set of results confirm the three phase operation of the proposed converter.

Line frequency switching of the ASC switches are shown in Fig. 3.23a. The gate emitter voltage of Q_{a1} ($v_{GE,Q_{a1}}$) is high (+15V) when the line current $i_a > 0$. This experimental result validates line frequency switching of the ASC switches. Fig. 3.23a also presents the primary current corresponding to phase a (i_{pa}) and the HFT primary neutral current ,i_X over a line cycle. The waveform of i_{pa} is high frequency square wave with magnitude sinusoidally varying over line cycle. The envelope of i_{pa} has a peak of $i_{pa,pk} = \dfrac{I_{pk}}{n} = 8.9$ A. Unlike i_{pa}, the envelope of i_X never becomes zero. The envelope of i_X has a periodicity of $\dfrac{T_0}{6}$ with peak value

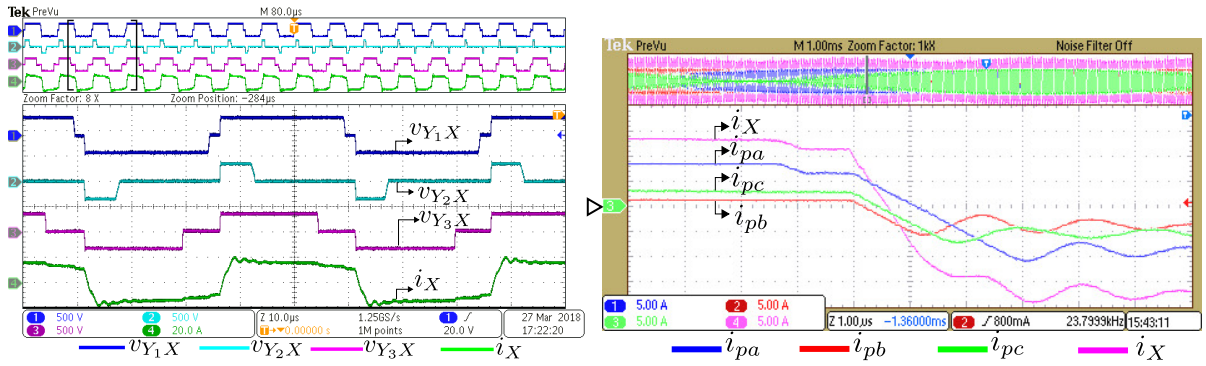
$i_{X,pk} = 2i_{pa,pk} = 17.8$ A and minimum value $\frac{\sqrt{3}i_{X,pk}}{2} = 15.4$ A. Such envelope of i_X helps to achieve complete soft-switching of leg S_1-S_2 over a line cycle.



(a) (b)

Figure 3.23: (a) Line frequency switching of secondary switch- [CH1] $v_{GE,Q_{a1}}$ (25V/div.), [CH2] i_a (35A/div.), [CH3] i_{pa} (35A/div.), [CH4] i_X (35A/div.). Time scale 2ms/div. (b) HFT primary voltage and current- [CH1] v_{Y_1X} (250V/div.), [CH2] i_{pa} (10A/div.). Time scale 10μs/div.

Fig. 3.23b presents HFT primary voltage (v_{Y_1X}) and current (i_{pa}) waveforms over two switching cycle ($2T_s$). HFT primary current polarity changes when applied voltage is changed from zero to $\pm V_{dc}$ (zero to active state) as shown in Fig. 3.3. Fig. 3.23b confirms that HFT flux balance is achieved in one switching cycle.



(a) (b)

Figure 3.24: (a) HFTs input voltages and neutral current- [CH1] v_{Y_1X} (500V/div.), [CH2] v_{Y_2X} (500V/div.), [CH3] v_{Y_3X} (500V/div.), [CH4] i_X (20A/div.). Time scale 10μs/div., (b) Converter primary currents- [CH1] i_{pa} (5A/div.), [CH2] i_{pb} (5A/div.), [CH3] i_{pc} (5A/div.), [CH4] i_X (5A/div.). Time scale 1μs/div.

Fig. 3.24a shows 3ϕ primary voltages (v_{Y_1,Y_2,Y_3-X}) of HFTs along with neutral current i_X over two switching cycles. The experimental waveforms are matched with the analytical waveforms shown in Fig. 3.3. From the figure, the zero to active state transition occurs simultaneously in all the three phases and during this time i_X also changes its direction. The leg $S_1 - S_2$ are switched at this instant. Active to zero transitions are not synchronised.

Fig. 3.24b shows the enlarged view of primary currents during a zero to active state transition. From the figure, the 3ϕ primary currents $i_{pa,pb,pc}$ fall with same slope $\frac{V_{dc}}{L_{lk}}$ where as i_X initially falls rapidly with a slope $\frac{3V_{dc}}{L_{lk}}$ as discussed in section 3.3 and shown in Fig. 3.12. The oscillation observed in the current waveforms are result of resonant ringing of secondary diode bridge parasitic capacitances with HFT series inductances (L_{lk}).

3.5.3 Verification of converter switching process

The switching strategy of the DSC legs $S_{A3}-S_{A4}$, $S_{B3}-S_{B4}$ and $S_{C3}-S_{C4}$ are similar. Hence only the transitions of $S_{A3}-S_{A4}$ are considered for discussion. In a high frequency switching cycle (T_s), $S_{A3}-S_{A4}$ are switched twice during active to zero state transitions. During one transition S_{A4} is turned ON and S_{A3} is turned OFF and in the next transition S_{A4} is turned OFF and S_{A3} is ON. The switching process in both the transitions are same. Similarly, in a switching cycle (T_s) there are two zero to active state transitions during which leg S_1-S_2 are switched. And here also, the switching process wise both the transitions of S_1-S_2 are similar. So, it is sufficient to check any one transition in legs $S_{A3}-S_{A4}$ and S_1-S_2 to verify the soft-switching process.

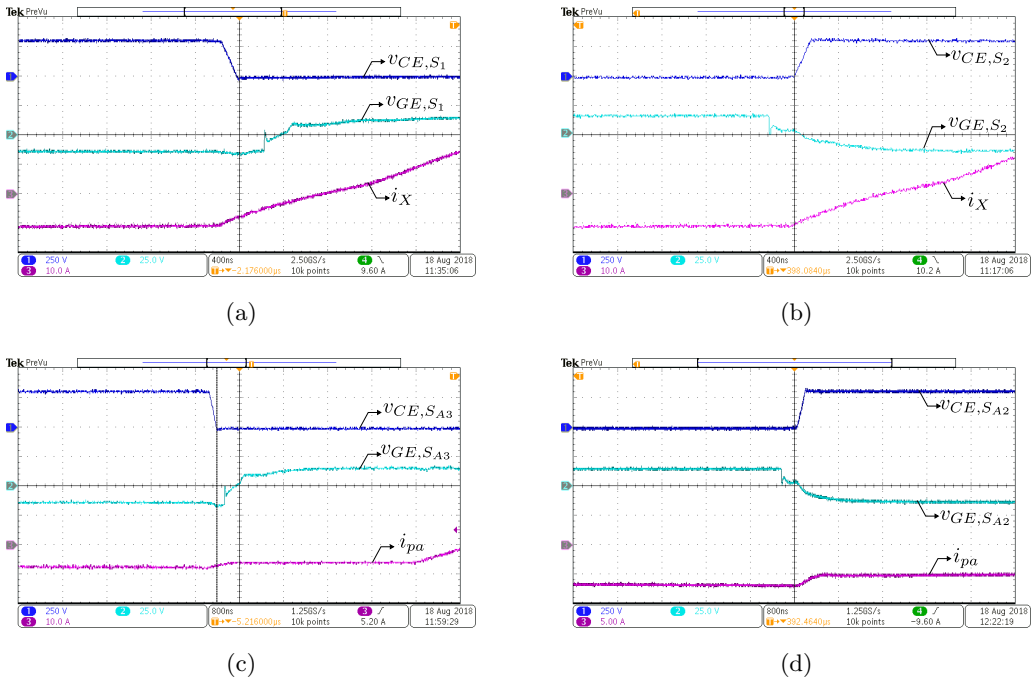


Figure 3.25: Switching transition waveforms of leg S_1-S_2-(a) turn ON of S_1, (b) turn OFF of S_2. Switching transition waveforms of leg $S_{A3}-S_{A4}$-(c) turn ON of S_{A3}, (d) turn OFF of S_{A4}

In Fig. 3.25a shows the turn ON transition of S_1. It is seen from the figure that the collector emitter voltage v_{CE,S_1} first falls to zero and the pole current i_X is negative which indicates the anti parallel diode of S_1 is in conduction. Before the direction of i_X is changed, the gate-emitter voltage v_{GE,S_1} is applied to achieve zero-voltage turn ON of S_1. Fig. 3.25b

shows the turn OFF transition of S_2. It is seen that the voltage across S_2, v_{CE,S_2} starts rising some time after the removal of the gating pulse, v_{GE,S_2} (when v_{GE,S_2} is approximately zero or is negative). Due to presence of capacitance across S_2, the voltage across S_2 rises slowly which results in reduced turn OFF loss of S_2.

Fig. 3.25c shows the turn ON transition of S_{A3}. From the figure it is seen that the gating pulse $v_{GE,S_{A3}}$ is applied after the collector emitter voltage $v_{CE,S_{A3}}$ becomes zero. As the pole current (i_{pa}) direction does not change during the transition, the anti-parallel diode of S_{A3} is in conduction. So the turn ON of S_{A3} is a zero voltage transition (ZVS). In Fig. 3.25d the turn OFF transition of S_{A4} is shown. The collector emitter voltage ($v_{CE,S_{A4}}$) starts rising some time after the gating pulse $v_{GE,S_{A4}}$ is removed and when $v_{GE,S_{A4}}$ is approximately zero or negative. Due to device capacitance, $v_{CE,S_{A4}}$ rises slowly, results in reduced turn OFF loss.

3.5.4 Experimentally measured loss

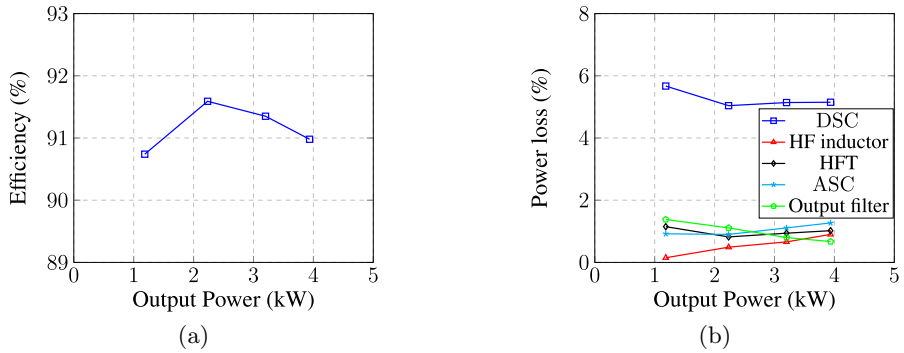


Figure 3.26: (a) Efficiency of the prototype of topology 2, (b) Power loss at different stages of topology 2

Fig. 3.26a presents the converter efficiency for a variation of output power from 1kW to 4kW with input DC supply 350V. The converter has a peak efficiency of 91.6% at 2.2kW load. In Fig. 3.26b the variation of power losses in different stages of the converter are plotted with the variation of output power. Among different stages the high frequency switched DSC incurs maximum loss. The loss is reduced with the increase of output power as the soft-switching zone is increased. Loss contributed by the line frequency switched ASC is relatively less (around 1%). This result shows the effectiveness of the line frequency switching based modulation strategy.

Fig. 3.27a shows power loss distribution at 3.94kW output power obtained experimentally and analytically. The analytically estimated losses are closely matching with the experimentally obtained values. Fig. 3.27b presents a pie chart showing experimentally obtained losses at 3.94kW output power. Out of total power loss, the DSC incurs 57% loss whereas 14% is the contribution by the ASC.

Fig. 3.28 presents the DSC loss variation over the output power range. Experimental and analytical loss of the DSC is presented along with complete hard switched loss. The soft-switching of the DSC significantly reduces the converter loss at high output power.

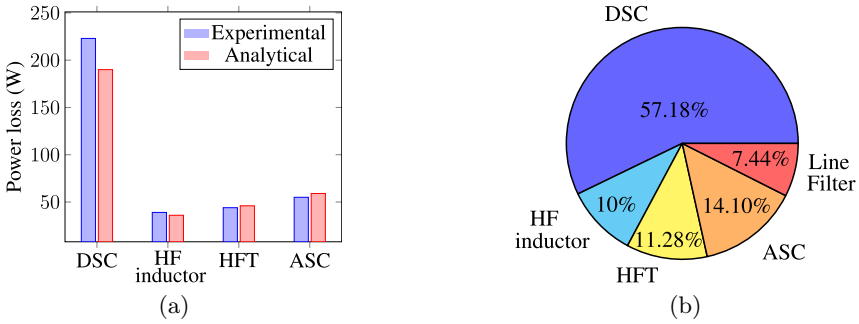


Figure 3.27: (a) Power loss break down at 3.94kW output power obtained experimentally and analytically, (b) Percentage loss distribution shown at 3.94kW output power obtained experimentally

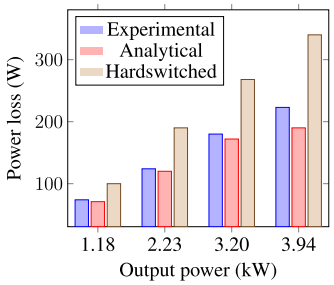


Figure 3.28: DSC power loss: experimental, analytical and complete hard-switched

3.6 Conclusion

In this chapter a single-stage unidirectional 3ϕ high-frequency link inverter topology is introduced which employs less number of active switches and has better soft-switching performance compared to the topology 1 presented in chapter 2. Like the topology 1, this converter has ability to support only UPF load and for any reactive compensation additional shunt compensator is needed. The active switches of ASC of the new topology are line frequency switched. The steady state operation of the converter is presented with detailed circuit analysis. To achieve ZVS turn ON of the DSC active switches, the conditions on dead times are derived. It is seen that with proper choice of dead time, the ZVS turn ON of the reference leg of the DSC can be ensured over complete line cycle. A detailed discussion is presented comparing the soft-switching performance of the new topology with the topology 1. Due to similarity in the modulation strategy, the input DC link current and the pole voltage waveforms of the new topology are similar to the topology 1. Hence the new converter has similar filtering requirements as topology 1 discussed in chapter 2. To estimate the converter power loss analytically, the closed form loss expressions are presented. The converter operation, particularly, different aspects of the modulation strategy, ZVS transitions are experimentally verified on laboratory scale hardware prototype. Efficiency and Power loss at different stages are experimentally measured. The analytically estimated power loss is verified with experimentally obtained values. Like topology 1, this topology is primarily targeted for grid integration of utility scale photovoltaic sources.

Chapter 4

Unidirectional HFL DC-3ϕ AC Conversion with Three Pulsating DC Links: Topology-3

4.1 Introduction

In chapter 3, a new HFL inverter topology is explored which employs reduced number of active switches and has improved soft-switching performance compared to the topology 1 described in chapter 2. Like in topology 1, here the ASC active switches are line frequency switched. To generate three pulsating DC links, here the DSC employs four half-bridge legs . Though these DSC switches have same blocking voltage but the RMS current of one pair switches ($S_1 - S_2$ in Fig. 3.2) is three times higher than other six switches and hence have higher conduction loss. Asymmetry in current ratings and power losses of the half-bridge legs of the DSC increase converter cost and design complexities. For example, relatively complex heat-sink arrangement is needed for thermal management of the converter. Moreover as discussed in section 3.3.10 of chapter 3, though one DSC half bridge leg ($S_1 - S_2$) of the topology 2 can be soft-switched over complete line cycle, remaining three legs are soft-switched in some parts of the line cycle like in topology 1. Additionally, in literature [30], a unidirectional topology with six DSC active switches are reported whereas the topology 2 employs 8 active switches in the DSC. Hence there are scopes for further improvement of the topology 2 considering the above aspects.

In this chapter a new converter topology is explored which further reduces the number of half-bridge legs employed on the DSC and achieves soft-switching of all the DSC legs over complete line cycle. The blocking voltage, RMS current, power loss of all the DSC legs are identical which simplifies converter design and reduces cost. The structure of the ASC remains same as topology 2 (Fig.3.2) and the adopted modulation strategy ensures line frequency switching of all the active switches in ASC like topology-2. The derivation of the new topology along with the modulation strategy is discussed in details. The converter switching process is presented. The soft-switching conditions of the DSC legs are derived. The soft-switching performance is compared with topology 2. The filtering requirements in terms of input current and output voltage THDs are derived. The analytical expressions of the converter power loss is derived. The operation of the converter is experimentally verified in a 3.7kW hardware prototype. The content of this chapter is reported in [42].

4.2 Topology synthesis and modulation strategy

As we have seen in the last two chapters, the main objective of the DSC is to generate sinusoidal PWM HFAC voltages across the three transformer primary windings. To generate PWM HFAC from the input DC voltage, phase shift modulation is adopted. In case of phase shift modulation, the gating signals of all active switches of the DSC are with 50% duty ratio. As we have seen in topology 1 and 2, the DSC half-bridge legs are categorised into reference and non-reference legs. The reference legs are marked in red in Fig. 3.1a and 3.2a. The primary terminals of a HFT is connected between the poles of one reference and one non-reference half bridge legs. To apply PWM HFAC across HFT terminals, the gating signals of the non-reference half bridge leg are phase shifted w.r.t the gating signals of the reference leg. In these topologies the legs do not change their roles i.e. a leg which is identified as reference leg, remains so through out the line cycle. Same is true for any non-reference leg. A new topology is explored in this section where the roles of the DSC legs are changed over the line cycle i.e. a half-bridge leg which is identified as a reference leg in some part of the line cycle becomes a non-reference leg in the other parts of the line cycle. As the legs share their role over the line cycle, a dedicated reference leg like the one used in topology 2 (Fig. 3.2a), is not needed here. The new topology which is termed as topology 3 is shown in Fig. 4.1.

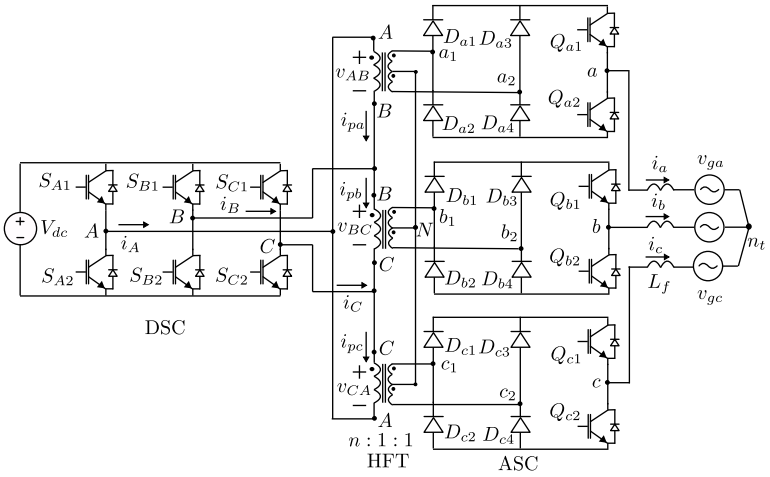


Figure 4.1: (a) 3ϕ HFL inverter with 3 pulsating DC link: topology 3

The topology 3 employ three half-bridge legs on the DSC. Three HFTs are used like in topology 1 and 2. The primary windings of these three HFTs are connected in delta. The three terminals of the delta are connected to the poles of the DSC half-bridge legs A, B and C. Sinusoidal pulse width modulation is implemented on the DSC. What follows is a detailed discussion of the modulation strategy of the DSC. The ASC has same structure and switching strategy as in topology 1 and 2. Hence the details are not discussed here. The ASC switching scheme is shown in Fig. 4.2.

To generate balanced three phase average pole voltages given in (4.1), the three-phase

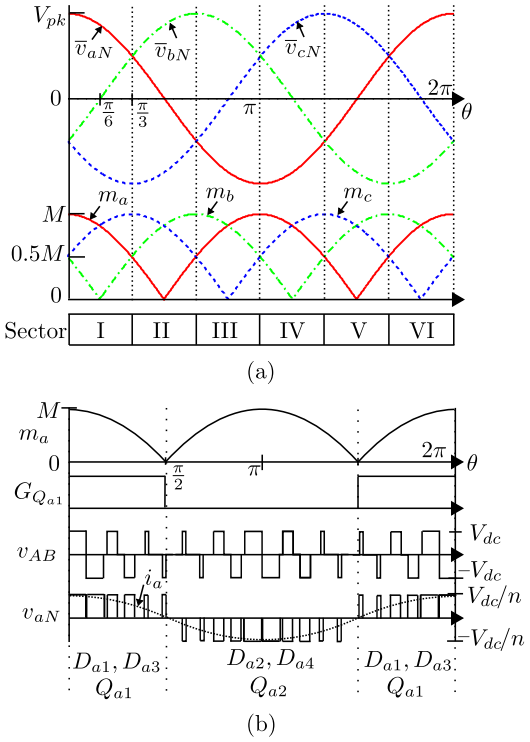


Figure 4.2: (a) Average pole voltages and the modulation signals, (b) Switching strategy of ASC

modulation signals, m_a, m_b and m_c are given in (4.2) (see Fig. 4.2a).

$$\begin{aligned}
\overline{v}_{aN}(\theta) &= V_{pk}\cos\theta \\
\overline{v}_{bN}(\theta) &= V_{pk}\cos\left(\theta - \frac{2\pi}{3}\right) \\
\overline{v}_{bN}(\theta) &= V_{pk}\cos\left(\theta + \frac{2\pi}{3}\right)
\end{aligned} \tag{4.1}$$

$$\begin{aligned}
m_a(\theta) &= M|\cos\theta| \\
m_b(\theta) &= M|\cos\left(\theta - \frac{2\pi}{3}\right)| \\
m_c(\theta) &= M|\cos\left(\theta + \frac{2\pi}{3}\right)|
\end{aligned} \tag{4.2}$$

Where $M = \dfrac{nV_{pk}}{V_{dc}}$. Let m_{max}, m_{mid} and m_{min} are defined as follows.

$$\begin{aligned}
m_{max} &= max(m_a, m_b, m_c) \\
m_{mid} &= mid(m_a, m_b, m_c) \\
m_{min} &= min(m_a, m_b, m_c)
\end{aligned} \tag{4.3}$$

Using (4.2), the relation between m_{max}, m_{mid} and m_{min} is given in (4.4) (see Fig. 4.2a).

$$m_{max} = m_{mid} + m_{min} \tag{4.4}$$

Applying KVL across the HFT primary windings-

$$v_{AB} + v_{BC} + v_{CA} = 0 \tag{4.5}$$

Using the three legs of the DSC, we want to generate PWM HFAC voltage waveform like v_{AB} (see Fig. 4.2b) across each transformer primary terminals. Equation (4.5) implies that at any given instant of time sum of the applied primary terminal voltages are zero. As (4.4) has to be satisfied along with (4.5), there are two possible ways to apply the primary voltages over T_s as shown in Fig. 4.3. The two cases result in two different switching strategies. It is seen that

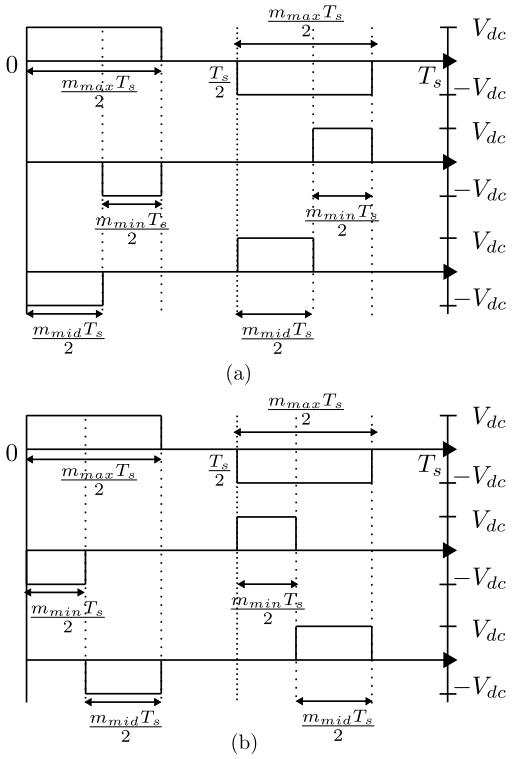


Figure 4.3: Possible transformer primary voltages over T_s- (a) case I, (b) case II

Table 4.1: Reference leg in different sectors

Sector	I	II	III	IV	V	VI
θ	$(0, \frac{\pi}{3})$	$(\frac{\pi}{3}, \frac{2\pi}{3})$	$(\frac{2\pi}{3}, \pi)$	$(\pi, \frac{4\pi}{3})$	$(\frac{4\pi}{3}, \frac{5\pi}{3})$	$(\frac{5\pi}{3}, 2\pi)$
Ref. Leg	A	C	B	A	C	B

the soft-switching performance of case I is better than the case II. Hence, case I is considered for the DSC modulation. For example, when $\theta \in [0, \frac{\pi}{6}]$ (see Fig. 4.4), $m_{max} = m_a$, $m_{mid} = m_c$ and $m_{min} = m_b$. To apply the transformer primary voltages following case I, the switching strategy of the DSC in this duration is described here.

In the DSC, the two switches of a half-bridge leg are complementary switched with a dead time. Each active switch of the DSC has a square wave gating pulse with 50% duty ratio and period T_s. In the given duration of θ, leg A is considered as the reference leg. The gating pulse of S_{A1}, $G_{S_{A1}}$, is shown in Fig. 4.4. The gating signal S_{B1}, $G_{S_{B1}}$, is phase shifted w.r.t $G_{S_{A1}}$

by $\frac{m_a T_s}{2}$. The gating pulse of S_{C1}, $G_{S_{C1}}$ is phase shifted by $\frac{m_c T_s}{2}$ w.r.t $G_{S_{A1}}$. The phase shifts are obtained by comparing m_a and m_c with unity peak saw-tooth carrier of period $\frac{T_s}{2}$ (Fig. 4.4). The switching strategy applies the transformer primary voltages v_{AB}, v_{BC} and v_{CA} with pulse widths $\frac{m_a T_s}{2}$, $\frac{m_b T_s}{2}$ and $\frac{m_c T_s}{2}$ respectively as shown in Fig. 4.4. The applied transformer primary voltages in Fig. 4.4, matches with the case I in Fig. 4.3.

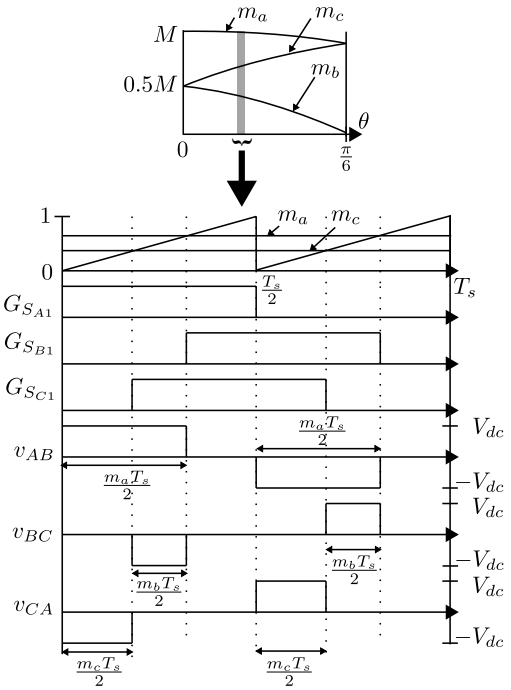


Figure 4.4: DC side converter modulation in sector I

Following the above strategy, the reference leg needs to be changed every 60° as shown in Table 4.1. These regions of θ are termed as sectors e.g. when $\theta \in [0, \frac{\pi}{3}]$, sector is I. In the next section, steady state operation of the converter is presented in details. The selection of dead time of the DSC legs are described to achieve ZVS switching of all the DSC active switches over complete line cycle.

4.3 Steady state operation and circuit analysis

The steady state operation of the DSC over a switching cycle (T_s) is described here. It is assumed that the ASC switches do not change states over T_s under consideration. The operation presented here shows that all six active switches of the DSC are zero voltage switched (ZVS). For the switching analysis, the device capacitances C_s and leakage inductance of the HFTs seen from primary (L_{lk}) are considered. As the transformers are identical, the leakage inductances are considered to be equal. In the analysis, the conditions on dead-time are derived to ensure ZVS over a complete line cycle. For ease of analysis, the slowly varying, properly filtered line currents are assumed as constant current sinks over T_s with magnitudes I_j where $j \in \{a, b, c\}$.

The variations of I_j in sector I $\left(\theta \in [0, \frac{\pi}{3}]\right)$ are given in (4.6) and (4.7).

$$\begin{aligned} I_a &= I_{pk}\cos\theta \\ I_c &= I_{pk}\cos\left(\frac{\pi}{3}-\theta\right) \end{aligned} \tag{4.6}$$

$$I_b = \begin{cases} I_{pk}\cos\left(\theta+\frac{\pi}{3}\right), & \theta \in [0, \frac{\pi}{6}] \\ I_{pk}\sin(\theta-\frac{\pi}{6}), & \theta \in [\frac{\pi}{6}, \frac{\pi}{3}] \end{cases} \tag{4.7}$$

The converter operation is described for the first half of sector I $\left(\theta \in [0, \frac{\pi}{6}]\right)$ when $i_a = I_a$, $i_b = -I_b$ and $i_c = -I_c$ and $I_a > I_c > I_b$. For balanced operation, $I_a = I_b + I_c$, as can be seen from (4.6) and (4.7). Based on the directions of i_a, i_b and i_c, the line frequency switched Q_{a1}, Q_{b2} and Q_{c2} are kept ON throughout the switching cycle (T_s). In one half of a switching cycle, the converter goes through 9 distinct modes of operation. These modes can be divided as steady conduction modes (mode 1, 4 and 6) and switching transition modes. As shown in Fig. 4.4, the DSC half-bridge legs are switched in the following order $C-B-A$ over one half of T_s. Mode 2 and 3 describe the transition of leg C. The transition of leg B is presented in mode 5. The switching process of leg A is divided into mode 7, 8 and 9. The circuit dynamics in the other half of T_s is similar. The switching waveforms in the first half of sector I are presented in Fig. 4.5.

4.3.1 Steady conduction mode I

Mode 1 ($t_0 < t < t_1$, Fig 4.5) In the DSC, S_{A1}, S_{B2} and S_{C2} are ON and thus the applied voltages across the HFT primary windings are $v_{AB} = V_{dc}$, $v_{BC} = 0$ and $v_{CA} = -V_{dc}$. Fig. 4.6a shows the circuit configuration in mode 1. Fig. 4.6b presents the simplified equivalent circuit. The primary currents in the HFTs are given as $i_{pa} = \frac{I_a}{n}$, $i_{pb} = \frac{I_b}{n}$ and $i_{pc} = -\frac{I_c}{n}$. The applied voltage polarity and the direction of currents shown in Fig. 4.6a and Fig. 4.6b indicate that the phases a and c are in active state, transferring power from DC to AC side, whereas the phase b is in zero state i.e. no active power is transferred from DC source to load. The DSC pole currents $i_{A,B,C}$ are obtained by applying KCL at nodes A, B and C respectively.

$$\begin{aligned} i_A &= i_{pa} - i_{pc} = \frac{I_a + I_c}{n} \\ i_B &= i_{pb} - i_{pa} = -\frac{I_a - I_b}{n} = -\frac{I_c}{n} \\ i_C &= i_{pc} - i_{pb} = -\frac{I_c + I_b}{n} = -\frac{I_a}{n} \end{aligned} \tag{4.8}$$

In secondary, (D_{a1}, Q_{a1}), (D_{b4}, Q_{b2}) and (D_{c2}, Q_{c2}) are conducting the line currents.

4.3.2 Switching transition of leg C

Mode 2 ($t_1 < t < t_2$, Fig 4.5) The circuit configuration is shown in Fig. 4.7a and the simplified equivalent circuit is given in Fig. 4.7b. This mode starts at t_1, when the gating

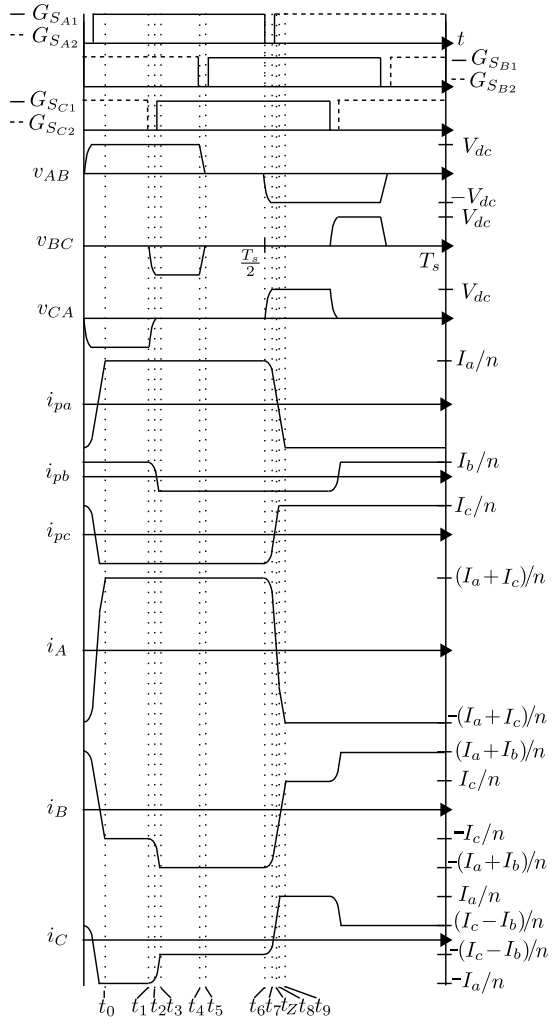


Figure 4.5: DSC waveforms over T_s in sector I ($\theta \in [0, \frac{\pi}{6}]$)

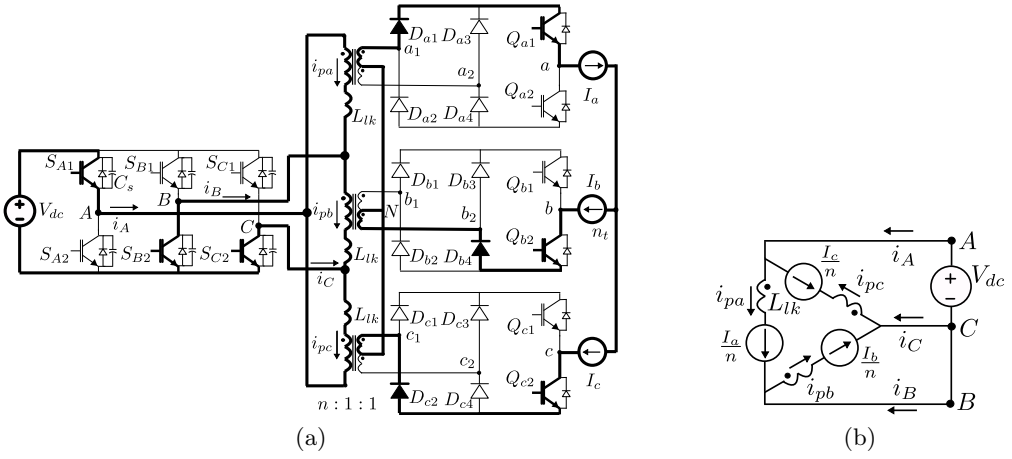


Figure 4.6: Mode 1 -(a) Circuit diagram, (b) Equivalent circuit

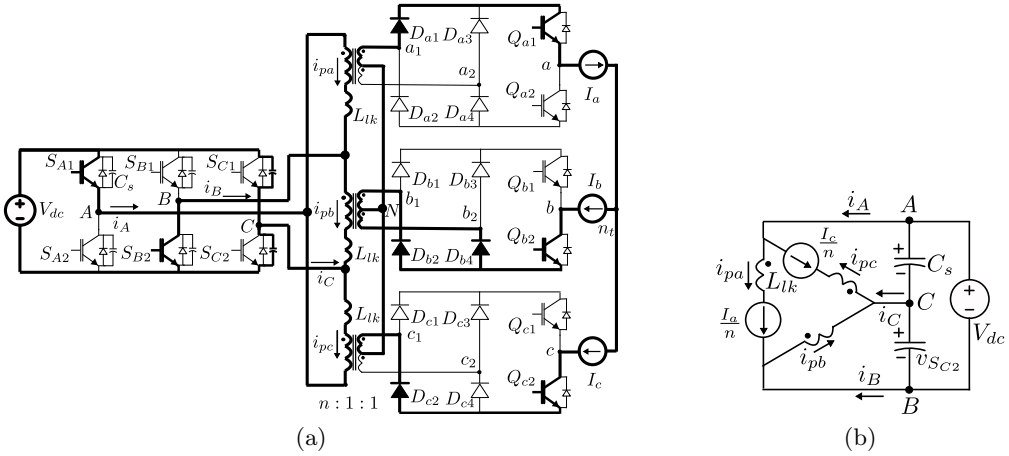


Figure 4.7: Mode 2- (a) Circuit diagram, (b) Equivalent circuit

pulse of S_{C2} is removed. The voltage across S_{C2}, $v_{S_{C2}}$, can not change abruptly due to device capacitance C_s. The slow rise of $v_{S_{C2}}$ helps to reduce turn OFF loss of S_{C2}. The pole current i_C starts charging the device capacitance (C_s) across S_{C2} and discharging the capacitance across S_{C1}. The applied voltage polarity across HFT terminals B and C, forward biases the secondary diode D_{b2} and hence the HFT secondary terminals b_1 and b_2 are shorted through the diode bridge (see Fig. 4.7a). This also shorts the current source I_b. As seen from Fig. 4.7b, the voltage polarity across C, B is against the direction of the primary current i_{pb} and hence i_{pb} falls (see Fig. 4.5). The applied voltage polarities across the HFT primary terminals- (A, B) and (C, A) are same as in mode 1 (see Fig. 4.6b and 4.7b). Hence the conduction states of secondary diode bridges $D_{a1} - D_{a4}$, $D_{c1} - D_{c4}$ and the half-bridge legs $Q_{a1} - Q_{a2}$, $Q_{c1} - Q_{c2}$ remain unchanged. The circuit equations in this mode are shown in (4.9).

$$
\begin{aligned}
v_{S_{C2}} &= -v_{BC} = \frac{\omega_r L_{lk} I_a}{n} \sin \omega_r (t - t_1) \\
i_{pb} &= \frac{I_a}{n} \cos \omega_r (t - t_1) - \frac{I_c}{n} \\
i_B &= -\frac{I_a}{n} (1 - \cos \omega_r (t - t_1)) - \frac{I_c}{n} \\
i_C &= -\frac{I_a}{n} \cos \omega_r (t - t_1) \\
(t_2 - t_1) &= \frac{1}{\omega_r} \sin^{-1} \left(\frac{n V_{DC}}{\omega_r L_{lk} I_a} \right)
\end{aligned}
\tag{4.9}
$$

Where $\omega_r = \dfrac{1}{\sqrt{2 L_{lk} C_s}}$. At t_2, $v_{S_{C2}}$ becomes equal to V_{DC} and this mode ends. To charge the $v_{S_{C2}}$ to V_{DC}, (4.10) needs to be satisfied. Otherwise the circuit goes into a resonating oscillation mode.

$$
n V_{dc} \leq \omega_r L_{lk} I_a \tag{4.10}
$$

The duration of mode 2, $(t_2 - t_1)$, is shown in (4.9). In our considered zone of operation, $\theta \in [0, \frac{\pi}{6}]$, $(t_2 - t_1)$ has maximum value at $\theta = \frac{\pi}{6}$ when I_a $(= 0.87 I_{pk})$ is minimum.

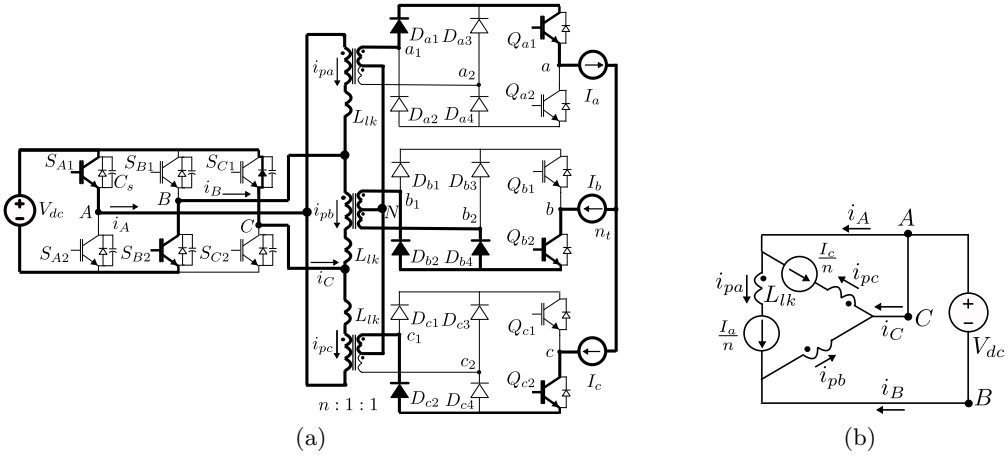


Figure 4.8: Mode 3- (a) Circuit diagram, (b) Equivalent circuit

Mode 3 ($t_2 < t < t_3$, Fig 4.5) After t_2, the anti-parallel diode of S_{C1} comes in conduction as shown in Fig. 4.8a. The simplified equivalent circuit is shown in Fig. 4.8b. S_{C1} is turned ON after t_2 to achieve ZVS. To ensure ZVS ON throughout our considered zone of operation, the dead-time, DT_C, between $S_{C1} - S_{C2}$ should be greater than maximum value of $(t_2 - t_1)$ and the condition is given in (4.11).

$$DT_C \geq \frac{1}{\omega_r} \sin^{-1}\left(\frac{1.15nV_{DC}}{\omega_r L_{lk} I_{pk}}\right) \tag{4.11}$$

In this mode, the applied voltage across the primary terminals (B, C) is $v_{BC} = -V_{dc}$ and is against the direction of i_{pb}. Hence i_{pb} falls in this mode also. i_{pb} becomes zero and changes its direction. In secondary, soft current commutation between the diodes D_{b2} and D_{b4} takes place. The primary currents are given in (4.12).

$$\begin{aligned} i_{pb} &= i_{pb}(t_2) - \frac{V_{dc}}{L_{lk}}(t - t_2) \\ i_B &= i_B(t_2) - \frac{V_{dc}}{L_{lk}}(t - t_2) \\ i_C &= i_C(t_2) + \frac{V_{dc}}{L_{lk}}(t - t_2) \end{aligned} \tag{4.12}$$

At t_3, $i_{pb} = -\frac{I_b}{n}$ and this mode ends. D_{b4} is reverse biased. The DSC pole currents are given as $i_A(t_3) = \frac{I_a + I_c}{n}$, $i_B(t_3) = -\frac{I_a + I_b}{n}$ and $i_C(t_3) = -\frac{I_c - I_b}{n}$. In this mode only the HFT primary current i_{pb} changes its direction. The directions of DSC pole currents $i_{A,B,C}$ remain same as in mode 1.

4.3.3 Steady conduction mode II

Mode 4 ($t_3 < t < t_4$, Fig 4.5) The circuit configuration in this mode is shown in Fig. 4.9a. In DSC, S_{A1}, S_{B2} and the anti-parallel diode of S_{C1} are in conduction. Thus the applied voltages across the primary windings are- $V_{AB} = V_{dc}$, $v_{BC} = -V_{dc}$ and $v_{CA} = 0$. The simplified

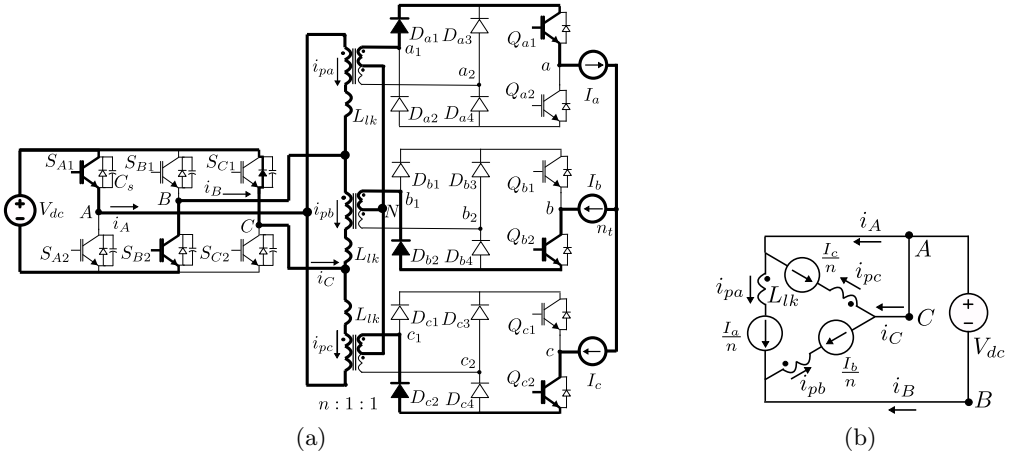


Figure 4.9: Mode 4- (a) Circuit diagram, (b) Equivalent circuit

equivalent circuit is shown in Fig. 4.9b. Shown voltage polarities and current directions in the equivalent circuit, indicate that the active power is transferred from DC to AC side via phase a and b. Whereas phase c is in zero state. The primary winding currents in this mode are given as $i_{pa} = \frac{I_a}{n}$, $i_{pb} = -\frac{I_b}{n}$ and $i_{pc} = -\frac{I_c}{n}$. The DSC pole currents are $i_A = \frac{I_a + I_c}{n}$, $i_B = -\frac{I_a + I_b}{n}$ and $i_C = -\frac{I_c - I_b}{n}$ (see Fig. 4.5).

4.3.4 Switching transition of leg B

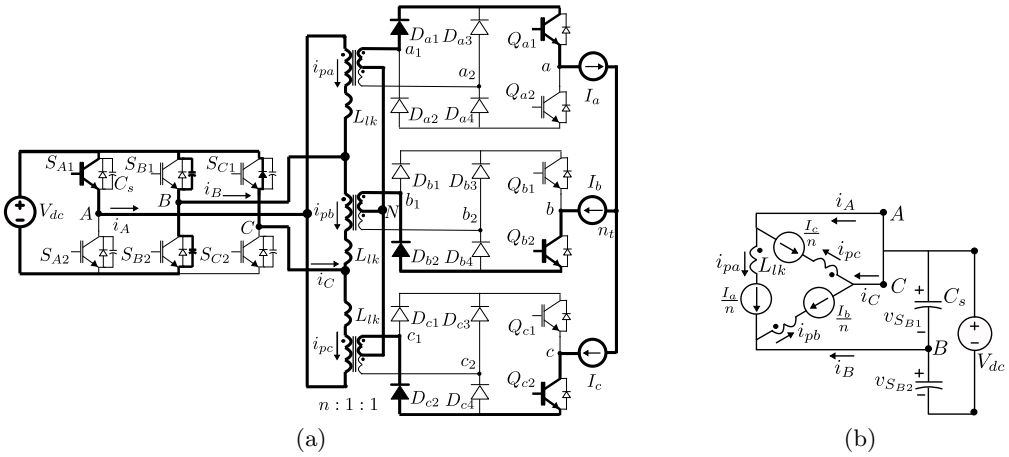


Figure 4.10: Mode 5- (a) Circuit diagram, (b) Equivalent circuit

Mode 5 ($t_4 < t < t_5$, Fig 4.5) This mode begins at t_4 when the gating pulse of S_{B2} is removed. The circuit diagram in this mode is shown in Fig. 4.10a. The device capacitance (C_s) slows down the voltage rise across S_{B2} and thus the turn OFF loss of S_{B2} is reduced. Fig. 4.10b presents the simplified equivalent circuit. The pole current i_B charges the capacitance across S_{B2} and discharges the capacitance across S_{B1} as shown in Fig. 4.10b. In this mode, the primary voltage polarities of the HFTs are same as in mode 4. Hence the conduction states of the secondary side diode bridges are unaltered. The primary winding currents ($i_{pa,pb,pc}$) and the DSC pole currents ($i_{A,B,C}$) do not change in this mode. The circuit dynamics in this mode

is shown in (4.13).

$$\begin{aligned} v_{S_{B1}} &= V_{dc} - \frac{(I_a + I_b)}{2nC_s}(t - t_4) \\ v_{S_{B2}} &= \frac{(I_a + I_b)}{2nC_s}(t - t_4) \\ t_5 - t_4 &= \frac{2nC_sV_{dc}}{(I_a + I_b)} \end{aligned} \tag{4.13}$$

$v_{S_{B1}}$ and $v_{S_{B2}}$ are voltages across S_{B1}, S_{B2} respectively. At $t = t_5$, $v_{S_{B2}} = V_{dc}$ and this mode ends. The duration $(t_5 - t_4)$, is given in (4.13). In our considered range of $\theta \in [0, \frac{\pi}{6}]$, $(t_5 - t_4)$ is maximum at $\theta = \frac{\pi}{6}$, when $(I_a + I_b)$ is minimum and is equal to $0.87I_{pk}$.

4.3.5 Steady conduction mode III

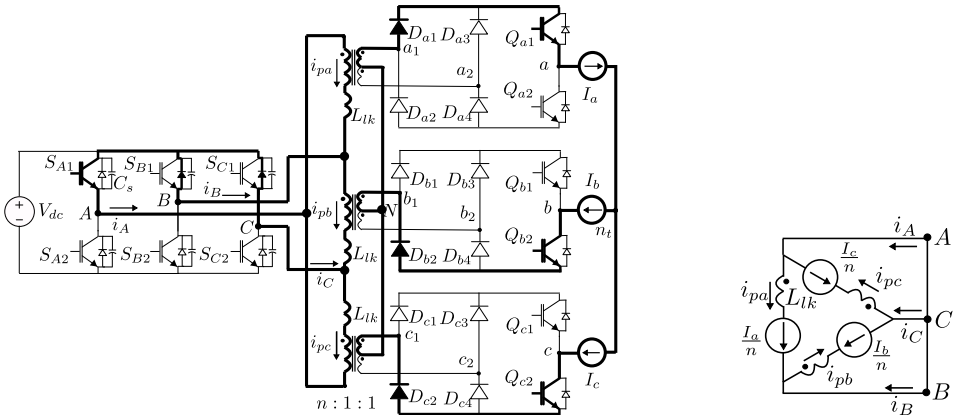


Figure 4.11: Mode 6- (a) Circuit diagram, (b) Equivalent circuit

Mode 6 ($t_5 < t < t_6$, Fig 4.5) The circuit configuration of mode 6 is shown in Fig. 4.11a. As seen from the figure, in the DSC, S_{A1} and the anti-parallel diodes of S_{B1}, S_{C1} are in conduction. To achieve ZVS turn ON of S_{B1}, gating pulse of S_{B1} should be applied after t_5 when the anti-parallel diode is in conduction. To achieve soft turn ON through out the considered interval of $\theta \in [0, \frac{\pi}{6}]$, the dead-time between $S_{B1} - S_{B2}$, DT_B, should be greater than the maximum duration of $(t_5 - t_4)$. The condition is given in (4.14).

$$DT_B \geq \frac{2.3nC_sV_{dc}}{I_{pk}} \tag{4.14}$$

The applied primary voltages in this mode are $v_{AB} = v_{BC} = v_{CA} = 0$. The simplified equivalent circuit is shown in Fig. 4.11b. In this mode, all three phases are in zero or free-wheeling state.

4.3.6 Switching transition of leg A

Mode 7 ($t_6 < t < t_7$, Fig 4.5 and Fig. 4.12) This mode begins at t_6 when S_{A1} is turned OFF. The circuit configuration is shown in Fig. 4.13a. As explained earlier, the device

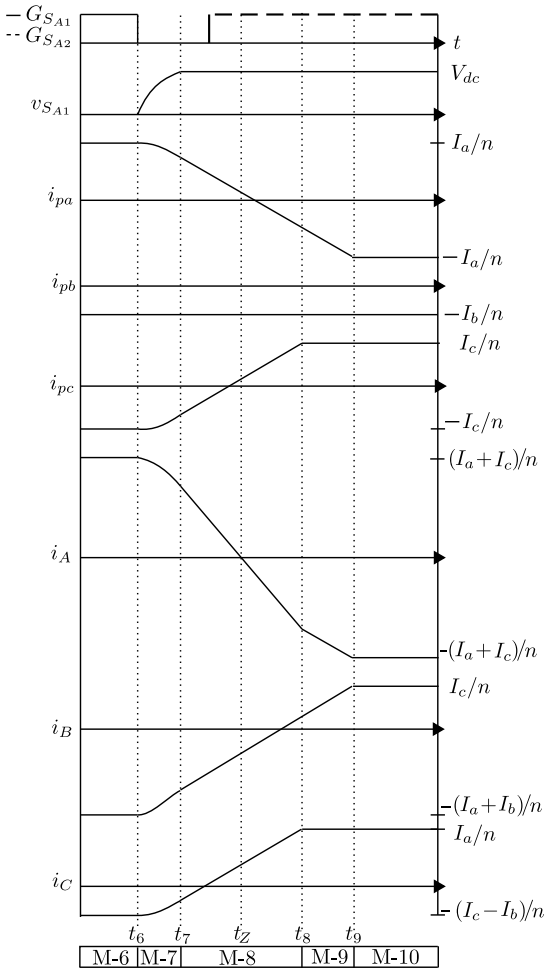


Figure 4.12: Enlarged current wave forms in Mode 7-9

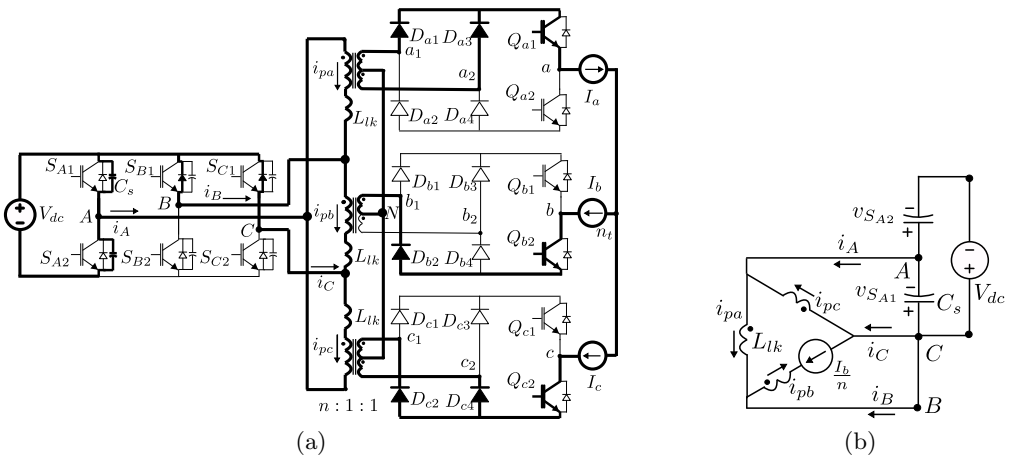


Figure 4.13: Mode 7- (a) Circuit diagram, (b) Equivalent circuit

capacitance (C_s) across S_{A1} helps to reduce the turn OFF loss. The pole current i_A, begins to charge the capacitor across S_{A1} and discharge the capacitor across S_{A2}. The simplified equivalent circuit is shown in Fig. 4.13b. The voltage polarities across the primary terminals (A, B) and (C, A) forward bias the secondary diodes D_{a3} and D_{c4} respectively. And thus the secondary terminals of the two HFTs, (a_1, a_2) and (c_1, c_2) are shorted by the diode bridges $D_{a1} - D_{a4}$ and $D_{c1} - D_{c4}$ respectively. The current sinks I_a and I_c are also shorted. As seen in Fig. 4.13b, the applied voltage polarities are against the directions of the primary currents i_{pa} and i_{pc}. Hence i_{pa} and i_{pc} starts to decrease in this mode whereas the primary current $i_{pb} = -\frac{I_b}{n}$ remains unchanged. The circuit equations in this mode are given in (4.15).

$$\begin{aligned}
i_{pa} &= \frac{I_a}{n} - \frac{(I_a + I_c)}{2n}(1 - \cos\omega_r'(t - t_6)) \\
i_{pc} &= -\frac{I_c}{n} + \frac{(I_a + I_c)}{2n}(1 - \cos\omega_r'(t - t_6)) \\
i_A &= \frac{(I_a + I_c)}{n}\cos\omega_r'(t - t_6) \\
i_B &= -\frac{(I_a + I_b)}{n} + \frac{(I_a + I_c)}{2n}(1 - \cos\omega_r'(t - t_6)) \\
i_C &= -\frac{(I_c - I_b)}{n} + \frac{(I_a + I_c)}{2n}(1 - \cos\omega_r'(t - t_6)) \\
v_{CA} &= -v_{AB} = v_{S_{A1}} = \frac{(I_a + I_c)\omega_r' L_{lk}}{2n}\sin\omega_r'(t - t_6)
\end{aligned} \tag{4.15}$$

Where $v_{S_{A1}}$ is the voltage across S_{A1} and $\omega_r' = \frac{1}{\sqrt{L_{lk}C_s}}$. At the end of this mode at t_7, $v_{S_{A1}} = V_{dc}$ and $v_{S_{A2}} = 0$. The anti-parallel diode of S_{A2} is forward biased. To charge the capacitor (C_s) across S_{A1} to V_{dc}, following condition should be satisfied, $(I_a + I_c)\omega_r' L_{lk} \geq 2nV_{dc}$. Otherwise, the circuit enters into a resonating oscillation mode with frequency ω_r' and remains there till S_{A2} is turned ON. Also this results in hard turn ON of S_{A2}. The interval $(t_7 - t_6)$, is given as, $(t_7 - t_6) = \frac{1}{\omega_r'}\sin^{-1}\left(\frac{2nV_{dc}}{(I_a + I_c)\omega_r' L_{lk}}\right)$. $(t_7 - t_6)$ has maximum value at $\theta = 0$ and $\theta = \frac{\pi}{3}$ in sector I , where $(I_a + I_c) = 1.5I_{pk}$ is minimum. To achieve ZVS turn ON of S_{A2}, the gating pulse of S_{A2} should be applied after t_7 when the anti-parallel diode is conducting. Considering maximum value of $(t_7 - t_6)$, the dead time between $S_{A1} - S_{A2}$, DT_A, should satisfy (4.16).

$$DT_A \geq \frac{1}{\omega_r'}\sin^{-1}\left(\frac{1.33nV_{DC}}{\omega_r' L_{lk} I_{pk}}\right) \tag{4.16}$$

The transformer primary currents, i_{pa} and i_{pc} along with the DSC pole currents, $i_{A,B,C}$ linearly change their directions in next two modes. S_{C1} and S_{B1} are already ON (ZVS) in mode 3 and mode 6 respectively. So, based on the direction of i_B and i_C, at first the anti-parallel diodes and then the switches S_{B1} and S_{C1} conduct respectively.

Mode 8 ($t_7 < t < t_8$, Fig 4.5 and Fig. 4.12) The circuit configuration is shown in Fig.4.14a and the corresponding simplified equivalent circuit is presented in Fig. 4.14b. As seen from these figures, the voltage applied across the primary terminals (A, B) and (C, A) are

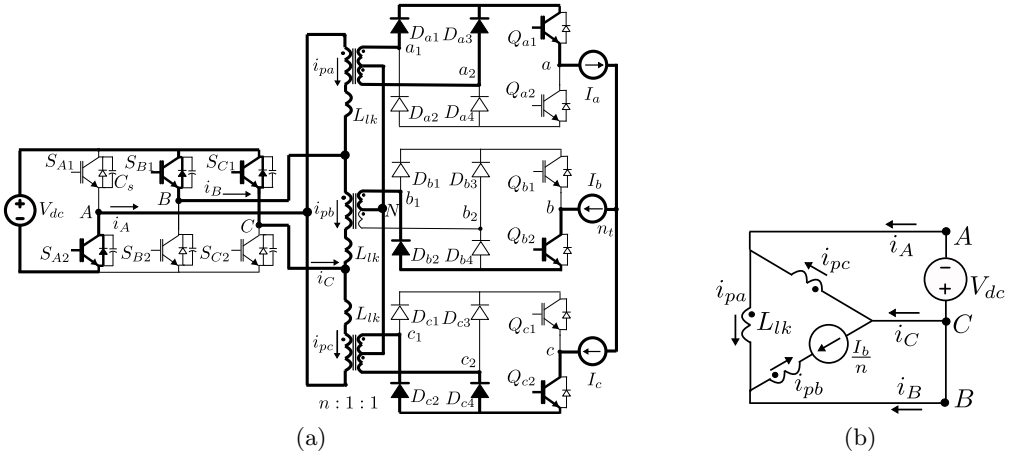


Figure 4.14: Mode 8- (a) Circuit diagram, (b) Equivalent circuit

against the direction of primary currents i_{pa} and i_{pc}. Hence, i_{pa} and i_{pc} fall further in this mode. The circuit dynamics are given in (4.17).

$$\begin{aligned} i_{pa} &= i_{pa}(t_7) - \frac{V_{dc}}{L_{lk}}(t - t_7) \\ i_{pc} &= i_{pc}(t_7) + \frac{V_{dc}}{L_{lk}}(t - t_7) \\ i_A &= i_A(t_7) - \frac{2V_{dc}}{L_{lk}}(t - t_7) \\ i_{B,C} &= i_{B,C}(t_7) + \frac{V_{dc}}{L_{lk}}(t - t_7) \end{aligned} \tag{4.17}$$

In secondary, I_a is transferred linearly from diode D_{a1} to D_{a3}. Similarly, I_c is also transferred from D_{c2} to D_{c4}. i_{pc} changes its direction in this mode. At t_8, $i_{pc} = \frac{I_c}{n}$ and $i_C = \frac{I_a}{n}$ and this mode ends. At t_8, I_c is completely transferred from D_{c2} to D_{c4} and D_{c2} is reverse biased.

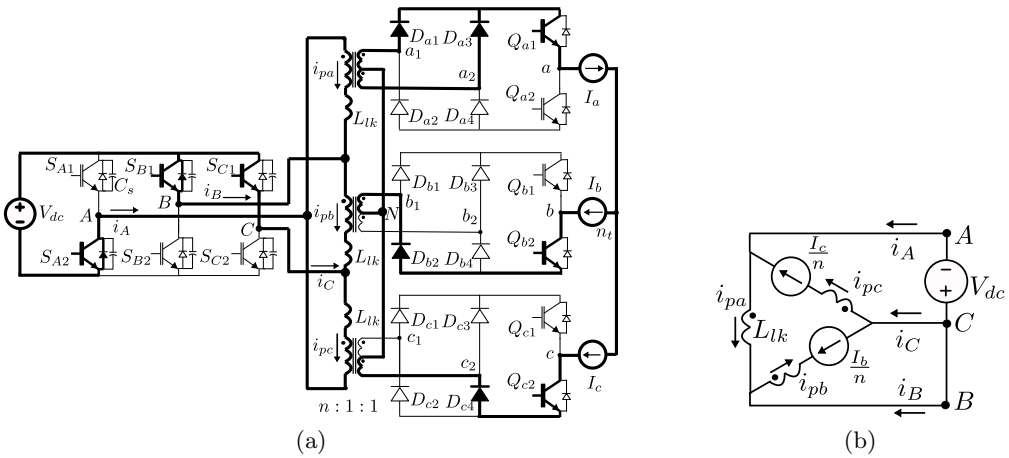


Figure 4.15: Mode 9- (a) Circuit diagram, (b) Equivalent circuit

Mode 9 ($t_8 < t < t_9$, Fig 4.5 and Fig. 4.12) The circuit configuration is presented in Fig. 4.15a and the corresponding simplified equivalent circuit is shown in Fig. 4.15b. In this mode, the slope of the pole current i_A is changed from $\frac{2V_{dc}}{L_{lk}}$ to $\frac{V_{dc}}{L_{lk}}$, as the primary current i_{pc} is clamped to $\frac{I_c}{n}$. The slope of the primary current i_{pa} and pole current i_B remain $\frac{V_{dc}}{L_{lk}}$. i_{pa} and $i_{A,B}$ change their directions. At t_9, $i_{pa} = -\frac{I_a}{n}$, $i_A = -\frac{(I_a + I_c)}{n}$ and $i_B = \frac{I_c}{n}$ and this mode ends. At t_9, I_a is shifted completely to D_{a3} from D_{a1} and D_{a1} is reverse biased.

4.3.7 Steady conduction mode I

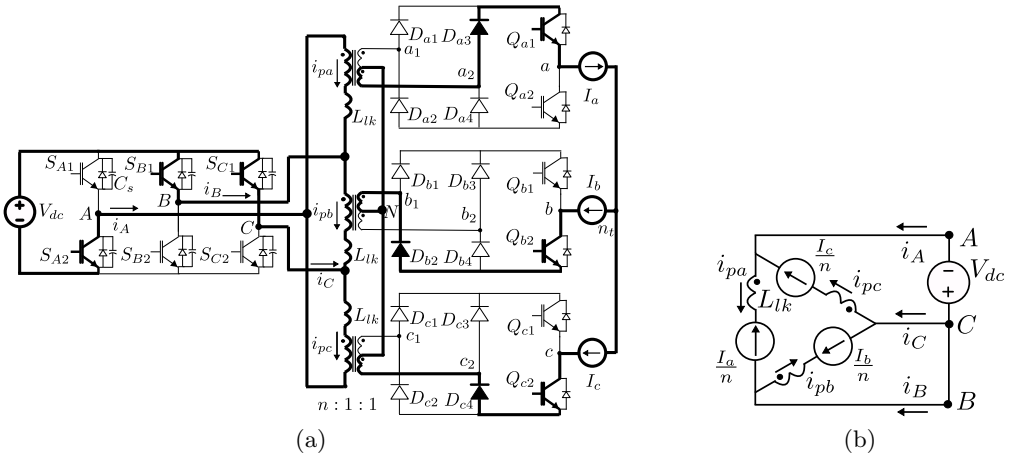


Figure 4.16: Mode 10- (a) Circuit diagram, (b) Equivalent circuit

Mode 10 ($t > t_9$, Fig 4.5) The circuit configuration and simplified equivalent circuit are presented in Fig. 4.16a and Fig. 4.16b respectively. Phase a and phase c are in active power transfer mode whereas the phase b is in zero state as indicated by the voltage polarities and current directions in Fig. 4.16b. Mode 10 is equivalent to Mode 1.

The above discussion presents the DSC operation in one half of T_s. Similar switching process is followed in the next half with other symmetrical switches. In the other half of sector I ($\theta \in [\frac{\pi}{6}, \frac{\pi}{3}]$), the DSC legs are switched in following order- $B - C - A$ (over one half of T_s). The transition of leg B has two modes same as discussed in mode 2 and 3. The transition of leg C follows a similar process discussed in mode 5. The transition of leg A is same as discussed in mode 7-9. The DSC has a similar sequence of operation in other sectors. For example, the DSC legs are switched in the order of B-A-C over one half of T_s in sector II ($\theta \in [\frac{\pi}{3}, \frac{\pi}{2}]$). Here, the process of switching transitions of leg B and leg A are same as described in Mode 2-3 and in mode 5 respectively. leg C has similar switching transition as described in Mode 7-9.

4.3.8 Estimation of limits on dead times to ensure ZVS

From above discussion, in the considered rage of θ, $\left(\theta \in [0, \frac{\pi}{3}]\right)$, it is seen that during the switching transition of leg B and leg C, respective pole currents i_B and i_C do not change their directions. But the pole current i_A changes its direction during the switching transition of leg

A. Note that, leg A is the reference leg over the considered range of θ. To achieve ZVS, these impose a strict upper limit on the dead time of leg A switches. To avoid hard-switching, the lower limits of the dead times of legs A, B, C switches are already given in (4.16), (4.14) and (4.11) respectively.

To ensure ZVS turn ON of $S_{A1} - S_{A2}$ the gating signal should be applied before the pole current, i_A becomes zero at t_Z and thereafter changes its direction and hence the anti-parallel diode stops conducting (see Fig. 4.12). So, there must be an upper limit of DT_A such that $DT_A < (t_Z - t_6) = \Delta t_Z$. To achieve ZVS ON over our considered range of $\theta \in [0, \frac{\pi}{6}]$, $DT_A < \Delta t_{Z,min}$. Here our objective is to find out $t_{Z,min}$. For the ease of estimation, the duration of mode 7, $(t_7 - t_6)$ and the change of current magnitudes in mode 7 are considered negligible. Hence, $i_A(t_6) \simeq i_A(t_7) = \dfrac{(I_a + I_c)}{n}$ and $i_{pc}(t_6) \simeq i_{pc}(t_7) = -\dfrac{I_c}{n}$. At the end of mode 8, at t_8, $i_{pc}(t_8) = \dfrac{I_c}{n}$. In mode 8, i_A has a slope of $\dfrac{2V_{dc}}{L_{lk}}$ and in mode 9 the slope is $\dfrac{V_{dc}}{L_{lk}}$. It is important to find out the slope of i_A between t_6 and t_Z. Using (4.6), (4.7) and (4.17), The interval $(t_8 - t_6) = (i_{pc}(t_8) - i_{pc}(t_6))\dfrac{L_{lk}}{V_{dc}} = \dfrac{2I_cL_{lk}}{nV_{dc}}$ and $i_A(t_8) = i_A(t_6) - \dfrac{2V_{dc}}{L_{lk}}(t_8 - t_6) = -\dfrac{I_{pk}}{2n}(\cos\theta + 3\sqrt{3}\sin\theta)$. $i_A(t_8)$ is negative in our considered range of θ. So, i_A changes its direction in mode 8 with a slope $\dfrac{2V_{dc}}{L_{lk}}$. Hence Δt_Z is given in (4.18).

$$\Delta t_Z = \frac{(I_a + I_c)L_{lk}}{2nV_{dc}} = \frac{\sqrt{3}I_{pk}L_{lk}}{2nV_{dc}}\cos\left(\frac{\pi}{6} - \theta\right) \tag{4.18}$$

At $\theta = 0$ and $\theta = \frac{\pi}{3}$, Δt_Z is minimum and $\Delta t_{Z_{min}} = \dfrac{0.75I_{pk}L_{lk}}{nV_{dc}}$. Hence the upper limit of the dead time, DT_A, between the gating signals of $S_{A1} - S_{A2}$ is given in (4.19).

$$DT_A \leq \frac{0.75I_{pk}L_{lk}}{nV_{dc}} \tag{4.19}$$

Following the modulation strategy of the topology 3, from sector to sector, the three legs of the DSC interchange their roles. For example, in sector II, leg C is considered as reference as shown in Table 4.1. Similar to leg A in sector I, leg C has a strict upper limit on dead time to achieve ZVS over complete sector II. Due to symmetry in pole current waveforms, the upper limit can be expressed as in (4.19). Same can be said for leg B in sector III. Hence to achieve ZVS turn ON over complete line cycle, by combining (4.16), (4.14), (4.11) and (4.19), the dead time of all three DSC legs is given as in (4.20).

$$max\left[\frac{1}{\omega_r'}\sin^{-1}\left(\frac{1.33nV_{DC}}{\omega_r'L_{lk}I_{pk}}\right), \frac{1}{\omega_r}\sin^{-1}\left(\frac{1.15nV_{DC}}{\omega_rL_{lk}I_{pk}}\right), \frac{2.3nC_sV_{dc}}{I_{pk}}\right] \leq DT \leq \frac{0.75I_{pk}L_{lk}}{nV_{dc}} \tag{4.20}$$

As $\omega_r' = \sqrt{2}\omega_r$, (4.20) can be further reduced to (4.21).

$$max\left[\frac{1}{\omega_r}\sin^{-1}\left(\frac{1.15nV_{DC}}{\omega_rL_{lk}I_{pk}}\right), \frac{2.3nC_sV_{dc}}{I_{pk}}\right] \leq DT \leq \frac{0.75I_{pk}L_{lk}}{nV_{dc}} \tag{4.21}$$

4.3.9 Comparison of soft-switching performance between topology 2 and 3

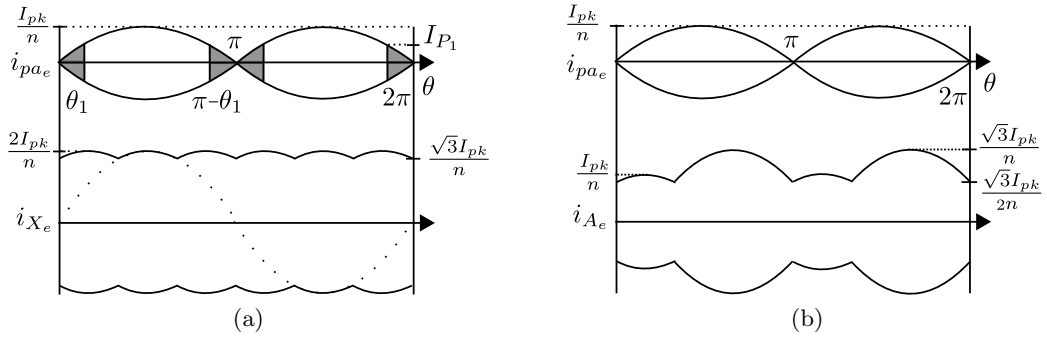


Figure 4.17: DSC pole current envelope- (a) topology 2, (b) topology 3

Fig. 4.17a shows the DSC pole current envelopes of the topology 2 shown in Fig. 3.2a. The envelope of the pole current i_X of leg $S_1 - S_2$, i_{X_e} is shown over one line cycle. The pole current envelope of leg $S_{A3} - S_{A4}$, i_{pa_e} is also presented. Other two pole currents i_{pb} and i_{pc} have similar envelop as i_{pa_e}. The As discussed in section 3.3.10 of chapter 3, the magnitude of i_{X_e} varies sinusoidally between $\frac{\sqrt{3}I_{pk}}{n}$ and $\frac{2I_{pk}}{n}$ over a line cycle and never becomes zero. A dead time can be set using (3.12), such that $S_1 - S_2$ is soft-switched over complete line cycle. But the magnitude of remaining three legs of the DSC have pole current envelops (as i_{pa_e}, shown in Fig. 3.19) become zero twice over a line cycle. Hence these legs are hard-switched in the shaded regions of Fig. 3.19 when the pole current magnitudes are small. The boundary of hard-switching zone, θ_1, is given in (B.7).

On the other hand, the pole current envelope of leg A of the topology 3, i_{A_e} is shown in Fig. 4.17b. The other two legs B and C have similar pole current envelops. The magnitude of the pole current envelops are always greater than $\frac{\sqrt{3}}{2}nI_{pk}$ as seen in Fig. 4.17b. **Hence the ZVS turn ON of the all the DSC switches can be ensured through out the line cycle by satisfying (4.21).**

One important observation is that though the pole currents of the DSC legs are different, both the topologies have same transformer currents. HFT primary current envelops, i_{pa_e}, of the two topologies are shown in Fig. 4.17. So, both the topologies have similar loss in HFTs.

4.4 Converter design

We have designed the converter for a target application of grid integration of utility scale solar photo-voltaic. The specification of the design is given in Table 2.1. The topology is modulated at the 85% of its maximum possible modulation index. Hence the modulation index $M = \frac{nV_{pk}}{V_{dc}} = 0.85$. Thus the high frequency transformer (HFT) primary to secondary turns ratio is $n = 2.0$.

4.4.1 Device blocking voltage and RMS currents

For UPF operation, (2.24) and (2.25) are valid here. The RMS current in DSC switches, $S_{A1} - S_{C2}$, is given below.

$$I_{RMS,S_{A1}-S_{C2}} = \frac{I_{pk}}{n}\sqrt{0.46 + 0.24M} = \frac{\sqrt{0.2 + 0.1M}}{M}\frac{P}{V_{dc}} \tag{4.22}$$

The peak current through $S_{A1} - S_{C2}$ is $I_{pk,S_{A1}-S_{C2}} = \frac{\sqrt{3}I_{pk}}{n} = \frac{2}{\sqrt{3}M}\frac{P}{V_{dc}}$. With $M = 0.85$, $I_{RMS,S_{A1}-S_{C2}} = 0.64\frac{P}{V_{dc}}$ and $I_{pk,S_{A1}-S_{C2}} = 1.36\frac{P}{V_{dc}}$. The Blocking voltage of DC side switches are V_{dc}.
Due to structural similarity, the peak and RMS currents, blocking voltage of the ASC power devices are same as topology 1. The RMS currents of the HFTs are also same as topology 1.

4.4.2 Estimation of Converter Power Loss

In this section, power loss expressions of the DSC of the topology 3 is analytically derived. The detailed derivation steps are given in Appendix A. As the switching strategy of the ASC and the current and voltage waveforms seen by the HFTs are same as topology 1, the power loss expressions of the ASC switches, diodes and HFTs are same as given in section 2.4.2 of chapter 2.

Loss estimation of DSC switches and diodes

To estimate the conduction loss of a switch, first the RMS and average currents through the switch are estimated. Using (2.30) the conduction loss expression of the switch is obtained.

The conduction loss in a switch of $S_{A1} - S_{C2}$ is given as-

$$P_{C_{S_{A1}}} = (0.46 + 0.24M)\frac{I_{pk}^2 R_{CE}}{n^2} + (0.28 + 0.25M)\frac{I_{pk}V_{CE}}{n} \tag{4.23}$$

Where V_{CE} and R_{CE} are constant voltage drop and on state resistance of the IGBT module respectively. The conduction loss expression of an anti-parallel diode of switches $S_{A1} - S_{C2}$ is given as

$$P_{C_{D,SA1}} = (0.29 - 0.26M)\frac{I_{pk}^2 R_D}{n^2} + (0.28 - 0.25M)\frac{I_{pk}V_D}{n} \tag{4.24}$$

The anti-parallel diodes have a voltage drop V_D and on state resistance R_D.
The turn ON of DSC switches are ZVS.

4.4.3 Design of high frequency transformers

The ASC structure and HFTs of topology 3 is same as topology 1. The applied voltage and the currents of the HFTs are also same as in topology 1. Hence the area product of the HFTs used in topology 3 is same as topology 1 and is given in subsection 2.4.3 of chapter 2.

4.4.4 Input and Output Filter Requirement of the Converter

At the DC input of the converter, a capacitor is required to support the high frequency switching ripple current. Similarly, at the output port, inductors are required to filter out the high frequency voltage ripple. We have seen in chapter 3, THD is a measure of filter requirement. In this section we have estimated input current and output pole voltage THDs of the topology 3.

Filter capacitance requirement at the input of the converter

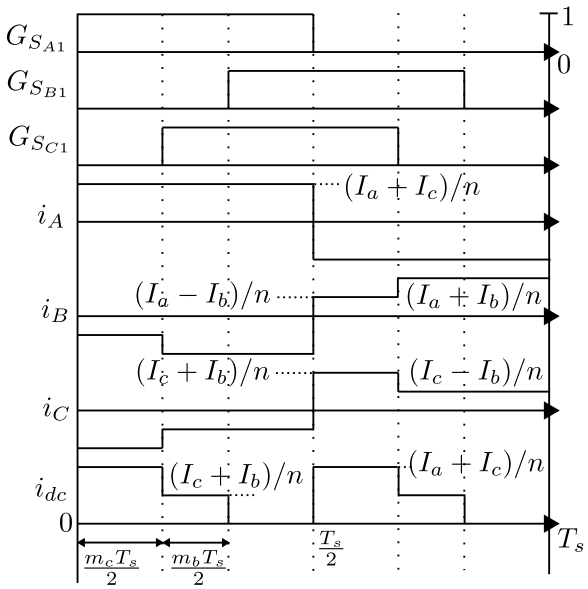


Figure 4.18: Input DC link current of the proposed converter in sector I ($\theta \in (0, \frac{\pi}{6})$)

In Fig. 4.18, i_{dc} is the current drawn from the DC link for switching operation of the DSC. Net DC link current is given by $i_{dc} = i_A{\cdot}G_{S_{A1}} + i_B{\cdot}G_{S_{B1}} + i_C{\cdot}G_{S_{C1}}$. In $\theta \in (0, \frac{\pi}{6})$ the modulation signals are given as $m_a = M\cos\theta$ and $m_b = M\cos\left(\theta + \frac{\pi}{3}\right)$ and $m_c = M\sin\left(\theta + \frac{\pi}{6}\right)$. In $\theta \in (0, \frac{\pi}{6})$ the line current magnitudes are $I_a = I_{pk}\cos\theta$, $I_b = I_{pk}\cos\left(\theta + \frac{\pi}{3}\right)$ and $I_c = I_{pk}\sin\left(\theta + \frac{\pi}{6}\right)$ respectively. The DC link current i_{dc} has symmetry over $\frac{\pi}{6}$. The RMS of DC link current can be derived as follows.

$$\begin{aligned} i_{dc,rms}^2 =& \frac{6}{\pi}\int_0^{\frac{\pi}{6}} \left[\left(\frac{I_a + I_c}{n}\right)^2 m_c + \left(\frac{I_b + I_c}{n}\right)^2 m_b\right] d\theta \\ =& \frac{15M}{2\pi}\left(\frac{I_{pk}}{n}\right)^2 = 2.387M\left(\frac{I_{pk}}{n}\right)^2 \end{aligned} \tag{4.25}$$

The average DC link current $i_{dc,avg}$ can be derived from input and output power balance and

is given as $i_{dc,avg} = \dfrac{3MI_{pk}}{2n}$. The ripple current RMS, $\tilde{i}$ is given as

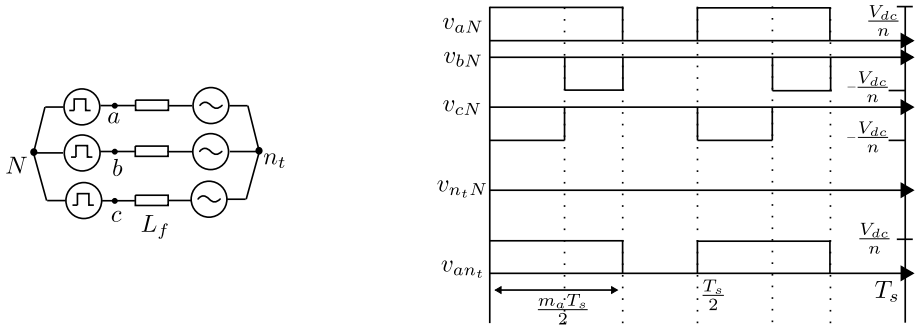
$$\begin{aligned}\tilde{i} =& \sqrt{i_{dc,rms}^2 - i_{dc,avg}^2} \\ =& \frac{I_{pk}}{n}\sqrt{(2.387M - 2.25M^2)}\end{aligned} \tag{4.26}$$

THD_I is given as

$$THD_I = \frac{\tilde{i}}{i_{dc,avg}} = \frac{\sqrt{(2.387M - 2.25M^2)}}{1.5M} \tag{4.27}$$

For $M = 0.85$, THD_I is 0.498.

Output filter inductance requirement



(a) (b)

Figure 4.19: (a) Equivalent circuit of the converter seen from load, (b) Pole voltage waveforms of the converter in sector I ($\theta \in (0, \frac{\pi}{6})$)

Fig. 4.19a shows the equivalent circuit configuration of the converter (seen from the load). For balanced 3ϕ load, $v_{an_t} + v_{bn_t} + v_{cn_t} = 0$. By applying KVL, in sector 1, following circuit equation can be written-

$$\begin{aligned} v_{aN} &= v_{an_t} + v_{n_tN} \\ v_{bN} &= v_{bn_t} + v_{n_tN} \\ v_{cN} &= v_{cn_t} + v_{n_tN} \\ v_{n_tN} &= \frac{v_{aN} + v_{bN} + v_{cN}}{3} \end{aligned} \tag{4.28}$$

Thus $v_{an_t} = v_{aN} - v_{n_tN} = \dfrac{2v_{aN} - v_{bN} - v_{cN}}{3}$. Based on the proposed modulation strategy, applied pole voltages in sector-I ($\theta \in [0, \frac{\pi}{6}]$) are shown in Fig. 4.19b. It is seen that, $v_{an_t} = v_{aN}$, $v_{bn_t} = v_{bN}$ and $v_{cn_t} = v_{cN}$ as $v_{n_tN} = 0$. In sector-I, the modulation signal is given as $m_a = M\cos\theta$. The waveform of v_{an_t} has quarter wave symmetry. The RMS of the pole voltage, v_{an_t}

is expressed as -

$$\begin{aligned} v_{an_t,rms}^2 =& \frac{2}{\pi}\left(\int_0^{\frac{\pi}{2}} m_a \left(\frac{V_{dc}}{n}\right)^2 d\theta\right) \\ =& \frac{2}{\pi n^2} M V_{dc}^2 = 0.64M\left(\frac{V_{dc}}{n}\right)^2 \end{aligned} \tag{4.29}$$

The RMS of fundamental component of v_{an_t} is $v_{an_t,rms1} = \frac{V_{pk}}{\sqrt{2}} = \frac{MV_{dc}}{\sqrt{2}n}$. The ripple voltage RMS of v_{an_t} can be expressed as-

$$\tilde{v} = \sqrt{v_{an_t,rms}^2 - v_{an_t,rms1}^2} = \frac{V_{dc}}{n}\sqrt{[0.64M - 0.5M^2]} \tag{4.30}$$

The output pole voltage THD is given as-

$$THD_V = \frac{\tilde{v}}{v_{an_t,rms1}} = \frac{\sqrt{[1.273M - M^2]}}{M} \tag{4.31}$$

For the modulation index $M = 0.85$, THD_V is 0.7.

4.5 Experimental validation

4.5.1 Experimental set-up

The operation of the topology 3 is experimentally verified using a 3.7 kW hardware prototype (see Fig. 4.20). Table 4.2 presents the operating condition. 1200V, 75A SEMIKRON IGBT modules (SKM75GB123D) are used to implement the half-bridge legs of the converter. Secondary diode bridges use IXYS fast recovery 1200V, 75A diodes, MEE 75-12 DA. Optically isolated gate driver, ACPL 339J, with driving voltage level ± 15V, is used to drive the IGBTs. The switching frequency of the DSC is 20kHz. A 600 ns dead-time that satisfies all the dead-time conditions derived in the last section is provided between two IGBTs of a half-bridge leg. Three ferrite core (E 80/38/20) HFTs with turns ratio 51:34:34 are used. The transformers have leakage inductance (seen from primary) in the order of 6-8μH. To satisfy the dead-time condition given in (4.20), an additional 48 μH inductor is connected in series with each primary winding of the HFTs. To implement the modulation strategy and to generate gating signals of the IGBTs, an ARM-FPGA based system-on-chip (SoC) control platform, Xilinx Zynq-7000 is used.

Table 4.2: Operating condition of topology 3

Output power (P)	3.7kW
Output peak voltage (V_{pk})	190V
DC input (V_{dc})	350V
HFT turns ratio (n)	3/2
Line frequency ($f_o = \frac{\omega_o}{2\pi}$)	50Hz
Switching frequency ($f_s = \frac{1}{T_s}$)	20kHz

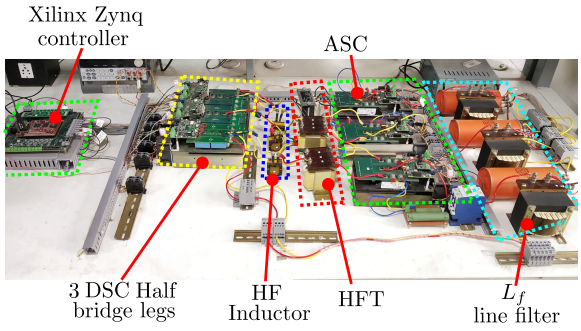


Figure 4.20: Hardware prototype

4.5.2 Experimental validation of modulation strategy

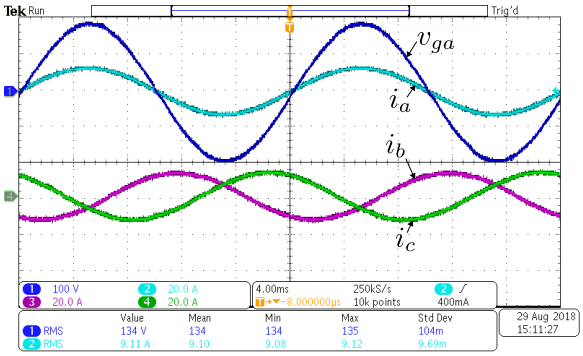


Figure 4.21: Line output- [CH1] v_{ga} (100V/div.), [CH2] i_a (20A/div.), [CH3] i_b (20A/div.), [CH4] i_c (20A/div.). Time scale 4ms/div.

A balanced 3ϕ, 50 Hz AC voltage source ($v_{ga,gb,gc}$) is connected to the converter. Input DC bus voltage is 350 V. M is adjusted to get the peak of output phase voltage (V_{pk}) of 190 V. Fig. 4.21 shows the phase voltage v_{ga} and line currents $i_{a,b,c}$. The experimentally measured peak value (I_{pk}) of the line currents is 12.9 A. The theoretically estimated $I_{pk} = \frac{P}{1.5V_{pk}} = 12.98$ A. At 50 Hz, the impedance of line filter ($L_f = 2.5$mH) is relatively small. Hence v_{ga} is almost in phase with the line current i_a.

The unipolar PWM pole voltage w.r.t HFT neutral, v_{aN}, is shown in Fig. 4.22. v_{aN} has voltage levels $\frac{V_{dc}}{n} = 233$V and zero. In this figure, in [CH3], the HFT primary voltage, v_{AB} is shown. v_{AB} is PWM high frequency AC with voltage levels of $\pm V_{dc} = \pm 350$ V and zero. The primary winding current i_{pa} and the DSC pole current i_A are also shown in 4.22. The waveform of i_{pa}, as seen in the figure, is high frequency square-wave with magnitude varied sinusoidally over a line cycle. The envelope of i_{pa} has the experimentally measured peak of 8.6 A. The theoretically estimated peak is $\frac{I_{pk}}{n}$=8.65A. Unlike i_{pa}, the envelope of i_A never touches time axis as seen in Fig. 4.22. This pole current envelope helps to achieve soft-turn ON of the leg switches $S_{A1} - S_{A2}$ over complete line cycle. The current envelope has a measured peak of $\sqrt{3}I_{pk}/n$ =14.9A.

Switching cycle waveforms of the transformer primary voltages ($v_{AB,BC,CA}$) and the primary currents (i_{pa}, i_{pb}) are shown in Fig. 4.23a (in sector I, $\theta \approx \frac{\pi}{90}$). Steady-state magnitude of primary currents, i_{pa} and i_{pb}, are $\frac{I_a}{n} = 8.65\cos(\frac{\pi}{90}) \approx 8.6$ A and $\frac{I_b}{n} = 8.65\cos(\frac{\pi}{90} + \frac{\pi}{3}) \approx$

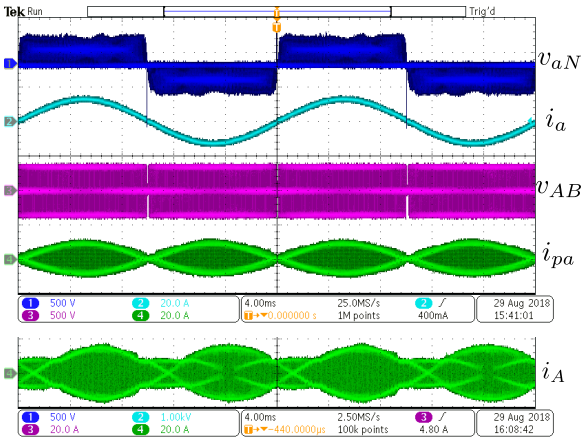
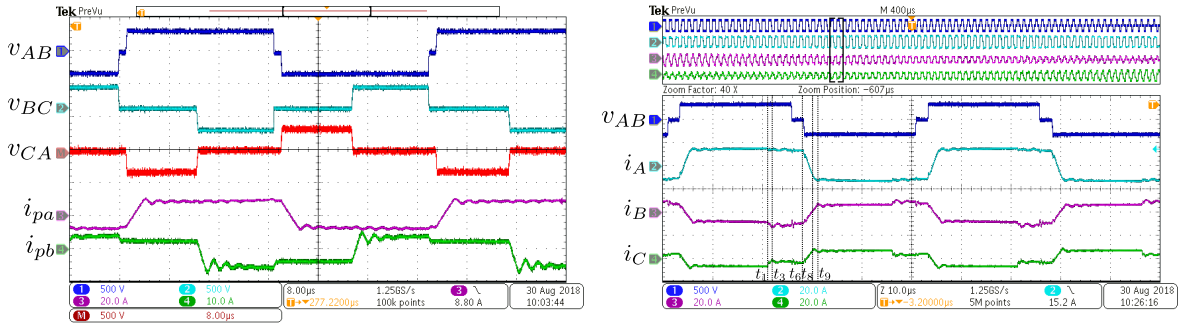


Figure 4.22: Pole voltage and current waveforms- [CH1] v_{aN} (500V/div.), [CH2] i_a (20A/div.), [CH3] v_{AB} (500V/div.), [CH4] i_{pa} (20A/div.); [CH4] i_A (20A/div.). Time scale 4ms/div.



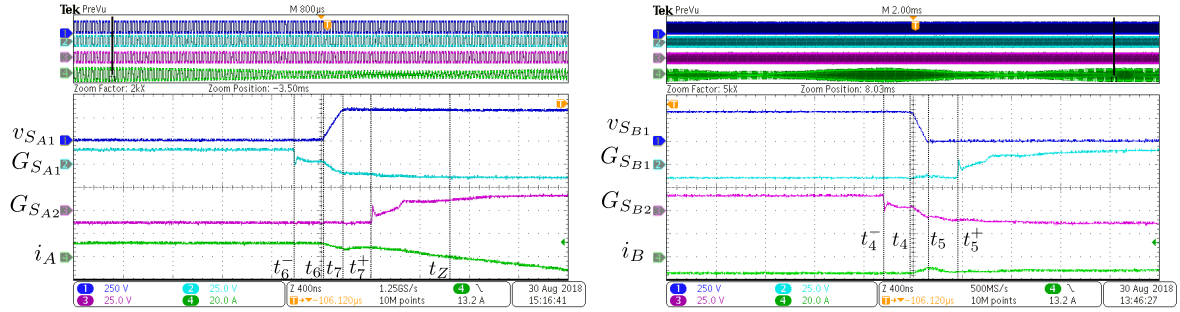
(a) (b)

Figure 4.23: (a) Transformer primary voltages and primary currents (in sector I at $\theta \approx \frac{\pi}{90}$) - [CH1] v_{AB} (500V/div.), [CH2] v_{BC} (500V/div.), [M] v_{CA} (500V/div.), [CH3] i_{pa} (20A/div.), [CH4] i_{pb} (10A/div.). Time scale 8μs/div. (b) Primary voltage and the DSC pole currents (in sector I at $\theta \approx \frac{\pi}{18}$)- [CH1] v_{AB} (500V/div.), [CH2] i_A (20A/div.), [CH3] i_B (20A/div.), [CH4] i_C (20A/div.). Time scale 10μs/div.

3.9 A respectively. This result verifies the analytical voltage and current waveforms shown in Fig. 4.4 and Fig. 4.5. Hence, the modulation strategy and operation of the DSC described in Section 4.2 and 4.3 are also verified. As expected, it is seen that the polarity of primary winding current changes only when the applied primary voltage jumps to $\pm 350V$ from zero. Flux balance of HFT is achieved over T_s.

Fig. 4.23b presents the DSC pole currents $i_{A,B,C}$ in sector I at $\theta \approx \frac{\pi}{18}$. The experimental waveforms closely match with the analytical pole current waveforms in sector I shown in Fig. 4.5. The steady-state magnitude of i_A is 13.9 A. From the experimental result, the change in magnitude of pole currents i_B and i_C in Mode 2-3 ($t_1 < t < t_3$) are clearly observable. As discussed in section 4.3, i_B and i_C do not change their direction in Mode 2-3. The pole currents change their direction in Mode 7-9 ($t_6 < t < t_9$) as seen in Fig. 4.23b.

4.5.3 Experimental validation of ZVS of the DSC



(a) (b)

Figure 4.24: (a) Switching transition of leg A (in sector I at $\theta \approx \frac{\pi}{18}$)- [CH1] $v_{S_{A1}}$ (250V/div.), [CH2] $G_{S_{A1}}$ (25V/div.), [CH3] $G_{S_{A2}}$ (25V/div.), [CH4] i_A (20A/div.). Time scale 400ns/div. (b) Switching transition of leg B (in sector I at $\theta \approx \frac{\pi}{18}$)- [CH1] $v_{S_{B1}}$ (250V/div.), [CH2] $G_{S_{B1}}$ (25V/div.), [CH3] $G_{S_{B2}}$ (25V/div.), [CH4] i_B (20A/div.). Time scale 400ns/div.

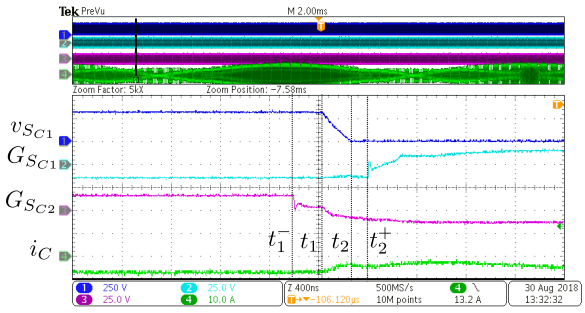


Figure 4.25: Switching transition of leg C (in sector I at $\theta \approx \frac{\pi}{18}$)- [CH1] $v_{S_{C1}}$ (250V/div.), [CH2] $G_{S_{C1}}$ (25V/div.), [CH3] $G_{S_{C2}}$ (25V/div.), [CH4] i_C (10A/div.). Time scale 400ns/div.

Switching transition of leg A

The switching transition of leg A in sector I (at $\theta \approx \frac{\pi}{18}$) is presented in Fig. 4.24a. This result verifies the switching process discussed in Mode 7-9 in section 4.3. The gating pulse of

S_{A1}, $G_{S_{A1}}$, is withdrawn at t_6^-. As seen in Fig. 4.24a, at t_6, $v_{S_{A1}}$ starts to build up. Due to device capacitance C_s, voltage changes slowly across S_{A1} and hence the turn OFF loss of S_{A1} has reduced. At t_7, $v_{S_{A1}} = V_{dc} = 350V$, $v_{S_{A2}} = 0V$ and the pole current i_A is still positive i.e. flowing in the same direction. Hence the anti-parallel diode of S_{A2} is in conduction. To achieve ZVS turn ON, at t_7^+, the gating pulse of S_{B2}, $G_{S_{B2}}$ is applied before i_A becomes zero. Sometime after, i_A becomes zero and then changes its direction at t_Z.

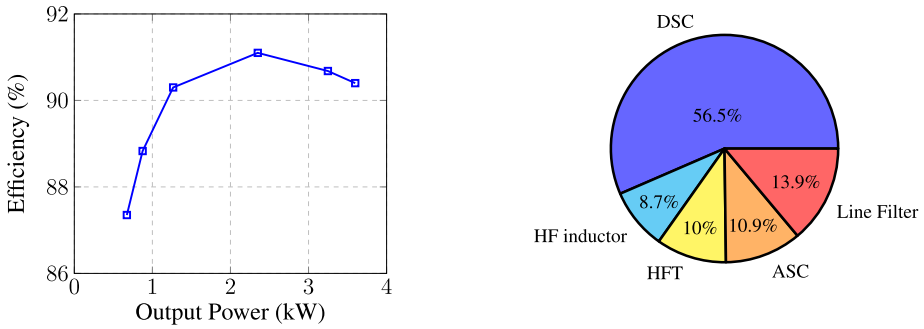
Switching transition of leg B

Fig. 4.24b shows the switching transition of leg B described in Mode 5-6 in section 4.3. As seen in the figure, S_{B2} is ON and conducting initially. The gating pulse of S_{B2} is withdrawn at t_4^-. The voltage across $S_{B1} - S_{B2}$ starts changing slowly and linearly at t_4. Due to device capacitance C_s, the slow change in voltage helps to reduce the turn OFF loss of S_{B2}. The voltage across S_{B1}, $v_{S_{B1}}$, falls to zero at t_5. Sometime after, at t_5^+, S_{B1} is turned ON. Thus ZVS turn ON of S_{B1} is ensured.

Switching transition of leg C

Fig. 4.25 shows the switching transition of $S_{C1} - S_{C2}$ discussed in Mode 2-3 in section 4.3. The gating pulse of S_{C2} is removed at t_1^-. As seen in the figure, sometime after, at t_1, the voltages across $S_{C1} - S_{C2}$ start to change. Due to device capacitance C_s, the turn OFF loss of S_{C2} is reduced. The voltage across S_{C1}, $v_{S_{C2}}$, becomes zero at t_2. The pole current (i_C) direction does not change. Hence the anti-parallel diode of S_{C1} is in conduction. At t_2^+, gating pulse of S_{C1} is applied ensuring ZVS turn ON of S_{C1}.

4.5.4 Measured loss and efficiency



(a) (b)

Figure 4.26: (a) Efficiency of the proposed DC-AC converter, (b) Loss distribution at 2.35kW output power

Fig. 4.26a presents the experimentally measured efficiency of the converter with DC input 350V. The plot is given for a range of output power from 0.6kW to 3.7kW. As seen in the figure, the converter has a peak efficiency of 91.1% at 2.35kW output power. Fig. 4.26b shows

the loss distribution of the converter at 2.35kW output. Out of total loss, The DSC has a loss of 56.5% and the line frequency switched ASC has loss of only 11%.

4.6 Conclusion

This chapter introduced a single-stage unidirectional 3ϕ high-frequency link inverter topology with reduced number of active switches and improved soft-switching performance compared to the topology 1 and 2 presented in the previous chapters. The converter supports only UPF operation and for any reactive power support additional shunt compensator is needed. The active switches of the ASC of the new topology are line frequency switched like topology 1 and 2. Zero voltage turn ON of all the active switches of the DSC can be ensured over entire line cycle, which is not possible in topology 1 and 2. The steady state operation of the converter is presented with detailed circuit analysis. The conditions on dead times are derived to ensure ZVS of the DSC. A comparison of the soft-switching performance of the new topology is presented with the topology 2. To find out the filtering requirement of the new topology, input current and output voltage THDs are estimated. To estimate the converter power loss analytically, the closed form loss expressions are presented. Different aspects of the modulation strategy, ZVS transitions are experimentally verified on laboratory scale hardware prototype. Efficiency and Power loss at different stages are experimentally measured.

Chapter 5

Unidirectional HFL DC-3ϕ AC Conversion with Two Pulsating DC Links: Topology-4

5.1 Introduction

The unidirectional high-frequency-link DC-AC converter topologies discussed so-far can support only unity power factor load. To compensate the line filter drop and to support any other power factor load, additional shunt compensator is need as discussed in section 2.6 of chapter 2. Though the topologies are targeted for grid integration of utility scale PV or fuel cell where the power flow is unidirectional (DC to AC), in case of large scale PV plants, reactive power support with power factor $\pm$ 0.9/0.95 is essential at the grid end [43, 44]. Additionally, the topologies discussed so-far has three pulsating DC links which require three HFTs and three sets of diode bridge rectifiers.

In this chapter, a new unidirectional HFL inverter topology is introduced which has two pulsating DC links and employs two HFTs and two diode bridges. Like the topologies discussed in the chapters 2, 3 and 4, all the active switches in the ASC are low frequency switched. Though unidirectional, this new topology has inherent ability to support $\pm$ 0.866 power factor load and does not require additional shunt compensator. Hence suitable for the grid integration of large scale PV. In this chapter, the derivation of the topology is discussed in detail. The high frequency switched DSC of the new converter is soft-switched throughout the line cycle. Detailed circuit operation and switching process are presented in this chapter. To achieve ZVS, the upper and lower bounds on the dead time of the DSC legs are derived. The converter power loss is obtained analytically. The filtering requirements in terms of input current and output voltage THDs are presented. Design and implementation aspects of a 2kW hardware prototype is first discussed followed by experimental results are presented to verify the converter operation. The content of this chapter is reported in [45].

5.2 Converter Configuration and Modulation Strategy

In this section, a detailed discussion is presented to show the generation of the balanced three phase AC voltages from two pulsating DC links with sinusoidal average voltages with the help of a low frequency switching network. Then the generation of the two pulsating DC links with

desired average voltages is described.

Fig. 5.1 shows the configuration of the new topology, topology 4. *po* and *oq* are the two pulsating DC links connected in series. A three-level T-type neutral point clamp (NPC) 3ϕ inverter is used to generate the balanced three phase line voltages from the pulsating DC links. To generate the pulsating DC links, isolated DC-DC converter is used as shown in Fig. 5.1. The DSC of the topology 4 has three half bridge legs, $S_1 - S_2$, $S_{A1} - S_{A2}$ and $S_{B1} - S_{B2}$. Two high frequency transformers (HFT), Tr_1 and Tr_2 with turns ratio $n : 1$ are employed. The primary windings of the HFTs are connected in series and form the node N which is again connected to the pole of leg $S_1 - S_2$. The other to terminals of the primary windings are connected to the poles of the remaining two DSC legs. The secondary windings of Tr_1 and Tr_2 are connected to the diode-bridge rectifiers $D_1 - D_4$, $D_5 - D_8$ respectively. The output terminals of the diode-bridges are connected in series and thus form the pulsating DC links *po* and *oq*. The converter is connected to a balanced 3ϕ voltage source through filter inductors L_f as shown in Fig. 5.1.

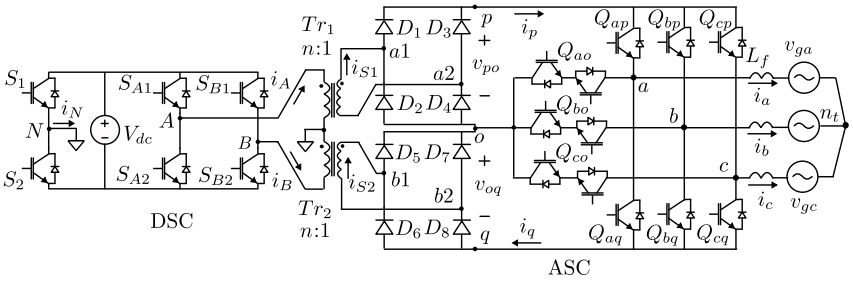


Figure 5.1: Configuration of the topology 4

5.2.1 Generation of balanced 3ϕ voltages from two pulsating DC links

At first, we will describe a switching strategy of the three level NPC inverter. Then, with the given switching strategy of the NPC inverter, to generate the balanced three phase line frequency average pole voltages (Fig. 5.2), $\overline{v}_{ab} = \sqrt{3}V_{pk}\sin\theta$, $\overline{v}_{bc} = \sqrt{3}V_{pk}\sin\left(\theta - \frac{2\pi}{3}\right)$ and $\overline{v}_{ca} = \sqrt{3}V_{pk}\sin\left(\theta + \frac{2\pi}{3}\right)$, we will further find out the required average DC link voltages ($\overline{v}_{po}$, $\overline{v}_{oq}$) and the relation ship between the DC link currents (i_p, i_q) and the line currents (i_a, i_b, i_c).

The ASC three level NPC is switched six times over a line cycle ($\theta \in (0, 2\pi)$). Henceforth, the three level NPC inverter structure of the ASC is called as unfolder. The switching states of the unfolder is given in Table 5.1. The switching states are defined based on the connections between the DC link nodes (p, o, q) and the unfolder poles (a, b, c). The unfolder poles (a, b, c) can be connected to the node p through the switches $Q_{(a,b,c)p}$, node o through the switches $S_{(a,b,c)o}$ and node q through the switches $Q_{(a,b,c)q}$ respectively. Unfolder switching state $[oqp]$ indicates that the pole a is connected to node o through Q_{ao}, the pole b is connected to node q through Q_{bq} and the pole c is connected to node p through Q_{cp}. Similarly the other states are also defined. Following the switching states, the unfolder two quadrant switches are switched at line frequency whereas the four quadrant switches are switched at twice of the line frequency

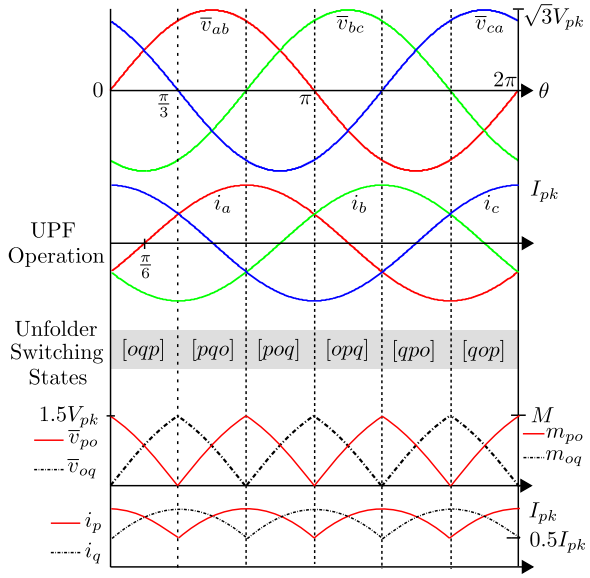


Figure 5.2: Modulating strategy of the unfolder

hence incurring negligible switching loss.

Table 5.1: Unfolder switching states

θ	$[0,\frac{\pi}{3}]$	$[\frac{\pi}{3},\frac{2\pi}{3}]$	$[\frac{2\pi}{3},\pi]$	$[\pi,\frac{4\pi}{3}]$	$[\frac{4\pi}{3},\frac{5\pi}{3}]$	$[\frac{5\pi}{3},2\pi]$
State	$[oqp]$	$[pqo]$	$[poq]$	$[opq]$	$[qpo]$	$[qop]$

From the switching states of the unfolder, the DC link average voltages ($\overline{v}_{po}$ and $\overline{v}_{oq}$) and currents i_p, i_q are obtained and are given in Table 5.2. For example, when the switching state is

Table 5.2: Rectifier output voltages and currents

Unfolder State	$[oqp]$	$[pqo]$	$[poq]$	$[opq]$	$[qpo]$	$[qop]$
$\overline{v}_{po}$	$\overline{v}_{ca}$	$-\overline{v}_{ca}$	$\overline{v}_{ab}$	$-\overline{v}_{ab}$	$\overline{v}_{bc}$	$-\overline{v}_{bc}$
$\overline{v}_{oq}$	$\overline{v}_{ab}$	$-\overline{v}_{bc}$	$\overline{v}_{bc}$	$-\overline{v}_{ca}$	$\overline{v}_{ca}$	$-\overline{v}_{ab}$
i_p	i_c	i_a	i_a	i_b	i_b	i_c
i_q	$-i_b$	$-i_b$	$-i_c$	$-i_c$	$-i_a$	$-i_a$

$[oqp]$, the unfolder switches Q_{ao}, Q_{bq} and Q_{cp} are ON. Hence, the DC link port po is connected across the unfolder pole terminals ca and oq is connected across ab. Thus $\overline{v}_{po} = \overline{v}_{ca}$, $\overline{v}_{oq} = \overline{v}_{ab}$ and the DC link currents $i_p = i_c$ and $i_q = -i_b$. To generate the average DC link voltages as given in Table 5.2, the modulation signals of the DSC, $m_{po} = \dfrac{n\overline{v}_{po}}{V_{dc}}$ and $m_{oq} = \dfrac{n\overline{v}_{oq}}{V_{dc}}$ are shown in Fig. 5.2. M is defined as $M = \dfrac{1.5nV_{pk}}{V_{dc}}$ and $M \in [0, 1]$.

5.2.2 Generation two pulsating DC links from input DC bus

The DSC is phase shift modulated (PSM) to generate average rectifier output voltages $\overline{v}_{po} = \dfrac{m_{po}V_{dc}}{n}$ and $\overline{v}_{oq} = \dfrac{m_{oq}V_{dc}}{n}$. The modulation strategy over a switching cycle T_s is shown in Fig. 5.3. F is a high frequency (HF) square wave signal with period T_s and 50% duty ratio.

T_s is considered to be flux balance cycle of the HFTs. A unity magnitude, unipolar saw-tooth carrier (C) with period $\frac{T_s}{2}$, aligned with F is considered. Two switches in each half-bridge leg of the DSC are complementary switched with a dead time to avoid short circuit of the DC source, V_{dc}. F is assigned to be the gating signal of S_1, G_{S_1}. The modulation signals m_{po} and

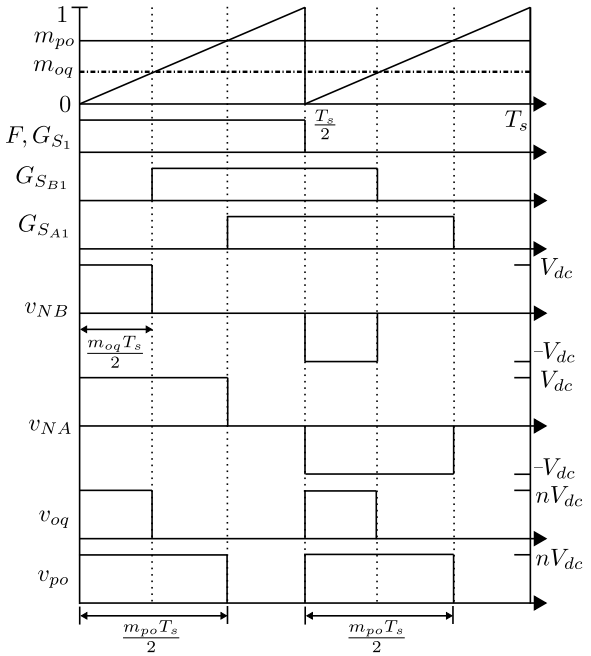


Figure 5.3: Modulation of DC side bridge

m_{oq} are compared with the saw-tooth carrier to generate the gating signals of $S_{A1} - S_{A2}$ and $S_{B1} - S_{B2}$ respectively. Slowly varying modulation signals are approximated as constant over a switching cycle T_s. The gating signal of S_{A1}, $G_{S_{A1}}$ is (a square wave with period T_s and 0.5 duty ratio) phase shifted by $\frac{m_{po}T_s}{2}$ w.r.t F. Similarly, the gating signal of S_{B1}, $G_{S_{B1}}$ is phase shifted by $\frac{m_{oq}T_s}{2}$ w.r.t F as shown in Fig. 5.3. The suggested modulation strategy generates pulse width modulated (PWM) high frequency AC voltages v_{NA} and v_{NB} with voltage levels $\pm V_{dc}$ and 0 which are fed to Tr_1 and Tr_2 respectively. In the secondary, the diode bridges $D_1 - D_4$ and $D_5 - D_8$ rectify the high frequency AC and generate pulsating DC voltages v_{po} and v_{oq} with required average $\overline{v}_{po}$, $\overline{v}_{oq}$ respectively.

5.2.3 Non-unity power factor operation

Though the topology 4 has diode rectifiers in the ASC and does not employ any DC link capacitors after the rectifier stage, it can support upto 30° leading and lagging power factor stand alone load. The rectifier output currents i_p and i_q are positive instantaneously. Following Table 5.2 and Fig. 5.2, in state $[pqo]$, it can be seen that $i_p(= i_a)$ becomes negative when i_a lags more than 30°. Similarly $i_q(= -i_b)$ becomes negative when i_b leads more than 30°. The negative DC link currents cannot be supported by the diode bridges and hence the converter operation is power factor restricted.

5.3 Steady-state Operation of the Converter

The converter operation at UPF, over one switching cycle T_s, is described in detail when the unfolder switching state is $[oqp]$. In other unfolder states, similar switching strategy is followed. In the analysis, DSC device capacitances (C_s) and the leakage inductances (seen from primary) L_{lk_1}, L_{lk_2} of Tr_1 and Tr_2 respectively are considered. Considering the leakage inductances of the transformers are of same order, $L_{lk_1} \simeq L_{lk_2} = L_{lk}$. The DSC active switches are zero voltage switched (ZVS) over complete line cycle. ZVS is achieved using C_s and L_{lk}. Following the switching state $[oqp]$, the unfolder switches Q_{ao}, Q_{bq} and Q_{cp} are kept ON. Hence, the link currents $i_p = i_c = I_{pk}\cos\theta$ and $i_q = -i_b = I_{pk}\sin\left(\theta + \frac{\pi}{6}\right)$ (see Fig. 5.2 and Table 5.2). The

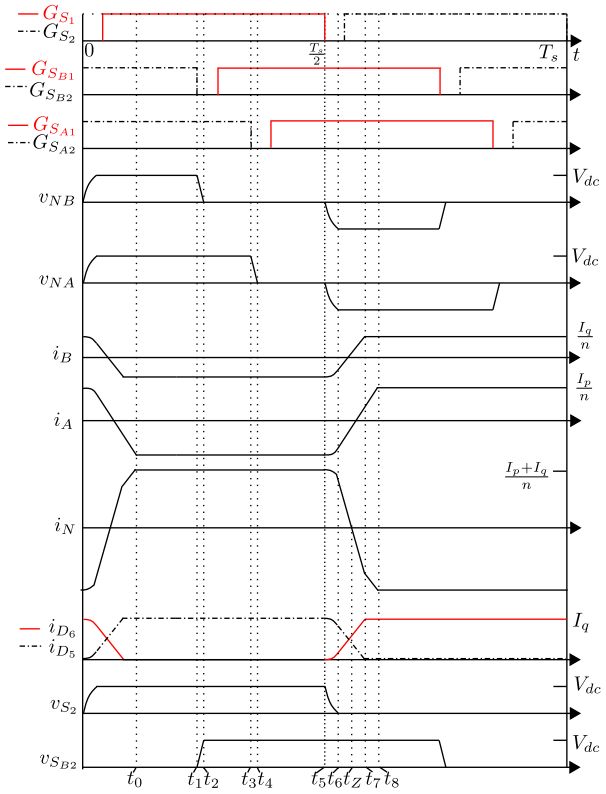
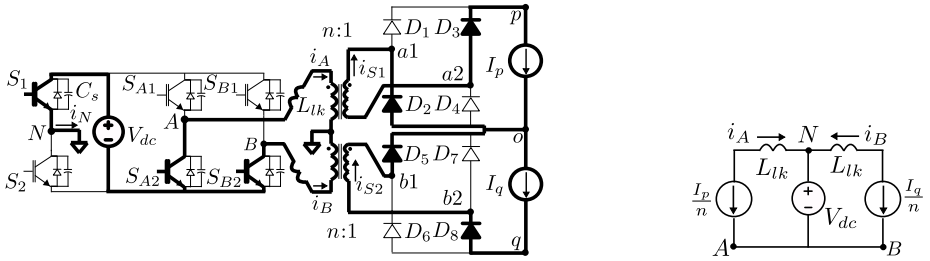


Figure 5.4: Important switching waveforms over T_s

unfolder and the three phase load can be replaced by two current sinks I_p and I_q connected across the DC links po and oq (see Fig. 5.5a). I_p and I_q are the rectifier output currents, i_p, i_q, respectively, over T_s. If $i_{a,b,c}$ are properly filtered and has negligible ripple, I_p and I_q can be considered as constant current sinks. In the following analysis $I_p > I_q$ is considered ($\theta \in [0, \frac{\pi}{6}]$). Thus $m_{po} > m_{oq}$ as seen in Fig. 5.2. The analysis will be similar in the other half i.e. $\theta \in [\frac{\pi}{6}, \frac{\pi}{3}]$, when $I_p < I_q$. What follows is a detailed description of the switching process of the DSC and current commutation of ASC diode bridges in one half of the switching cycle. In the other half cycle, circuit evolves in similar fashion. Fig. 5.4 presents key waveforms during switching transitions.

5.3.1 Mode I ($t_0 < t < t_1$ Fig. 5.5)

S_1, S_{A2} and S_{B2} are conducting in the DSC. V_{dc} is applied across HFT primary terminals NA and NB. In the secondary, D_2, D_3 and D_5, D_8 are conducting I_p and I_q respectively. Reflected transformer primary currents $i_{A,B}$ are shown in Fig. 5.4. $i_A = -\frac{I_p}{n}$, $i_B = -\frac{I_q}{n}$ and $i_N = \frac{I_p + I_q}{n}$. Equivalent circuit is shown in Fig. 5.5b. The voltage polarity and current directions

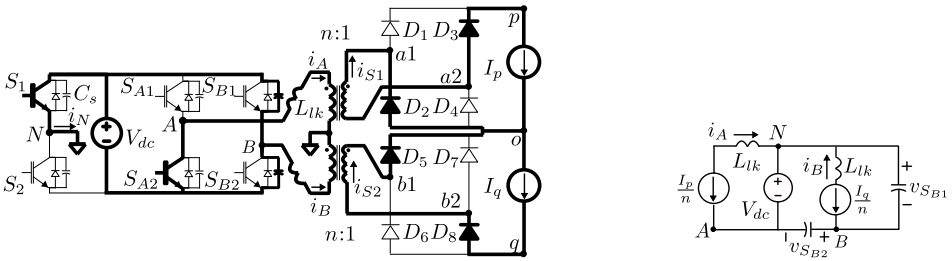


(a) (b)

Figure 5.5: Mode I-(a) circuit diagram, (b) equivalent circuit

indicate the active power transfer from DC source to load through both the transformers and diode bridges.

5.3.2 Mode II ($t_1 < t < t_2$ Fig. 5.6)



(a) (b)

Figure 5.6: Mode II-(a) circuit diagram, (b) equivalent circuit

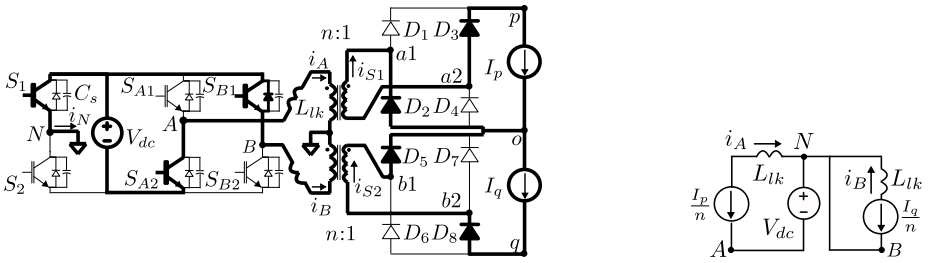
At t_1, S_{B2} is turned OFF. Due to C_s voltage across S_{B2} changes slowly which reduces turn OFF loss. i_B starts charging the capacitance across S_{B2} and discharging the capacitance across S_{B1}. The equivalent circuit is shown in Fig. 5.6b. The voltage dynamics across $S_{B1} - S_{B2}$ can be described by (5.1).

$$\begin{aligned} v_{S_{B1}} &= V_{dc} - \frac{I_q}{2nC_s}(t - t_1) \\ v_{S_{B2}} &= \frac{I_q}{2nC_s}(t - t_1) \end{aligned} \tag{5.1}$$

At t_2, $v_{S_{B1}} = 0$. The anti-parallel diode across S_{B1} is forward biased.

5.3.3 Mode III ($t_2 < t < t_3$ Fig. 5.7)

The anti-parallel diode of S_{B1} is conducting. The primary terminals N, B of Tr_2 is shorted. In this mode, no active power is transferred from source to load through Tr_2 and the diode bridge $D_5 - D_8$. The voltage across NA is V_{dc}. Active power is transferred from source to load



(a) (b)

Figure 5.7: Mode III-(a) circuit diagram, (b) equivalent circuit

trough Tr_1 and diode bridge $D_1 - D_4$. Equivalent circuit is shown in Fig. 5.7b. Gating pulse of S_{B1} is applied in this mode to achieve ZVS turn ON of S_{B1} when the anti-parallel diode is conducting. To achieve ZVS turn ON of S_{B1} the dead time (DT_B) between the gating signals of $S_{B1} - S_{B2}$ is given in (5.2).

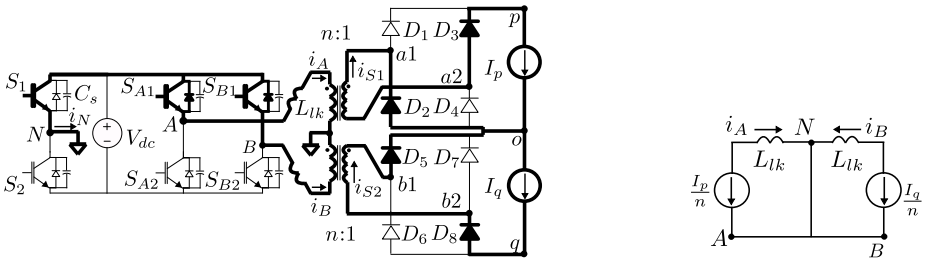
$$DT_B \geq \frac{2nC_sV_{dc}}{I_q} \tag{5.2}$$

$\frac{2nC_sV_{dc}}{I_q}$ is maximum when I_q is minimum i.e. $I_{q,min} = 0.5I_{pk}$ at $\theta = 0$. So, to achieve ZVS turn ON through out the line cycle $DT_B \geq \frac{2nC_sV_{dc}}{I_{q,min}} = \frac{4nC_sV_{dc}}{I_{pk}}$.

5.3.4 Mode IV ($t_3 < t < t_4$)

At t_3, S_{A2} is turned OFF. Due to device capacitance the voltage across S_{A2} changes slowly thus reduces turn OFF loss. In this mode the circuit dynamics is similar as discussed in Mode II. At the end of this mode the anti-parallel diode of S_{A1} is forward biased.

5.3.5 Mode V ($t_4 < t < t_5$ Fig. 5.8)

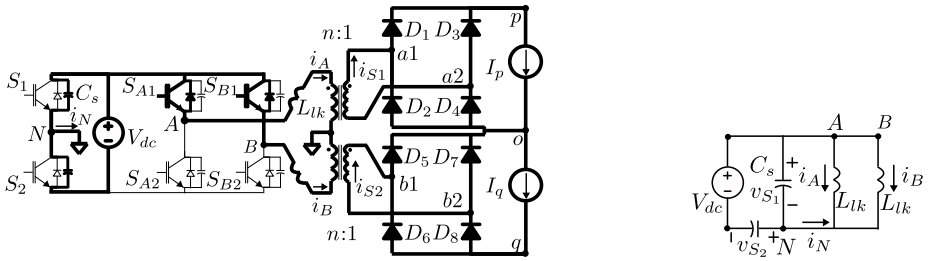


(a) (b)

Figure 5.8: Mode V-(a) circuit diagram, (b) equivalent circuit

After t_4, the anti-parallel diode of S_{A1} is conducting. Now both transformer primaries are shorted by S_1 and anti-parallel diodes of $S_{A1,B1}$. The converter is in zero state and no active power is transferred from DC source to load. The equivalent circuit is shown in Fig. 5.8b. Gating signal of S_{A1} is applied in this state to ensure ZVS turn ON. Like $S_{B1} - S_{B2}$, dead time between the gating signals of $S_{A1} - S_{A2}$ should be $DT_A \geq \frac{4nC_sV_{dc}}{I_{pk}}$.

5.3.6 Mode VI ($t_5 < t < t_6$ Fig. 5.9)



(a) (b)

Figure 5.9: Mode VI-(a) circuit diagram, (b) equivalent circuit

At t_5, S_1 is turned OFF. The device capacitance helps to reduce turn OFF loss by slowing down the rise of voltage across S_1. The pole current i_N starts charging the capacitance across S_1 and discharging the capacitance across S_2. Appeared voltage polarity across NA and NB forward bias D_1, D_4 and D_6, D_7. Secondary windings of Tr_1 and Tr_2 are shorted through diode bridges. The equivalent circuit is shown in Fig. 5.9b. The transition can be described by (5.3).

$$\begin{aligned} &i_A + i_B + i_N = 0 \\ &v_{S_1} + v_{S_2} = V_{dc} \\ &C_s(dv_{S_1}/dt - dv_{S_2}/dt) = i_N \\ &v_{S_1} = L_{lk}\frac{di_A}{dt} = L_{lk}\frac{di_B}{dt} \end{aligned} \tag{5.3}$$

Equation (5.3) is solved with initial conditions $v_{S_1}(t_5) = 0$, $i_N(t_5) = \dfrac{(I_p + I_q)}{n}$, $i_A(t_5) = -\dfrac{(I_p)}{n}$ and $i_B(t_5) = -\dfrac{(I_q)}{n}$. The voltage across S_1, v_{S_1} and currents are given in (5.4).

$$\begin{aligned} v_{S_1}(t) &= \frac{\omega_r L_{lk}}{2n}(I_p + I_q)\sin\omega_r(t - t_5) \\ i_N(t) &= \frac{(I_p + I_q)}{n}\cos\omega_r(t - t_5) \\ i_A(t) &= -\frac{I_p}{n} + \frac{I_p + I_q}{2n}(1 - \cos\omega_r(t - t_5)) \\ i_B(t) &= -\frac{I_q}{n} + \frac{I_p + I_q}{2n}(1 - \cos\omega_r(t - t_5)) \end{aligned} \tag{5.4}$$

Where $\omega_r = \dfrac{1}{\sqrt{L_{lk}C_s}}$. This mode ends at t_6 when $v_{S_1} = V_{dc}$ and $v_{S_2} = 0$. From (5.4), to completely charge C_s across S_1 to V_{dc}, following condition needs to be satisfied- $(I_p + I_q) \geq \dfrac{2nV_{dc}}{\omega_r L_{lk}}$. Otherwise, the circuit enters into a resonating oscillation mode and results in hard turn ON of S_2. The minimum value of $(I_p + I_q)$ over a line cycle is $I_{(p+q),min} = 1.5I_{pk}$ (at $\theta = 0$ and $\frac{\pi}{3}$). So, the condition on I_{pk} is given in (5.5).

$$I_{pk} \geq \frac{4nV_{dc}}{3\omega_r L_{lk}} \tag{5.5}$$

5.3.7 Mode VII ($t_6 < t < t_7$ Fig. 5.10)

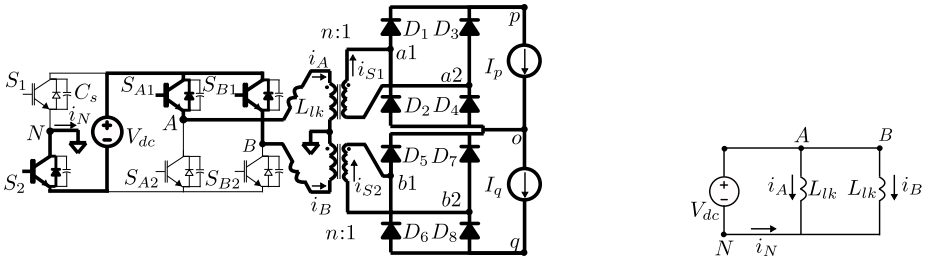


Figure 5.10: Mode VII-(a) circuit diagram, (b) equivalent circuit

After t_6, the anti-parallel diode across S_2 starts conducting i_N. To achieve ZVS ON, gating pulse of S_2 is applied when the anti-parallel diode is conducting. The dead time DT_N between the gating pulses of $S_1 - S_2$ should satisfy (5.6).

$$DT_N \geq (t_6 - t_5)_{max} = \frac{1}{\omega_r} \sin^{-1}\left(\frac{4nV_{dc}}{3\omega_r L_{lk} I_{pk}}\right) \tag{5.6}$$

The equivalent circuit in this mode is shown in Fig. 5.10b. The primary currents, i_A and i_B are changed linearly. $i_{A,B,N}$ are given in (5.7).

$$\begin{aligned} i_A &= i_A(t_6) - \frac{V_{dc}}{L_{lk}}(t - t_6) \\ i_B &= i_B(t_6) - \frac{V_{dc}}{L_{lk}}(t - t_6) \\ i_N &= i_N(t_6) - \frac{2V_{dc}}{L_{lk}}(t - t_6) \end{aligned} \tag{5.7}$$

In the secondary, current changes linearly between diode pairs $(D_{1,4})$, $(D_{2,3})$ and $(D_{5,8})$, $(D_{6,7})$. Current through D_5 and D_6 are shown in Fig. 5.4. As S_2, $S_{A1,B1}$ are ON, i_A, i_B and i_N can change their direction and build up in the opposite directions. At t_7, when $i_B = \frac{I_q}{n}$, this mode ends.

5.3.8 Mode VIII ($t_7 < t < t_8$ Fig. 5.11)

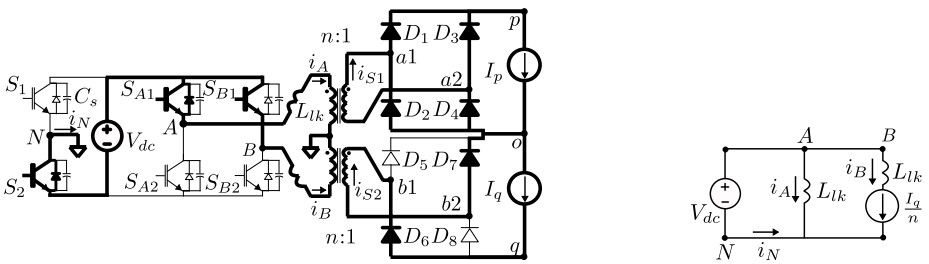


Figure 5.11: Mode VIII-(a) circuit diagram, (b) equivalent circuit

D_5 and D_8 are reverse biased and stop conducting whereas D_6 and D_7 are conducting I_q.

The equivalent circuit is shown in Fig. 5.11b. i_A and i_N changes linearly with slope $\frac{V_{dc}}{L_{lk}}$. At t_8, $i_A = \dfrac{I_p}{n}$, $i_N = -\dfrac{I_p + I_q}{n}$ and this mode ends.

5.3.9 Mode IX ($t_8 < t < t_9$ Fig. 5.12)

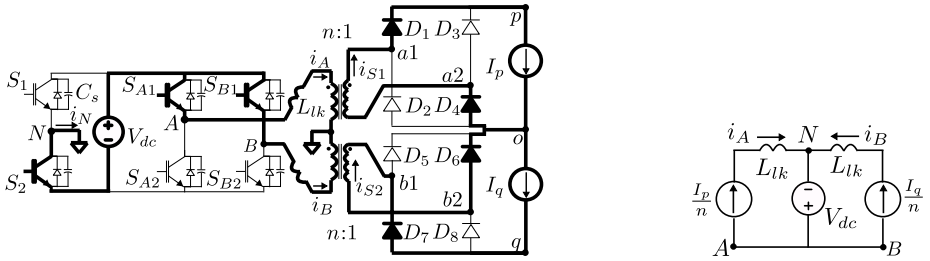


Figure 5.12: Mode IX-(a) circuit diagram, (b) equivalent circuit

After t_8, D_2, D_3 are reverse biased. D_1 and D_4 conduct I_p. In the primary, S_2, S_{A1} and S_{B1} are conducting. The converter is in next active state. Active power is transferred from DC source to load through both the transformers and the diode bridges. The equivalent circuit is shown in Fig. 5.12b. The circuit condition is similar as in Mode I.

The above discussion shows the switching process of the converter in one half of the switching cycle T_s , when the unfolder state is [*oqp*]. In next half of the switching cycle, similar switching sequences are followed with other symmetrical switches. In the other unfolder states, the NPC inverter can be replaced with two current sources I_p and I_q connected across the DC links. So, similar circuit dynamics as discussed above, will be observed through out the line cycle.

5.3.10 Estimation of limits on dead times to ensure ZVS

From above discussion, it is seen that during the switching transitions of leg $S_{A1} - S_{A2}$ and leg $S_{B1} - S_{B2}$, respective pole currents i_A and i_B do not change their directions. But the pole current i_N changes its direction during the switching transition of leg $S_1 - S_2$. Hence, to achieve ZVS turn ON, a strict upper limit is imposed on the dead time of leg $S_1 - S_2$. To avoid hard-turn ON of the DSC switches, the lower limits of the dead times, $DT_{A,B,N}$, are already given above.

To ensure ZVS turn ON of $S_1 - S_2$ the gating signal should be applied before the pole current, i_N becomes zero at t_Z and thereafter changes its direction and hence the anti-parallel diode stops conducting (see Fig. 5.4). So, there must be an upper limit of DT_N such that $DT_N < (t_Z - t_5) = \Delta t_Z$. To achieve ZVS ON throughout the line cycle, $DT_N \leq \Delta t_{Z,min}$. The envelope of i_N, i_{Ne} is shown in Fig. 5.13. Due to wave symmetry, the estimation of $\Delta t_{Z,min}$ is only carried out for $0 \leq \theta \leq \dfrac{\pi}{6}$ where $I_p = I_{pk}\cos\theta$ and $I_q = I_{pk}\sin\left(\theta + \dfrac{\pi}{6}\right)$. The duration of Mode VI, $(t_6 - t_5)$ and the change in magnitude of $i_{N,A,B}$ in this mode are considered negligible (as C_s is relatively small). Thus $i_N(t_5) \simeq i_N(t_6) = \dfrac{I_p + I_q}{n}$ and $i_B(t_5) \simeq i_B(t_6) = -\dfrac{I_q}{n}$. Between t_6, t_7 the slope of i_N is $\dfrac{2V_{dc}}{L_{lk}}$ and between t_7, t_8 the slope changes to $\dfrac{V_{dc}}{L_{lk}}$. The

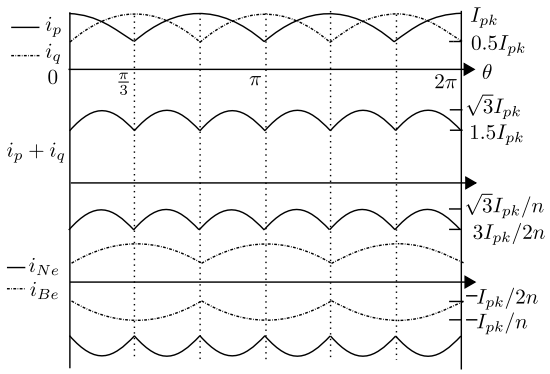


Figure 5.13: DSC pole current envelopes at UPF operation of the converter

slope of i_N between t_6, t_Z needs to be checked over our considered interval. From the above assumption, $(t_7 - t_5) = \dfrac{2I_q L_{lk}}{nV_{dc}}$ and $i_N(t_7) = i_N(t_5) - \dfrac{2V_{dc}}{L_{lk}}(t_7 - t_5) = -\dfrac{I_{pk}}{2n}(3\sqrt{3}\sin\theta + \cos\theta)$. $i_N(t_7)$ is negative in the considered range of θ i.e i_N changes its direction in Mode VII with slope $\dfrac{2V_{dc}}{L_{lk}}$. Therefore, $\Delta t_Z = \dfrac{L_{lk}}{2V_{dc}} i_N(t_5) = \dfrac{\sqrt{3}L_{lk}I_{pk}}{2nV_{dc}} \cos\left(\dfrac{\pi}{6} - \theta\right)$. At $\theta = 0$, Δt_Z is minimum and $\Delta t_{Z,min} = \dfrac{0.75 I_{pk} L_{lk}}{nV_{dc}}$. So, combining with (5.6), the dead time between the gating signals of $S_1 - S_2$ switch-pair is given in (5.8).

$$\frac{1}{\omega_r}\sin^{-1}\left(\frac{4nV_{dc}}{3\omega_r L_{lk} I_{pk}}\right) \leq DT_N \leq \frac{0.75 I_{pk} L_{lk}}{nV_{dc}} \tag{5.8}$$

In this section, the soft-switching conditions of the DSC are derived for UPF operation of the converter. At UPF, soft-switching can be achieved for all the switches of the DSC over the complete line cycle. Similar conditions can be derived for other power factor operation. It can be shown that at $\pm 30°$ PF operation, soft turn ON of $S_1 - S_2$ can be achieved over the complete line cycle whereas $S_{A1} - S_{B2}$ are hard-switched in some small durations of the line cycle.

5.4 Converter Design

We have designed the converter for a target application of grid integration of utility scale solar photo-voltaic. The specification of the design is given in Table 2.1. The topology is modulated at the 85% of its maximum possible modulation index. Hence the modulation index $M = \dfrac{1.5nV_{pk}}{V_{dc}} = 0.85$. Thus the high frequency transformer (HFT) primary to secondary turns ratio is $n = 1.33$.

5.4.1 Device blocking voltage and RMS currents

For UPF operation, (2.24) is valid. Replacing V_{pk} with $V_{pk} = \frac{MV_{dc}}{1.5n}$, following equation can be written

$$\begin{aligned} \frac{I_{pk}}{n} &= \frac{1}{M}\frac{P}{V_{dc}} \\ I_{pk} &= \frac{2P}{3V_{pk}} \end{aligned} \tag{5.9}$$

Using (5.9), the RMS current in switch $S_1 - S_2$ is given below.

$$I_{RMS,S_1-S_2} = \frac{I_{pk}}{n}\sqrt{\frac{3}{8\pi}(3\sqrt{3}+2\pi)} = \frac{1.17}{M}\frac{P}{V_{dc}} \tag{5.10}$$

The peak current through $S_1 - S_2$ is $I_{pk,S_1-S_2} = \frac{\sqrt{3}I_{pk}}{n} = \frac{\sqrt{3}}{M}\frac{P}{V_{dc}}$. With $M = 0.85$, $I_{RMS,S_1-S_2} = 1.38\frac{P}{V_{dc}}$ and $I_{pk,S_1-S_2} = 2.03\frac{P}{V_{dc}}$. The RMS current in $S_{A1} - S_{B2}$ is expressed as follows.

$$I_{RMS,S_{A1}-S_{B2}} = \frac{I_{pk}}{n}\sqrt{\frac{5M\sqrt{3}}{12\pi}} = \frac{0.48}{\sqrt{M}}\frac{P}{V_{dc}} \tag{5.11}$$

The peak current of $S_{A1} - S_{B2}$ is $I_{pk,S_{A1}-S_{B2}} = \frac{I_{pk}}{n} = \frac{P}{MV_{dc}}$. With $M = 0.85$, $I_{RMS,S_{A1}-S_{B2}} = 0.52\frac{P}{V_{dc}}$ and $I_{pk,S_{A1}-S_{B2}} = 1.176\frac{P}{V_{dc}}$.
The Blocking voltage of DSC switches are V_{dc}.
Using (5.9), the RMS current of ASC diodes $D_1 - D_8$ is given as follows.

$$I_{RMS,D_1-D_8} = I_{pk}\sqrt{\frac{3}{2\pi}\left(\frac{\sqrt{3}}{8}+\frac{\pi}{6}\right)} = 0.396\frac{P}{V_{pk}} \tag{5.12}$$

The RMS current of ASC two quadrant devices $Q_{ap} - Q_{cq}$ is expressed as-

$$I_{RMS,Q_{ap}-Q_{cq}} = \sqrt{\frac{1}{2\pi}\left(\frac{\sqrt{3}}{4}+\frac{\pi}{3}\right)}I_{pk} = 0.323\frac{P}{V_{pk}} \tag{5.13}$$

The RMS current of ASC four quadrant devices $Q_{ao} - Q_{co}$ is expressed as-

$$I_{Q_{ao}-Q_{co}} = \sqrt{\left(\frac{1}{12}-\frac{\sqrt{3}}{8\pi}\right)}I_{pk} = 0.08\frac{P}{V_{pk}} \tag{5.14}$$

Peak current of ASC diodes and two quadrant devices are given as $I_{pk,D_1-D_8} = I_{pk,Q_{ap}-Q_{cq}} = I_{pk} = 0.67\frac{P}{V_{pk}}$. The Peak current of ASC four quadrant devices is $I_{pk,Q_{ao}-Q_{co}} = 0.5I_{pk} = 0.33\frac{P}{V_{pk}}$.
The blocking voltage of ASC diodes and four quadrant devices is $\frac{V_{dc}}{n} = \frac{1.5}{M}V_{pk}$. For $M = 0.85$,

blocking voltage is $1.765V_{pk}$. The blocking voltage of ASC two quadrant switches is $\frac{2V_{dc}}{n} = 3.53V_{pk}$.

The detailed derivation steps of the RMS currents are given in Appendix A.

5.4.2 Estimation of Converter Power Loss

Closed form expressions of power losses in active switches and diodes of the converter are given in this section. The detailed derivation steps of the conduction loss are given in Appendix A. The conduction loss in a switch is given in (2.30). The expressions of I_{avg} and I_{RMS} are derived first to obtain the conduction loss expression.

Loss estimation of DSC switches and diodes

Over a switching cycle all of the DSC active switches S_1-S_{B2} and the anti-parallel diodes of $S_{A1} - S_{A2}$ and $S_{B1} - S_{B2}$ take part in conduction. The anti-parallel diodes of S_1 and S_2 conducts for very small durations during switching transitions. Hence the conduction losses in these diodes are neglected. Using (2.30) the conduction loss of these switches and their anti-parallel diodes are estimated.

The conduction loss in switch pair $S_1 - S_2$ is given as-

$$P_{C_{S_1}} = P_{C_{S_2}} = \frac{0.827V_{CE}I_{pk}}{n} + 1.37\frac{R_{CE}I_{pk}^2}{n^2} \tag{5.15}$$

The conduction loss of a switch of $S_{A1} - S_{B2}$ are given as-

$$P_{C_{S_{A1}}} = \frac{MV_{CE}I_{pk}}{4n} + \frac{5\sqrt{3}M}{12\pi n^2}R_{CE}I_{pk}^2 \tag{5.16}$$

The conduction loss expression of an anti-parallel diode of the switch pairs $S_{A1} - S_{A2}$ and $S_{B1} - S_{B2}$ is given as-

$$P_{C_{D,SA1}} = (0.41 - 0.254M)\frac{V_D I_{pk}}{n} + (0.353 - 0.23M)\frac{R_D I_{pk}^2}{n^2} \tag{5.17}$$

As the DSC is soft-switched, switching loss is negligible.

Loss estimation of ASC switches and diodes

The conduction loss in a ASC diode of $D_1 - D_8$ is given as

$$P_{C_{D_1}} = 0.41V_D I_{pk} + 0.36R_D I_{pk}^2 \tag{5.18}$$

The conduction loss in a ASC two quadrant switch of $Q_{ap} - Q_{cq}$ is given as

$$P_{C_{Q_{ap}}} = 0.276V_{CE}I_{pk} + 0.235R_{CE}I_{pk}^2 \tag{5.19}$$

The conduction loss in a ASC four quadrant switch of $Q_{ao} - Q_{co}$ is given as

$$P_{C_{Q_{ao}}} = 0.04 V_{CE} I_{pk} + 0.014 R_{CE} I_{pk}^2 \tag{5.20}$$

The conduction loss in an anti-parallel diode of the four quadrant switches $Q_{ao} - Q_{co}$ is given as

$$P_{C_{D_{Q_{ao}}}} = 0.04 V_D I_{pk} + 0.014 R_D I_{pk}^2 \tag{5.21}$$

5.4.3 Design of high frequency transformers

The RMS current of HFT primary winding is $I_{RMS,p} = \dfrac{0.84 I_{pk}}{n} = 0.84 \dfrac{P}{M V_{dc}}$. For $M = 0.85$, $I_{RMS,p} = 0.99 \dfrac{P}{V_{dc}}$. The RMS current of HFT secondary winding is $I_{RMS,s} = 0.84 I_{pk} = 0.56 \frac{P}{V_{pk}}$.

Next we will find the area product of the HFTs. The area product which is the product of the core and window area of the HFT, indicates the transformer size.

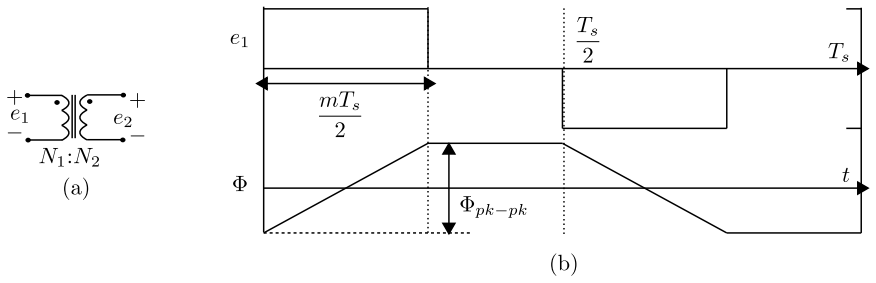


Figure 5.14: (a) Two winding HFT (b) HFT voltage and flux waveforms over a switching cycle

Area product of HFTs used in topology 4

In topology 4, two winding HFTs are used as shown in Fig. 5.14a. The applied HFT primary voltage (e_1) is duty cycle modulated square wave with magnitude V_{dc}. The duty cycle is maximum at the peak of the modulation signals m_{po}, m_{oq} ($M = 0.85$) (see Fig. 5.2). The maximum of the peak-peak flux (see Fig. 5.14) is estimated as follows.

$$\Phi_{pk-pk,max} = \frac{1}{N_1} \int_0^{\frac{MT_s}{2}} e_1 dt = \frac{M V_{dc} T_s}{2 N_1} \tag{5.22}$$

Where N_1 and N_2 are HFT primary and secondary turns. The peak flux density (B_{max}) is related to $\Phi_{pk-pk,max}$ through HFT core area A_c.

$$A_c B_{max} = \frac{\Phi_{pk-pk,max}}{2} = \frac{M V_{dc}}{4 N_1 f_s} \tag{5.23}$$

The switching frequency $f_s = \frac{1}{T_s}$. HFT window area (A_w) is estimated as follows.

$$A_w K_w = \frac{N_1 I_{RMS,p}}{J} + \frac{N_2 I_{RMS,s}}{J} = \frac{2N_1 I_{RMS,p}}{J} \tag{5.24}$$

where K_w is the window fill factor and J is the current density. The primary and secondary winding RMS currents are $I_{RMS,p} = \frac{0.84 N_2 I_{pk}}{N_1}$, $I_{RMS,s} = 0.84 I_{pk}$ respectively. The product of window and core area is estimated as follows.

$$A_c A_w = \frac{M V_{dc}}{4 N_1 f_s B_{max}} \frac{2 N_1 I_{RMS,p}}{J K_w} = 0.42 \frac{P}{K_w J B_{max} f_s} \tag{5.25}$$

Where output power is $P = \frac{3 V_{pk} I_{pk}}{2} = \frac{M N_2 V_{dc} I_{pk}}{N_1}$.

Copper loss estimation of the HFTs

The conduction loss of HFT is given as $I^2_{RMS,p}(R_p + n^2 R_s)$. Where $I_{RMS,p} = \frac{0.84 I_{pk}}{n}$ is the RMS current of the primary winding. R_p and R_s are primary and secondary winding resistance. At the switching frequency below 40kHz, the HFT core (EPCOS ferrite) loss is negligible.

5.4.4 Input and Output Filter Requirement of the Converter

At the DC input of the converter, a capacitive filter is required to support the high frequency switching ripple current. Similarly, at the output port, inductors are employed to filter out the high frequency components of the pole voltages. As seen in chapter 3, the filter requirement can be expressed in terms of THD. In this section we have given the closed form expressions of input current and output pole voltage THDs of the topology 4.

Input filter capacitance requirement

DC link current over a switching cycle is shown in Fig. 5.15. In Fig. 5.15, i_{dc_A} is the current drawn from the DC link for the switching operation of $S_{1,2}$ and S_{A_1,A_2}. Similarly i_{dc_B} is defined. Net DC link current is given by $i_{dc} = i_{dc_A} + i_{dc_B}$. In $\theta \in (0, \frac{\pi}{3})$ the modulation signals are given as $m_{po} = 1.155M \cos\left(\theta + \frac{\pi}{6}\right)$ and $m_{oq} = 1.155M \sin\theta$ (see Fig. 5.2). In $\theta \in (0, \frac{\pi}{3})$ the magnitude of i_{dc_A} and i_{dc_B} are given as $\frac{I_p}{n} = \frac{I_{pk}}{n}\cos\theta$ and $\frac{I_q}{n} = \frac{I_{pk}}{n}\sin\left(\theta + \frac{\pi}{6}\right)$ respectively. I_{pk} is the peak value of the output line current. The DC ink current i_{dc} has symmetry over $\frac{\pi}{6}$. The RMS of DC link current can be derived as follows.

$$\begin{aligned} i^2_{dc,rms} =& \frac{6}{\pi} \int_0^{\frac{\pi}{6}} \left[\left(\frac{I_p + I_q}{n} \right)^2 m_{oq} + \left(\frac{I_p}{n} \right)^2 (m_{po} - m_{oq}) \right] d\theta \\ =& 1.3356 M \left(\frac{I_{pk}}{n} \right)^2 \end{aligned} \tag{5.26}$$

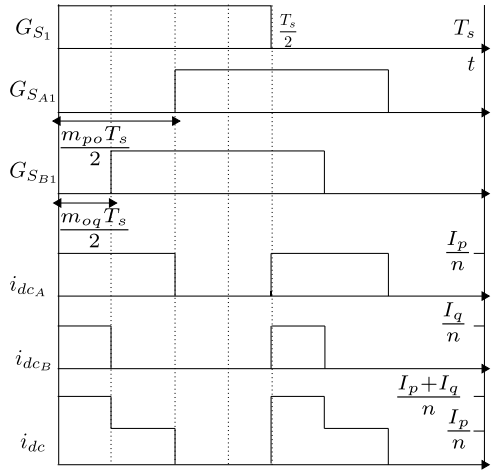


Figure 5.15: Input DC link current of the topology 4

The average DC link current $i_{dc,avg}$ can be derived from input and output power balance and is given as $i_{dc,avg} = \frac{MI_{pk}}{n}$. The ripple current RMS, $\tilde{i}$ is given as

$$\begin{aligned}\tilde{i} &= \sqrt{i_{dc,rms}^2 - i_{dc,avg}^2} \\ &= \frac{I_{pk}}{n}\sqrt{(1.3356M - M^2)}\end{aligned} \tag{5.27}$$

THD_I is given as

$$THD_I = \frac{\tilde{i}}{i_{dc,avg}} = \frac{\sqrt{(1.3356M - M^2)}}{M} \tag{5.28}$$

For $M = 0.85$, THD_I is 0.756.

Output filter inductance requirement

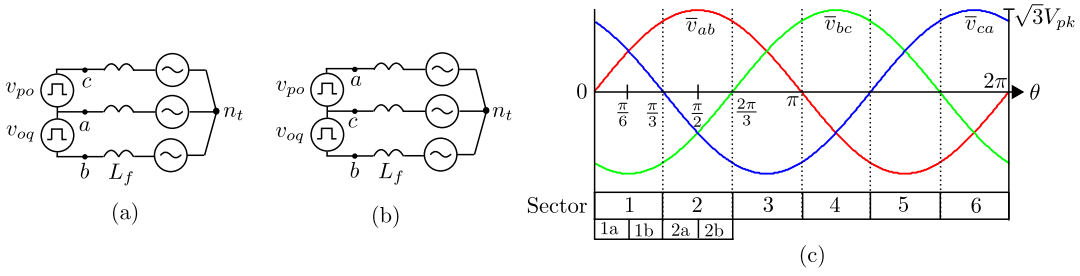


Figure 5.16: Equivalent circuit (seen from load) of the topology 4 in (a) sector-1 , (b) sector-2. (c) Sectors of operation

Fig. 5.16a and 5.16b show the equivalent circuit configuration of the converter (seen from the load) in sector 1 and sector 2 (unfolder states [*oqp*] and [*pqo*] respectively). Sectors are shown in Fig. 5.16c. For balanced 3ϕ load, $v_{an_t} + v_{bn_t} + v_{cn_t} = 0$. By applying KVL, in sector

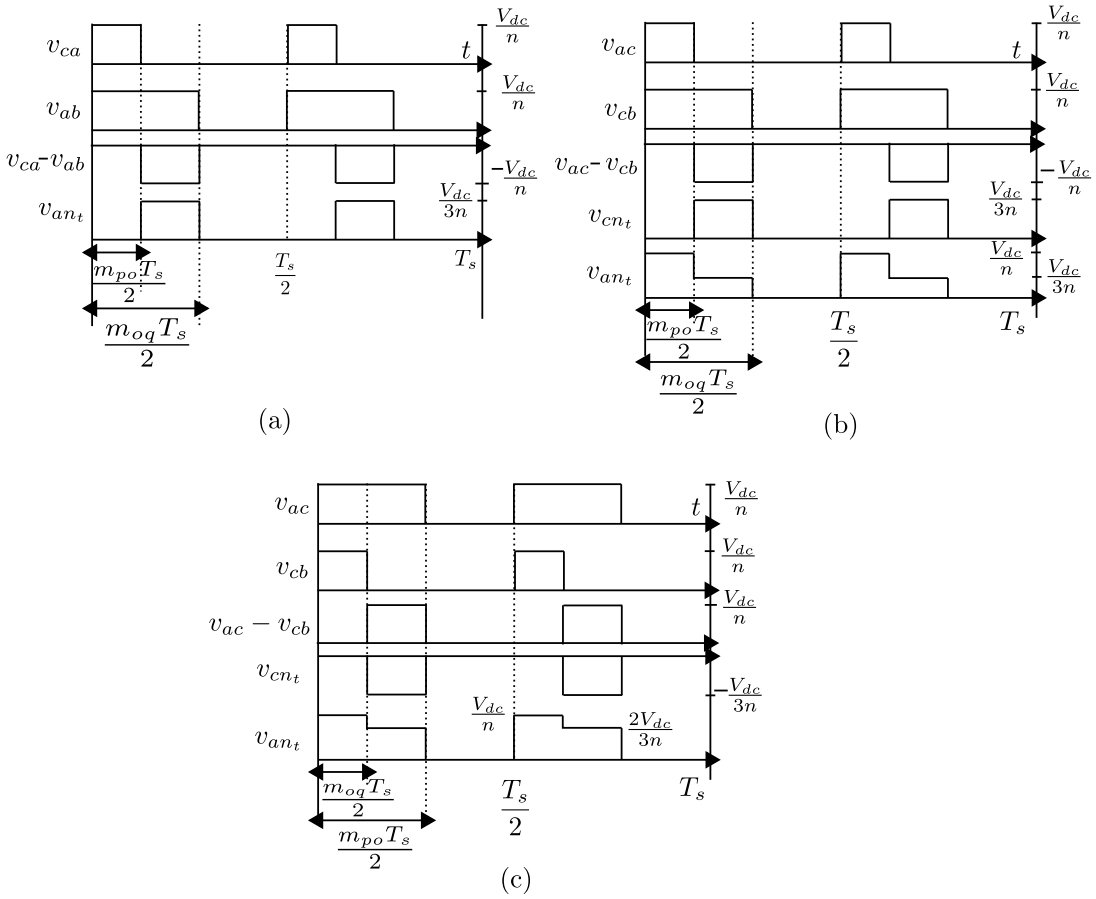


Figure 5.17: Pole voltage (v_{an_t}) waveform of the topology 4 in (a) sector-1b , (b) sector-2a. (c) Sectors-2b

1, following circuit equation can be written-

$$\begin{aligned} v_{ca} &= v_{cn_t} - v_{an_t} \\ v_{ab} &= v_{an_t} - v_{bn_t} \\ v_{ca} - v_{ab} &= -3v_{an_t} \end{aligned} \tag{5.29}$$

Thus $v_{an_t} = -\frac{1}{3}(v_{ca} - v_{ab})$. Based on the proposed modulation strategy, applied pole voltages in sector-1b ($\theta \in [\frac{\pi}{6}, \frac{\pi}{3}]$) are shown in Fig. 5.17a. The modulation signals in this sector are $m_{oq} = 1.155M\sin\theta$ and $m_{po} = 1.155M\cos(\theta + \frac{\pi}{6})$ are shown in Fig. 5.2. In sector 1b (S-1b) the RMS of pole voltage v_{an_t} is expressed as (see Fig. 5.17)-

$$\begin{aligned} V^2_{an_{t_{S-1b}}} =& \left(\frac{V_{dc}}{3n}\right)^2 (m_{oq} - m_{po}) \\ =& 2M\left(\frac{V_{dc}}{3n}\right)^2 \sin\left(\theta - \frac{\pi}{6}\right) \end{aligned} \tag{5.30}$$

Similarly in sector 2, by applying KVL, we get $v_{cn_t} = -\frac{1}{3}(v_{ca} - v_{ab})$ and $v_{an_t} = \frac{2}{3}v_{ac} + \frac{1}{3}v_{cb}$ (see Fig. 5.16b). In sector 2a (S-2a) i.e. $\theta \in (\frac{\pi}{3}, \frac{\pi}{2})$, the pole voltage ($v_{an_t}$) RMS is given by (see Fig. 5.17b)-

$$V^2_{an_{t_{S-2a}}} = \left(\frac{V_{dc}}{n}\right)^2 m_{po} + \left(\frac{V_{dc}}{3n}\right)^2 (m_{oq} - m_{po}) \tag{5.31}$$

where $m_{oq} = 1.155M\cos(\theta - \frac{\pi}{6})$ and $m_{po} = 1.155M\sin(\theta - \frac{\pi}{3})$. Similarly in sector 2b (S-2b), i.e. $\theta \in (\frac{\pi}{2}, \frac{2\pi}{3})$ the pole voltage (v_{an_t}) RMS is as follows (see Fig. 5.17c).

$$V^2_{an_{t_{S-2b}}} = \left(\frac{V_{dc}}{n}\right)^2 m_{oq} + \left(\frac{2V_{dc}}{3n}\right)^2 (m_{po} - m_{oq}) \tag{5.32}$$

The waveform of v_{an_t} has quarter wave symmetry. The line cycle RMS of v_{an_t} can be expressed as-

$$\begin{aligned} v^2_{an_t,rms} =& \frac{2}{\pi}\left(\int_{\frac{\pi}{6}}^{\frac{\pi}{3}} V^2_{an_{t_{S-1b}}} + \int_{\frac{\pi}{3}}^{\frac{\pi}{2}} V^2_{an_{t_{S-2a}}} + \int_{\frac{\pi}{2}}^{\frac{2\pi}{3}} V^2_{an_{t_{S-2b}}}\right) d\theta \\ =& 0.31M\left(\frac{V_{dc}}{n}\right)^2 \end{aligned} \tag{5.33}$$

The RMS of fundamental component of v_{an_t} is $v_{an_t,rms1} = \dfrac{V_{pk}}{\sqrt{2}} = \dfrac{\sqrt{2}MV_{dc}}{3n}$. The ripple voltage RMS of v_{an_t} can be expressed as-

$$\tilde{v} = \frac{V_{dc}}{n}\sqrt{[0.31M - 0.22M^2]} \tag{5.34}$$

The voltage THD is given as-

$$THD_V = \frac{\tilde{v}}{v_{an_t,rms1}} = 2.12\frac{\sqrt{[0.31M - 0.22M^2]}}{M} \tag{5.35}$$

For $M = 0.85$, THD_V is 0.8.

5.5 Experimental Results

5.5.1 Setup and operating condition

The operation of the converter discussed so far is experimentally verified in a 2kW hardware prototype. The experimental hardware is shown in Fig. 5.18. Table 5.3 presents the operating condition. The active switches in DSC are implemented with 1200V, 75 A SEMIKRON IGBT modules and are switched at 20kHz. IXYS 1200V, 75A diode modules MEE 75-12 DA are used in the secondary rectifiers. The NPC inverter is implemented with INFINEON IKW40N120H3 discrete IGBTs (1200V, 40A). Optically isolated gate drivers ACPL-339J are used to drive all the IGBTs with gate-emitter voltage levels $\pm 15V$. The dead-time provided between two

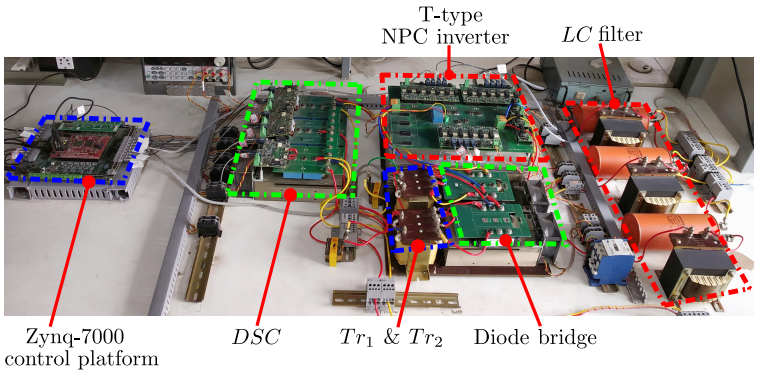


Figure 5.18: Hardware prototype

Table 5.3: Operating condition of topology 4

Output power (P)	2.15kW
DC input (V_{dc})	230V
HFT turns ratio (n)	3/4
L-L peak voltage ($\sqrt{3}V_{pk}$)	270V
Switching frequency ($f_s = \frac{1}{T_s}$)	20kHz
Line frequency ($f_o = \frac{\omega_o}{2\pi}$)	50Hz

active switches in a leg of DSC is 600 ns which satisfies all the dead-time limits derived in last section. An overlap time of 800ns is provided between two consecutive gating signals of the NPC inverter. The turns ratio of Tr_1 and Tr_2 are selected as 51 : 68. EPCOS ferrite E cores (E80/38/20) are used. The leakage inductances seen from primary of Tr_1 and Tr_2 are 6.5 μH and 5.3 μH respectively. Additional series inductance of 36 μH is connected in series with each primary winding to achieve soft-switching of the DSC and hence $L_{lk} \simeq 42\mu$H. 2.5 mH inductance is used as line filter (L_f) at the converter output. Xilinx Zynq-7010 based control platform is used to implement the modulation strategy.

5.5.2 Verification of modulation strategy

The converter is connected to a balanced 3ϕ voltage source $v_{g(a,b,c)}$ with line-line peak ($\sqrt{3}V_{pk}$) 270V. The input DC supply is 230 V. Fig. 5.19a presents the UPF operation of the converter with an output power (P) of 2.15 kW. The phase voltage v_{ga} and line current i_a are in same phase as seen in Fig. 5.19a. The peak of the line current $I_{pk} = \dfrac{2P}{3V_{pk}} = 9.1$ A. 3ϕ balanced line currents $i_{a,b,c}$ are shown in Fig. 5.19a.

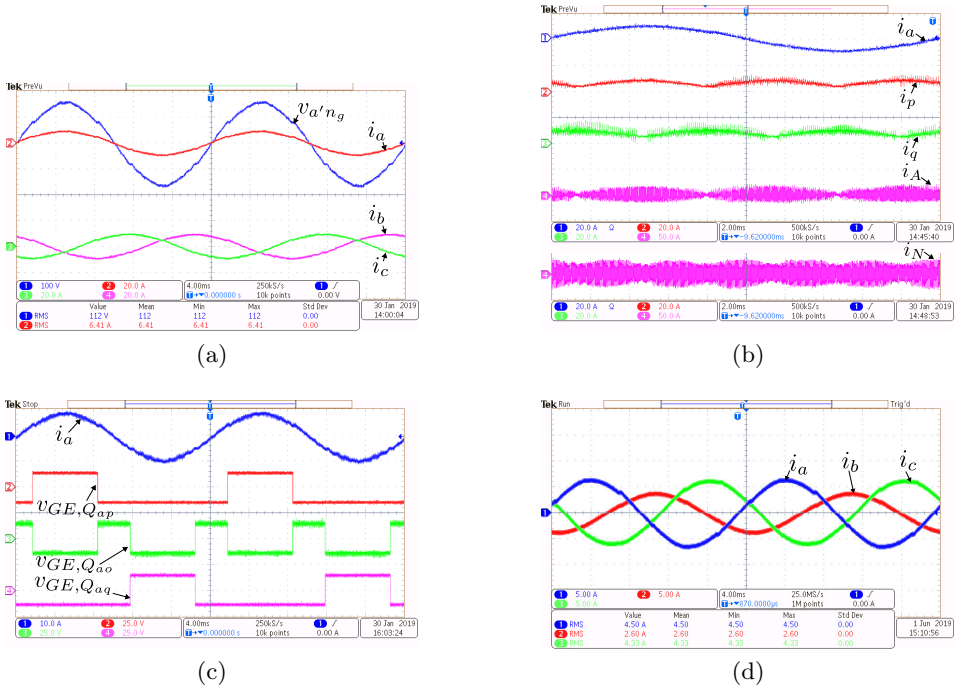


Figure 5.19: (a) UPF operation- [CH1] v_{ga} (100V/div.), [CH2]-[CH4]: line currents (20A/div.). (b) [CH1]-[CH4]: i_a, i_p, i_q (20A/div.), DSC pole currents $i_{A,N}$ (50A/div.) . (c) Line switching of NPC leg- [CH1] i_a (20A/div.), [CH2]-[CH4]: Gate-emitter voltages of Q_{ap}, Q_{ao}, Q_{aq} (25V/div.). (d) Unbalance operation- [CH1]-[CH3]: i_a, i_b and i_c (5A/div.).

The rectifier output currents i_p, i_q and DSC pole currents i_A and i_N are shown in Fig. 5.19b over a line cycle. i_p and i_q have the peak of 9.1 A (I_{pk}) and the experimental waveforms are matched as shown in Fig. 5.13. The envelope of i_A and i_N have peak values of $\dfrac{\sqrt{3}I_{pk}}{n} = 21$A and $\dfrac{3I_{pk}}{2n} = 18.2$A respectively. Experimentally obtained envelops of i_A and i_N are similar to what is analytically predicted in Fig. 5.13.

Fig. 5.19c presents the line current i_a and gate emitter voltages of Q_{ap}, Q_{ao} and Q_{aq} of the NPC inverter. Q_{ap} and Q_{aq} are switched at line frequency (50 Hz) whereas Q_{ao} are switched at twice of the line frequency. This result verifies the low frequency switching strategy of NPC inverter.

Experimental result of the converter supporting unbalanced load is shown in Fig. 5.19d. The three phase unbalanced line currents ($i_a - i_c$) have peak values of 6.36A, 3.68A and 6.12A respectively. The Phase angles between $i_{a,b}$, $i_{b,c}$ and $i_{c,a}$ are 116°, 102° and 142° respectively.

Fig. 5.20a shows the pulse width modulated high frequency AC (v_{NA}) applied across Tr_1

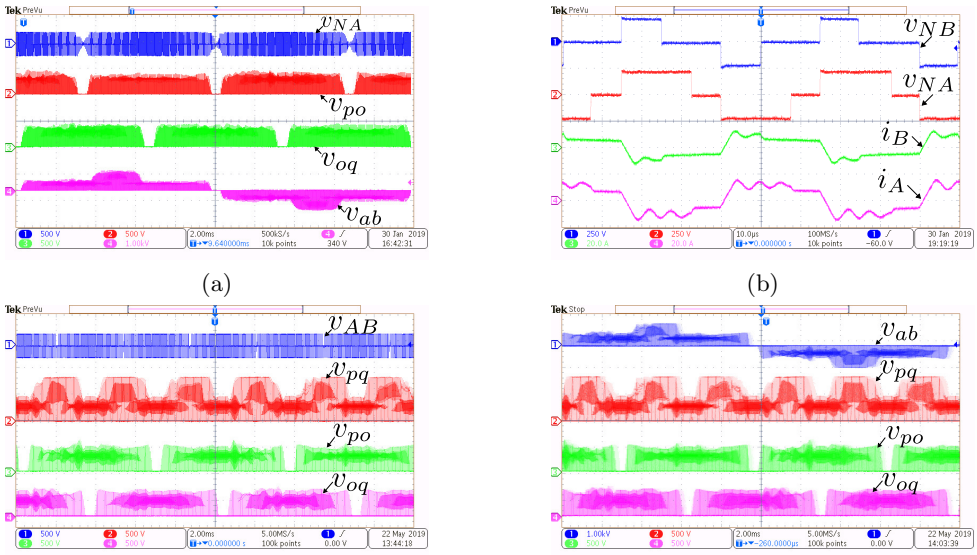


Figure 5.20: (a) [CH1] HFT primary voltage- v_{NA}, rectifier output voltages- [CH2] v_{po}, [CH3] v_{oq} (500V/div), [CH4] NPC inverter pole voltage- v_{ab} (1kV/div.). (b) Waveforms over switching cycle- [CH1]-[CH2]: v_{NB}, v_{NA} (250V/div.) and [CH3]-[CH4]: i_B, i_A (20A/div.). (c) [CH1] v_{AB}, [CH2]-[CH4]: v_{pq}, v_{po}, v_{oq} (500V/div). (d) [CH1] v_{ab} (1kV/div)., [CH2]-[CH4]: v_{pq}, v_{po}, v_{oq} (500V/div).

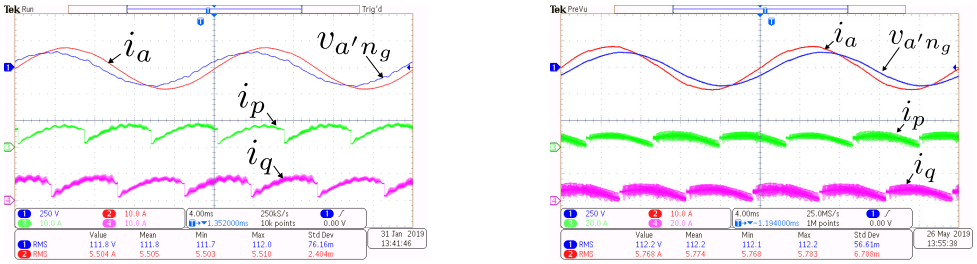
primary. The voltage levels of v_{NA} are ± 230 V and 0. The rectifier output voltages v_{po} and v_{oq} are shown in [CH2] and [CH3] respectively. The pulsating v_{po} and v_{oq} have voltage levels $\frac{V_{dc}}{n} = 307$ V and 0. Thus Fig. 5.20a verifies pulsating intermediate DC link without any capacitor. In [CH4], the NPC inverter pole voltage v_{ab} is shown. v_{ab} has steady state voltage levels- ± 307 V (V_{dc}/n), ± 614 V ($2V_{dc}/n$) and 0.

The primary voltages ($v_{NA,NB}$) and currents ($i_{A,B}$) of Tr_1 and Tr_2 are shown in Fig. 5.20b. This result verifies the transformer voltage and current waveforms presented in Fig. 5.4. Transformer flux balance is achieved over one switching cycle. From the figure, across the primary windings, 0 to $\pm V_{dc}$ transitions happen simultaneously in both the transformers. At these instants, $S_1 - S_2$ are switched and $i_{A,B}$ change directions. But $\pm V_{dc}$ to 0 transitions are not synchronised.

Fig. 5.20c shows the pulse width modulated high frequency AC voltage, v_{AB}. The voltage levels of v_{AB} are ± 230 V and 0. The secondary DC link voltage v_{pq} is shown in [CH2]. The pulsating v_{pq} has voltage levels $\frac{2V_{dc}}{n} = 614$ V, $\frac{V_{dc}}{n} = 307$ V and 0 V. The rectifier output voltages v_{po} and v_{oq} are shown in [CH3] and [CH4] respectively.

Fig. 5.20d shows the pulse width modulated pole voltage, v_{ab}. v_{ab} has steady state voltage levels- ± 307 V (V_{dc}/n), ± 614 V ($2V_{dc}/n$) and 0. v_{pq}, v_{po} and v_{oq} are shown in [CH2]-[CH4] respectively.

Fig. 5.21a shows the lagging power factor operation of the proposed converter. From the figure, i_a lags v_{ga} by 26.7°. The converter is supplying $\cos 26.7° = 0.89$ lagging power factor load. This figure also shows rectifier output currents i_p and i_q and they are positive over the line cycle. The converter operation supplying 0.896 power factor leading load is shown Fig. 5.21b. The line current i_a leads the output voltage by 26.4°. The rectifier output currents i_p and i_q are shown in Fig. 5.21b.

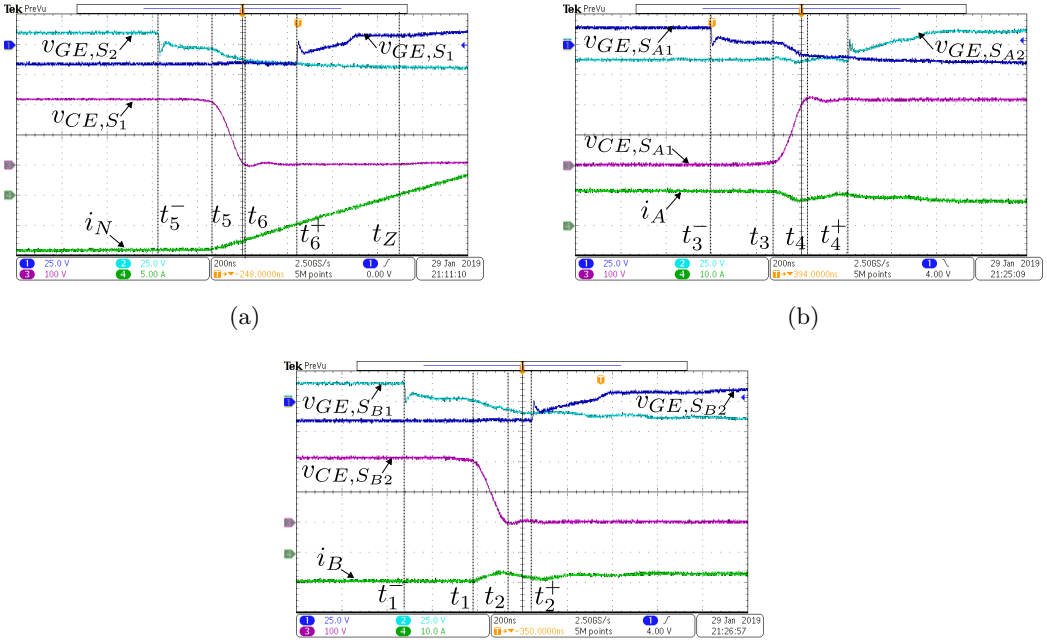


(a) (b)

Figure 5.21: (a) Non UPF operation (PF-0.89 lagging)- [CH1]: v_{ga} (250V/div.), [CH2]-[CH4]: i_a, i_p and i_q (10A/div.), (b) Non UPF operation (PF-0.896 leading)- [CH1]: v_{ga} (250V/div.), [CH2]-[CH4]: i_a, i_p and i_q (10A/div.)

5.5.3 Verification of soft-switching of the DSC legs

In the following discussion turn ON transitions of S_1, S_{A2} and S_{B2} and turn OFF of S_2, S_{A1} and S_{B1} are described.



(a) (b)

(c)

Figure 5.22: Switching transition waveforms- (a) Turn OFF of S_2 and turn ON of S_1. (b) Turn OFF of S_{A1} and turn ON of S_{A2}. (c) Turn OFF of S_{B1} and turn ON of S_{B2}.

Fig. 5.22a shows the switching transition of leg $S_1 - S_2$. S_2 was ON and conducting pole current i_N. S_1 was blocking $v_{CE,S_1} = V_{dc}$. At t_5^-, the gating pulse of S_2 is withdrawn. After sometime at t_5, voltages across $S_1 - S_2$ start changing. Slow change in voltage across S_2 due to device capacitance helps to reduce turn OFF loss of S_2. During this time i_N changes as per (5.4) in Mode VI of section 5.3. At t_6, $v_{CE,S_1} = 0$ and after that i_N changes linearly as per (5.7) in Mode VIII of section 5.3. At t_6^+, gating pulse of S_1, v_{GE,S_1} is applied (before i_N changes its direction). As $v_{CE,S_1} = 0$, zero voltage turn ON (ZVS) of S_1 is ensured. At t_Z, i_N becomes zero and changes its direction.

Switching transition of $S_{A1} - S_{A2}$ is shown in Fig. 5.22b. Before t_3^-, S_{A1} was conducting

i_A and S_{A2} was blocking V_{dc}. At t_3^-, gating pulse of S_{A1} is removed. After sometime at t_3, voltages across $S_{A1} - S_{A2}$ begin to change. Voltage across S_{A1}, $v_{CE,S_{A1}}$, slowly builds upto V_{dc} and the voltage across S_{A2} becomes zero at t_4. Slow change in voltage across S_{A1} due to device capacitance helps to reduce turn OFF loss of S_{A1}. As i_A does not change its direction, the anti-parallel diode of S_{A2} is in conduction after t_4. At t_4^+, gating pulse of S_{A2}, $v_{GE,S_{A2}}$ is applied when $v_{CE,S_{A2}} = 0$ and thus ZVS turn ON is achieved. This transition verifies the operation in Mode IV of section 5.3.

Switching transition of $S_{B1} - S_{B2}$ is presented in Fig. 5.22c. The switching process is similar to the transition of $S_{A1} - S_{A2}$. The switching process verifies the converter operation in Mode II and III of section 5.3. Due to device capacitance, slow rise in voltage across S_{B1} helps to reduce turn OFF loss of S_{B1}. From Fig. 5.22c, it is clearly seen that the gating signal of S_{B2} is applied when the voltage across S_{B2}, $v_{CE,S_{B2}}$ is zero and thus ensuring ZVS turn ON of S_{B2}.

5.5.4 Experimentally measured power loss

The converter is operated with input 230V DC for a variation of output load 0.57kW to 2.42kW. The power loss is measured at different stages of the converter. Fig. 5.23a shows the measured efficiency of the converter. The prototype has maximum efficiency 86.52 % at 1.76kW output power. The experimentally obtained power losses in different stages of the converter are shown in Fig. 5.23b. The experimental and analytical loss distribution of the converter at 1.76kW output power is shown in Fig. 5.23c. As seen from the figure, the analytically estimated power losses at the different stages of the converter are closely matched with the experimentally obtained losses. A pie chart showing the share of loss in different stages at 1.76kW output power is shown in Fig. 5.23d.

Table 5.4: Devices used in experiment and optimal design

		Part No.	V_{CE}/V_D	R_{CE}/R_D
DSC	Used	SKM75GB123D (1200V, 75A)	1.8V	38 mΩ
	Optimal Design	IRFP4137PbF (300V, 38A)	-	56mΩ
DBR	Used	MEE 75-12 DA (1200V, 75A)	1.5V	3.65mΩ
	Optimal Design	DPG20C400PC (400V, 20A)	0.77V	19.8mΩ
NPC	Used	IKW40N120H3 (1200V, 40A)	2.05V	-
	Optimal Design	IKP28N65ES5 (650V, 28A)	1.06V	14mΩ

The experimental prototype is not optimally designed for 2-3kW power level and hence has the relatively low peak efficiency of 86.52%. We have optimally designed the converter at 2.15kW with the devices listed in Table 5.4. The design has an analytically estimated efficiency of 94.7%. The method of analytical estimation is already verified with the existing hardware. As the chosen devices in the optimal design has better conduction loss parameters as shown in

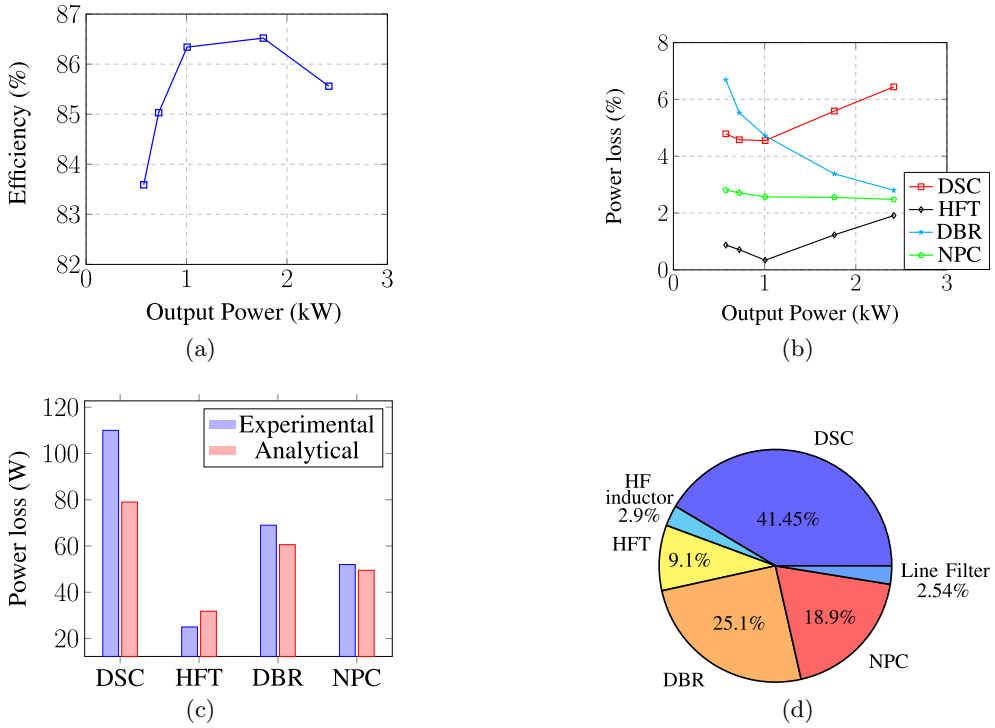


Figure 5.23: (a) Experimentally obtained efficiency of the converter. (b) Variation of power losses with load at various stages of the converter. (c) Loss distribution estimated analytically and obtained experimentally at 1.76kW. (d) Share of loss at 1.76kW output power

Table 5.4 and as the loss is primarily due to conduction, the optimal design has better efficiency.

5.6 Conclusion

This chapter introduced a new single-stage unidirectional 3ϕ high-frequency link PWM inverter topology with two pulsating DC links. Unlike the topologies in previous chapters this converter supports non unity power factor stand alone loads upto $\pm$ 0.866 which is experimentally verified. The generation of three phase balanced pole voltages from two pulsating DC links with sinusoidal average voltages with the help of a low frequency switching network (three level NPC inverter) is discussed in details. The modulation of DSC to generate the pulsating DC links with desired average voltages is described. The circuit analysis of the converter in all the switching modes over a switching cycle is presented in details. The analysis gives the conditions on dead times that ensures ZVS switching of the DSC half-bridge legs throughout the line cycle. To estimate the power loss of the converter analytically, the closed form expressions of the converter power losses are provided. The input current and output voltage THDs, a measure of converter filtering requirement, are also presented. The operation of converter, particularly, different aspects of the modulation strategy, ZVS transitions are experimentally verified on a 2kW hardware prototype. The experimental results are presented with detailed discussions. The converter efficiency and different stage power losses are experimentally measured. The analytically estimated power loss is verified with experimentally obtained values.

Chapter 6

Topology Comparison

6.1 Introduction

Four different unidirectional single-stage HFL three-phase inverter topologies are introduced in chapters 2-5. These topologies have some common characteristics like ASCs are low frequency switched and DSCs are mostly soft-switched over the entire line cycle. Out of these four topologies, only topology 4 can support non UPF power factor (upto $\pm$ 0.866) standalone load. To understand the merits of these topologies, a thorough topological comparison is necessary with the exiting multi-stage high frequency link converter solution.

In this chapter a topological comparison of these topologies with an exiting multi-stage topology is presented. At first topologies 1,2 and 3 are compared. Then the topology 4 and the multi-stage topology are compared. Finally a loss comparison of topologies 3, 4 and the multi-stage topology are presented. The comparison has mainly four aspects- a) converter hardware which describes number of semiconductors used, their blocking voltage, RMS and peak currents; b) High frequency isolation which evaluates number and size of the HFTs, RMS currents of the windings, maximum applied volt-seconds; c) converter input and output filtering requirements which involves estimation of input current and output voltage THDs; d) power loss where we have evaluated the conduction and switching loss in the semiconductors analytically. To perform the comparison fairly, all the topologies under consideration are designed for same operating conditions with given input and output voltages and output power. The switching frequency and modulation index are considered same for all the topologies. For generalization, the parameters of the comparison are evaluated in terms of output power (P), input DC voltage (V_{dc}) or peak output voltage (V_{pk}) and switching frequency (f_s). The parameters are presented in tabular forms. The observations of the comparisons are described in details.

6.2 Basis of comparison

To compare the performances of the unidirectional single stage high frequency link (HFL) inverter topologies (Topology 1-4) discussed in the chapters 2-5, we have designed each topology for a target application of grid integration of utility scale solar photo-voltaic. The specification of the design is given in Table 6.1. The detailed designs of these topologies are given in the section of *Converter design* of the respective chapters. The design of the multi-stage topology is given in Appendix C.

At rated condition the inverter is supplying 200kW of active power at unity power factor

Table 6.1: Target design specification

Parameter	Value
Output power (P)	200 kW
Operation power factor	UPF
Input DC (V_{dc})	800V
Output phase AC peak (V_{pk})	339V (415V L-L RMS)
Switching frequency (f_s)	20kHz
Line frequency (f_o)	50Hz

(UPF) to a 415V (line to line RMS), 50Hz three-phase utility from an 800V DC source. The multi-stage solution has two stages- a unidirectional DC-DC converter (phase-shifted full-bridge (PSFB)) followed by a three-phase voltage source inverter (Fig. 6.1). All the topologies are modulated at the 85% of its maximum possible modulation index.

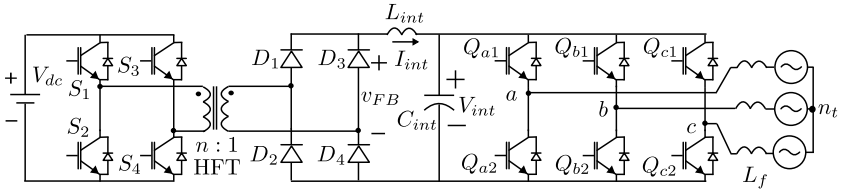


Figure 6.1: Unidirectional Multi-stage HFL topology

6.3 Topology comparison: topology 1, 2 and 3

In this section the topologies 1,2 and 3 are compared. The comparison has four major parts-a) power semiconductors, b) HFTs, c) Filter requirements and d) power loss.

6.3.1 Power semiconductors

In this section we have compared the number of semiconductors used in the topologies under consideration, their blocking voltages, peak and RMS currents. These parameters are already computed in the respective chapters. Table 6.2 and 6.3 presents the comparison of power semiconductors.

Summary of observation

From the above tables the following observations can be made.

- On the DSC, topology 1 employs maximum number of active switches (12 nos.) with low RMS and peak currents.
- Topology 2 has 8 active switches. Out of which 2 switches have higher RMS and peak currents compared to the remaining 6 switches.

Table 6.2: Comparison of DSC power semiconductors of topologies 1,2 and 3

		Scaling Factor	Topology 1	Topology 2	Topology 3
DSC	No. of switches	—	12	8	6
	No of diodes	—	—	—	—
	Blocking voltage	V_{dc}	1	1	1
	RMS current	$\frac{P}{V_{dc}}$	0.39 ($S_{A,B,C_{1,2}}$), 0.33($S_{A,B,C_{3,4}}$)	1.06($S_{1,2}$) 0.33(S_{A3}-S_{C4})	0.64
	Peak current	$\frac{P}{V_{dc}}$	0.78	1.575($S_{1,2}$) 0.79(S_{A3}-S_{C4})	1.36
	Switching	—	Partially Soft-switched	Partially Soft-switched	Soft-switched

Table 6.3: Comparison of ASC power semiconductors of topologies 1,2 and 3

		Scaling Factor	Topology 1,2,3
ASC	No. of switches	—	6
	No. of Diodes	—	12
	Blocking voltage	V_{pk}	2.35
	RMS current	$\frac{P}{V_{pk}}$	0.334(Q_{a1}-Q_{c2}), 0.236(D_{a1}-D_{c4})
	Peak current	$\frac{P}{V_{pk}}$	0.67
	Switching	—	Low frequency switched
	Interstage DC link	—	Three pulsating
	PF support	—	UPF

- Topology 3 employs 6 switches with same RMS and peak currents on the DSC. RMS current is relatively higher compared to topology 1 and 2.
- The blocking voltage of the DSC switches of all three topologies is V_{dc}.
- The DSC switches of the topology 3 are soft-switched throughout the line cycle. Though mostly soft-switched, DSC switches of topology 1 and 2 are hard-switched in some parts of the line cycle.
- The ASC structure of all the three topologies are same.
- On the ASC, 6 line frequency switched devices and 12 diodes are employed. All three topologies have same switch and diode blocking voltage, RMS and peak currents.
- Topology 1, 2 and 3 have three pulsating intermediate DC links.
- The topologies 1, 2 and 3 do not support reactive power. Additional shunt compensator is essential to supply reactive power.

6.3.2 High frequency transformers

Each of topology 1, 2 and 3, employs three winding high frequency transformers with same input and output voltages, currents and area products. The design of the transformers is given in chapter 2. The details of these transformers are presented in Table 6.4.

Table 6.4: Comparison of High frequency transformers of topology 1, 2 and 3

	Scaling Factor	Topology 1, 2, 3
RMS current (primary winding)	$\frac{P}{V_{dc}}$	0.557
RMS current (secondary winding)	$\frac{P}{V_{pk}}$	0.334
Maximum applied volt-seconds	$\frac{V_{dc}}{f_s}$	0.425
Area product	$\frac{P}{f_s J B_m K_w}$	0.242
No. of HFTs	–	3
Turns ratio	–	$0.85\frac{V_{dc}}{V_{pk}}$:1:1

Summary of observation

From the above table the following observations can be made.

- The topologies 1, 2 and 3 employs 3 HFTs each having one primary and two secondary windings.
- As these topologies employ same HFTs, they have same winding RMS currents, area product, maximum applied volt-seconds, turns ratio as given in Table 6.4.

6.3.3 Filter requirements

As discussed in section 2.4.4 of chapter 2, voltage and current THDs are effective measures of inductive and capacitive filter requirements respectively of a converter. We have already estimated the input current and output voltage THDs of the topologies 1-3 in the respective chapters. Due to similarity in switching strategy and structure, topology 1 and 2 have same input current and output voltage THDs. Here we have compared the THDs of the topologies 1-3 in Table 6.5 for the operating condition given in Table 6.1.

Table 6.5: Filter comparison - topology 1, 2 and 3

	Topology 1, 2	Topology 3
DSC (THD_I)	0.55	0.498
ASC (THD_V)	0.6	0.7

Summary of observation

From the above table following observations are made.

- Topology 3 has slightly better input current THD compared to topologies 1 and 2.
- Topologies 1 and 2 have relatively better output voltage THD compared to topology 3.

6.3.4 Power loss

The analytical expressions of the converter power loss are given in chapters 2-4 for the respective topologies. The detailed derivation steps are given in Appendix A. To perform a thorough comparison of the converter power losses, we have considered that all the topologies employ switches with same device parameters like R_{CE}, V_{CE}, R_D, V_D, E_{ON} and E_{OFF}. Then the conduction losses of the DSC switches are further expressed in terms of $\frac{V_{CE}P}{V_{dc}}$ and $\frac{R_{CE}P^2}{V_{dc}^2}$. For diodes R_{CE}, V_{CE} are replaced with R_D, V_D respectively. In case of ASC switches and diodes, V_{dc} in the scaling factors are replaced with V_{pk}. The switching losses of the active switches are also expressed in terms of $\frac{f_s P E_R}{P_R}$ where $E_R = E_{ON_R} + E_{OFF_R}$ and $P_R = V_{CC} I_C$.

Table 6.6: Comparison of power loss of topologies 1,2 and 3

Topology			DSC			ASC	
		Scaling factor	Switch	diode	Scaling factor	Switch	diode
Topology 1	Conduction loss	$V_{CE}P/V_{dc}$	2.49	0.49	$V_{CE}P/V_{pk}$	1.27	1.27
		$R_{CE}P^2/V_{dc}^2$	1.586	0.26	$R_{CE}P^2/V_{pk}^2$	0.67	0.67
	Swithing loss	PE_Rf_s/P_R	0.36		PE_Rf_s/P_R	0	
Topology 2	Conduction loss	$V_{CE}P/V_{dc}$	2.49	0.49	$V_{CE}P/V_{pk}$	1.27	1.27
		$R_{CE}P^2/V_{dc}^2$	2.91	0.26	$R_{CE}P^2/V_{pk}^2$	0.67	0.67
	Swithing loss	PE_Rf_s/P_R	0.18		PE_Rf_s/P_R	0	
Topology 3	Conduction loss	$V_{CE}P/V_{dc}$	2.317	0.32	$V_{CE}P/V_{pk}$	1.27	1.27
		$R_{CE}P^2/V_{dc}^2$	2.45	0.25	$R_{CE}P^2/V_{pk}^2$	0.67	0.67
	Switching loss	PE_Rf_s/P_R	0		PE_Rf_s/P_R	0	

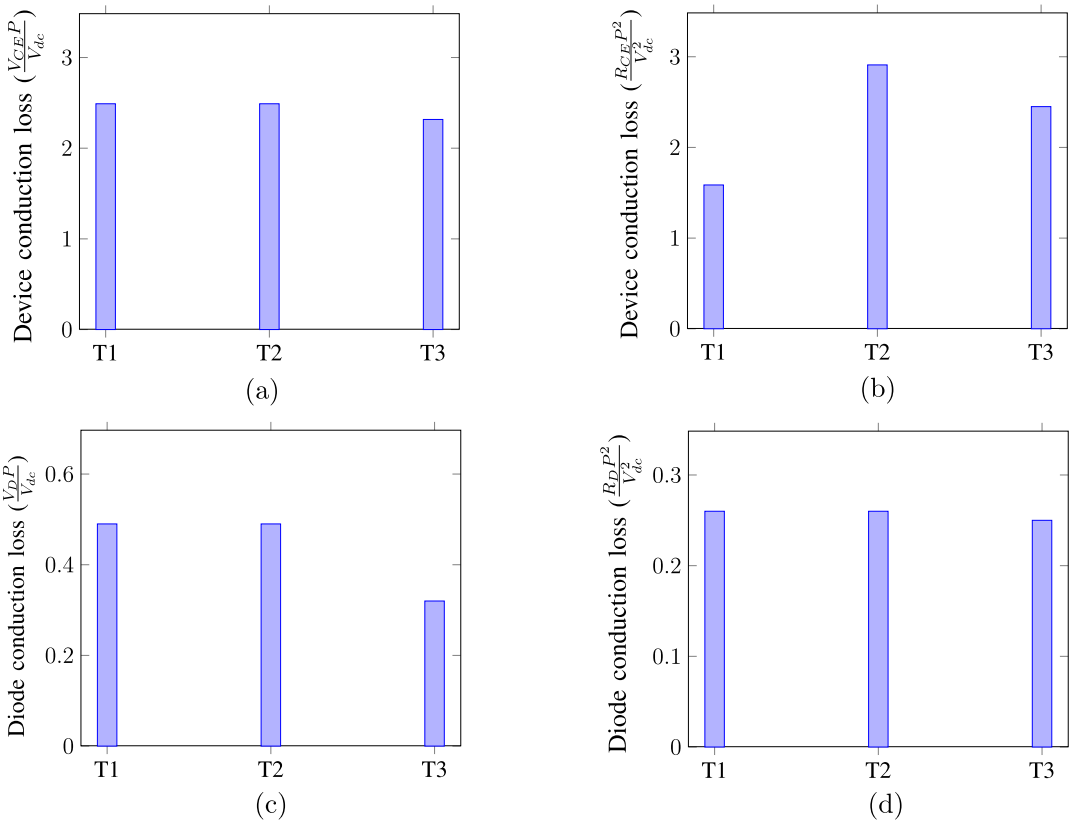


Figure 6.2: DSC conduction loss comparison-Topology 1,2 and 3. Device loss-(a) due to V_{CE}, (b) due to R_{CE}. Diode loss- (c) due to V_D, (d) due to R_D.

To compute the switching losses of the topologies 1 and 2, θ_1 (see Fig. 2.19) is considered 20°. Finally the losses are tabulated in Table 6.6. Due to same structure and modulation strategy, the power loss in ASC of all the three topologies are same. Whereas the DSCs have different power losses. For better visualization the DSC conduction losses of the three topologies are presented as bar charts in Fig. 6.2.

Summary of observation

From the above table following observations are made.

- *DSC conduction loss*- The devices of topology 1 have lower conduction loss where as DSC diodes of topology 3 have lower conduction loss. Topology 2 has relatively higher conduction loss. Overall, the DSCs of these topologies have almost comparable conduction losses.
- *DSC switching loss*- The DSCs of the topology 1 and 2 incur small amount of switching loss. The DSC of topology 3 is soft-switched throughout line cycle. Hence incur no switching loss
- *ASC conduction loss*-Due to same structure and modulation strategy, the ASC conduction losses of all the three topologies are same.
- *ASC switching loss*-As ASCs are line frequency switched, switching losses are negligible.

6.4 Topology comparison: topology 4 and multi-stage topology

In this section the topology 4 and the multi-stage topology are compared. The comparison has four major parts-a) power semiconductors, b) HFTs, c) Filter requirements and d) power loss.

6.4.1 Power semiconductors

In this section we have compared the number of semiconductors used in the topologies under consideration, their blocking voltages, peak and RMS currents. These parameters are already computed in chapter 5 and appendix C respectively. Table 6.7 presents the comparison of power semiconductors.

Summary of observation

From Table 6.7, the following observations can be made.

- On the DSC, topology 4 employs 6 switches where as the multi-stage topology uses 4 switches.
- Two DSC switches of topology 4 have relatively higher RMS and peak currents. Remaining devices have similar currents as multi-stage topology.

Table 6.7: Comparison of power loss of topologies 4 and multi-stage topology

		Scaling Factor	Topology 4	Multi-stage
DSC	No. of switches	—	6	4
	Blocking voltage	V_{dc}	1	1
	RMS current	$\frac{P}{V_{dc}}$	1.38($S_{1,2}$), 0.52(S_{A1}-S_{B2})	0.83($S_{1,2}$), 0.77($S_{3,4}$)
	Peak current	$\frac{P}{V_{dc}}$	2.04($S_{1,2}$), 1.18(S_{A1}-S_{B2})	1.2
	Switching	—	Soft-switched	Soft-switched
ASC	No. of switches	—	12	6
	No. of Diodes	—	8	4
	Blocking voltage	V_{pk}	3.53(Q_{ap}-Q_{cq}), 1.76(Q_{ao}-Q_{co}), 1.76($D_1 - D_8$)	2.0(Q_{a1}-Q_{c2}), 2.35(D_1-D_4)
	RMS current	$\frac{P}{V_{pk}}$	0.323(Q_{ap}-Q_{cq}), 0.08(Q_{ao}-Q_{co}), 0.396($D_1 - D_8$)	0.327(Q_{a1}-Q_{c2}), 0.35($D_1 - D_4$)
	Peak current	$\frac{P}{V_{pk}}$	0.67(Q_{ap}-Q_{cq}), 0.33(Q_{ao}-Q_{co}), 0.67($D_1 - D_8$)	0.67(Q_{a1}-Q_{c2}), 0.5($D_1 - D_4$)
	Switching	—	Low frequency switched	Hard switched
	Interstage DC link	—	Two pulsating	one fixed
	PF support	—	$\pm$.866	Any

- The blocking voltage of the DSC switches of both the topologies is V_{dc}.
- The DSC of both the topologies are soft-switched throughout the line cycle.
- The ASCs of topology 4 has 12 low frequency switched active devices and 8 diodes. The multi-stage topology employs 6 switches on the ASC along with 4 diodes. These ASC switches are high-frequency hard switched.
- ASC switches and diodes of both the topologies have comparable peak and RMS currents.
- Topology 4 has two pulsation DC links as it does not require any inter-stage filter capacitors. The multi-stage solution employs inter-stage DC link filter capacitor which affects the converter power density and reliability. The interstage DC link is fixed here.
- The topology 4 supports upto $\pm$ 0.866 power factor operations. The multi-stage topology supports any power factor operation.

6.4.2 High frequency transformers

Table 6.8: Comparison of High frequency transformers of topology 4 and multi-stage topology

	Scaling Factor	Topology 4	Multi-stage
RMS current (primary winding)	$\frac{P}{V_{dc}}$	0.99	1.2
RMS current (secondary winding)	$\frac{P}{V_{pk}}$	0.56	0.5
Maximum applied volt-seconds	$\frac{V_{dc}}{f_s}$	0.425	0.425
Area product	$\frac{P}{f_s J B_m K_w}$	0.42	0.5
No. of HFTs	–	2	1
Turns ratio	–	$0.57\frac{V_{dc}}{V_{pk}}$:1	$0.424\frac{V_{dc}}{V_{pk}}$:1

Topology 4 employs two high frequency transformers where as the multi-stage topology employ one HFT. The design of the transformers is given in chapter 5 and appendix C respectively. The comparison of these transformers are presented in Table 6.8.

Summary of observation

From the above table, the observations are as follows-

- Topology 4 employs 2 HFTs whereas the multi-stage topology uses only one.
- Winding RMS currents of the HFTs of both the topologies are comparable.
- Area product of a HFT of the multi-stage topology is slightly higher than the topology 4.
- The maximum applied volt-seconds of the HFTs used in both the topologies are same.

6.4.3 Filter requirements

Table 6.9: Filter comparison - topology 4 and multi-stage topology

	Topology 4	Multi-stage
DSC (THD_I)	0.756	0.42
ASC (THD_V)	0.8	0.69
Intermediate DC Link	–	0.42 (THD_V, PSFB), 0.48 (THD_I, 3ϕVSI)

We have already estimated the input current and output voltage THDs of the topology 4 and multi-stage topology in chapter 5 and appendix C respectively. Here we have compared the THDs in Table 6.5 for the operating condition given in Table 6.1.

Summary of observation

From the above table following observations are made.

- Input current THD of the multi-stage topology is better than the topology 4. The output voltage THDs of both the topologies are comparable.
- Multi-stage topology needed additional inter-stage filtering. Inter-stage DC bus voltage and current THDS are given in Table 6.9. Hence overall filtering requirement of the multi-stage topology is relatively higher compared to topology 4.

6.4.4 Power loss

The analytical expressions of the converter power losses are given in chapter 5 and appendix C for the respective topologies. The detailed derivation steps are given in Appendix A. Similar to topologies 1-3, the conduction losses of the DSC switches are expressed in terms of $\frac{V_{CE}P}{V_{dc}}$ and

$\frac{R_{CE}P^2}{V_{dc}^2}$. For diodes R_{CE}, V_{CE} are replaced with R_D, V_D respectively. In case of ASC switches and diodes V_{dc} of the scaling factors are replaced with V_{pk}. The switching losses of the active switches are also expressed in terms of $\frac{f_s P E_R}{P_R}$ where $E_R = E_{ON_R} + E_{OFF_R}$ and $P_R = V_{CC} I_C$. Finally the losses are tabulated in Table 6.10.

Table 6.10: Comparison of power loss of topology 4 and multi-stage topology

Topology			DSC			ASC	
		Scaling factor	Switch	diode	Scaling factor	Switch	diode
Topology 4	Conduction loss	$V_{CE}P/V_{dc}$	2.945	0.91	$V_{CE}P/V_{pk}$	1.26	2.347
		$R_{CE}P^2/V_{dc}^2$	4.87	0.87	$R_{CE}P^2/V_{pk}^2$	0.664	1.317
	Swithing loss	PE_Rf_s/P_R	0		PE_Rf_s/P_R	0	
Multi-stage	Conduction loss	$V_{CE}P/V_{dc}$	2.18	0.18	$V_{CE}P/V_{pk}$	1.156	1.125
		$R_{CE}P^2/V_{dc}^2$	2.56	0.21	$R_{CE}P^2/V_{pk}^2$	0.61	0.563
	Swithing loss	PE_Rf_s/P_R	0		PE_Rf_s/P_R	2.55	

Summary of observation

From the above table following observations are made.

- *Conduction loss*- Topology 4 has relatively higher conduction loss compared to multi-stage topology
- *Switching loss*- The DSC of both the topologies are soft-switched throughout line cycle. The ASC of topology 4 is low frequency switched hence has negligible switching loss. The ASC of the multi-stage topology is hard-switched and hence incurs significant switching loss.

6.5 Loss comparison: Topology 3, 4 and multi-stage topology

In section 6.3, we have compared the topologies 1, 2 and 3 which only supports UPF operation. It is seen that topology 1 uses more switches with lower RMS currents where as topology 3 employs less number of active switches with higher RMS current. The conduction losses of these topologies are comparable. Topology 3 does not have any switching loss, whereas DSCs of topology 1 and 2 incur small switching loss.

In section 6.4 we have compared topology 4 and existing multi-stage topology. These topologies can support non-UPF operation. The topology 4 employs more active switches and the conduction loss is relatively high compared to the multi-stage topology. But the total filtering requirement is more in multi-stage topology. Additionally, the ASC of the multi-stage topology incurs high switching loss whereas the topology 4 has negligible switching loss as the DSC is soft-switched and ASC is low frequency switched.

Here a comprehensive performance comparison between the above two groups are given. From the first group, topology 3 is chosen. The power loss of topology 3, 4 and multi-stage

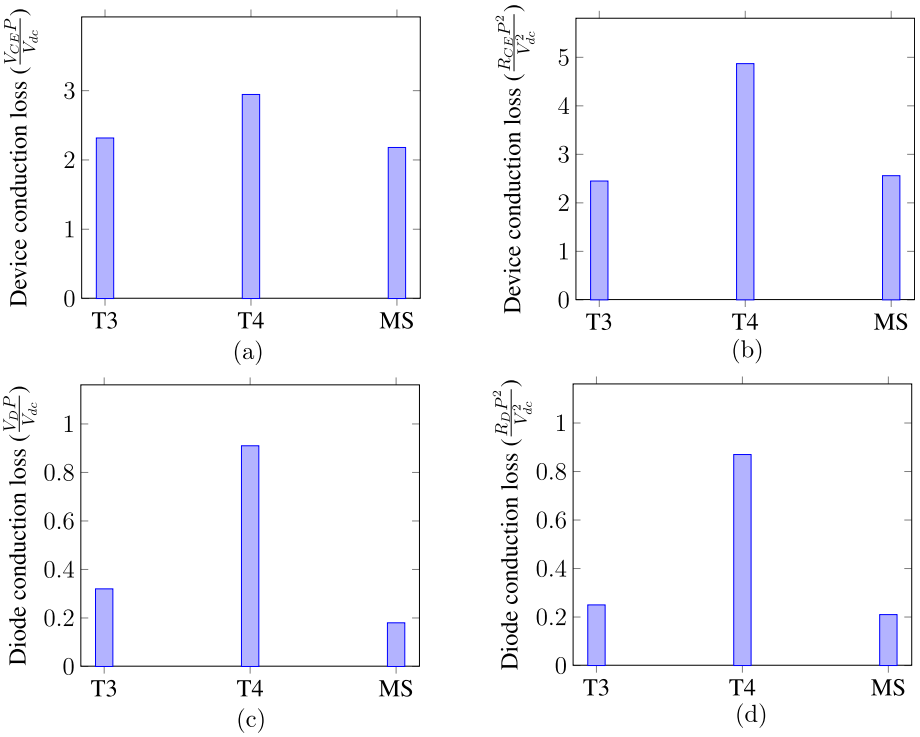


Figure 6.3: DSC conduction loss comparison-Topology 3,4 and multi-stage (MS). Device loss- (a) due to V_{CE}, (b) due to R_{CE}. Diode loss- (c) due to V_D, (d) due to R_D.

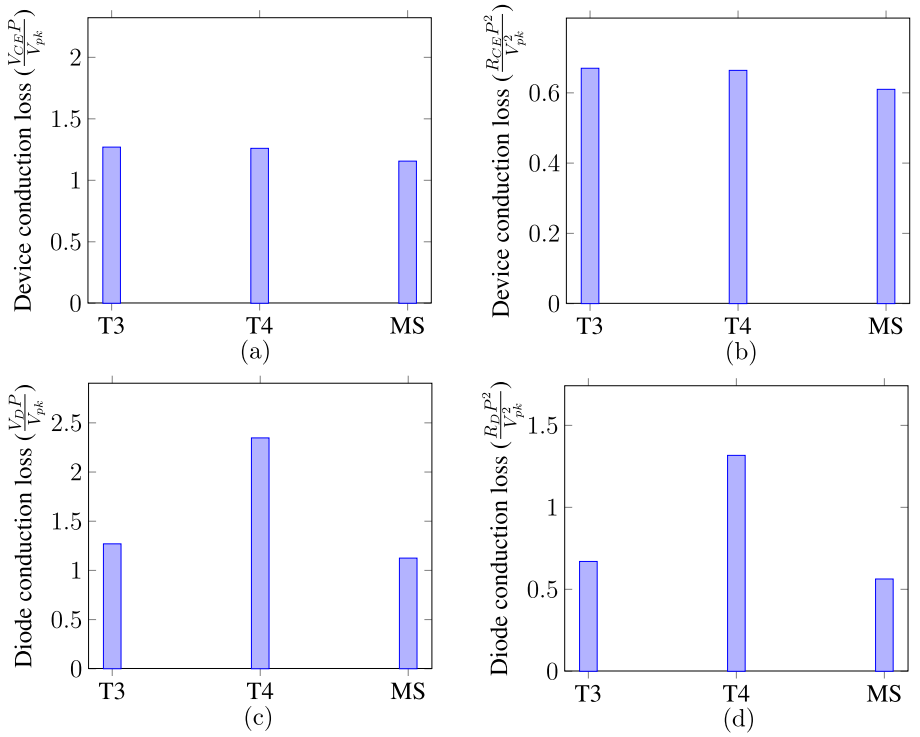


Figure 6.4: ASC conduction loss comparison-Topology 3,4 and multi-stage (MS). Device loss- (a) due to V_{CE}, (b) due to R_{CE}. Diode loss- (c) due to V_D, (d) due to R_D.

topology are compared here. Fig. 6.3 and 6.4 show the conduction losses of DSC and ASC

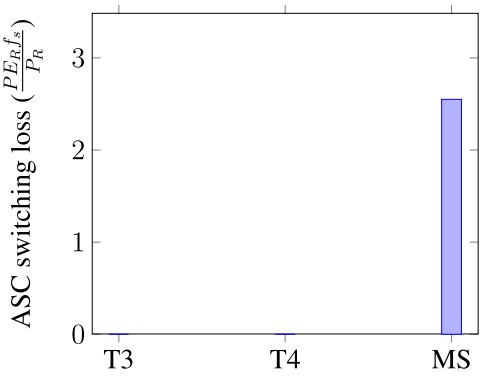


Figure 6.5: ASC switching loss comparison-Topology 3,4 and multi-stage (MS)

respectively. As the DSCs of the considered topologies are soft-switched, only the switching losses of ASCs are presented in Fig. 6.5.

6.5.1 Summary of observation

From the above figures following observations can be made.

- *DSC conduction loss*- the topology 3 and the multi-stage topology have similar conduction losses where as the topology 4 has relatively higher conduction loss.
- *ASC conduction loss*- the conduction losses of the ASC devices of all the three topologies are comparable whereas the ASC diodes of topology 4 have relatively higher losses.
- *Switching loss*- The DSCs of all the three topologies are soft-switched throughout the line cycle. The ASCs of topology 3 and 4 are low frequency switched hence incur negligible switching loss. Whereas the ASC of the multi-stage topology is high-frequency hard switched incurring significant switching loss.
- Due to switching loss, multi-stage topology incurs higher power loss compared to topology 3. Topology 4 has relatively higher conduction loss compared to topology 3 but it can support non UPF operation upto $\pm$ 0.866 PF. Whereas topology 3 supports only UPF operation and to support any non UPF operation additional shunt compensator is needed.

6.6 Conclusion

In this chapter we compared different performance parameters like- number of semiconductors used, their blocking voltages, RMS currents; filtering requirements; size of the HFTs; power losses of the topologies presented in chapters 2-5 with a standard unidirectional multi-stage HFL topology. The topologies in chapters 2-5 employ more number of semiconductor devices with similar blocking voltages and RMS currents compared to the existing multi-stage solution. The topologies discussed in this thesis though incurred comparable or slightly higher conduction loss, the switching losses are either zero or negligibly small, unlike the multi-stage topology. Thus

the topologies discussed in this thesis provide solutions with power loss independent switching frequency, which was one of the objective of this work. The topologies 1-4 have comparable input and output filtering requirements, compared to the multi-stage solution evaluated at same switching frequency, modulation index, operating power factor, input voltage and output power. But the overall filtering requirements of the topologies discussed in this thesis are less compared to the multi-stage topology as inter-stage filtering are avoided hence have improved power density and reliability. The topologies in chapters 2-5 employ multiple HFTs with lower area-product compared to one HFT in the multi-stage topology. Out of the topologies 1-4, topologies 4 incurs higher conduction loss compared to topologies 1-3 but have the ability to support non UPF power factor standalone load upto $\pm$ 0.855. The topology 3 incurs lower power loss compared to the multi-stage solution. Topologies 1-3 support only UPF operation and to support non UPF load, additional shunt compensators are needed. Thus the topologies discussed in chapters 2-5, are ideal solutions for grid integration of PV and fuel cells and have definite advantages over the existing solutions described above.

Chapter 7

Conclusions and Future Work

The unidirectional single-stage three-phase high-frequency-link DC-AC converters are viable solutions for grid integration of PV and fuel cell where the power flow is unidirectional (DC source to AC grid). In this thesis we have explored two types of unidirectional HFL inverter topologies- a) the topologies with three pulsating DC links and b) the topologies with two pulsating DC links. The suggested modulation strategies ensure either line frequency switching of the active switches or soft-switching without additional snubber. Hence the converter switching losses are negligible. Though these converters employ higher number of power semiconductors on both side of the HFTs to process the power, due to negligible or low switching loss these solutions can be competitive to the conventional solutions with line frequency transformers.

7.1 Conclusion

The high frequency link three-phase inverter topologies to interface utility scale PV to the AC grid are considered in this thesis. The motivation of the thesis is to design the converter topologies and their modulation strategy to ensure high quality output, efficiency, power density and reliability. Four new high frequency link inverter topologies are introduced and designed in this thesis. The major contributions are summarised as follows.

7.1.1 Introduction of the new converter topologies

The thesis introduced three unidirectional HFL topologies with three pulsating DC links and one topology with two pulsating DC links. These converters have three major components-a) DC side converter (DSC), b) high frequency transformers (HFT) and c) AC side converter (ASC). In all the topologies the pulse width modulation was implemented on the DSC which involves high frequency switching of the active switches of DSC. The modulation and associated high frequency switching of the active switches of ASC were avoided. This methodology results in negligible switching loss of the ASC and hence improves converter efficiency. Further, the high frequency switched DSCs were soft-switched without additional snubber circuit. The introduced topologies did not use any interstage filter capacitors and hence interstage DC links were pulsating. Hence the overall filtering requirement of the topologies were less compared to traditional multi-stage converter solution. Thus the converters discussed in this thesis are efficient and compact solutions for grid integration of PV and fuel cell. The major difference between the two and three pulsating DC links based topologies is that the topology with two pulsating DC links supports $\pm$ 0.866 power factor operation and incur relatively higher

conduction loss. The topologies with three DC links support only UPF operation. An additional shunt compensator is needed to support reactive power.

7.1.2 Analysis of switching process of the converters

Switching process of all the topologies over a switching cycle were presented through detailed circuit analysis. The topologies have several modes of operation over a switching cycle. Simplified equivalent circuits were given for all the modes of operation. The critical switching waveforms were presented depicting the operation of the converters over a switching cycle. The circuit analysis considered non-idealities like DSC device parasitic capacitances and the leakage inductances of the HFTs. Closed form expressions of various circuit parameters like device voltages, pole currents were obtained from the circuit analysis in each mode of operation. To achieve ZVS turn ON of the DSC switches through out the line cycle, conditions on dead times were derived for all the topologies.

7.1.3 Experimental validation of operation

The operation of the converter topologies were experimentally verified in laboratory scale hardware prototypes with power range 2-6kW. The topologies were supplied from a input DC source with voltage range 200-500V. Different aspects of the modulation strategy like generation of balanced three phase AC outputs, low frequency switching of the ASC active switches, flux balance of the HFTs over a switching cycle, non-UPF operation of the converter, critical pole voltages and pole currents were experimentally validated and the experimental waveforms were presented in the thesis. The switching transition waveforms of the DSC active switches were shown along with detailed discussions to show the ZVS operation of the DSC. The experimentally measured efficiency plots of the topologies were shown. The power losses at the different stages of the converters were experimentally measured.

7.1.4 Analysis and comparison of performances

The performance of the topologies introduced in the thesis were compared with the conventional multi-stage topology. The main aspects of the performance comparison are a) hardware comparison- where number of semiconductors used, their blocking voltages, RMS and peak currents were compared; b) high frequency transformer comparison- where number of transformers used, their area-products, RMS of winding currents, maximum applied volt-seconds were compared; c) filtering requirement comparison- where input current and output voltage THDs were compared; d) power loss comparison- where conduction and switching loss of the DSCs and ASCs were compared. The topologies introduced in the thesis employ more number of semiconductor devices with similar blocking voltages and RMS currents compared to the existing multi-stage solution. The new topologies though incurred comparable or slightly higher conduction loss, the switching losses are either zero or negligibly small, unlike the existing multi-stage topology. Thus the topologies discussed in this thesis provide high power density converter solutions with reduced switching loss, which was main objective of this work.

7.2 Scope of future work

Some interesting and important research topics which have not been explored in this thesis and can be carried out in future are identified as follows.

- The closed loop grid connected control of the topologies supplying power at UPF have not been explored. The control is different from the conventional $P - Q$ control of the grid connected inverters because the topologies 1, 2 and 3 do not have ability to supply reactive power and topology 4 has limited capability of supplying reactive power.

- The operation of these topologies connected with the grid are required to be explored during grid disturbances like faulty grid conditions or any grid transients. Fault ride through capabilities of these topologies need to be investigated.

- Single stage unidirectional HFL inverter topologies have one major drawback. There is no alternative path for circulation of pole currents during an event of the failure of the ASC active switches. Any such event results in disruption of pole currents (which are current sources) and associated over voltage across the healthy devices of the ASC causing further damage of the devices. Additional auxiliary circuits or modification in topology structure are required to be explored to avoid such problems.

- To ensure ZVS turn ON of the DSC switches over the entire line cycle, additional inductances in series with the HFTs are added. These inductors experience large current swing, and incur significant core losses. Two approaches in this regard can be explored-a) design of high frequency inductors with appropriate core material, b) integration of the additional inductance with the HFT.

- The ASC devices and diodes of the topologies presented in this thesis experience over voltage during zero to active state transition. Simple RCD snubbers were employed during experiment to suppress the voltage overshoot. This approach causes additional loss in the snubber. Active or passive snubber circuits suitable for these topologies with low loss need to be explored.

- The total number of semiconductors used in the new topologies are high compared to a conventional multi-stage solution. Hence there are further scope of improvement from the topology aspect keeping the main objectives, line switching of ASC active switches and soft-switching of the DSC switches, intact.

Appendix A

Estimation of Conduction Loss

The conduction loss expressions of the topologies 1-5 are given in the respective chapters. The detailed derivations are not included in the main chapters. Here detailed derivations of conduction losses of the topology 4 are provided as an example. Similar procedure is followed to calculate conduction loss in case of other topologies discussed in this thesis.

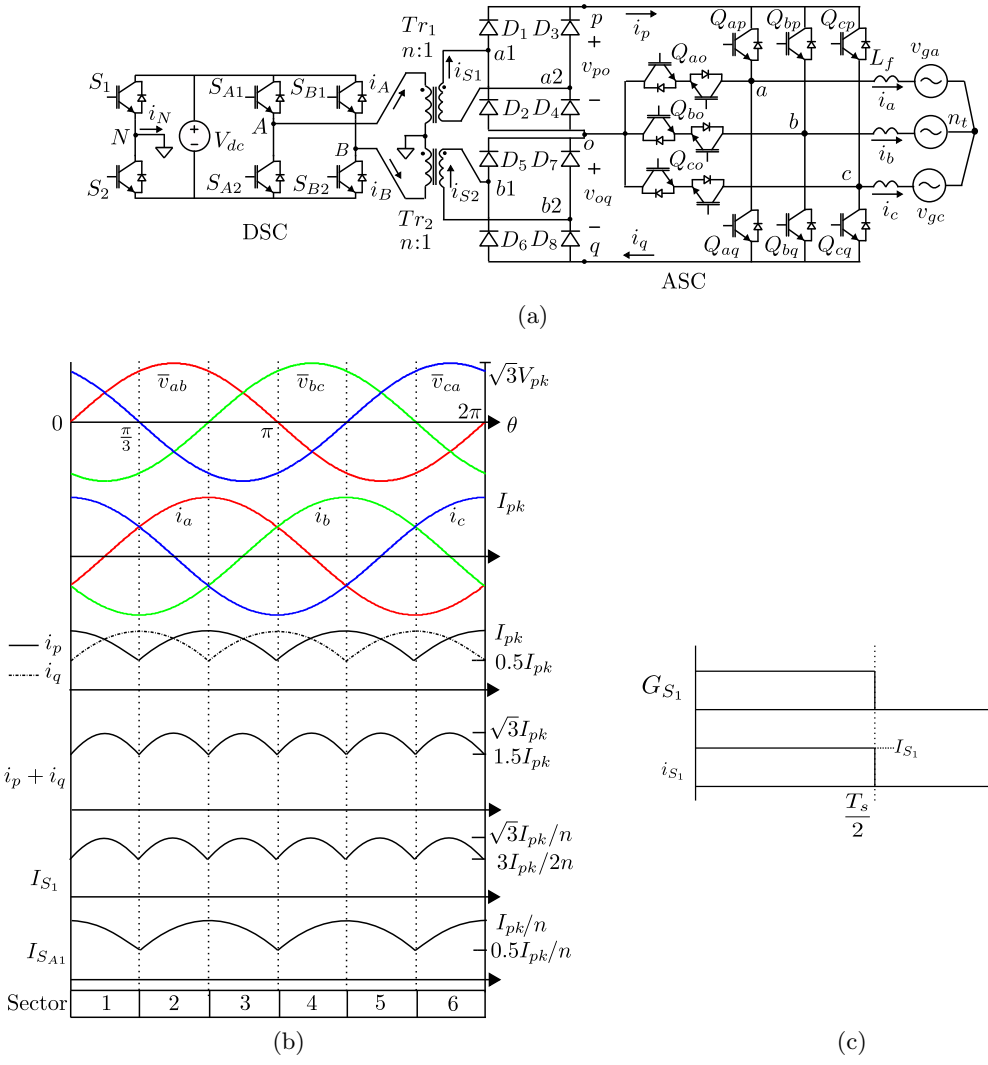


Figure A.1: (a) Topology 4, (b) Current wave forms of topology 4 for UPF operation, (c) Gating signal and current waveform of the switch S_1

A.1 Conduction loss expression of S_1

The conduction loss of switch S_1 is expressed as in (A.1)

$$P_{C_{S_1}} = V_{CE} I_{S_1,avg} + R_{CE} I^2_{S_1,RMS} \tag{A.1}$$

$I_{S_1,avg}$ and $I_{S_1,RMS}$ are the average and RMS current through S_1 respectively.

The current through S_1 (see Fig. A.1) is a switching frequency (f_s) current with sinusoidally varying magnitude. The envelope of the current through S_1, i_{S_1} at UPF operation is shown in Fig. A.1b. The envelope has a periodicity over $\frac{\pi}{3}$ as seen in the Fig. A.1b. Over $0 < \theta < \frac{\pi}{3}$, the magnitude of i_{S_1}, I_{S_1} is given as in (A.2).

$$I_{S_1} = \frac{\sqrt{3} I_{pk}}{n} \cos\left(\frac{\pi}{6} - \theta\right) \tag{A.2}$$

From Fig. A.1c, S_1 conducts for $\frac{T_s}{2}$ duration over a switching cycle, T_s. The RMS current through S_1, $I_{S_1,RMS}$ is given as

$$\begin{aligned} I^2_{S_1,RMS} &= \frac{3}{2\pi} \int_0^{\frac{\pi}{3}} \frac{3 I^2_{pk}}{n^2} \cos^2\left(\frac{\pi}{6} - \theta\right) d\theta \\ &= 1.37 \frac{I^2_{pk}}{n^2} \end{aligned} \tag{A.3}$$

The average current through S_1, $I_{S_1,avg}$ is given as

$$\begin{aligned} I_{S_1,avg} &= \frac{3}{2\pi} \int_0^{\frac{\pi}{3}} \frac{\sqrt{3} I_{pk}}{n} \cos\left(\frac{\pi}{6} - \theta\right) d\theta \\ &= 0.83 \frac{I_{pk}}{n} \end{aligned} \tag{A.4}$$

Hence using (A.1), the conduction loss through the device S_1 is given as

$$P_{C_{S_1}} = \frac{0.83 V_{CE} I_{pk}}{n} + 1.37 \frac{R_{CE} I^2_{pk}}{n^2} \tag{A.5}$$

S_2 has similar current waveform as S_1. Hence, has same loss expression.

A.2 Conduction loss expression of S_{A1}

The conduction loss of switch S_{A1} is expressed as in (A.6)

$$P_{C_{S_{A1}}} = V_{CE} I_{S_{A1},avg} + R_{CE} I^2_{S_{A1},RMS} \tag{A.6}$$

$I_{S_{A1},avg}$ and $I_{S_{A1},RMS}$ are the average and RMS current through S_{A1} respectively.

The current through S_{A1} (see Fig. A.2) is a switching frequency current with sinusoidally varying magnitude, $I_{S_{A1}}$. The current magnitude $I_{S_{A1}}$ at UPF operation is shown in Fig. A.1b over a line cycle. $I_{S_{A1}}$ has a periodicity over $\frac{2\pi}{3}$ as seen in the Fig. A.1b and has symmetry

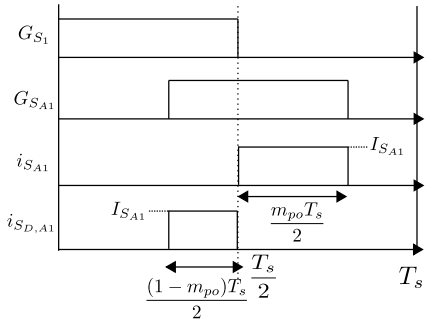


Figure A.2: Gating signal and current waveform of the switch S_{A1}

over $\frac{\pi}{3}$. Over $0 < \theta < \frac{\pi}{3}$, $I_{S_{A1}}$ is given as in (A.7).

$$I_{S_{A1}} = \frac{I_{pk}}{n}\cos\theta \tag{A.7}$$

From Fig. A.2, S_{A1} conducts for $\frac{m_{po}T_s}{2}$ duration over a switching cycle, T_s. Where m_{po} is the modulation signal and over $0 < \theta < \frac{\pi}{3}$, $m_{po} = 1.155M\cos\left(\frac{\pi}{6}+\theta\right)$. The RMS current through S_{A1}, $I_{S_{A1},RMS}$ is given as

$$\begin{aligned} I^2_{S_{A1},RMS} &= \frac{3}{2\pi}\int_0^{\frac{\pi}{3}} m_{po} I^2_{S_{A1}} d\theta \\ &= \frac{5\sqrt{3}}{12\pi}\frac{MI^2_{pk}}{n^2} \\ &= 0.23\frac{MI^2_{pk}}{n^2} \end{aligned} \tag{A.8}$$

The average current through S_{A1}, $I_{S_{A1},avg}$ is given as

$$\begin{aligned} I_{S_{A1},avg} &= \frac{3}{2\pi}\int_0^{\frac{\pi}{3}} m_{po} I_{S_{A1}} d\theta \\ &= \frac{MI_{pk}}{4n} \end{aligned} \tag{A.9}$$

Hence using (A.6), the conduction loss through the device S_{A1} is given as

$$P_{C_{S_{A1}}} = \frac{MV_{CE}I_{pk}}{4n} + \frac{0.23MR_{CE}I^2_{pk}}{n^2} \tag{A.10}$$

S_{A2}, S_{B1} and S_{B2} have similar current waveforms. Hence, have same loss expressions.

As seen in the Fig. A.2, the anti-parallel diode of S_{A1} conducts for $\frac{(1-m_{po})T_s}{2}$ duration over a switching cycle, T_s and has the current magnitude $I_{S_{A1}}$. The RMS current through the anti-parallel diode of S_{A1}, $I_{S_{D,A1},RMS}$ is given as

$$\begin{aligned} I^2_{S_{D,A1},RMS} &= \frac{3}{2\pi}\int_0^{\frac{\pi}{3}} (1-m_{po}) I^2_{S_{A1}} d\theta \\ &= (0.353 - 0.23M)\frac{I^2_{pk}}{n^2} \end{aligned} \tag{A.11}$$

The average current through the anti-parallel diode of S_{A1}, $I_{S_{D,A1},avg}$ is given as

$$\begin{aligned} I_{S_{D,A1},avg} &= \frac{3}{2\pi}\int_0^{\frac{\pi}{3}}(1-m_{po})I_{S_{A1}}d\theta \\ &= (0.41-0.254M)\frac{I_{pk}}{n} \end{aligned} \tag{A.12}$$

The power loss in the anti-parallel diode of S_{A1} is given as

$$P_{C_{D,S_{A1}}} = (0.41-0.254M)\frac{V_D I_{pk}}{n} + (0.353-0.23M)\frac{R_D I_{pk}^2}{n^2} \tag{A.13}$$

The anti-parallel diodes of S_{A2}, S_{B1} and S_{B2} have similar current waveforms. Hence, have same loss expression. The anti parallel diodes of $S_1 - S_2$ briefly conducts during commutation. Their losses are neglected.

A.3 Conduction loss expression of D_1

The diodes in the secondary rectifier ideally conduct for one half of the switching cycle as shown in Fig. A.3. D_1 has same current envelope as i_p. i_p has a periodicity over $\frac{2\pi}{3}$ as seen in the

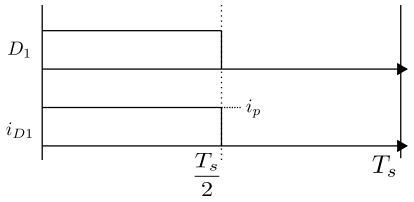


Figure A.3: Current waveform of the diode D_1

Fig. A.1b and has symmetry over $\frac{\pi}{3}$. Over $0 < \theta < \frac{\pi}{3}$, i_p is given as in (A.14).

$$i_p = I_{pk}\cos\theta \tag{A.14}$$

The RMS current through D_1, $I_{D_1,rms}$ is given as

$$\begin{aligned} I_{D_1,RMS}^2 &= \frac{3}{2\pi}\int_0^{\frac{\pi}{3}} i_p^2 d\theta \\ &= 0.353 I_{pk}^2 \end{aligned} \tag{A.15}$$

The average current through D_1, $I_{D_1,avg}$ is given as

$$\begin{aligned} I_{D_1,avg} &= \frac{3}{2\pi}\int_0^{\frac{\pi}{3}} i_p d\theta \\ &= 0.41 I_{pk} \end{aligned} \tag{A.16}$$

The power loss in D_1 is given as

$$\begin{aligned} P_{C_{D_1}} =& V_D I_{D_1,avg} + R_D I^2_{D_1,RMS} \\ =& 0.41 V_D I_{pk} + 0.353 R_D I^2_{pk} \end{aligned} \tag{A.17}$$

Due to similar current waveforms, the other diodes in the two diode bridges have same loss expressions.

A.4 Conduction loss expression of Q_{ap}

Based on the modulation strategy of topology 4, the gating signal of Q_{ap} is shown in Fig. A.4. When Q_{ap} is ON, it conducts i_a. Over $\frac{\pi}{3} < \theta < \pi$, when Q_{ap} is ON, i_a is given as in (A.18).

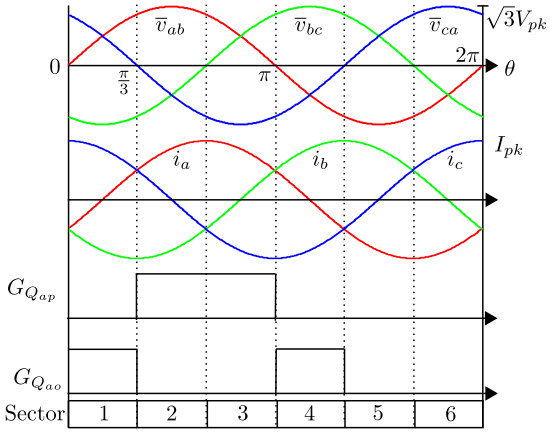


Figure A.4: Gating signal and current waveform of the switch Q_{ap}

$$i_a = I_{pk} \sin\left(\theta - \frac{\pi}{6}\right) \tag{A.18}$$

The RMS current through Q_{ap}, $I_{Q_{ap},RMS}$ is given as

$$\begin{aligned} I^2_{Q_{ap},RMS} &= \frac{1}{2\pi} \int_{\frac{\pi}{3}}^{\pi} i_a^2 d\theta \\ &= 0.24 I^2_{pk} \end{aligned} \tag{A.19}$$

The average current through Q_{ap}, $I_{Q_{ap},avg}$ is given as

$$\begin{aligned} I_{Q_{ap},avg} &= \frac{1}{2\pi} \int_{\frac{\pi}{3}}^{\pi} i_a d\theta \\ &= 0.28 I_{pk} \end{aligned} \tag{A.20}$$

The conduction loss through the device Q_{ap} is given as

$$P_{C_{Q_{ap}}} = 0.28 V_{CE} I_{pk} + 0.24 R_{CE} I^2_{pk} \tag{A.21}$$

Q_{aq}, Q_{bp}, Q_{bq}, Q_{cp} and Q_{cq} have similar current waveforms. Hence, have same loss expressions.

A.5 Conduction loss expression of Q_{ao}

Based on the modulation strategy discussed in the submitted manuscript, the gating signal of Q_{ao} is obtained and is shown in Fig. A.4. When Q_{ao} is ON, it conducts i_a. Q_{ao} is a four quadrant switch as shown in Fig. A.1a. When i_a is positive, one two quadrant switch and anti-parallel diode of another two quadrant switch conduct and when i_a is negative, other switch and diode come into conduction. Q_{ao} conducts twice over a line cycle. Over $\frac{\pi}{6} < \theta < \frac{\pi}{3}$, i_a is given as in (A.18). The RMS current through a two quadrant switch of Q_{ao}, $I_{Q_{ao},RMS}$ is given as

$$\begin{aligned} I^2_{Q_{ao},RMS} &= \frac{2}{2\pi}\int_{\frac{\pi}{6}}^{\frac{\pi}{3}} i_a^2 d\theta \\ &= 0.014 I^2_{pk} \end{aligned} \tag{A.22}$$

The average current through a two quadrant switch of Q_{ao}, $I_{Q_{ao},avg}$ is given as is given as

$$\begin{aligned} I_{Q_{ao},avg} &= \frac{2}{2\pi}\int_{\frac{\pi}{6}}^{\frac{\pi}{3}} i_a d\theta \\ &= 0.04 I_{pk} \end{aligned} \tag{A.23}$$

The conduction loss through a two quadrant switch of Q_{ao} is given as

$$P_{C_{Q_{ao}}} = 0.04 V_{CE} I_{pk} + 0.014 R_{CE} I^2_{pk} \tag{A.24}$$

The anti-parallel diode also have same RMS and avg current expression. Hence the conduction loss of an anti-parallel diode of a a two quadrant switch of Q_{ao} is given as

$$P_{C_{D_{Q_{ao}}}} = 0.04 V_D I_{pk} + 0.014 R_D I^2_{pk} \tag{A.25}$$

The other two quadrant switch and its anti-parallel diode of Q_{ao} have same loss expressions. Q_{bo} and Q_{co} have similar current waveforms. Hence, have same loss expressions.

Appendix B

Estimation of turn ON ZVS bounds of topology 1

B.1 Limits on dead time during zero to active state transition

To achieve ZVS turn ON of the incoming switch during zero to active state transition, the limits on dead time is given in (2.22). The limits are expanded as

$$\begin{aligned} &\frac{1}{\omega_p}\sin^{-1}\left(\frac{nV_{dc}}{\omega_p L_{lk} I_a}\right) \leq DT \leq \frac{1}{\omega_p}\sin^{-1}\left(\frac{nV_{dc}}{\omega_p L_{lk} I_a}\right) + i_{pa}(t_3)\frac{L_{lk}}{V_{dc}} \\ &\Rightarrow \frac{1}{\omega_p}\sin^{-1}\left(\frac{nV_{dc}}{\omega_p L_{lk} I_a}\right) \leq DT \leq \frac{1}{\omega_p}\sin^{-1}\left(\frac{nV_{dc}}{\omega_p L_{lk} I_a}\right) + \frac{\sqrt{(\omega_p L_{lk} I_a)^2 - (nV_{dc})^2}}{n\omega_p V_{dc}} \end{aligned} \tag{B.1}$$

Let us consider $R = \frac{nV_{dc}}{I_a}$, $R_o = \sqrt{\frac{L_{lk}}{2C_s}}$, $x = \frac{R}{R_o} = \frac{nV_{dc}}{\omega_p L_{lk} I_a}$ where $\omega_p = \frac{1}{\sqrt{2C_s L_{lk}}}$. The condition in (B.1) can be rewritten as in (B.2)

$$\sin^{-1} x \leq \omega_p DT \leq \left(\sin^{-1} x + \frac{\sqrt{1-x^2}}{x}\right) \tag{B.2}$$

Where $0 < x \leq 1$. For $x > 1$, i.e. $nV_{dc} > \omega_p L_{lk} I_a$, soft-switching can not be ensured as discussed in Sub-mode I of subsection 2.3.3 of chapter 2. The limits of $\omega_p DT$ with variation of load current magnitude I_a are shown in Fig. B.1. The range to achieve ZVS with variation

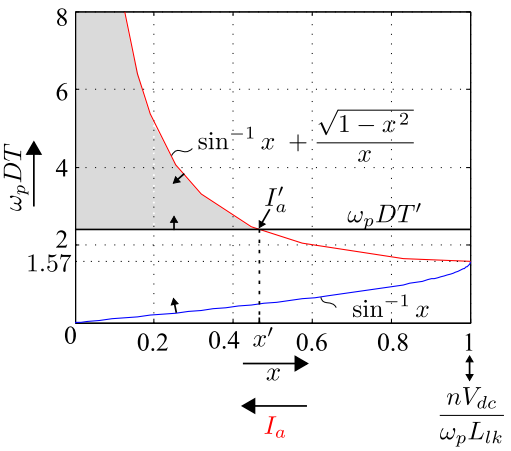


Figure B.1: The variation of limits on dead time with I_a during zero to active state transition

of I_a is maximum when $\omega_p DT = 1.57$. DT' is the minimum required dead time for a given device technology. Hence the shaded area in Fig. B.1 is the actual operating zone to achieve ZVS turn ON. For a given choice of dead time, DT', corresponding x' and I'_a (see Fig. B.1) can be found by solving (B.3). I'_a is the minimum current magnitude for which ZVS turn ON can be ensured.

$$\begin{aligned} \omega_p DT' &= \left(\sin^{-1} x' + \frac{\sqrt{1-x'^2}}{x'} \right) \\ I'_a &= \frac{nV_{dc}}{\omega_p L_{lk} x'} \end{aligned} \tag{B.3}$$

As discussed in chapter 2, and seen above, the soft-switching of the DSC switches depends

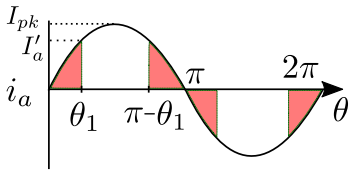


Figure B.2: Shaded area showing hard-switching region of DSC switches over a line cycle

on the current magnitude (I_a) (see equations (2.14) and (2.22)). Again the current magnitude varies sinusoidally over a line cycle. Near zero crossing of the line current, I_a is small which results in hard-switching of the DSC. The range of soft turn ON of $S_{A1} - S_{A4}$ over one half of line cycle is indicated as $(\theta_1, \pi - \theta_1)$, as shown in Fig. B.2. The shaded region indicates hard turn ON zone of the DSC over a line cycle for a given load. For a given dead time DT', θ_1 of switch pair $S_{A1} - S_{A2}$ can be given as in (B.4).

$$\theta_{1,S_{A1,2}} = \sin^{-1}\left(\frac{I'_a}{I_{pk}}\right) \tag{B.4}$$

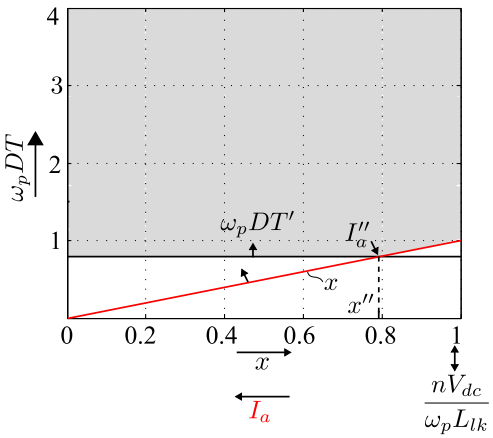


Figure B.3: The variation of $\omega_p DT$ with I_a to ensure ZVS during active to zero state transition

B.2 Limits on dead time during active to zero state transition

To achieve ZVS turn ON of the incoming switch during active to zero state transition, the limit on dead time is given in (2.14). The limit is further given as

$$\begin{aligned} DT &\geq \frac{nC_T V_{dc}}{I_a} \\ \Rightarrow \omega_p DT &\geq x \end{aligned} \tag{B.5}$$

The plot of $\omega_p DT$ with variation of load current magnitude I_a are shown in Fig. B.3. DT' is the device technology imposed minimum required dead time. With this given dead time, actual range of ZVS is the shaded area shown in Fig. B.5. For the given choice of dead time, DT', corresponding x'' and I_a'' (see Fig. B.3) can be found by solving (B.6). I_a'' is the minimum current magnitude for which ZVS turn ON can be ensured.

$$\begin{aligned} x'' &= \omega_p DT' \\ I_a'' &= \frac{nV_{dc}}{\omega_p L_{lk} x''} \end{aligned} \tag{B.6}$$

θ_1 for the leg $S_{A3} - S_{A4}$ can be given as in (B.7).

$$\theta_{1,S_{A3,4}} = \sin^{-1}\left(\frac{I_a''}{I_{pk}}\right) \tag{B.7}$$

Appendix C

Design of unidirectional multi-stage topology

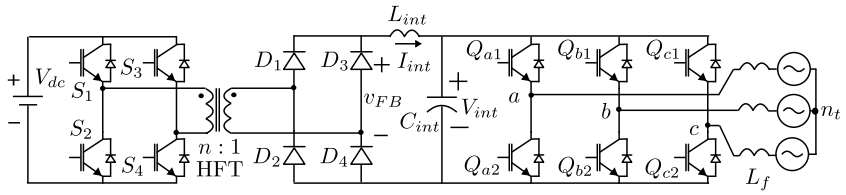


Figure C.1: Conventional unidirectional multi-stage HFL topology

The unidirectional multi-stage high frequency link inverter is shown in Fig. C.1. As seen from the figure the converter has two stages- a unidirectional DC-DC converter (phase-shifted full-bridge (PSFB)) followed by a three-phase voltage source inverter. Inter stage DC link voltage is fixed as filter capacitor is employed. We have designed the topology for a target application of grid integration of utility scale solar photo-voltaic. The specification of the design is given in Table 6.1.

To be consistent, for the multi-stage solution, we have operated both the DC-DC and the three-phase inverter near 85% of their respective maximum voltage transfer ratio. The DC-DC converter is modulated as phase-shifted full bridge (PSFB) converter so that the four active switches in the DC side full-bridge is fully soft-switched, [46]. The three-phase inverter is modulated with standard conventional space vector PWM (CSVPWM) [47]. The intermediate DC link voltage (V_{int}) is maintained at 680 V. v_{FB} is the PSFB diode bridge output voltage. The PSFB duty ratio $D = \dfrac{nV_{int}}{V_{dc}} = 0.85$. Hence, the HFT turns ratio (n) is 1. The modulation index of 3ϕ VSI is $M = \dfrac{\sqrt{3}V_{pk}}{V_{int}} = 0.864$.

C.1 Device blocking voltage and RMS current

Fig.C.1 shows the multi-stage topology. For the UPF operation following equations can be written.

$$\begin{aligned} P &= \frac{3}{2}V_{pk}I_{pk} = V_{dc}I_{dc} = V_{int}I_{int} \\ V_{int} &= D\frac{V_{dc}}{n} \\ V_{pk} &= \frac{MV_{int}}{\sqrt{3}} \end{aligned} \tag{C.1}$$

Where V_{int} and I_{int} are intermediate DC link voltage and DC link current as shown in Fig. C.1. Ripples in V_{int} and I_{int} are considered negligible due to proper filtering.
Using (C.1), $\frac{I_{int}}{n} = \frac{P}{DV_{dc}}$. RMS current in DSC switches $S_1 - S_2$ is given as follows.

$$I_{RMS,S_1-S_2} = \frac{I_{int}}{\sqrt{2}n} = \frac{1}{\sqrt{2D}}\frac{P}{V_{dc}} \tag{C.2}$$

For $D = 0.85$, $I_{RMS,S_1-S_2} = 0.83\frac{P}{V_{dc}}$. The RMS current of $S_3 - S_4$ is given by-

$$I_{RMS,S_3-S_4} = \frac{\sqrt{D}I_{int}}{\sqrt{2}n} = \frac{1}{\sqrt{2D}}\frac{P}{V_{dc}} \tag{C.3}$$

For $D = 0.85$, $I_{RMS,S_3-S_4} = 0.77\frac{P}{V_{dc}}$. Peak current of DSC switches is $I_{pk,S_1-S_4} = \frac{I_{int}}{n} = \frac{1}{D}\frac{P}{V_{dc}}$. With $D = 0.85$, $I_{pk,S_1-S_4} = 1.2\frac{P}{V_{dc}}$. Blocking voltage of DC side devices is V_{dc}.
Using (C.1), $I_{int} = \frac{MP}{\sqrt{3}V_{pk}}$. The RMS current of the ASC diodes is expressed as-

$$I_{RMS,D_1-D_4} = \frac{I_{int}}{\sqrt{2}} = \frac{M}{\sqrt{6}}\frac{P}{V_{pk}} \tag{C.4}$$

The peak current of diodes is $I_{pk,D_1-D_4} = I_{int} = \frac{MP}{\sqrt{3}V_{pk}}$. For $M = 0.864$, $I_{RMS,D_1-D_4} = 0.353\frac{P}{V_{pk}}$ and $I_{pk,D_1-D_4} = 0.5\frac{P}{V_{pk}}$. The blocking voltage of the diodes is $\frac{V_{dc}}{n} = \frac{\sqrt{3}}{MD}V_{pk}$. With $M = 0.864$, Blocking voltage of the diodes is given as $2.36V_{pk}$.
The RMS current of the ASC switches are given as-

$$I_{RMS,Q_{a1}-Q_{c2}} = I_{pk}\sqrt{\left[\frac{1}{8} + \frac{M}{\sqrt{3}\pi} - \frac{10M}{48\pi}\right]} = 0.67\sqrt{\left[\frac{1}{8} + \frac{M}{\sqrt{3}\pi} - \frac{10M}{48\pi}\right]}\frac{P}{V_{pk}} \tag{C.5}$$

With $M = 0.864$, $I_{RMS,Q_{a1}-Q_{c2}} = 0.32\frac{P}{V_{pk}}$. Peak current through secondary switches is $I_{pk,Q_{a1}-Q_{c2}} = I_{pk} = 0.67\frac{P}{V_{pk}}$. The blocking voltage of secondary switches $V_{int} = \frac{\sqrt{3}}{M}V_{pk}$. With $M = 0.864$, blocking voltage is $V_{int} = 2V_{pk}$.

C.2 Estimation of Converter Power Loss

The conduction loss in switch pair $S_1 - S_2$ is given as-

$$P_{C_{S_1}} = 0.5\left(V_{CE}\left(\frac{I_{int}}{n}\right) + R_{CE}\left(\frac{I_{int}}{n}\right)^2\right) \tag{C.6}$$

The conduction loss of switches $S_3 - S_4$ are given as-

$$P_{C_{S_3}} = 0.5D\left(V_{CE}\left(\frac{I_{int}}{n}\right) + R_{CE}\left(\frac{I_{int}}{n}\right)^2\right) \tag{C.7}$$

The conduction loss expression of anti-parallel diodes of switch pairs $S_3 - S_4$ is given by-

$$P_{C_{D,S_3}} = 0.5(1-D)\left(V_D\left(\frac{I_{int}}{n}\right) + R_D\left(\frac{I_{int}}{n}\right)^2\right) \tag{C.8}$$

The conduction loss in a secondary diode of $D_1 - D4$ is given expressed as-

$$P_{C_{D_1}} = 0.5\left(V_D I_{int} + R_D {I_{int}}^2\right) \tag{C.9}$$

In ASC, the conduction loss of each IGBT switch of the CSVPWM modulated 3ϕ VSI operated at UPF is given as-

$$P_{C_{Q_1}} = V_{CE} I_{pk}\left(\frac{1}{2\pi} + \frac{M}{4\sqrt{3}} + \frac{(\sqrt{3}-1)M}{32\sqrt{3}\pi}\right) + I_{pk}^2 R_{CE}\left(\frac{1}{8} + \frac{M}{\sqrt{3}\pi} - \frac{10M}{48\pi}\right) \tag{C.10}$$

The conduction loss of anti-parallel diodes of $Q_{a1} - Q_{c2}$ is expressed as-

$$P_{C_{D_{Q_{a1}}}} = V_D I_{pk}\left(\frac{1}{2\pi} - \frac{M}{4\sqrt{3}} - \frac{(\sqrt{3}-1)M}{32\sqrt{3}\pi}\right) + I_{pk}^2 R_D\left(\frac{1}{8} - \frac{M}{\sqrt{3}\pi} + \frac{10M}{48\pi}\right) \tag{C.11}$$

The 3ϕ VSI of ASC is hard-switched. The switching loss of a switch (say Q_{a1}) is given as-

$$P_{S_{Q_{a1}}} = \frac{\sqrt{3}V_{pk}I_{pk}f_s}{\pi M}\left(\frac{E_{ON_R} + E_{OFF_R}}{V_{CC}I_C}\right) \tag{C.12}$$

C.3 Design of high frequency transformers

C.3.1 Winding RMS currents

The RMS current of HFT primary winding is $I_{RMS,p} = \frac{I_{int}}{n} = \frac{1}{D}\frac{P}{V_{dc}}$. For $D = 0.85$, $I_{RMS,p} = 1.2\frac{P}{V_{dc}}$. The RMS current of HFT secondary winding is $I_{RMS,s} = I_{int} = \frac{M}{\sqrt{3}}\frac{P}{V_{pk}}$. For $M = 0.864$, $I_{RMS,s} = 0.5\frac{P}{V_{dc}}$.

C.3.2 Area product of the HFT used in multi-stage topology

In multi-stage topology, one 2 winding HFT is used as shown in Fig. C.1. The applied HFT primary voltage (e_1) is wave with magnitude V_{dc}. The duty cycle $D = 0.85$. The peak-peak

flux is estimated as follows.

$$\Phi_{pk-pk,max} = \frac{1}{N_1}\int_0^{\frac{DT_s}{2}} e_1 dt = \frac{DV_{dc}T_s}{2N_1} \tag{C.13}$$

Where N_1 and N_2 are HFT primary and secondary turns. The peak flux density (B_{max}) is related to $\Phi_{pk-pk,max}$ through HFT core area A_c.

$$A_c B_{max} = \frac{\Phi_{pk-pk,max}}{2} = \frac{DV_{dc}}{4N_1 f_s} \tag{C.14}$$

The switching frequency $f_s = \frac{1}{T_s}$. HFT window area (A_w) is estimated as follows.

$$A_w K_w = \frac{N_1 I_{RMS,p}}{J} + \frac{N_2 I_{RMS,s}}{J} = \frac{2N_1 I_{RMS,p}}{J} \tag{C.15}$$

where K_w is the window fill factor and J is the current density. The RMS current of HFT primary winding is $I_{RMS,p} = \frac{I_{int}}{n} = \frac{1}{D}\frac{P}{V_{dc}}$.

The product of window and core area is estimated as follows.

$$A_c A_w = \frac{DV_{dc}}{4N_1 f_s B_{max}} \frac{2N_1 I_{RMS,p}}{JK_w} = 0.5\frac{P}{K_w J B_{max} f_s} \tag{C.16}$$

C.4 Input and Output Filter Requirement of the Converter

Input current THD is given as-

$$THD_I = \frac{\sqrt{D(1-D)}}{D} \tag{C.17}$$

For $D = 0.85$, $THD_I = 0.42$

Intermediate DC link voltage THD is given as

$$THD_{V_{int}} = \frac{\sqrt{D(1-D)}}{D} \tag{C.18}$$

For $D = 0.85$, $THD_{V_{int}} = 0.42$

Intermediate DC link current THD (due to 3ϕ VSI) is given as

$$THD_{I_{int}} = \frac{\sqrt{2M\left[\frac{1}{\pi} + \left(\frac{4}{\pi} - \frac{3}{2}M\right)\right]}}{\sqrt{3}M} \tag{C.19}$$

For $M = 0.864$, $THD_{V_{int}} = 0.48$

Output Voltage THD is given as-

$$THD_V = \frac{1}{M}\sqrt{\left[\frac{4M}{\pi} - M^2\right]} \tag{C.20}$$

For $M = 0.864$, $THD_V = 0.69$

List of Publications

Publications from the Thesis Work

Journal Publications:

J1. Anirban Pal, Kaushik Basu, "A PWM ZVS High-Frequency-Link Three-Phase Inverter with T-type NPC Unfolder", in *IEEE Transactions on Industrial Electronics*, vol. PP, no. 99, pp. 1-1, DOI 10.1109/TIE.2019.2942540.

J2. Anirban Pal, Kaushik Basu, "A Single-Stage Soft-Switched Isolated Three-Phase DC-AC Converter with Three-Phase Unfolder", in *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1-1, DOI: 10.1109/TPEL.2019.2935875.

J3. Anirban Pal, Kaushik Basu, "A Soft-switched High Frequency link Single-Stage Three-Phase Inverter for Grid Integration of Utility Scale Renewables", in *IEEE Transactions on Power Electronics*, vol. 34, no. 9, pp. 8513-8527, Sept. 2019.

J4. Anirban Pal, Kaushik Basu, "A Unidirectional Single-Stage Three-Phase Soft-switched Isolated DC-AC Converter", in *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1142-1158, Feb. 2019.

Conference Publications:

C1. Anirban Pal, Kaushik Basu, "A Zero-Current-Switched PWM Full Bridge DC-DC Converter", in *Proc. IEEE Energy Conversion Conference and Exposition (ECCE)*, 2019.

C2. Manmohan Mahapatra, Anirban Pal, Kaushik Basu, "Soft Switched Multilevel Unidirectional High Frequency Link DC/AC converter for Medium Voltage Grid Integration", in *Proc. IEEE International Conference on Industrial Electronics for Sustainable Energy Systems (IESES)*, 2018.

C3. Anirban Pal, Kaushik Basu, "A Novel Modulation Strategy for Active Rectification of a Snubber Less Soft-switched Single Stage 3ϕ High Frequency Link DC-AC Converter", in *Proc. IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, 2017.

C4. Anirban Pal, Kaushik Basu, "A Unidirectional Soft-switched Isolated Three Level Inverter for Grid Integration of Renewable Energy Sources", in *Proc. IEEE International Conference on Signal Processing, Informatics, Communication and Energy Systems (SPICES)*, 2017.

C5. Anirban Pal, Kaushik Basu, "A Unidirectional Snubber Less Fully Soft-switched Single Stage Three Phase High Frequency Link DC/AC Converter", in *Proc. IEEE International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017-ECCE Asia)*, 2017.

C6. Anirban Pal, Kaushik Basu, "A Unidirectional Snubber Less Partially Soft-switched High Frequency Link Three Phase Inverter", in *Proc. IEEE Applied Power Electronic Conference (APEC)*, 2017.

C7. Anirban Pal, Kaushik Basu, "A Bidirectional Snubber Less Soft-switched High Frequency Link DC/AC Converter", in *Proc. IEEE India International Conference on Power Electronics (IICPE)*, 2016.

C8. Anirban Pal, Kaushik Basu, "A Partially Soft-switched DC/AC High Frequency Link Unidirectional Converter for Medium Voltage Grid Integration", in *Proc. National Power Electronic Conference (NPEC)*, 2015.

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