# Hardware Emulation of a Long Transmission Line by High Frequency Power Electronic Converter for the study of Switching Transients

A Thesis

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By

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Dedicated

To my

Father Shri. Anadi Mazumdar

and

Mother Smt. Mana Mazumdar

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# Abstract

To ensure smooth functioning of the grid, the reliability and robustness of the power system equipment needs to be precisely evaluated during their development process. But direct on-field tests of most of the equipment are not possible. This urges for having an emulated environment which will operate in real-time thereby capturing all the physical phenomenon of the Hardware Under Test (HUT). The control and protection equipments are generally tested by Hardware-In-The-Loop (HIL) technology, where a Real-Time Simulator (RTS) implemented on a digital platform, interacts with the HUT in real-time. Also high power rating devices can be tested by adopting a different technology known as Power-Hardware-In-The-Loop (PHIL), where a Power Amplifier (PA) acts as the interface between the RTS and HUT. The most expensive component of the PHIL is the general purpose RTS like Opal-RT or RTDS. To reduce the cost, RTS can be made application specific. This Application Specific-Real-Time Simulator (AS-RTS) and the PA collectively simulating the test environment for the HUT is termed as the Hardware Emulator (HE) of that particular application. Being the fundamental component of the power system, HE of transmission line is required to bridge the gap between the source and load emulators. Hence a programmable type of Transmission Line hardware Emulator (TLE) needs to be developed which will have the flexibility of emulating transmission line with varying line parameters. The general architecture of a TLE comprises of two major components, namely, Observer and Power Amplifier, where the AS-RTS for the TLE is termed as the Observer. With the line end voltages as the input, the Observer solves the emulated line model in real-time and estimates the line end currents which are then tracked by the PA by controlling its output currents. Utilizing the flexibility of controlling power electronic converters, the PA is comprised of two back-to-back $3\phi$ Voltage Source Converters (VSCs) operating under closed loop current control mode. Based on similar architecture, emulation for short lines during steady state and $3\phi$ short-circuit faults are reported in literature, where the transmission line is modeled as a lumped resistor in series with a lumped inductor. For analyzing the performance of the grid at the transmission level, it becomes necessary to consider long lines. Emulation of a distributed parameter lossy transmission line during steady state and $3\phi$ faults using Method of Characteristics (MOC) has also been performed. However with MOC, the computational burden of the Observer significantly increases.

Hardware emulation of energization of a long transmission line is not addressed in either of the previous work. Simultaneous switching of all the phases of one end of the transmission line with a shunt reactor connected at the other end has been studied in this work and the transients in the source end line currents during the instant of switching has been emulated by the developed TLE. When an unenergized transmission line is suddenly connected to a voltage source, high frequency transients appear in the line currents due to the travelling wave phenomenon before the attainment of steady state. After studying different line models for lossy long lines, a travelling wave based numerical solution is identified which can be solved by the Observer in real-time. The Observer is implemented on a Zynq System-On-Chip (SoC) platform from Xilinx. As the transient current contains high frequency components, the switching frequency of the VSC should be sufficiently high in order to minimize the phase loss of the current control loop of the PA. So a Silicon Carbide (SiC) based power electronic converter has been designed and fabricated to implement the PA of the TLE. A comprehensive analysis has been made to choose the switching frequency of the power electronic converter and the sampling frequency of the Observer, while adhering to the power and digital hardware constraints (maximum switching frequency limit, clock speed, etc.). Further, the hardware topology for the implementation of the TLE as well as scaling of the actual transmission line to laboratory level emulator without compromising on the system dynamics has been presented. Finally the relevant simulation waveforms are matched with the experimental results performed on the developed hardware prototype of the TLE, thus validating the TLE test bench setup.

# Contents

# List of Abbreviations

| | | |
|---|---|---|
| TNA | : | Transient Network Analyzer |
| RTS | : | Real-Time Simulator |
| AS-RTS | : | Application Specific-Real-Time Simulator |
| C-HUT | : | Control-Hardware Under Test |
| HIL | : | Hardware-In-The-Loop |
| PHIL | : | Power-Hardware-In-The-Loop |
| PA | : | Power Amplifier |
| P-HUT | : | Power-Hardware Under Test |
| HE | : | Hardware Emulator |
| TLE | : | Transmission Line Emulator |
| VSC | : | Voltage Source Converter |
| MOC | : | Method of Characteristics |
| AFEC | : | Active Front End Converter |
| FDM | : | Frequency Dependent Model |
| ZOH | : | Zero Order Hold |
| PS | : | Processing System |
| SRF | : | Synchronous Reference Frame |
| SRF-PLL | : | Synchronous Reference Frame-Phase Lock Loop |
| PI | : | Proportional Integral |
| PR | : | Proportional Resonant |
| RI | : | Resonant Integrator |
| PWM | : | Pulse Width Modulation |
| SiC | : | Silicon Carbide |
| SBD | : | Shottky Barrier Diode |
| FRD | : | Fast Recovery Diode |
| CSVPWM | : | Conventional Space Vector Pulse Width Modulation |
| PCB | : | Printed Circuit Board |

# List of Symbols

| | | |
|---|---|---|
| $V_{LL(RMS)}$ | : | $3\phi$ Line-Line (RMS) voltage of the sending end grid of actual transmission system |
| $V'_{LL(RMS)}$ | : | $3\phi$ Line-Line (RMS) voltage of the sending end grid of the emulated system |
| $S_{3\phi}$ | : | Apparent power rating of the original system |
| $l$ | : | Length of the transmission line |
| $c_{TL}$ | : | Wave velocity in the transmission line |
| $\tau$ | : | Wave travel time in the transmission line |
| $L$ | : | Line inductance per unit length of actual transmission line system |
| $C$ | : | Line capacitance per unit length of actual transmission line system |
| $R$ | : | Line resistance per unit length of actual transmission line system |
| $L_{sh}$ | : | Shunt reactor inductance of actual transmission line system |
| $Z_g$ | : | Grid impedance of actual transmission line system |
| $L_g$ | : | Grid inductance of actual transmission line system |
| $Z_c$ | : | Characteristic impedance of actual transmission line |
| $L'$ | : | Line inductance per unit length of scaled down emulated system |
| $C'$ | : | Line capacitance per unit length of scaled down emulated system |
| $R'$ | : | Line resistance per unit length of scaled down emulated system |
| $L'_{sh}$ | : | Shunt reactor inductance of scaled down emulated system |
| $Z'_g$ | : | Grid impedance of scaled down emulated system |
| $L'_g$ | : | Grid inductance of scaled down emulated system |
| $v_{seg(J)}$ | : | Phase to neutral voltage of the sending end grid |
| $v_{se(J)}$ | : | Phase to neutral voltage of the sending end of the transmission line |
| $v_{re(J)}$ | : | Phase to neutral voltage of the receiving end of the transmission line |
| $i_{se(J)}$ | : | Line current injected into the sending end of the transmision line |
| $i_{re(J)}$ | : | Line current injected into the receiving end of the transmision line |
| $i^{**}_{se(J)}$ | : | Observer generated value of sending end line current |
| $i^{**}_{re(J)}$ | : | Observer generated value of receiving end line current |
| $i^{*}_{se(J)}$ | : | Reference value of sending end line current to be tracked by the VSC |
| $T_{ob}$ | : | Sampling time period of the Observer |
| $T_{obc}$ | : | Computational time period of the Observer |
| $N$ | : | Size of the FIFO buffers used in the Observer |
| $T_{clk(PS)}$ | : | Instruction clock period of the PS |
| $F_{i(max)}$ | : | Maximum frequency content of the line end currents at the instant of switching |

| | | |
|---|---|---|
| $T_{sw}$ | : | Switching time period of the power electronic converter |
| $F_{c(aa)}$ | : | Cut-off frequency of the anti-aliasing filter |
| $S_{rated}$ | : | Apparent power rating of the SiC based power electronic converter |
| $P_{rated}$ | : | Active power rating of the SiC based power electronic converter |
| $F_{sw}$ | : | Switching frequency of the power electronic converter |
| $V_{DC}$ | : | DC bus voltage rating of the converter |
| $F_{line}$ | : | Line frequency of the grid |
| $Z_{(B)}$ | : | Base impedance of the actual transmission line system |
| $I_{(B)}$ | : | Base current of the actual transmission line system |
| $Z'_{(B)}$ | : | Base impedance of the scaled down emulated sytem |
| $I'_{(B)}$ | : | Base current of the scaled down emulated system |
| $L_f$ | : | Line filter inductance |
| $R_f$ | : | Line filter resistance |
| $\omega_{gc}$ | : | Gain cross-over frequency |
| $K_{pr}$ | : | Proportional gain of the PR controller of the PA of TLE |
| $K_{ir}$ | : | Resonant gain of the PR controller of the PA of TLE |
| $C_{snb}$ | : | DC link snubber capacitance of the power electronic converter |
| $M$ | : | Modulation index of the power electronic converter |
| $\phi$ | : | Load power factor angle |
| $r_{DS(+)}$ | : | Positive channel resistance of the SiC MOSFET |
| $r_{DS(-)}$ | : | Negative channel resistance of the SiC MOSFET |
| $T_s$ | : | Subcycle duration of CSVPWM |
| $v_{gs}$ | : | Gate to source voltage of the SiC MOSFET |
| $v_{ds}$ | : | Drain to source voltage of the SiC MOSFET |
| $C_{gs}$ | : | Gate to source capacitance of the SiC MOSFET |
| $C_{ds}$ | : | Drain to source capacitance of the SiC MOSFET |
| $V_{Th}$ | : | Threshold voltage of the SiC MOSFET |
| $V_M$ | : | Miller plateau voltage of the SiC MOSFET |
| $R_{gint}$ | : | Internal gate resistance of the SiC MOSFET |
| $B_{pk}$ | : | Peak flux density in the filter inductor |
| $I_{L_f(rms)}$ | : | RMS current rating of the filter inductor |
| $I_{L_f(pk)}$ | : | Peak current rating of the filter inductor |
| $I_{Gpk(TurnOn)}$ | : | Peak value of gate current during turn on of the MOSFET |
| $I_{Gpk(TurnOff)}$ | : | Peak value of gate current during turn off of the MOSFET |
| $K_p^{PLL}$ | : | Proportional gain of the PI controller of the SRF-PLL |
| $K_i^{PLL}$ | : | Integral gain of the PI controller of the SRF-PLL |
| $K_p^{CC}$ | : | Proportional gain of the current controller of the AFEC |
| $K_i^{CC}$ | : | Integral gain of the current controller of the AFEC |
| $K_p^{VC}$ | : | Proportional gain of the voltage controller of the AFEC |
| $K_i^{VC}$ | : | Integral gain of the voltage controller of the AFEC |

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# Chapter 1

# Introduction

## 1.1 Thesis Objective

Due to the risks involved, direct on-field tests of the power generation and the transmission equipments are not always possible. Also in many cases, the test environment may not be available. Therefore to address this problem, one needs to depend on simulation, which fails to capture all the physical phenomenon of the Hardware Under Test (HUT) in real-time. Hardware emulation is a solution to this problem. With an increase in the number of sophisticated devices getting connected to the power grid for integration of renewable sources, hardware emulation of transmission line becomes necessary to ensure smooth functioning and reliability of the grid. The objective of this work is to develop a hardware emulator of a long transmission line which will mimic its terminal characteristics both during the transient as well as steady state operation.

## 1.2 Motivation

Analog simulators like Transient Network Analyzer (TNA) [1] using scaled down power system components is one of the traditional way to simulate the network under test. In digital computers, the transient phenomenon is simulated by the mathematical representation of the system dynamics [2–4]. Even though the parameters of the system under study can be easily modified, digital simulation cannot be used for testing of control and protection equipment as it operates in non-real-time.

### 1.2.1 Hardware Emulation

With the advent of high speed computing, today digital simulators like Opal-RT, Typhoon-HIL and RTDS are available which can operate in real-time. This digital platform is termed as Real-Time Simulator (RTS). As shown in Fig. 1.1, the combination of RTS and the Control-Hardware Under Test (C-HUT) is generally known as

Hardware-In-The-Loop (HIL) technology [5–7]. The output quantities delivered by the C-HUT are captured and processed by the RTS in accordance to a mathematical model representing the emulated environment. Consequently the signals generated by the RTS is fed to the C-HUT as the inputs. Since the tests are performed in real-time, the obtained results can thus be used in design and development of the control equipment.

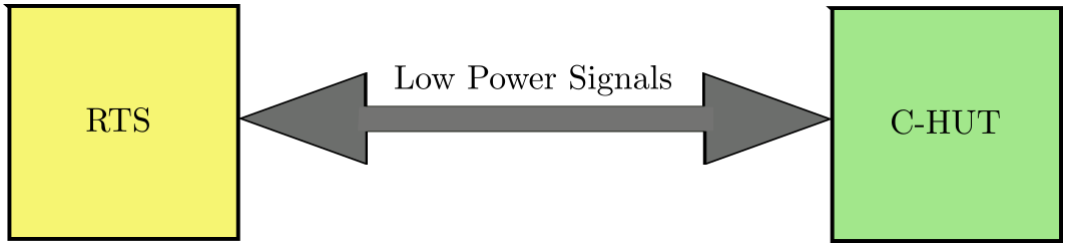


Figure 1.1: Schematic of a HIL System

Apart from testing of controllers like protection relays, generator exciter control system or controllers of a power electronic converter by HIL technology, power level apparatus can also be tested by adopting Power-Hardware-In-The-Loop (PHIL) technology. As shown in Fig. 1.2, PHIL includes a Power Amplifier (PA) as the interface between the RTS and the Power-Hardware Under Test (P-HUT), thus making energy transfer feasible. For these reasons, PHIL provide an effective means to evaluate the performance of the P-HUT, thereby reducing the risk of simulation inexactness.

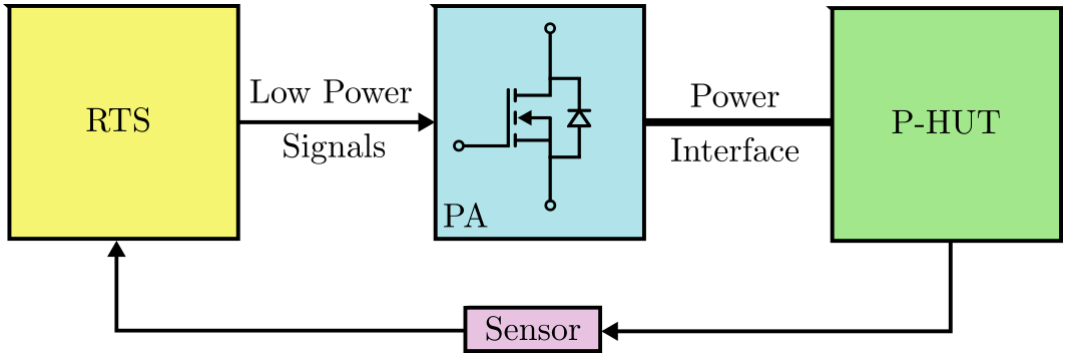


Figure 1.2: Schematic of a PHIL System

Photovoltaic inverter system has been emulated in [8] to study the impact of the solar energy sources in the power grid. PHIL emulation of variable speed wind turbine using doubly fed induction generator and permanent magnet synchronous machine is done in [9]. Various kind of faults in a grid has been emulated in [10]. Again testing of microgrids by PHIL technology is reported in [11, 12]. In [13, 14] a synchronous

generator emulator has been developed for power system testing. Similarly emulation of electrical load in real-time using PHIL technology has been reported in [15–17].

All these platforms focus on testing only one device or a small microgrid with a few buses, thus replacing the expensive RTS by an application specific digital processor inside an embedded platform. The block diagram schematic of this particular type of PHIL is shown in Fig. 1.3, where AS-RTS stands for the Application Specific-Real-Time Simulator. Here the AS-RTS and PA collectively emulating the test environment for the P-HUT is termed as the Hardware Emulator (HE). These HEs helped in replacing the physically unavailable equipment by creating a similar test condition through a user-friendly interface.

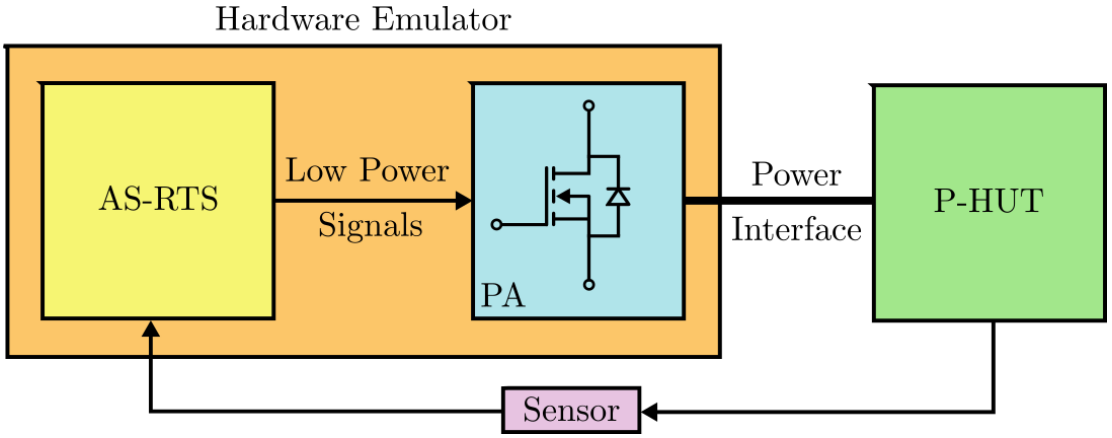


Figure 1.3: Schematic of a Hardware Emulator

### 1.2.2 Hardware Emulation of Transmission Line

Being the fundamental element of the power system, HE for transmission line is required to bridge the gap between the source (synchronous generator) and load emulators. Hence a programmable type of Transmission Line Emulator (TLE) needs to be developed which will have the flexibility of emulating transmission line with varying line parameters.

The general architecture of a TLE is shown in Fig. 1.4. The two major components of this setup is the Observer and the Power Amplifier. *The AS-RTS for the TLE is termed as Observer in this thesis. With the line end voltages ($v_{se(J)}$ and $v_{re(J)}$) as the input, the Observer solves the emulated line model in real-time and estimate the line end currents. These currents ($i^*_{se(J)}$ and $i^*_{re(J)}$) are then tracked by the PA by controlling its output currents.* The PA is comprised of two back-to-back $3\phi$ Voltage Source Converters (VSCs) operating under closed loop current control mode.

### Literature Survey

Based on similar architecture, emulation of short lossless transmission line during steady state has been reported in [18, 19]. The transmission line is modeled as a lumped inductor and is emulated by the VSCs using two approaches, namely, phasor domain model and time domain model. In phasor domain model, the terminal active and reactive powers drawn by the VSCs are controlled to emulate the ac transmission line. While, with the sending and receiving end voltages being known, the current carried by the transmission line is obtained by applying trapezoidal discrete methods in case of the time domain model. The calculated values of the currents are then tracked by the grid connected back-to-back $3\phi$ VSCs.

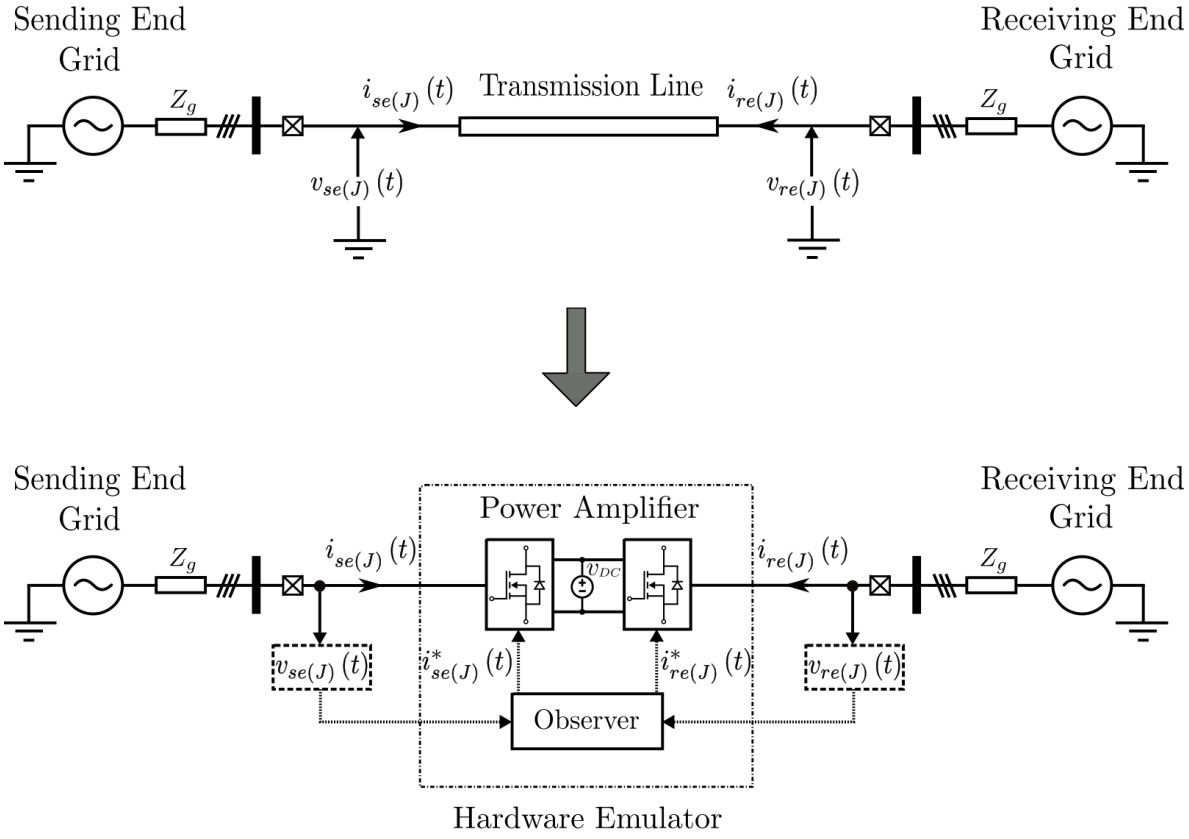


Figure 1.4: General Architecture of a Transmission Line Emulator

Again in [20] power electronic converter based TLE with $3\phi$ short-circuit fault emulation capability has been reported. Under normal operating conditions, the transmission line has been modeled as a single lumped resistor in series with a lumped inductor and during fault condition, two such cascaded sets of resistor and inductor

has been considered, where the junction has been treated as point of the $3\phi$ short-circuit fault. The values of the passive elements were determined by the parameters of the line emulated and also on the location of the fault. Considering the voltage at the point of the fault to be zero, the network is solved by using time domain model. The reference current generated are then tracked by the VSCs.

But for analyzing the performance of the grid at the transmission level, it becomes necessary to consider medium and long lines. In [21], a distributed parameter lossy transmission line has been emulated both during the steady state and $3\phi$ faults. Using Method of Characteristics (MOC), the governing equation (Telegrapher's) of the line is solved in real-time and the reference current generated are tracked by the VSCs. However, the MOC requires solving the line at different sections thus increasing the computational burden on the Observer.

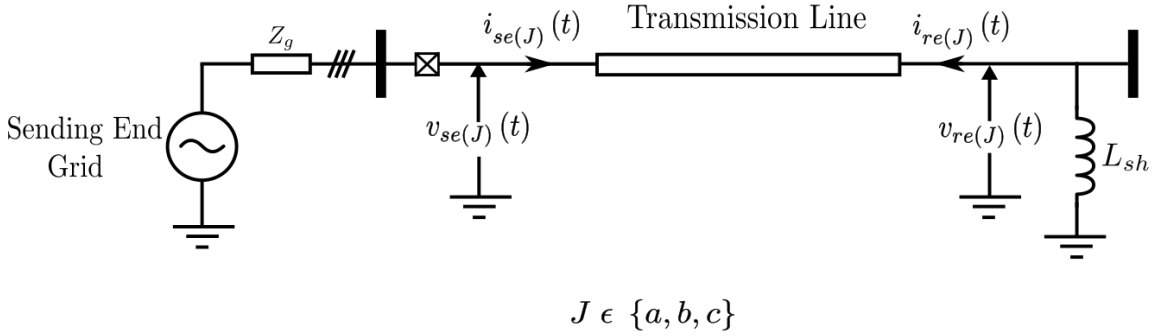


Figure 1.5: Switching of the Sending End of the Transmission Line with a Shunt Reactor placed at the Receiving End

## 1.3 Scope of the Thesis

Hardware emulation of energization of a long transmission line is not addressed in either of the previous work. As shown in Fig. 1.5, simultaneous switching of all the phases of the sending end of the transmission line with a shunt reactor connected at the receiving end has been studied in this work and the transients in the sending end line currents during the instant of switching has been emulated by the developed TLE. When an unenergized transmission line is suddenly connected to a voltage source, high frequency transients appear in the line currents before the attainment of steady state. For effectively capturing the transients, different line models for long lines have been studied and finally a travelling wave based numerical solution is identified which can be solved by the Observer in real-time. Moreover, the closed loop bandwidth of the current controller should be atleast ten times the maximum frequency component of the current to be tracked. Hence it becomes necessary to use wide band gap devices in the PA. So a Silicon Carbide (SiC) based power electronic converter has been

designed and fabricated in the laboratory. After performing a comprehensive analysis, a systematic method is proposed to choose the sampling frequency of the Observer as well as the switching frequency of the power electronic converter depending on the parameters of the emulated line. Further, a scaled hardware for the TLE is developed and tested.

## 1.4 Thesis Organization

The organization of the thesis is as follows : Chapter 2 provides the modelling and the solution of a distributed parameter lossy transmission line suitable for emulating the high frequency current transients. Chapter 3 describes the details of implementation of the real-time Observer in an embedded platform and also provides a methodology to choose the sampling frequency of the Observer and the switching frequency of the power electronic converter. Chapter 4 deals with scaling of the actual transmission line to laboratory level emulator, keeping the dynamics intact and also the hardware topology for the TLE test bench setup. Details of the controller design for the power amplifier has been discussed in Chapter 5. Finally the relevant simulation and experimental results are provided in Chapter 6 followed by conclusion in Chapter 7. Further the detailed design procedure of the SiC based power electronic converter has been provided in Appendix $A$ and the controller design for the Active Front End Converter (AFEC) in Appendix $B$. A quantitative comparison of the computational burden involved with the Bergeron's Model and the Method Of Characteristics for a processor based real-time implementation is provided in Appendix $C$.

# Chapter 2

# Numerical Solution of a Long Transmission Line

The oscillatory components present in the transient waveform can be characterized by their natural frequencies. However in the emulation process, the accurate determination of these oscillations is closely related to the equivalent circuit used to represent the system component. The time frame for switching events varies from micro to milliseconds, as far as insulation coordination is concerned. Therefore no component model is appropriate for all types of transient analysis and must be tailored to the scope of study. In this chapter we will identify a model of the transmission line which can be used to emulate the switching current transients of a long line by a power electronic converter in real time.

## 2.1 Transmission Line Models

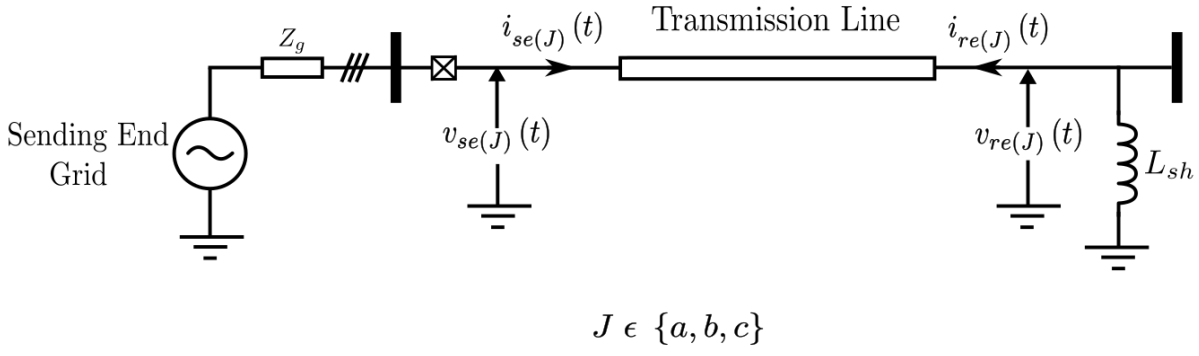


Figure 2.1: Circuit schematic of Voltage Switching of an Unenergized Transmission Line with Shunt Reactor connected at the Receiving End

*Considering Frequency Dependent Model (FDM) of the transmission line as the benchmark model, voltage switching action on the sending end of an actual physical transmission line with a shunt reactor connected on the receiving end, as shown in Fig.* 2.1 *has been simulated in PSCAD using FDM with standard set of parameters [22] given in Table-*2.1. The corresponding waveforms are shown in Fig. 2.2. The subscripts *se* and *re* denotes the sending and receiving end of the transmission line respectively.

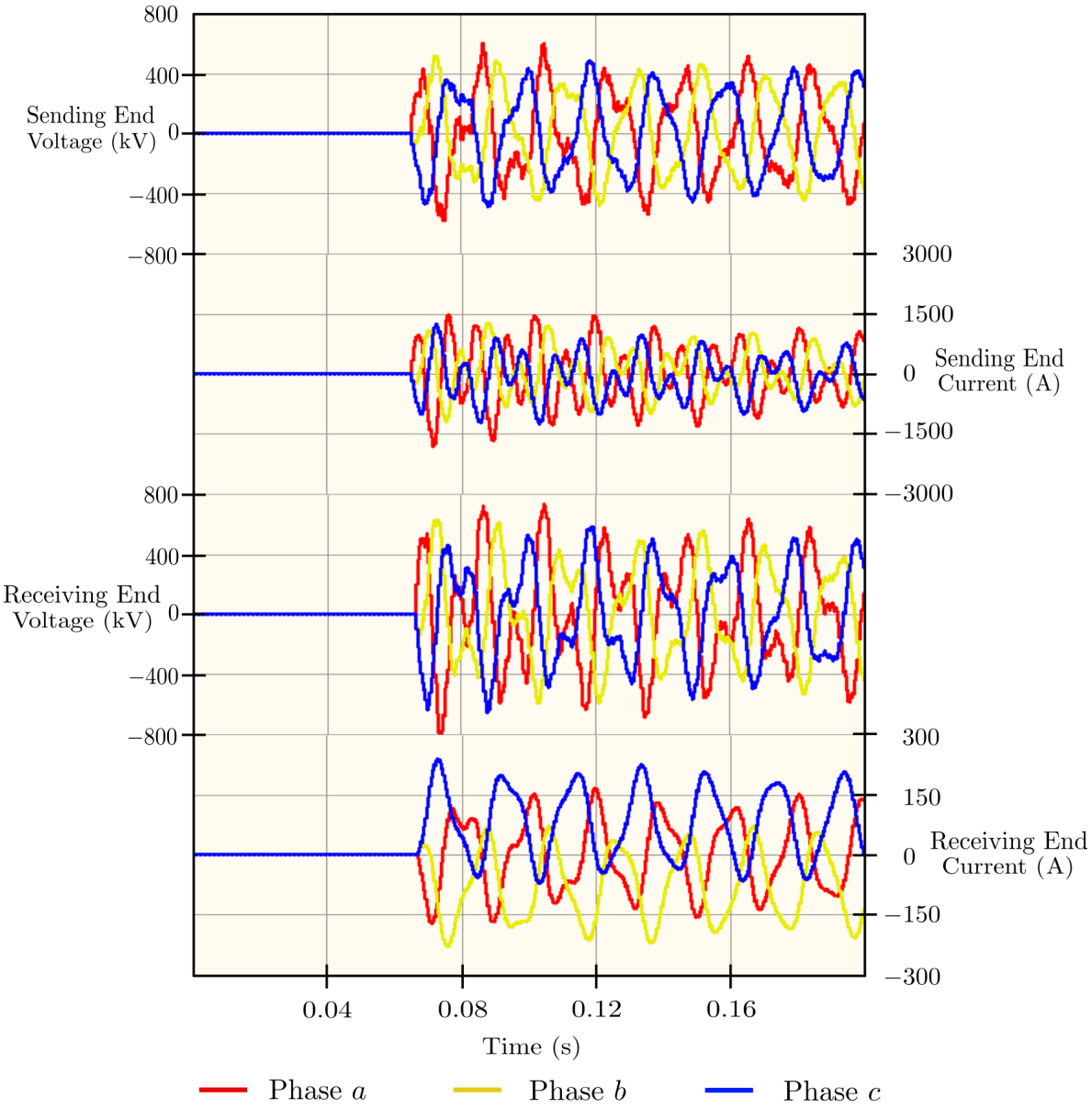


Figure 2.2: Waveforms for the Simulation of the Circuit shown in Fig. 2.1 with the parameters given in Table-2.1 using FDM in PSCAD software

Table 2.1: Parameters of the Actual Transmission Line under consideration

| Sl.No. | Parameter | Value |
|---|---|---|
| 1 | $3\phi$ Line-Line (RMS) voltage of sending end grid, $V_{LL(RMS)}$ | 400 kV |
| 2 | Nominal grid frequency, $F_{line}$ | 50 Hz |
| 3 | Apparent power rating of the system, $S_{3\phi}$ | 500 MVA |
| 4 | Line inductance per unit length, $L$ | 1 mH/km |
| 5 | Line capacitance per unit length, $C$ | 12.96 nF/km |
| 6 | Line resistance per unit length, $R$ | 0.03 Ω/km |
| 7 | Line length, $l$ | 400 km |
| 8 | Shunt reactor inductance, $L_{sh}$ | 10.2 H |
| 9 | Grid impedance (Inductive), $Z_g$ | 80 Ω |
| 10 | Grid inductance, $L_g = \frac{Z_g}{2*\pi*F_{line}}$ | 0.25 H |
| 11 | Switching instant | Positive peak of $a$ phase voltage |

### 2.1.1 Lumped Impedance based Models

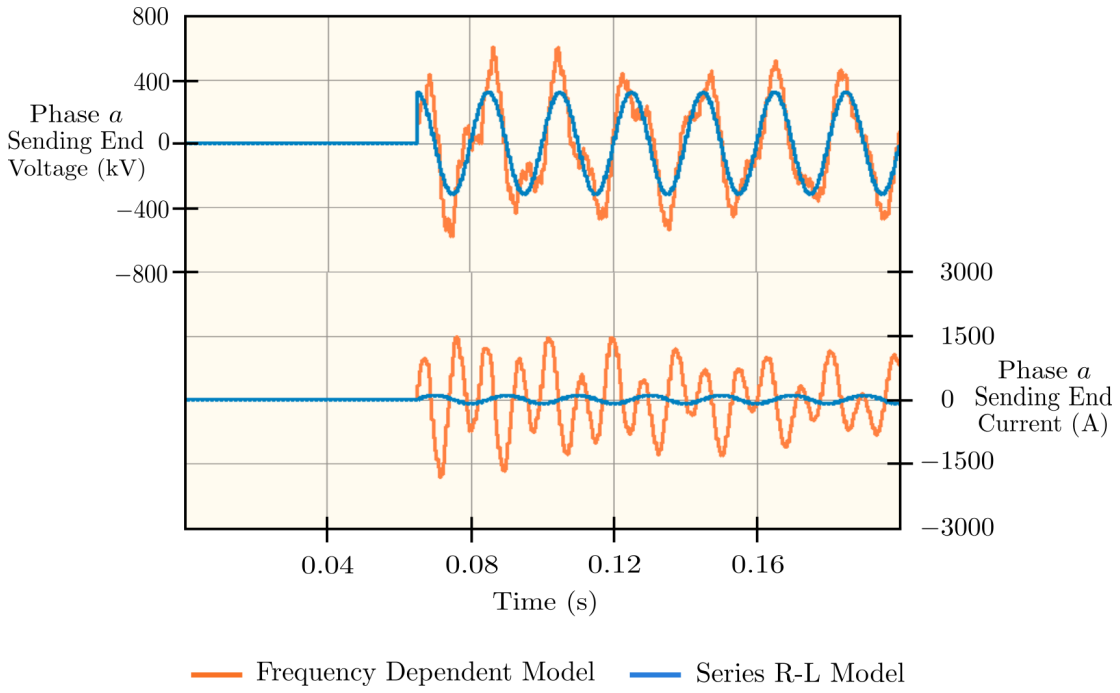


Figure 2.3: Waveforms for the Simulation of the Circuit shown in Fig. 2.1 with the parameters given in Table-2.1 using FDM and Series R-L Model in PSCAD software

A simple series connected resistance and inductance (R-L) model is fairly accurate for the short lines (length $< 80$ km), but not sufficient for the medium length lines or the long lines. For medium lines (80 km $<$ length $<$ 250 km), the nominal-$\pi$ lumped parameter model can be used for steady state analysis but fails to generate appropriate results during transients. And for long lines (length $> 250$ km), both the series R-L model and the nominal-$\pi$ model fails to generate the correct result both during the transients as well as the steady state conditions. *The results of the FDM of PSCAD has been compared with series R-L and nominal-$\pi$ models for the same switching event and parameters as provided in Table-*2.1 *and the mismatch in the sending end voltage and current of the 'a' phase are shown in Figs.* 2.3 *and* 2.4. Therefore for lines above 250 km, one must consider the fact that the parameters are not lumped but rather distributed.

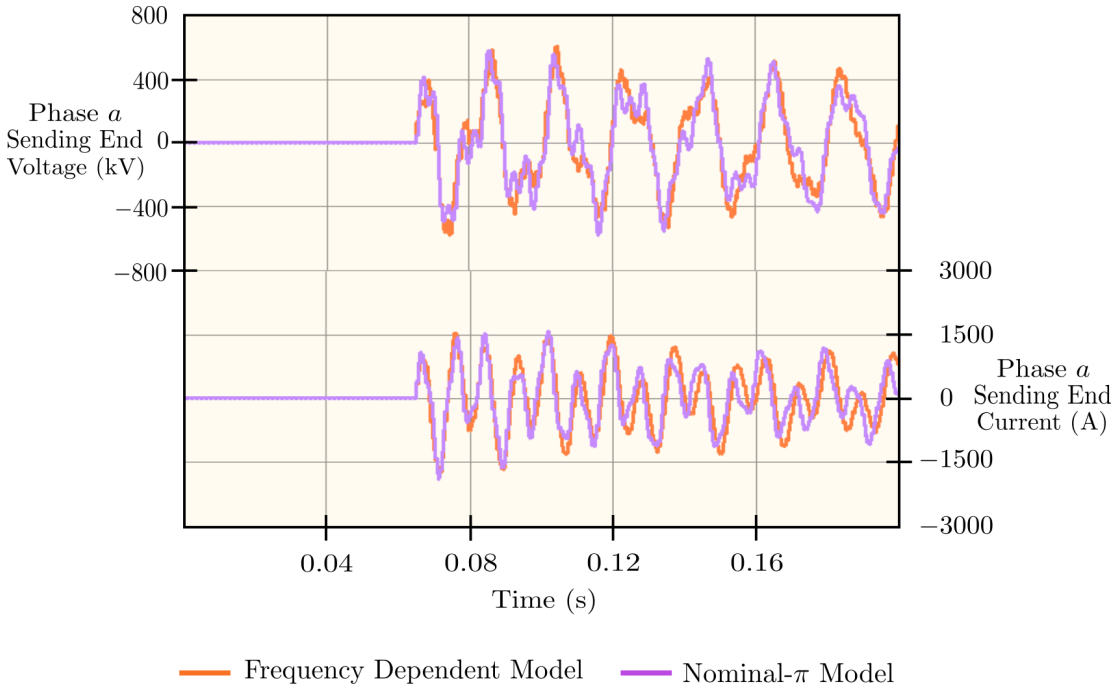


Figure 2.4: Waveforms for the Simulation of the Circuit shown in Fig. 2.1 with the parameters given in Table-2.1 using FDM and Nominal-$\pi$ Model in PSCAD software

### 2.1.2 Travelling Wave based Models

A potential candidate for the solution of the transmission line is the 'Method of Characteristics' (MOC) [23, 24]. The MOC uniformly distributes the line parameters thereby generating accurate result. But then for applying the MOC, the entire transmission line needs to be solved at several sections depending on the wave velocity in the line and the time interval at which the Observer solves the transmission line model in the embedded platform. Now for long line, as the number of line section increases,

the complexity enhances thereby putting an upper limit to the sampling frequency of the Observer. Since our aim is to emulate the switching current transients in a transmission line using power electronic converter, we are more interested in mimicking the transmission line behaviour as seen from its terminals. For this purpose we can visualize the line as a black box and focus only on the terminal quantities i.e. sending and receiving end voltages $\left(v_{se(a,b,c)} \text{ and } v_{re(a,b,c)}\right)$ and currents $\left(i_{se(a,b,c)} \text{ and } i_{re(a,b,c)}\right)$. In literature there are two models to represent a distributed parameter transmission line in terms of sending and receiving end quantities, namely, (a) Bergeron's Model and (b) Frequency Dependent Model (FDM). The FDM requires the characteristic admittance and the propagation function of the line to be fitted using a special curve fitting technique known as the vector fitting [25–27]. These additional complexities though give accurate results but incurs a large computational overhead and making it difficult for real-time implementation.

### Transmission Line Model Selection

Now as we are considering simultaneous switching of all the balanced 3 phases of the unenergized transposed transmission line, there is no possibility for the flow of zero sequence currents.

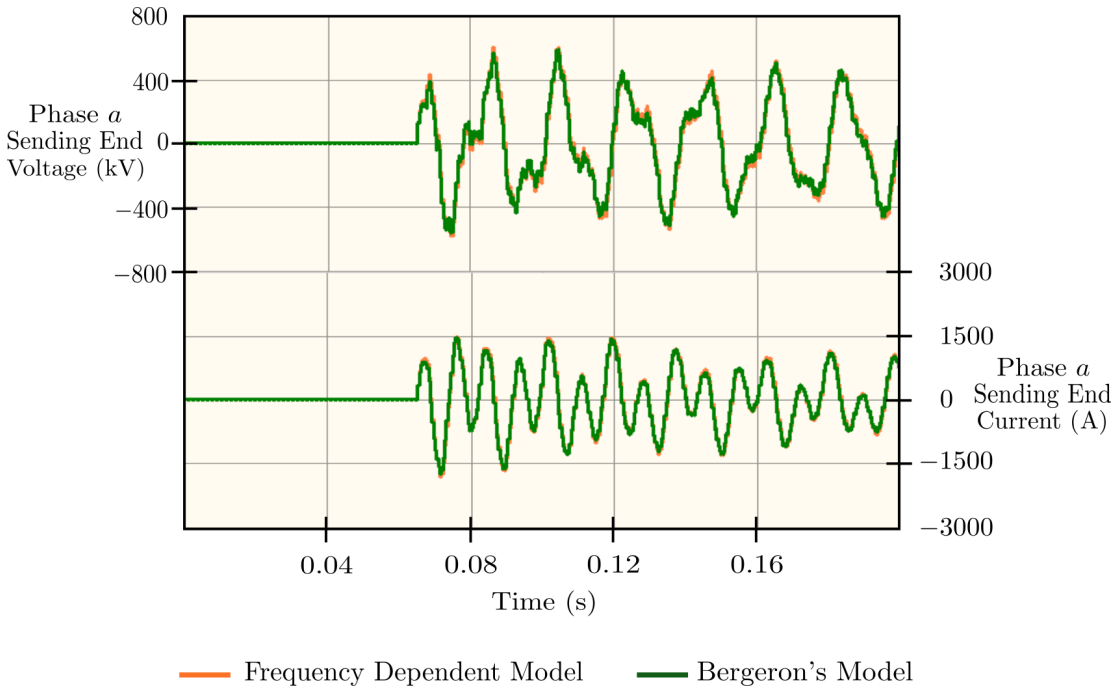


Figure 2.5: Waveforms for the Simulation of the Circuit shown in Fig. 2.1 with the parameters given in Table-2.1 using FDM and Bergeron's Model in PSCAD software

*Since it is the zero sequence parameters of the line which are frequency dependent [28], hence the travelling wave based Bergeron's Model and the FDM gives nearly*

*identical results for the simulation under consideration as shown in Fig.* 2.5. So in this work we will use Bergeron's Model as the numerical scheme to solve the transmission line in real-time and emulate by a power electronic converter. The detailed derivation of the Bergeron's Model based on the travelling wave phenomenon is given in the following sections.

## 2.2 Travelling Waves in a Transmission Line

When a transmission line is suddenly connected to a voltage source, the whole of the line is not energized all at once. It takes some time for the disturbance initiated at one end to be observed at the other end of the line. This is due to the presence of the distributed inductance and capacitance in the line. The launched voltage wave travels along the length of the line at certain velocity and is accompanied by a current wave. These two waves are related to each other by the characteristic impedance of the line. For simplicity of understanding, it is assumed that the $3\phi$ transmission lines are balanced and fully transposed throughout its length. Hence the analysis is being done on a per phase basis.

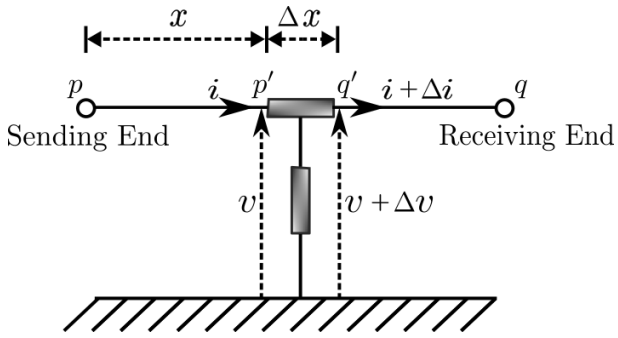


Figure 2.6: Analysis of a Single Phase Transmission Line on its elemental length

As shown in the Fig. 2.6, $v$ is the voltage at point $p'$ (which is at a distance $x$ from the sending end of the transmission line) and $v + \Delta v$ is the voltage at point $q'$ (which is at a distance $x + \Delta x$ from the sending end of the transmission line). Current, $i$ is being injected at $p'$ and $i + \Delta i$ is being drawn from $q'$. Let $R$, $L$, $C$ and $G$ be the line resistance, inductance, capacitance and conductance per unit length respectively.

$$\therefore v_{p'} - v_{q'} = -\Delta v = (R\Delta x)i + (L\Delta x)\frac{\partial i}{\partial t} \tag{2.1}$$

$$\Rightarrow -\frac{\Delta v}{\Delta x} = Ri + L\frac{\partial i}{\partial t} \tag{2.2}$$

Taking the limit as $\Delta x \longrightarrow 0$ the above equation becomes,

$$Ri + L\frac{\partial i}{\partial t} + \frac{\partial v}{\partial x} = 0 \tag{2.3}$$

Similarly applying KCL at the elemental length $p' - q'$, we get

$$-\Delta i = (G\Delta x)v + (C\Delta x)\frac{\partial v}{\partial t} \tag{2.4}$$

$$\Rightarrow -\frac{\Delta i}{\Delta x} = Gv + C\frac{\partial v}{\partial t} \tag{2.5}$$

Taking the limit as $\Delta x \longrightarrow 0$ the above equation becomes,

$$Gv + C\frac{\partial v}{\partial t} + \frac{\partial i}{\partial x} = 0 \tag{2.6}$$

Operating the equation 2.3 by $\frac{\partial}{\partial x}$ and equation 2.6 by $\left(R + L\frac{\partial}{\partial t}\right)$ and subtracting, we get

$$R\frac{\partial i}{\partial x} + L\frac{\partial^2 i}{\partial x \partial t} + \frac{\partial^2 v}{\partial x^2} - \left[G + C\frac{\partial}{\partial t}\right]\left[R + L\frac{\partial}{\partial t}\right]v - R\frac{\partial i}{\partial x} - L\frac{\partial^2 i}{\partial x \partial t} = 0$$

$$\Rightarrow \frac{\partial^2 v}{\partial x^2} = RGv + (LG + CR)\frac{\partial v}{\partial t} + LC\frac{\partial^2 v}{\partial t^2} \tag{2.7}$$

Again operating the equation 2.3 by $\left(G + C\frac{\partial}{\partial t}\right)$ and equation 2.6 by $\frac{\partial}{\partial x}$ and subtracting, we get

$$\left[R + L\frac{\partial}{\partial t}\right]\left[G + C\frac{\partial}{\partial t}\right]i + G\frac{\partial v}{\partial x} + C\frac{\partial^2 v}{\partial x \partial t} - G\frac{\partial v}{\partial x} - C\frac{\partial^2 v}{\partial x \partial t} - \frac{\partial^2 i}{\partial x^2} = 0$$

$$\Rightarrow \frac{\partial^2 i}{\partial x^2} = RGi + (LG + CR)\frac{\partial i}{\partial t} + LC\frac{\partial^2 i}{\partial t^2} \tag{2.8}$$

The equation 2.7 and 2.8 are known as the Telegrapher's equation. Considering the line to be lossless for the time being we put $R = G = 0$. Substituting $LC$ as $\frac{1}{c_{TL}^2}$ in equations 2.7 and 2.8 we get

$$\frac{\partial^2 v}{\partial x^2} = \frac{1}{c_{TL}^2}\frac{\partial^2 v}{\partial t^2} \tag{2.9}$$

and

$$\frac{\partial^2 i}{\partial x^2} = \frac{1}{c_{TL}^2}\frac{\partial^2 i}{\partial t^2} \tag{2.10}$$

Now we introduce new independent variables '$e$' and '$f$' where $e = x + c_{TL}t$ and $f = x - c_{TL}t$. So $v$ becomes a function of $e$ and $f$. Therefore we can write,

$$\frac{\partial v}{\partial x} = \frac{\partial v}{\partial e}\frac{\partial e}{\partial x} + \frac{\partial v}{\partial f}\frac{\partial f}{\partial x} = \frac{\partial v}{\partial e} + \frac{\partial v}{\partial f}$$

Differentiating the above equation once again with respect to $x$ we have,

$$\frac{\partial^2 v}{\partial x^2} = \frac{\partial^2 v}{\partial x \partial e} + \frac{\partial^2 v}{\partial x \partial f}$$

$$\Rightarrow \frac{\partial^2 v}{\partial x^2} = \left(\frac{\partial^2 v}{\partial e^2}\frac{\partial e}{\partial x} + \frac{\partial^2 v}{\partial f \partial e}\frac{\partial f}{\partial x}\right) + \left(\frac{\partial^2 v}{\partial f^2}\frac{\partial f}{\partial x} + \frac{\partial^2 v}{\partial e \partial f}\frac{\partial e}{\partial x}\right)$$

$$\Rightarrow \frac{\partial^2 v}{\partial x^2} = \frac{\partial^2 v}{\partial e^2} + 2\frac{\partial^2 v}{\partial e \partial f} + \frac{\partial^2 v}{\partial f^2} \tag{2.11}$$

Similarly we have,

$$\frac{\partial v}{\partial t} = \frac{\partial v}{\partial e}\frac{\partial e}{\partial t} + \frac{\partial v}{\partial f}\frac{\partial f}{\partial t} = c_{TL}\frac{\partial v}{\partial e} - c_{TL}\frac{\partial v}{\partial f}$$

Differentiating the above equation once again with respect to $t$ we get,

$$\frac{\partial^2 v}{\partial t^2} = c_{TL}\frac{\partial^2 v}{\partial t \partial e} - c_{TL}\frac{\partial^2 v}{\partial t \partial f}$$

$$\Rightarrow \frac{\partial^2 v}{\partial t^2} = c_{TL}\left(\frac{\partial^2 v}{\partial e^2}\frac{\partial e}{\partial t} + \frac{\partial^2 v}{\partial f \partial e}\frac{\partial f}{\partial t}\right) - c_{TL}\left(\frac{\partial^2 v}{\partial f^2}\frac{\partial f}{\partial t} + \frac{\partial^2 v}{\partial e \partial f}\frac{\partial e}{\partial t}\right)$$

$$\Rightarrow \frac{\partial^2 v}{\partial t^2} = c_{TL}^2\left(\frac{\partial^2 v}{\partial e^2} - 2\frac{\partial^2 v}{\partial e \partial f} + \frac{\partial^2 v}{\partial f^2}\right) \tag{2.12}$$

Putting equations 2.11 and 2.12 in 2.9 we get,

$$c_{TL}^2\left(\frac{\partial^2 v}{\partial e^2} - 2\frac{\partial^2 v}{\partial e \partial f} + \frac{\partial^2 v}{\partial f^2}\right) = c_{TL}^2\left(\frac{\partial^2 v}{\partial e^2} + 2\frac{\partial^2 v}{\partial e \partial f} + \frac{\partial^2 v}{\partial f^2}\right)$$

$$\Rightarrow \frac{\partial^2 v}{\partial e \partial f} = 0 \ \ [\because c_{TL} \neq 0]$$

Hence we can write,

$$\frac{\partial v}{\partial e} = g\left(e\right)$$

where, $g\left(e\right)$ is an arbitrary function of $e$. Therefore integrating the above equation with respect to $e$ we get,

$$v\left(x,t\right) = \int g\left(e\right)\ de + g_2\left(f\right)$$

Considering $\int g\left(e\right)\ de = g_1\left(e\right)$ we have,

$$v\left(x,t\right) = g_1\left(e\right) + g_2\left(f\right)$$

$$\Rightarrow v\left(x,t\right) = g_1\left(x + c_{TL}t\right) + g_2\left(x - c_{TL}t\right) \tag{2.13}$$

From the above equation we can say that $g_2$ is the component of the wave which travels in the forward direction i.e. from the sending end of the line to the receiving

end with speed $c_{TL}$ and $g_1$ is the component of the wave which travels in the backward direction i.e. from the receiving end of the line to the sending end with the same speed $c_{TL}$. Now putting $R = 0$ in the equation 2.3 we get,

$$\frac{\partial v}{\partial x} = -L\frac{\partial i}{\partial t} = \frac{\mathrm{d}g_1}{\mathrm{d}e}\frac{\partial e}{\partial x} + \frac{\mathrm{d}g_2}{\mathrm{d}f}\frac{\partial f}{\partial x} = \frac{\mathrm{d}g_1}{\mathrm{d}e} + \frac{\mathrm{d}g_2}{\mathrm{d}f}$$

$$\Rightarrow -Li\left(x,t\right) = \int \frac{\mathrm{d}g_1}{\mathrm{d}e}\, dt + \int \frac{\mathrm{d}g_2}{\mathrm{d}f}\, dt = \frac{g_1}{c_{TL}} - \frac{g_2}{c_{TL}}$$

$$\Rightarrow i\left(x,t\right) = \frac{g_2\left(x - c_{TL}t\right)}{\sqrt{L/C}} - \frac{g_1\left(x + c_{TL}t\right)}{\sqrt{L/C}}$$

With $R = 0$, the characteristic impedance of the line ($Z_c$) is given by $\sqrt{L/C}$.

$$\therefore i\left(x,t\right) = \frac{g_2\left(x - c_{TL}t\right)}{Z_c} - \frac{g_1\left(x + c_{TL}t\right)}{Z_c} \tag{2.14}$$

The equations 2.13 and 2.14 can be verified from [29].

## 2.3 Norton Model of a Transmission Line

### 2.3.1 Lossless Transmission Line

Multiplying equation 2.14 with $Z_c$ and adding with the equation 2.13 we get,

$$v\left(x,t\right) + Z_c i\left(x,t\right) = 2g_2\left(x - c_{TL}t\right) \tag{2.15}$$

Similarly multiplying equation 2.14 with $Z_c$ and subtracting from the equation 2.13 we get,

$$v\left(x,t\right) - Z_c i\left(x,t\right) = 2g_1\left(x + c_{TL}t\right) \tag{2.16}$$

From equation 2.15 we can say that $v\left(x,t\right) + Z_c i\left(x,t\right)$ is constant if $\left(x - c_{TL}t\right)$ is constant. Considering $l$ to be the line length, the travelling time, $\tau$ of the wave from the sending end ($p$) to the receiving end ($q$) can be written as,

$$\tau = \frac{l}{c_{TL}}$$

Therefore from the equation 2.15 we can say,

$$v\left(0, t - \tau\right) + Z_c i\left(0, t - \tau\right) = v\left(l,t\right) + Z_c i\left(l,t\right) \tag{2.17}$$

Defining the following variables,

$$\begin{aligned} v\left(0, t - \tau\right) &\text{ as } v_p\left(t - \tau\right) \\ i\left(0, t - \tau\right) &\text{ as } i_{pq}\left(t - \tau\right) \\ v\left(l,t\right) &\text{ as } v_q\left(t\right) \\ i\left(l,t\right) &\text{ as } -i_{qp}\left(t\right) \end{aligned}$$

The equation 2.17 can be written as,

$$v_p(t-\tau) + Z_c i_{pq}(t-\tau) = v_q(t) - Z_c i_{qp}(t)$$

$$\Rightarrow i_{qp}(t) = \frac{v_q(t)}{Z_c} - \frac{v_p(t-\tau)}{Z_c} - i_{pq}(t-\tau) \tag{2.18}$$

Defining $I_q(t-\tau) = -\frac{v_p(t-\tau)}{Z_c} - i_{pq}(t-\tau)$ the above equation then can be written as,

$$i_{qp}(t) = \frac{v_q(t)}{Z_c} + I_q(t-\tau) \tag{2.19}$$

Similarly for the other end of the line we can write,

$$i_{pq}(t) = \frac{v_p(t)}{Z_c} + I_p(t-\tau) \tag{2.20}$$

where, $I_p(t-\tau) = -\frac{v_q(t-\tau)}{Z_c} - i_{qp}(t-\tau)$. The equivalent circuit based on the equation 2.19 and 2.20 is shown in the Fig. 2.7.

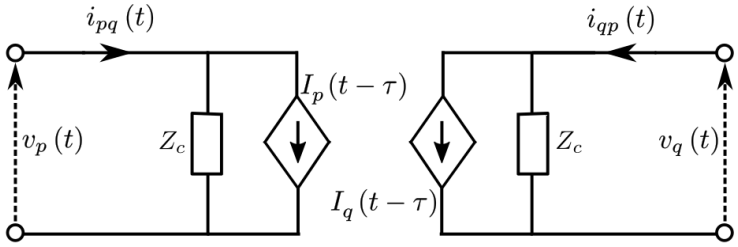


Figure 2.7: Norton Model of a Transmission Line

### 2.3.2 Lossy Transmission Line - Bergeron's Model

Now we will consider finite value of line resistance. The resistance will be inserted throughout the line by dividing its total length into several sections. Suppose the section length is $\Delta l$. Then the required number of sections is, $\frac{l}{\Delta l}$. The value of $\Delta l$ is chosen such that $\frac{R\Delta l}{2} \ll Z_c$, so that the wave while travelling through the line do not see a discontinuity.

**Example Case :**

A balanced $3\phi$, fully transposed 400 km long transmission line is considered with the following parameters : $R = 0.03\ \Omega$ /km, $L = 1 \times 10^{-3}$ H/km and $C = 12.96 \times 10^{-9}$ F/km.

$$\therefore Z_c = \sqrt{\frac{L}{C}} = \sqrt{\frac{1 \times 10^{-3}}{12.96 \times 10^{-9}}} = 277.78\ \Omega$$

Considering two sections, $\frac{R\Delta l}{2} = \frac{0.03\times200}{2} = 3\ \Omega$ which is much less than $Z_c$. So splitting the line into two sections will fetch accurate result. In this chapter we will develop the Norton model of the lossy line by splitting it in 2 sections. The equivalent model is shown in the Fig. 2.8, where $R_T = R \times l$.

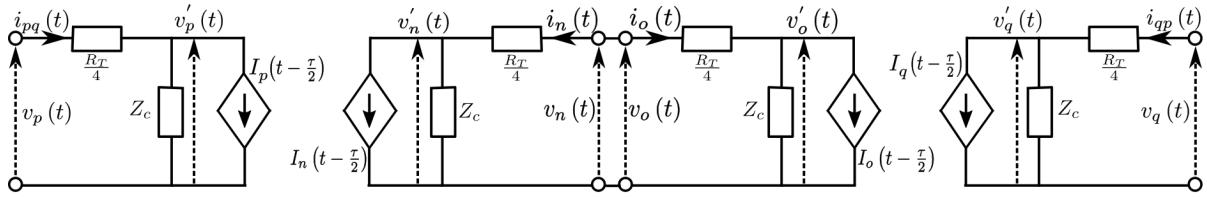


Figure 2.8: Cascading of 2 Sections of a Lossy Transmission Line

From Fig. 2.8 we can write,

$$i_{pq}(t) = \frac{v_p'(t)}{Z_c} + I_p\left(t - \frac{\tau}{2}\right)$$

Now from equations 2.18 and 2.19 we can similarly write,

$$I_p\left(t-\frac{\tau}{2}\right) = -\frac{v_n'\left(t-\frac{\tau}{2}\right)}{Z_c} - i_n\left(t-\frac{\tau}{2}\right)$$

$$\therefore i_{pq}(t) = \frac{v_p'(t)}{Z_c} - \frac{v_n'\left(t-\frac{\tau}{2}\right)}{Z_c} - i_n\left(t-\frac{\tau}{2}\right)$$

$$\Rightarrow i_{pq}(t) = \frac{v_p(t) - i_{pq}(t)\frac{R_T}{4}}{Z_c} - \frac{v_n\left(t-\frac{\tau}{2}\right) - i_n\left(t-\frac{\tau}{2}\right)\frac{R_T}{4}}{Z_c} - i_n\left(t-\frac{\tau}{2}\right)$$

$$\Rightarrow i_{pq}(t) = \frac{v_p(t)}{Z_c+\frac{R_T}{4}} - \frac{v_n\left(t-\frac{\tau}{2}\right)}{Z_c+\frac{R_T}{4}} - \left[\frac{Z_c-\frac{R_T}{4}}{Z_c+\frac{R_T}{4}}\right] i_n\left(t-\frac{\tau}{2}\right) \tag{2.21}$$

Defining $I_p'\left(t-\frac{\tau}{2}\right) = -\frac{v_n\left(t-\frac{\tau}{2}\right)}{Z_c+\frac{R_T}{4}} - \left[\frac{Z_c-\frac{R_T}{4}}{Z_c+\frac{R_T}{4}}\right] i_n\left(t-\frac{\tau}{2}\right)$ we get,

$$i_{pq}(t) = \frac{v_p(t)}{Z_c+\frac{R_T}{4}} + I_p'\left(t-\frac{\tau}{2}\right) \tag{2.22}$$

Now the Fig. 2.8 can be redrawn as as shown in Fig. 2.9.

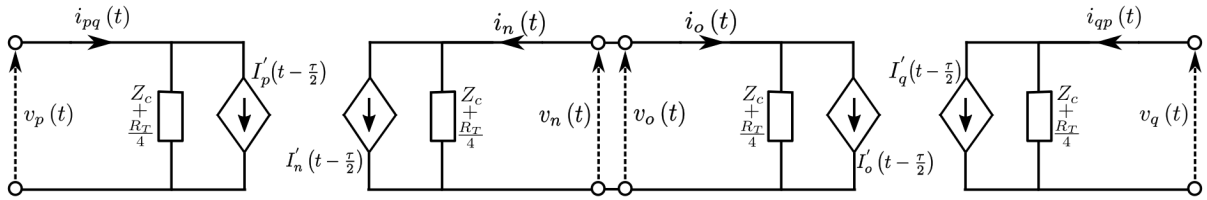


Figure 2.9: Reduced Cascaded Model of a 2 Section Lossy Transmission Line

Similarly we can write the following equations :

$$i_o\left(t-\frac{\tau}{2}\right)=\frac{v_o\left(t-\frac{\tau}{2}\right)}{Z_c+\frac{R_T}{4}}+I_o^{'}\left(t-\tau\right)$$

$$\Rightarrow i_o\left(t-\frac{\tau}{2}\right)=\frac{v_o\left(t-\frac{\tau}{2}\right)}{Z_c+\frac{R_T}{4}}-\frac{v_q\left(t-\tau\right)}{Z_c+\frac{R_T}{4}}-\left[\frac{Z_c-\frac{R_T}{4}}{Z_c+\frac{R_T}{4}}\right]i_{qp}\left(t-\tau\right) \tag{2.23}$$

$$i_{qp}\left(t\right)=\frac{v_q\left(t\right)}{Z_c+\frac{R_T}{4}}+I_q^{'}\left(t-\frac{\tau}{2}\right)$$

$$\Rightarrow i_{qp}\left(t\right)=\frac{v_q\left(t\right)}{Z_c+\frac{R_T}{4}}-\frac{v_o\left(t-\frac{\tau}{2}\right)}{Z_c+\frac{R_T}{4}}-\left[\frac{Z_c-\frac{R_T}{4}}{Z_c+\frac{R_T}{4}}\right]i_o\left(t-\frac{\tau}{2}\right) \tag{2.24}$$

and

$$i_n\left(t-\frac{\tau}{2}\right)=\frac{v_n\left(t-\frac{\tau}{2}\right)}{Z_c+\frac{R_T}{4}}+I_n^{'}\left(t-\tau\right)$$

$$\Rightarrow i_n\left(t-\frac{\tau}{2}\right)=\frac{v_n\left(t-\frac{\tau}{2}\right)}{Z_c+\frac{R_T}{4}}-\frac{v_p\left(t-\tau\right)}{Z_c+\frac{R_T}{4}}-\left[\frac{Z_c-\frac{R_T}{4}}{Z_c+\frac{R_T}{4}}\right]i_{pq}\left(t-\tau\right) \tag{2.25}$$

Now we will cascade the two half line sections and then eliminate the mid-point variables as only the terminals are of interest. We have already seen that,

$$I_p^{'}\left(t-\frac{\tau}{2}\right)=-\frac{v_n\left(t-\frac{\tau}{2}\right)}{Z_c+\frac{R_T}{4}}-\left[\frac{Z_c-\frac{R_T}{4}}{Z_c+\frac{R_T}{4}}\right]i_n\left(t-\frac{\tau}{2}\right)$$

$$\Rightarrow I_p^{'}\left(t-\frac{\tau}{2}\right)=-\frac{v_n\left(t-\frac{\tau}{2}\right)}{Z_c+\frac{R_T}{4}}+\left[\frac{Z_c-\frac{R_T}{4}}{Z_c+\frac{R_T}{4}}\right]i_o\left(t-\frac{\tau}{2}\right)$$

Putting equation 2.23 in the above equation we get,

$$I_p^{'}\left(t-\frac{\tau}{2}\right)=\left[\frac{Z_c-\frac{R_T}{4}}{\left(Z_c+\frac{R_T}{4}\right)^2}-\frac{1}{Z_c+\frac{R_T}{4}}\right]v_n\left(t-\frac{\tau}{2}\right)-\left[\frac{Z_c-\frac{R_T}{4}}{\left(Z_c+\frac{R_T}{4}\right)^2}\right]v_q\left(t-\tau\right)$$
$$-\left[\frac{Z_c-\frac{R_T}{4}}{Z_c+\frac{R_T}{4}}\right]^2 i_{qp}\left(t-\tau\right) \tag{2.26}$$

Solving for $v_n\left(t-\frac{\tau}{2}\right)$ from the equation 2.25 and substituting it in the equation 2.26, we get

$$I_p^{'}\left(t-\frac{\tau}{2}\right) = -\frac{\frac{R_T}{4}}{\left(Z_c+\frac{R_T}{4}\right)^2}\left[v_p\left(t-\tau\right)+\left(Z_c-\frac{R_T}{4}\right)i_{pq}\left(t-\tau\right)\right] - \frac{Z_c}{\left(Z_c+\frac{R_T}{4}\right)^2}\left[v_q\left(t-\tau\right)+\left(Z_c-\frac{R_T}{4}\right)i_{qp}\left(t-\tau\right)\right] \quad (2.27)$$

Therefore we can redefine $I_p^{'}\left(t-\frac{\tau}{2}\right)$ as $I_p^{''}\left(t-\tau\right)$. Similarly solving for the receiving end of the line we get,

$$i_{qp}\left(t\right) = \frac{v_q\left(t\right)}{Z_c+\frac{R_T}{4}} + I_q^{'}\left(t-\frac{\tau}{2}\right) \quad (2.28)$$

where,

$$I_q^{'}\left(t-\frac{\tau}{2}\right) = -\frac{\frac{R_T}{4}}{\left(Z_c+\frac{R_T}{4}\right)^2}\left[v_q\left(t-\tau\right)+\left(Z_c-\frac{R_T}{4}\right)i_{qp}\left(t-\tau\right)\right] - \frac{Z_c}{\left(Z_c+\frac{R_T}{4}\right)^2}\left[v_p\left(t-\tau\right)+\left(Z_c-\frac{R_T}{4}\right)i_{pq}\left(t-\tau\right)\right] \quad (2.29)$$

We can again redefine $I_q^{'}\left(t-\frac{\tau}{2}\right)$ as $I_q^{''}\left(t-\tau\right)$. The equivalent circuit based on the equations 2.22, 2.27, 2.28 and 2.29 is shown in the Fig. 2.10. The end results can be verified from [30, 31].

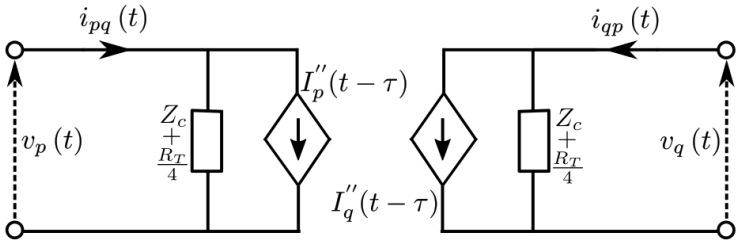


Figure 2.10: Travelling Wave based Bergeron's Model of a Lossy Transmission Line

## 2.4 Model to be implemented on Embedded Platform

For ease of analysis the terminal quantities of Fig. 2.10 are re-labeled as shown in Table-2.2.

Table 2.2: Re-labeling of Terminal Quantities of Fig. 2.10

| | |
|---|---|
| $v_p(t)$ | $v_{se(J)}(t)$ |
| $i_{pq}(t)$ | $i^{**}_{se(J)}(t)$ |
| $v_q(t)$ | $v_{re(J)}(t)$ |
| $i_{qp}(t)$ | $i^{**}_{re(J)}(t)$ |

where, $J \epsilon \{a, b, c\}$. Defining the quantities mentioned in Table-2.3, the equations 2.22, 2.27, 2.28 and 2.29 can be re-written as shown in 2.30 and 2.31. *To have the flexibility of implementing a programmable grid impedance in the experimental setup, a strong grid (sinusoidal voltage source) is used and the inductive grid impedance is emulated inside the embedded platform.* Equations 2.32 and 2.33 can be written by applying the boundary condition on the sending and receiving end of the line respectively. The equivalent circuit is shown in the Fig. 2.11. Therefore the equations 2.30, 2.31, 2.32 and 2.33 will be implemented in the embedded platform.

Table 2.3: Constants of Bergeron's Model

| $C_1$ | $C_2$ | $C_3$ | $C_4$ | $C_5$ |
|---|---|---|---|---|
| $\frac{1}{Z_c+\frac{R_T}{4}}$ | $\frac{\frac{R_T}{4}}{\left(Z_c+\frac{R_T}{4}\right)^2}$ | $\frac{\frac{R_T}{4}\left(Z_c-\frac{R_T}{4}\right)}{\left(Z_c+\frac{R_T}{4}\right)^2}$ | $\frac{Z_c}{\left(Z_c+\frac{R_T}{4}\right)^2}$ | $\frac{Z_c\left(Z_c-\frac{R_T}{4}\right)}{\left(Z_c+\frac{R_T}{4}\right)^2}$ |

$$i^{**}_{se(J)}(t) = C_1 v_{se(J)}(t) \underbrace{-C_2 v_{se(J)}(t-\tau) - C_3 i^{**}_{se(J)}(t-\tau) - C_4 v_{re(J)}(t-\tau) - C_5 i^{**}_{re(J)}(t-\tau)}_{I''_{s(J)}(t-\tau)} \tag{2.30}$$

$$i^{**}_{re(J)}(t) = C_1 v_{re(J)}(t) \underbrace{-C_2 v_{re(J)}(t-\tau) - C_3 i^{**}_{re(J)}(t-\tau) - C_4 v_{se(J)}(t-\tau) - C_5 i^{**}_{se(J)}(t-\tau)}_{I''_{r(J)}(t-\tau)} \tag{2.31}$$

$$v_{se(J)}(t) = v_{seg(J)}(t) - L_g \frac{\mathrm{d}i^{**}_{se(J)}(t)}{\mathrm{d}t} \tag{2.32}$$

and

$$v_{re(J)}(t) = -L_{sh} \frac{\mathrm{d}i^{**}_{re(J)}(t)}{\mathrm{d}t} \tag{2.33}$$

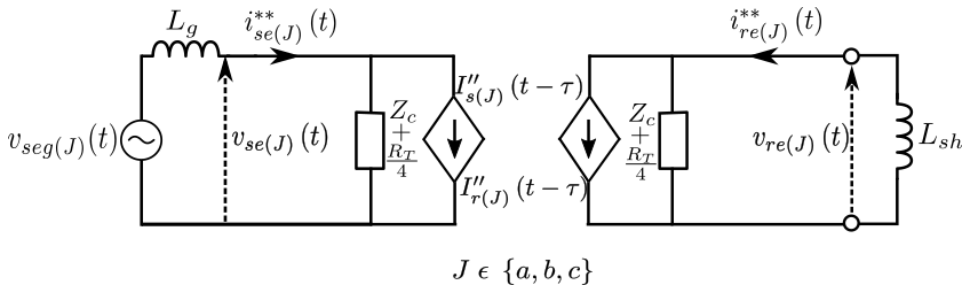


Figure 2.11: Equivalent Travelling Wave based model of the Transmission Line to be implemented in the Observer

## 2.5 Summary

1. For accurate prediction of the switching current transients of a long transmission line, a distributed parameter model needs to be solved.

2. Since we will emulate the transmission line with a power electronic converter, we need to mimick the transmission line behaviour as seen from its terminals.

3. With the sending end bus voltages of the line being known, the work is to accurately determine the terminal currents both during transients and steady state.

4. Since the result of the Bergeron's Model matches closely with the Frequency Dependent Model, so we select it as the numerical scheme to solve the distributed parameter transmission line on an embedded platform in real-time.

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# Chapter 3

# Development of a Real-Time Observer on an Embedded Platform

With the determination of the numerical scheme to solve the transmission line with its distributed parameters, the next thing to be addressed is the implementation of this scheme on an embedded platform so that the transmission line can be solved in real-time. In this chapter we will outline all the aspects regarding the choice of the sampling time period of the Observer ($T_{ob}$) as well as the switching period ($T_{sw}$) of the power electronic converter.

## 3.1 Discretized Equation of Bergeron's Model

Putting $t = kT_{ob}$ in the equations 2.30 and 2.31 of Chapter 2 we get,

$$i^{**}_{se(J)}(kT_{ob}) = C_1 v_{se(J)}(kT_{ob}) - C_2 v_{se(J)}(kT_{ob}-\tau) - C_3 i^{**}_{se(J)}(kT_{ob}-\tau) - C_4 v_{re(J)}(kT_{ob}-\tau) - C_5 i^{**}_{re(J)}(kT_{ob}-\tau) \quad (3.1)$$

and

$$i^{**}_{re(J)}(kT_{ob}) = C_1 v_{re(J)}(kT_{ob}) - C_2 v_{re(J)}(kT_{ob}-\tau) - C_3 i^{**}_{re(J)}(kT_{ob}-\tau) - C_4 v_{se(J)}(kT_{ob}-\tau) - C_5 i^{**}_{se(J)}(kT_{ob}-\tau) \quad (3.2)$$

The equation 3.1 and 3.2 demands the use of four memory buffers for each phase of the transmission line to store the past values of the sending and receiving end voltages and currents. Now $\tau$ must be an integral multiple of $T_{ob}$ in order to avoid the complex interpolation schemes [28]. Therefore $T_{ob}$ must be adjusted such that,

$$NT_{ob} = \tau \quad (3.3)$$

where $N$ is an integer. Therefore the size of the First In First Out (FIFO) buffers should be atleast $N$. Substituting equation 3.3 in the equations 3.1 and 3.2 and dropping the term $T_{ob}$, we get

$$i^{**}_{se(J)}[k] = C_1 v_{se(J)}[k] - C_2 v_{se(J)}[k-N] - C_3 i^{**}_{se(J)}[k-N] \\ - C_4 v_{re(J)}[k-N] - C_5 i^{**}_{re(J)}[k-N] \quad (3.4)$$

and,

$$i^{**}_{re(J)}[k] = C_1 v_{re(J)}[k] - C_2 v_{re(J)}[k-N] - C_3 i^{**}_{re(J)}[k-N] \\ - C_4 v_{se(J)}[k-N] - C_5 i^{**}_{se(J)}[k-N] \quad (3.5)$$

Now applying Backward Euler in the equations 2.32 and 2.33 of Chapter 2, we get

$$v_{se(J)}[k] = v_{seg(J)}[k] - \frac{L_g}{T_{ob}}\left(i^{**}_{se(J)}[k] - i^{**}_{se(J)}[k-1]\right) \quad (3.6)$$

and

$$v_{re(J)}[k] = -\frac{L_{sh}}{T_{ob}}\left(i^{**}_{re(J)}[k] - i^{**}_{re(J)}[k-1]\right) \quad (3.7)$$

respectively. From equations 3.6 and 3.7 we can once again write,

$$v_{se(J)}[k-N] = v_{seg(J)}[k-N] - \frac{L_g}{T_{ob}}\left(i^{**}_{se(J)}[k-N] - i^{**}_{se(J)}[k-N-1]\right) \quad (3.8)$$

and

$$v_{re(J)}[k-N] = -\frac{L_{sh}}{T_{ob}}\left(i^{**}_{re(J)}[k-N] - i^{**}_{re(J)}[k-N-1]\right) \quad (3.9)$$

Substituting $v_{se(J)}[k]$, $v_{se(J)}[k-N]$, $v_{re(J)}[k]$ and $v_{re(J)}[k-N]$ using equations 3.6, 3.8, 3.7 and 3.9 respectively into equations 3.4 and 3.5, we derive 3.10 and 3.11. The constants are defined in Table-3.1.

$$i^{**}_{se(J)}[k] = C_6 v_{seg(J)}[k] + C_7 i^{**}_{se(J)}[k-1] + C_8 v_{seg(J)}[k-N] + C_9 i^{**}_{se(J)}[k-N] \\ + C_{10} i^{**}_{se(J)}[k-N-1] + C_{11} i^{**}_{re(J)}[k-N] + C_{12} i^{**}_{re(J)}[k-N-1] \quad (3.10)$$

and

$$i^{**}_{re(J)}[k] = C_{13} i^{**}_{re(J)}[k-1] + C_{14} i^{**}_{re(J)}[k-N] + C_{15} i^{**}_{re(J)}[k-N-1] + C_{16} v_{seg(J)}[k-N] \\ + C_{17} i^{**}_{se(J)}[k-N] + C_{18} i^{**}_{se(J)}[k-N-1] \quad (3.11)$$

*Equations* 3.6, 3.10 *and* 3.11 *are solved in real-time to implement the Observer.* $v_{seg(J)}[k]$ *is the input,* $i^{**}_{se(J)}[k]$ *and* $i^{**}_{re(J)}[k]$ *are the state variables and* $v_{se(J)}[k]$ *and* $i^{**}_{se(J)}[k]$ *are the outputs.*

Table 3.1: Additional Observer Constants

| | | |
|---|---|---|
| $K_1 = 1 + C_1\frac{L_g}{T_{ob}}$ | $C_9 = \frac{-C_3+C_2\frac{L_g}{T_{ob}}}{K_1}$ | $C_{14} = \frac{-C_3+C_2\frac{L_{sh}}{T_{ob}}}{K_2}$ |
| $K_2 = 1 + C_1\frac{L_{sh}}{T_{ob}}$ | $C_{10} = \frac{-C_2\frac{L_g}{T_{ob}}}{K_1}$ | $C_{15} = \frac{-C_2\frac{L_{sh}}{T_{ob}}}{K_2}$ |
| $C_6 = \frac{C_1}{K_1}$ | $C_{11} = \frac{-C_5+C_4\frac{L_{sh}}{T_{ob}}}{K_1}$ | $C_{16} = \frac{-C_4}{K_2}$ |
| $C_7 = \frac{C_1\frac{L_g}{T_{ob}}}{K_1}$ | $C_{12} = \frac{-C_4\frac{L_{sh}}{T_{ob}}}{K_1}$ | $C_{17} = \frac{-C_5+C_4\frac{L_g}{T_{ob}}}{K_2}$ |
| $C_8 = \frac{-C_2}{K_1}$ | $C_{13} = \frac{C_1\frac{L_{sh}}{T_{ob}}}{K_2}$ | $C_{18} = \frac{-C_4\frac{L_g}{T_{ob}}}{K_2}$ |

## 3.2 Determination of Observer Computation Time

Xilinx make Zynq System-on-Chip (SoC) has been selected as the embedded platform which has an ARM Cortex-A9 based Processing System (PS). The required number of instruction cycles for execution of different operations or instructions [32] has been listed in the Table-3.2.

Table 3.2: Instruction Cycle Requirements by the Zynq SoC

| **Sl. No.** | **Instructions** | **Number of cycles** |
|---|---|---|
| 1 | Load and Store, $n_{ls}$ | 3 |
| 2 | Multiplication, $n_{mul}$ | 5 |
| 3 | Subtraction, $n_{sub}$ | 4 |
| 4 | Addition, $n_{add}$ | 4 |
| 5 | Move, $n_{mov}$ | 2 |
| 6 | Compare, $n_{cmp}$ | 3 |

### 3.2.1 Compuations to be done by the Observer in each Computational Cycle :

We consider that the $3\phi$ transmission line is balanced and transposed throughout its length. So we calculate the line end currents for two phases and the third one is taken as the negative sum of the other two phases. This will slightly reduce the computational burden for real-time implementation. The instructions to be executed in every computational cycle are as follows :

i. Feed the latest sending end voltage of the $a$ and $b$ phase of the transmission line. $[2 \times n_{ls}]$

ii. Referring equation 3.10, seven multiplication and six addition are involved for calculating the sending end current for each $a$ and $b$ phase. $[14 \times n_{mul}\ ,\ 12 \times n_{add}]$

iii. Referring equation 3.11, six multiplication and five addition are involved for calculating the receiving end current for each $a$ and $b$ phase. $[12 \times n_{mul}\ ,\ 10 \times n_{add}]$

iv. Referring equation 3.6, one multiplication and two subtraction are involved for calculating the sending end line voltage for each $a$ and $b$ phase. $[2 \times n_{mul}\ ,\ 4 \times n_{sub}]$

v. $N+1$ number of shifting operations in the memory buffers of the sending end grid voltage and current of $a$ and $b$ phase, so that it can be recycled and used. $\left[4 \times (N+1) \times n_{mov}\right]$

vi. $N+1$ number of shifting operations in the memory buffers of the receiving end current of $a$ and $b$ phase, so that it can be recycled and used. $\left[2 \times (N+1) \times n_{mov}\right]$

vii. Sending end current calculation for the $c$ phase. $[2 \times n_{sub}]$

The shifting operation in the memory buffers is done by a counter , which needs to be incremented and compared with the reference value. Denoting the instruction clock period of the PS as $T_{clk(PS)}$, the total computational time required by the Observer ($T_{obc}$) can be written as,

$$T_{obc} = T_{clk(PS)}[(2 \times n_{ls}) + (28 \times n_{mul}) + (22 \times n_{add}) + (4 \times n_{sub}) + ((N+1)\left(6 \times n_{mov} + n_{add} + n_{cmp}\right)) + (2 \times n_{sub})]$$

$$\Rightarrow T_{obc} = T_{clk(PS)}[(2 \times 3) + (28 \times 5) + (22 \times 4) + (4 \times 4) + (N+1)\left((6 \times 2) + 4 + 3\right) + (2 \times 4)]$$

$$\Rightarrow T_{obc} = T_{clk(PS)}\left[6 + 140 + 88 + 16 + 19(N+1) + 8\right] = T_{clk(PS)}\left[277 + 19N\right]$$

For floating point operation in the selected Zynq PS, $T_{clk(PS)}$ is approximately 6 ns.

$$\therefore T_{obc} \approx \left(1.66 + \frac{114}{1000}N\right) = \left(1.66 + \frac{114}{1000}\frac{\tau}{T_{ob}}\right)\mu s \tag{3.12}$$

*In Appendix C we have provided a quantitative comparison of the computational burden involved with the Bergeron's Model and the Method Of Characteristics for a processor based real-time implementation.*

## 3.3 Determination of Frequency Contents of the Sending End Line Currents during the instant of Switching the Transmission Line

Voltage switching action of an actual physical transmission line, as shown in Fig. 2.1 has been simulated in PSCAD software using the Bergeron's (constant frequency)

Model with the parameters provided in Table-2.1. The corresponding waveforms are shown in Fig. 3.1.

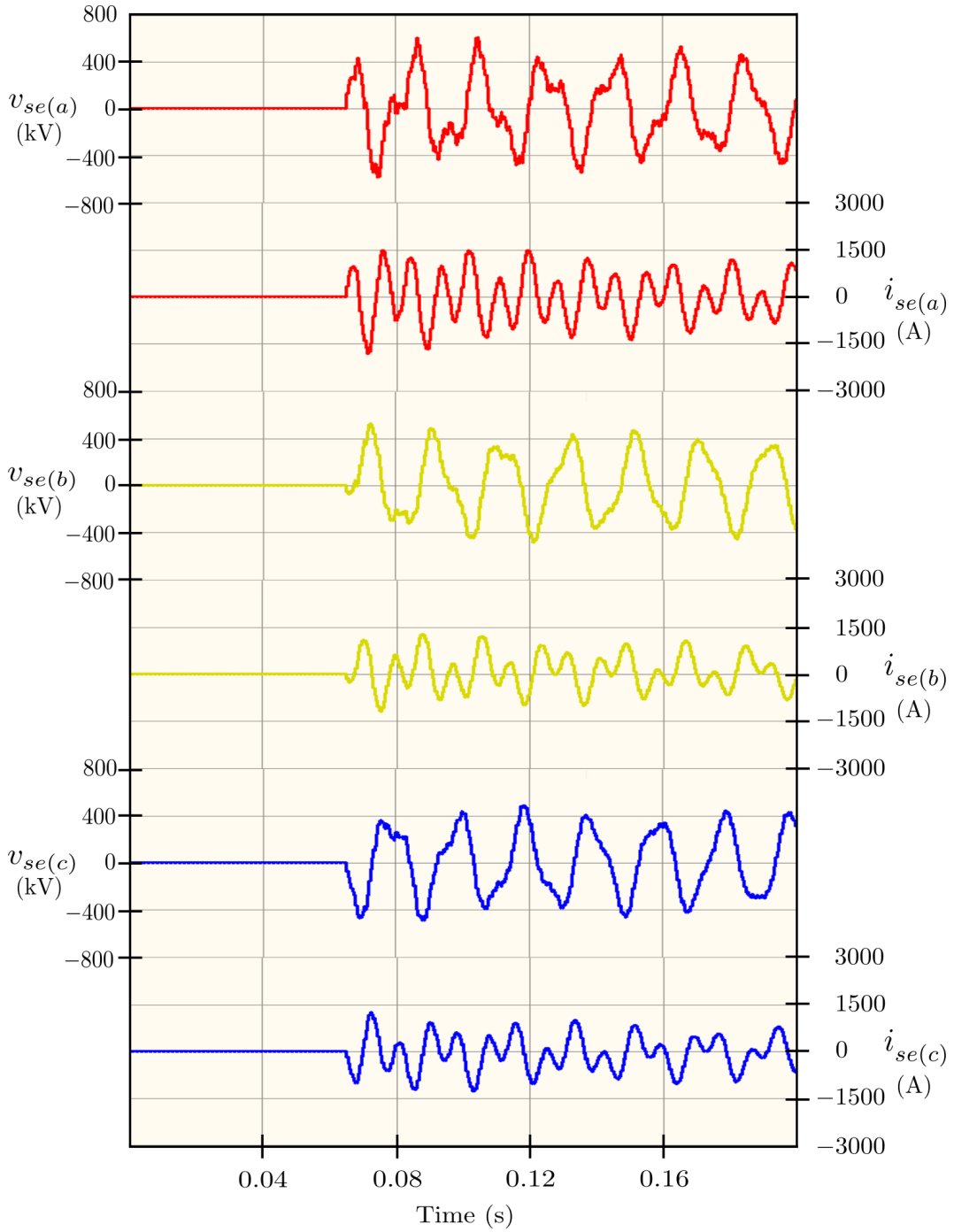


Figure 3.1: Sending End Voltage and Current waveforms for the Simulation of the Circuit shown in Fig. 2.1 with the parameters given in Table-2.1 using Bergeron's Model in PSCAD software

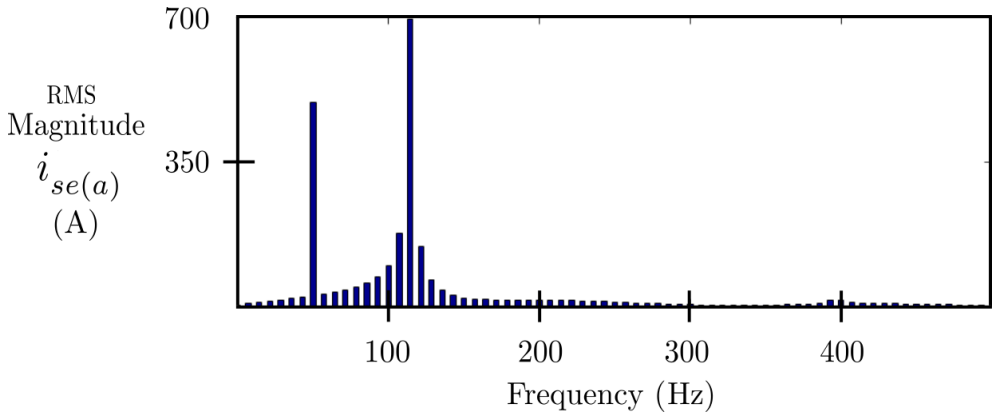


Figure 3.2: Harmonic Analysis of the $a$ phase Sending End Current of Fig. 3.1

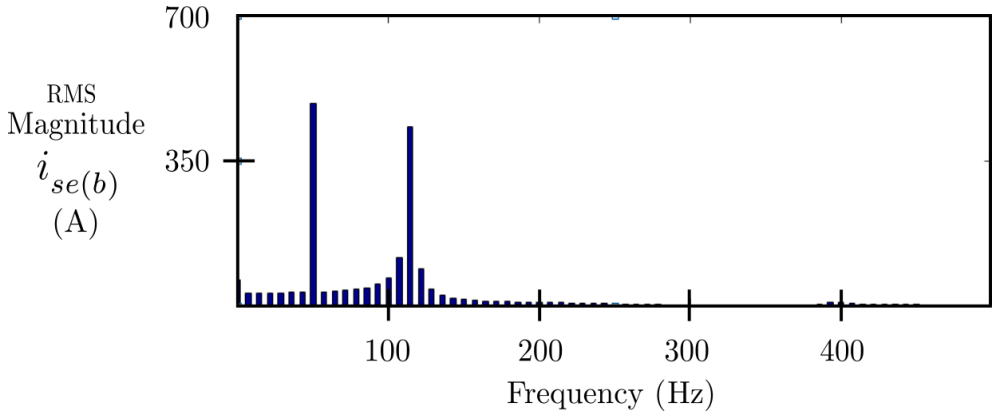


Figure 3.3: Harmonic Analysis of the $b$ phase Sending End Current of Fig. 3.1

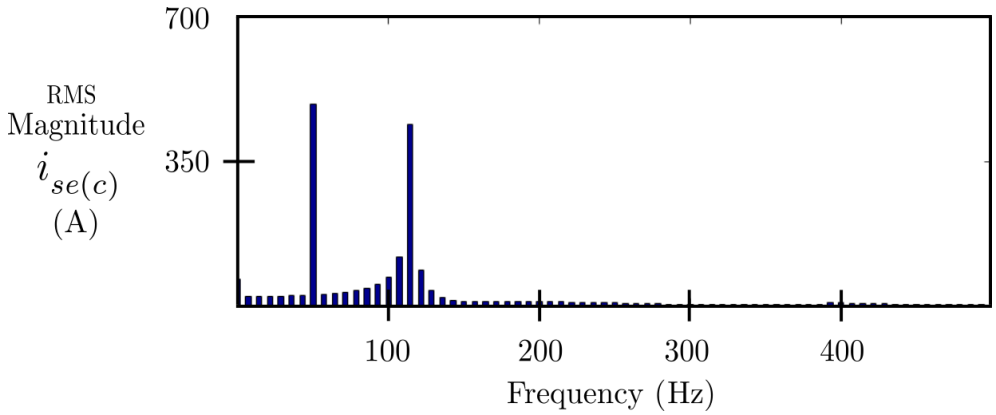


Figure 3.4: Harmonic Analysis of the $c$ phase Sending End Current of Fig. 3.1

The FFT analysis of the sending end current waveforms generated from the Bergeron's Model of PSCAD has been done at the switching instant of the line, choosing

the time window till the transients die down completely. The results of the FFT analysis are shown in the Figs. 3.2, 3.3 and 3.4. The maximum frequency content ($F_{i(max)}$) in the sending end line currents is found to be nearly 500 Hz. In this range of frequency, the change in the positive sequence line resistance and inductance due to the skin effect are negligible and so we obtain similar results both with the Frequency Dependent Model and the Bergeron's (constant frequency) Model.

## 3.4 Determination of $T_{ob}$ and $T_{sw}$

### 3.4.1 Constraints on Switching Period of the Power Electronic Converter

The switching frequency of the converter ($F_{sw}$) is kept atleast 10 times higher than the current control loop bandwidth to minimize the phase loss of the current control loop gain, which is again kept at 10 times the maximum frequency of the current signal to be tracked. So we can say that the minimum value of the switching frequency,

$$F_{sw(min)} = \frac{1}{T_{sw(max)}} = 10 \times 10 \times F_{i(max)} = 100 \times 500 = 50 \text{ kHz}$$

$$\Rightarrow T_{sw(max)} = 20\ \mu s\ \geq T_{sw} \tag{3.13}$$

Hence Silicon (Si) made Insulated Gate Bipolar Transistor (IGBT) based power electronic converter cannot be used to emulate the switching current transients of a transmission line as it cannot operate at such high switching frequencies. So a Silicon Carbide (SiC) based Metal Oxide Semiconductor Field Effect Transistor (MOSFET) converter is designed and developed to operate at a maximum switching frequency of 100 kHz.

$$\therefore T_{sw(min)} = 10\ \mu s\ \leq T_{sw} \tag{3.14}$$

### 3.4.2 Determination of Wave Travel Time

The length of the transmission line is considered to vary from 300 km to 500 km. Also we have seen in Chapter 2 that the wave velocity through the line depends on its inductance and capacitance per unit length. The wave velocity for the chosen line with the parameters shown in Table-2.1 is $2.78 \times 10^5$ km/s. Considering a standard set of line parameters [22], the range of wave velocity is found to vary from $2.5 \times 10^5$ km/s to $3 \times 10^5$ km/s. So the minimum wave travel time in the line,

$$\tau_{min} = \frac{300}{3 \times 10^5} = 1000\ \mu s \tag{3.15}$$

Similarly the maximum wave travel time in the line,

$$\tau_{max} = \frac{500}{2.5 \times 10^5} = 2000\ \mu s \tag{3.16}$$

### 3.4.3 Constraints on Observer Sampling Period

When voltage switching is done on a transmission line, a step voltage suddenly appears at the sending end of the transmission line. Now this applied step voltage, theoretically contains all possible frequency components. But in the current waveform we have seen that there is no component beyond 500 Hz. Since the system (Bergeron's Model) is a linear system, therefore we can say that it acts as a low pass filter with a cut-off frequency of 500 Hz. So we will come up with the same current waveforms even if we remove the components beyond 500 Hz from the input step voltage and apply it to the system (Bergeron's Model). Now to sample the input step voltage at a finite value of sampling frequency, we put an anti-aliasing filter before sampling the input. The cut-off frequency of the anti-aliasing filter ($F_{c(aa)}$) is kept at 5 kHz, so that there is negligible amount of phase loss to the components upto 500 Hz in the input step voltage. Also to provide sufficient guard band width, the minimum sampling frequency of the Observer is set at 5 times higher than the cut-off frequency of the anti-aliasing filter . So the maximum possible value of the Observer sampling period ,

$$T_{ob} \leq T_{ob(max)} = \frac{1}{5 \times F_{c(aa)}} = \frac{1}{5 \times (5 \times 10^3)} = 40\ \mu s \tag{3.17}$$

Therefore the minimum possible value of the size of FIFO Buffers is

$$N_{min} = \frac{\tau_{min}}{T_{ob(max)}} \tag{3.18}$$

$$\therefore N_{min} = \frac{1000}{40} = 25$$

In digital control of power converters, generally the controller output is updated at every switching period, $T_{sw}$. Therefore, it is not necessary to update the control loop reference signal coming from the Observer faster than this rate. Hence we can write,

$$T_{ob} \geq T_{sw} \tag{3.19}$$

Also as part of the Observer computations are done in every switching period of the power electronic converter, so we should ensure that,

$$T_{sw} \geq \Delta t + \frac{T_{obc}}{T_{ob}/T_{sw}} \tag{3.20}$$

where, $\Delta t$ is the time required to perform (i) Sensing and Signal Filtering, (ii) Closed-Loop Control and Duty Cycle Updation and (iii) Protection. $\Delta t$ is nearly 5 $\mu$s for the selected Zynq Processing System (PS). Substituting equation 3.12 in equation 3.20, we get

$$T_{sw} \geq \frac{5T_{ob}^2}{T_{ob}^2 - 1.66T_{ob} - 0.114\tau} \tag{3.21}$$

### 3.4.4 Steps to determine $N$, $T_{ob}$ and $T_{sw}$

In summary for a given $\tau$, $T_{ob}$ and $T_{sw}$ needs to satisfy equations 3.13, 3.14, 3.17, 3.19 and 3.21. For the line parameters provided in Table-2.1, the wave travel time for the line, $\tau = l\sqrt{LC} = 1440$ $\mu$s. Graphically this results in the shaded feasible region in the $T_{sw} - T_{ob}$ plane as shown in Fig. 3.5. Note here that the transmission line parameter $\tau$ affects determination of $T_{ob}$ and $T_{sw}$ through equation 3.21.

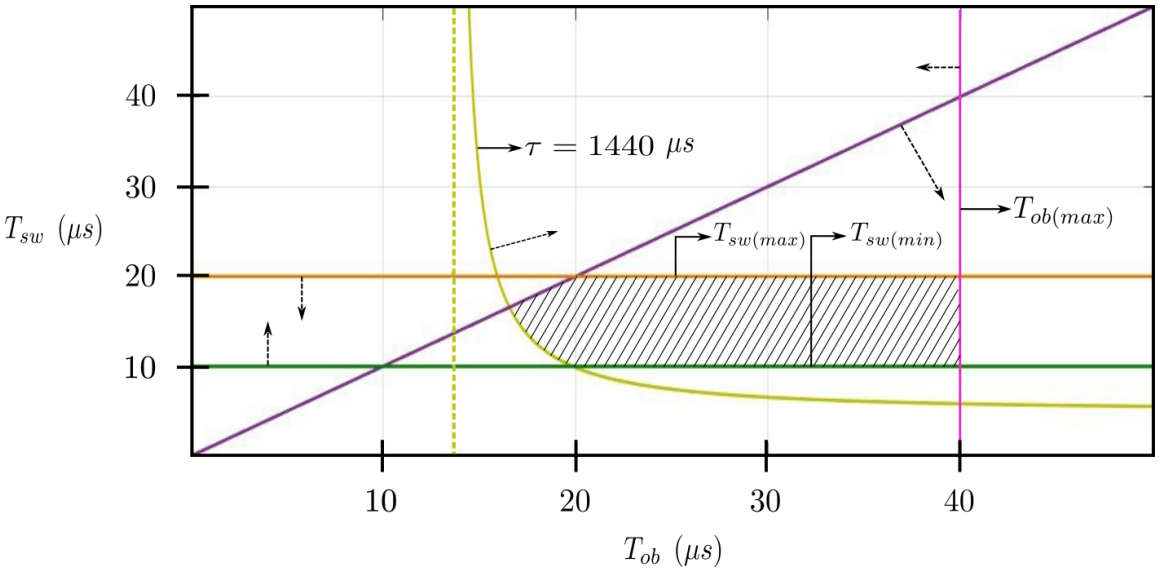


Figure 3.5: Feasible Region of $T_{ob}$ and $T_{sw}$ for $\tau = 1440$ $\mu$s

Substituting the extreme values of $\tau$ from equations 3.15 and 3.16 in equation 3.21, we come up with,

$$T_{sw} \geq \frac{5T_{ob}^2}{T_{ob}^2 - 1.66T_{ob} - 114} \tag{3.22}$$

and

$$T_{sw} \geq \frac{5T_{ob}^2}{T_{ob}^2 - 1.66T_{ob} - 228} \tag{3.23}$$

Fig. 3.6 shows how equation 3.21 changes for two extreme values of $\tau$. Based on this, a step by step procedure for selecting $N$, $T_{ob}$ and $T_{sw}$ is developed.

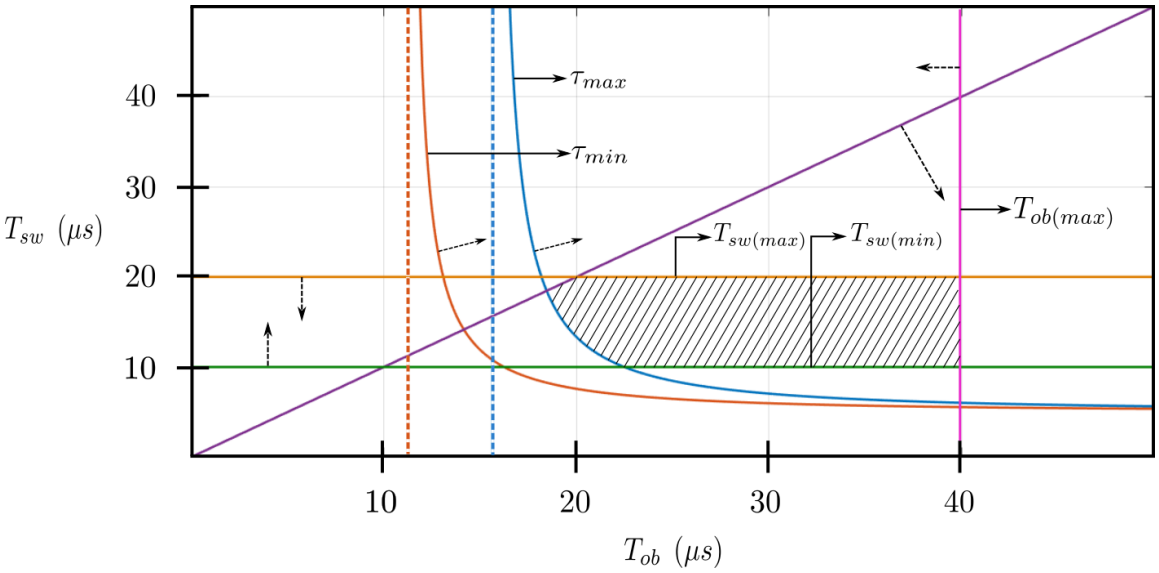


Figure 3.6: Feasible region of $T_{ob}$ and $T_{sw}$ for all possible values of $\tau$

**Step** 1 **- Determination of** $N$ **:** It is clear from Fig. 3.6, that for any value of $\tau$ it is possible to achieve $T_{ob}$ close to $T_{ob(max)}$ and $T_{sw}$ close to $T_{sw(max)}$. From equation 3.12, it can be seen that $T_{obc}$ reduces on maximizing the value of $T_{ob}$ for a given value of $\tau$. Hence the buffer size, $N$ is chosen as,

$$N = \left[\frac{\tau}{T_{ob(max)}}\right]_{ceil} \tag{3.24}$$

where the ceiling function $[x]_{ceil}$ rounds off $x$ to nearest higher integer.

**Step** 2 **- Determination of** $T_{ob}$ **:**

$$T_{ob} = \frac{\tau}{N} \tag{3.25}$$

Therefore it is ensured that the chosen $T_{ob}$ is always less than $T_{ob(max)}$.

**Step** 3 **- Determination of** $T_{sw}$ **:** In order to reduce the switching loss in the power electronic converter, $T_{sw}$ is selected on the higher side of its range, i.e. close to $T_{sw(max)}$. At the same time, for ease of implementation in the digital platform, $T_{sw}$ is chosen such that, $T_{ob}$ becomes an integral multiple of $T_{sw}$. Hence $T_{sw}$ is chosen as,

$$T_{sw} = \frac{T_{ob}}{\left[\frac{T_{ob}}{T_{sw(max)}}\right]_{ceil}} \tag{3.26}$$

## 3.5 Observer Development in MATLAB/Simulink

As shown in Fig. 3.7, a block has been developed in MATLAB/Simulink which acts as an Observer to solve the distributed parameter transmission line. The development of the block is based on the equations 3.6, 3.10 and 3.11. Considering the line parameters provided in Table-2.1 and using equations 3.24 and 3.25, the buffer size as well as the the sampling time period of the Observer has been chosen as shown below.

$$N = \left[\frac{1440}{40}\right]_{ceil} = 36$$

and

$$T_{ob} = \frac{1440}{36} = 40\ \mu s$$

Now as the reference current generated by the Observer gets updated at every $T_{ob}$, we need to hold this value since the closed loop control and duty update of the VSC takes place at every $T_{sw}$. This is done by using a Zero Order Hold (ZOH). Voltage switching action of the transmission line, as shown in Fig. 2.1 is then simulated with the parameters provided in Table-2.1. The corresponding waveforms of the simulation in MATLAB/Simulink are shown in Fig. 3.8. *So we see that the output of the developed Observer in the MATLAB/Simulink (Fig.* 3.8*) matches well with the Bergeron's Model of PSCAD (Fig.* 3.1*).* Hence this justifies that the choice of the Observer sampling time period as well as the buffer size as suggested in this chapter are correct.

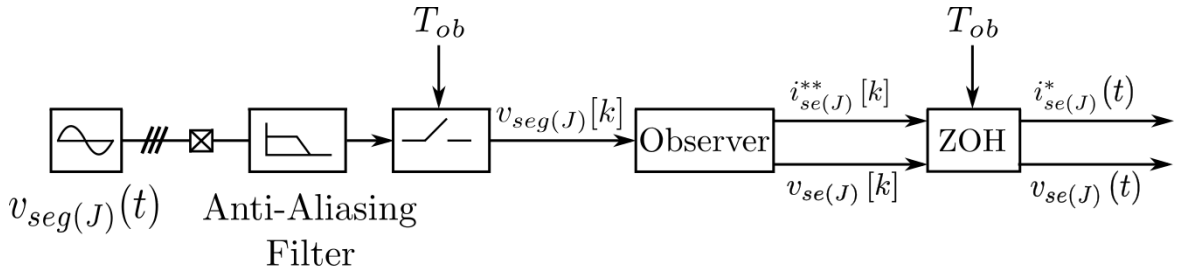


Figure 3.7: Block Diagram of Observer Simulation in MATLAB/Simulink software

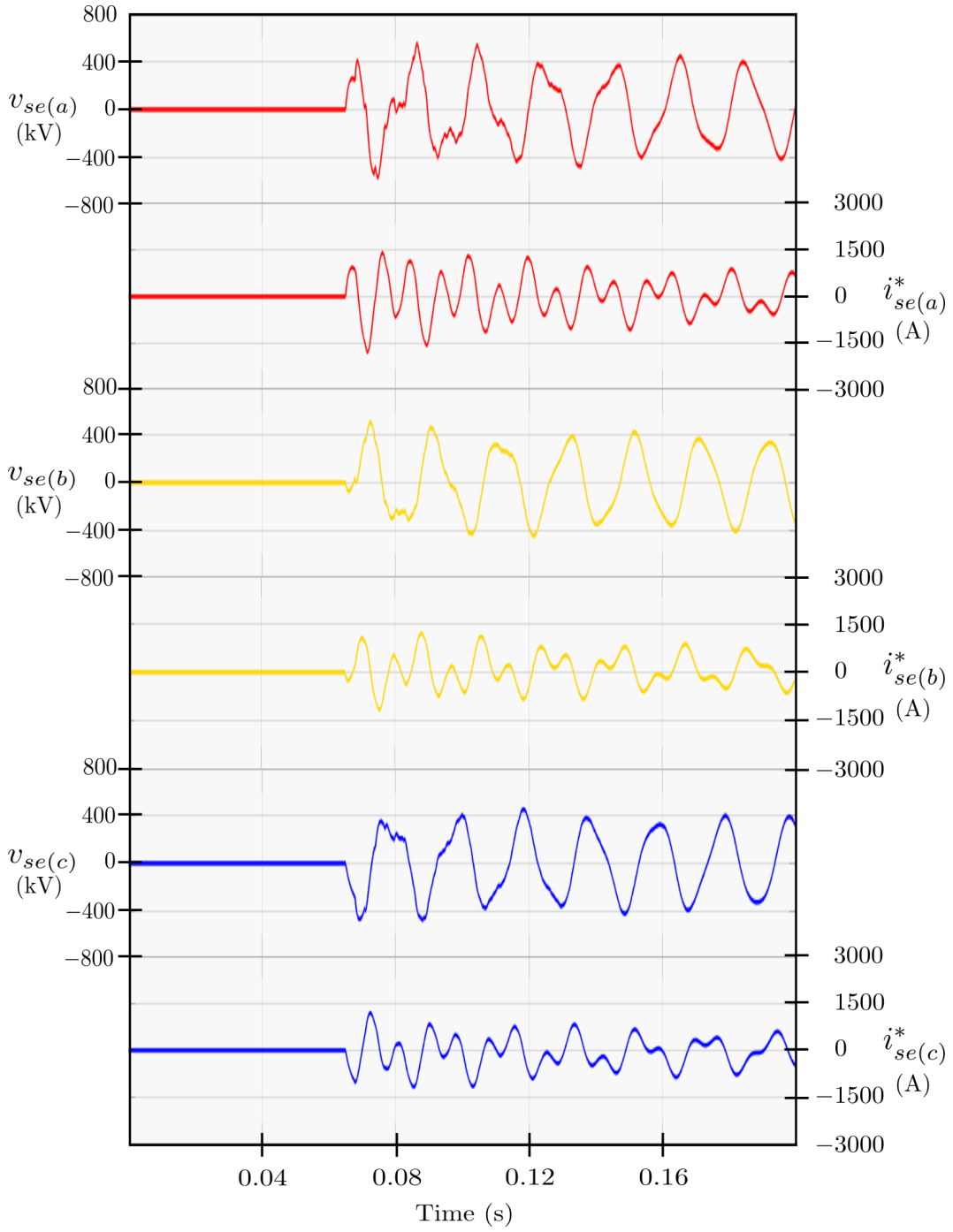


Figure 3.8: Sending End Voltage and Current Waveforms for the Simulation of the Circuit shown in Fig. 2.1 with the parameters given in Table-2.1 using the developed Observer in MATLAB/Simulink software

## 3.6 Summary

1. For avoiding complex interpolation schemes, it is ensured that the wave travel time in the line becomes an integral multiple of the sampling time period of the Observer.

2. The maximum and minimum possible values of the sampling time period of the Observer as well as the switching period of the power electronic converter has been evaluated.

3. Given the value of the wave travel time in the line and adhering to the constraints of the digital and power hardware, the values of the sampling period of the Observer and the switching period of the power electronic converter can be found out using the proposed algorithm.

4. The results obtained from the Bergeron's Model in PSCAD and the developed Observer in MATLAB/Simulink are verified.

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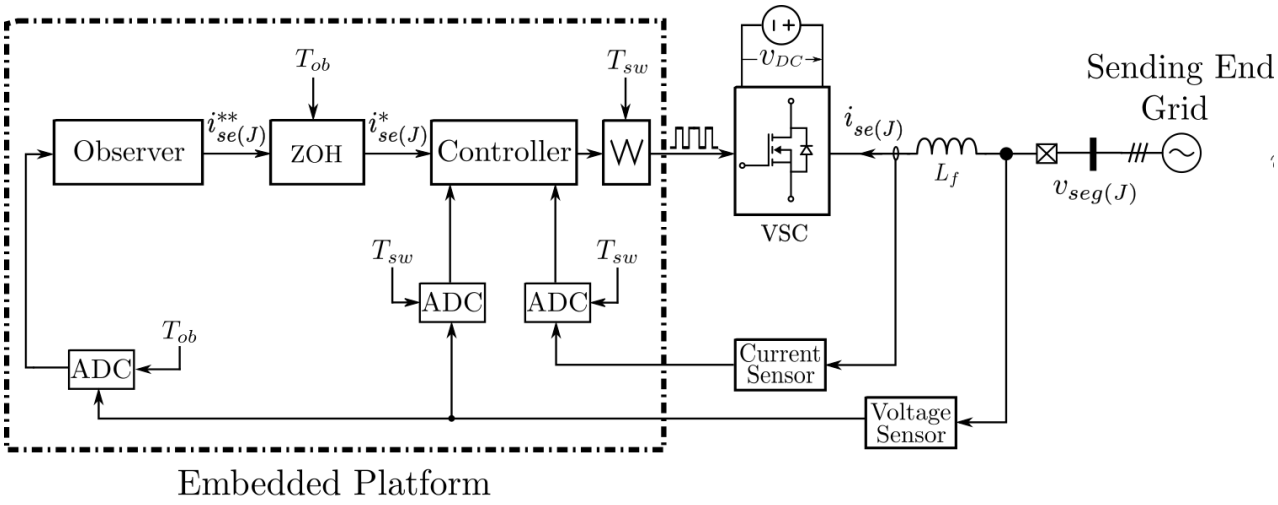
# Chapter 4

# Hardware Implementation of the Transmission Line Emulator System

In the previous chapter, we have shown how to implement the chosen numerical scheme on a digital platform to solve the distributed parameter, lossy transmission line in real-time. Hence this model will act as an Observer which will take up the instantaneous sending end grid voltages ($v_{seg(J)}$) of the transmission line as input and give the corresponding line end voltages and currents ($v_{se(J)}$ $i^{**}_{se(J)}$) as output. The sending end of the transmission line can be emulated by a $3\phi$ Voltage Source Converter (VSC), where we need to control the line currents of the VSC to track the currents provided by the Observer. So we design and develop a $3\phi$, 2-level modular type SiC MOSFET based VSC with the specifications given in Table-4.1. The detailed design procedure and hardware development of the SiC based power electronic converter is discussed in Appendix *A*. The Transmission Line Emulator (TLE) scheme is shown in Fig. 4.1. In this chapter we will discuss the hardware implementation of the laboratory scale TLE.

Table 4.1: Specifications of the developed Power Amplifier

| **Sl.No.** | **Parameter** | **Value** |
|---|---|---|
| 1 | Apparent power rating, $S_{rated}$ | 12.5 kVA |
| 2 | Switching frequency, $F_{sw}$ | 100 kHz |
| 3 | DC bus voltage, $V_{DC}$ | 800 V |
| 4 | $3\phi$ Line-Line (RMS) voltage, $V_{L-L(RMS)}$ | 415 V |
| 5 | Line frequency, $F_{line}$ | 50 Hz |




$$J \epsilon \{a, b, c\}$$

Figure 4.1: Schematic showing Transmission Line Emulation by Power Electronic Converter

## 4.1 Implementation Aspects

### 4.1.1 Scaling Down of the Actual System

For emulating the transmission line using laboratory level power electronic hardware, we need to scale down the system from actual power level to the power level which can be safely handled in the lab. But while scaling we should ensure that the system dynamics remains unaltered. Hence the wave velocity in both the actual and the scaled down transmission line should be same. The rated values of the $3\phi$ Line-Line (RMS) voltage ($V_{LL(RMS)}$) and the apparent power of the original system ($S_{3\phi}$) are taken as the base quantities for the actual system. With the parameters of the actual system provided in Table-2.1, the base impedance of the actual system can be written as,

$$Z_{(B)} = \frac{\left(V_{LL(RMS)}\right)^2}{S_{3\phi}} = \frac{\left(400 \times 10^3\right)^2}{500 \times 10^6} = 320\ \Omega \tag{4.1}$$

Now the base current in the actual system is,

$$I_{(B)} = \frac{S_{3\phi(B)}}{\sqrt{3} \times V_{(B)}} = \frac{500 \times 10^6}{\sqrt{3} \times 400 \times 10^3} = 721.69\ \text{Amp} \tag{4.2}$$

From Fig. 3.1 it is seen that the phase getting switched at the peak of its voltage, carries current of higher magnitude than the other phases during the transients. Therefore the maximum value of current ($I_m$) occurs in $a$ phase, which is nearly 1800 Amp. In terms of per unit, it can be expressed as, $I_{m(pu)} = \frac{1800}{721.69} = 2.5$. Now with

reference to the ratings of the device used in the VSC, the maximum possible value of current in the scaled down system ($I'_m$) is set at 28 Amp. Since the per unit values are same both in the original and the scaled down system for the conservation of the system dynamics, therefore the base current in the scaled down system can be obtained as,

$$I'_{(B)} = \frac{28}{2.5} = 11.2 \text{ Amp} \tag{4.3}$$

Choosing the voltage base of the scaled down system ($V'_{LL(RMS)}$) as 220 V, the base impedance of the scaled down system can be written as,

$$Z'_{(B)} = \frac{V'_{LL(RMS)}}{\sqrt{3} \times I'_{(B)}} = \frac{220}{\sqrt{3} \times 11.2} = 11.34\ \Omega \tag{4.4}$$

Denoting $R'$, $L'$ and $C'$ as the line resistance, inductance and capacitance per unit length of the scaled down transmission line system, we can write

$$R' = R \times \frac{Z'_{(B)}}{Z_{(B)}} \tag{4.5}$$

$$L' = L \times \frac{Z'_{(B)}}{Z_{(B)}} \tag{4.6}$$

and (4.7)

$$C' = C \times \frac{Z_{(B)}}{Z'_{(B)}} \tag{4.8}$$

Therefore the travel time of the wave in the scaled down transmission line,

$$\tau' = l \times \sqrt{L'C'} = l \times \sqrt{LC} = \tau \tag{4.9}$$

Similarly the value of the grid inductance and the line end reactor for the scaled down system can be obtained as,

$$L'_g = L_g \times \frac{Z'_{(B)}}{Z_{(B)}} \tag{4.10}$$

and (4.11)

$$L'_{sh} = L_{sh} \times \frac{Z'_{(B)}}{Z_{(B)}} \tag{4.12}$$

The parameters of the original and scaled down system are given in Table-4.2 and Table-4.3 respectively.

Table 4.2: Parameters of the Original Transmission Line System

| $Z_{(B)}$ | $R$ | $L$ | $C$ | $L_g$ | $L_{sh}$ |
|---|---|---|---|---|---|
| 320 Ω | 0.03 Ω/km | 1 mH/km | 12.96 nF/km | 0.25 H | 10.2 H |

Table 4.3: Parameters of the Scaled Down Transmission Line System

| $Z'_{(B)}$ | $R'$ | $L'$ | $C'$ | $L'_g$ | $L'_{sh}$ |
|---|---|---|---|---|---|
| 11.34 Ω | 1.063 mΩ/km | 35.4375 $\mu$H/km | 0.3657 $\mu$F/km | 9.03 mH | 0.36146 H |

### 4.1.2 Emulation of Transmission Line Losses

As the line emulated is a lossy line, so some active power ($P_{se}$) will be drawn from the sending end grid. This is actually the resistive loss occurring in the transmission line. So as shown in Fig. 4.2, this loss will be absorbed by the dc voltage source. But generally the available dc voltage sources do not have the capability to sink power. So to mitigate this problem, an Active Front End Converter (AFEC) is used to implement the dc source. The AFEC will maintain the required dc bus voltage and supply for the losses in the converter switches as well as absorb the resistive losses occurring in the emulated line. The controller design algorithm for the AFEC is discussed in Appendix $B$.

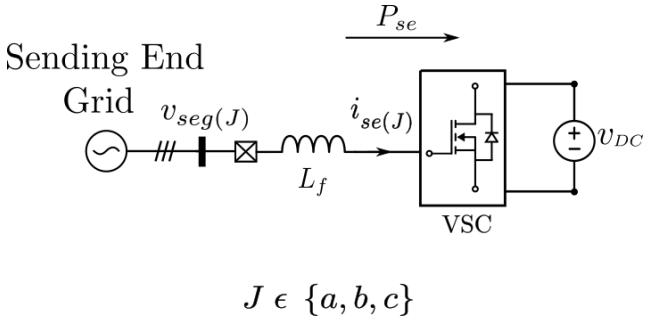
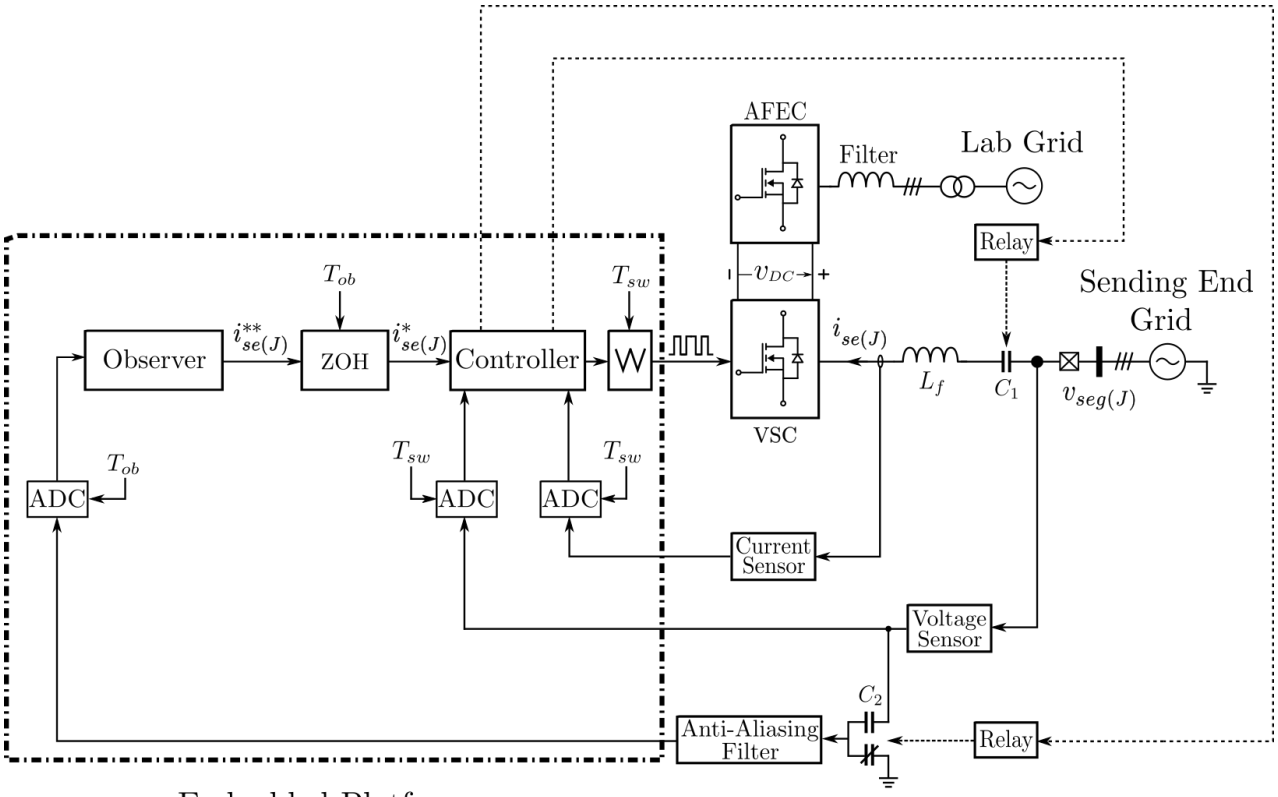



Figure 4.2: Schematic showing Transmission Line losses flowing into DC Bus

## 4.2 Proposed Scheme of Implementation of the Transmission Line Emulator Test Bench

Since the switching phenomenon of the transmission line will be emulated by a grid tied VSC, therefore the VSC should be properly synchronized to the grid before the emulation is being done. Hence we will make the VSC get connected to the grid and operate in current control mode with reference ($i^*_{se(J)}$) set at zero before the emulation

takes place. The sequence of connecting the converter to the grid is discussed in Section $A.7.3$ of Appendix $A$. Again to emulate the switching of the transmission line at different values of the phase voltage, we need to extract the voltage information of the grid before switching. To mitigate this problem we will use relay and contactors ($C_1$ and $C_2$) which will be controlled from the embedded system itself as shown in Fig. 4.3. For having the flexibility of implementing a programmable grid impedance in the experimental setup, a strong grid (sinusoidal voltage source) is used and the inductive grid impedance is emulated inside the embedded platform.




$$J \in \{a, b, c\}$$

Figure 4.3: Proposed Scheme for the Hardware Implementation of the TLE

The VSC is run in standalone mode generating the output voltage of same magnitude, frequency and phase as that of the grid. Once the grid synchronization is being done the contactor $C_1$ is closed and the VSC starts operating in zero current control mode. Then depending on the desired instant of switching, the contactor $C_2$ is energized thereby applying a step voltage at the input of the anti-aliasing filter, which passes the low frequency components (less than its cut-off frequency) to the Observer. This starts the emulation process and the VSC tracks the current generated by the Observer. The proposed scheme of the TLE setup is shown in Fig. 4.3.

## 4.3 Summary

1. For emulating the transmission line, the current references provided by the Observer needs to be tracked by the grid tied VSC.

2. A $3\phi$, $2-$level modular type VSC is designed and developed with the following specifications : a) $S_{rated}$ = 12.5 kVA, b)$F_{sw}$ = 100 kHz, c) $V_{DC}$ = 800 V, d)$V_{L-L(RMS)}$ = 415 V and e)$F_{Line}$ = 50 Hz.

3. Without compromising on system dynamics, the parameters of the actual transmission line system has been scaled for implementation of the TLE using laboratory level hardware.

4. The dc source is implemented by AFEC, to maintain the required dc bus voltage and also to absorb the resistive losses of the emulated line as well as to supply the losses in the converter switches and filters.

5. To have the flexibility of emulating the switching of the transmission line at different values of the phase voltage, relays and contactors are used for controlled switching.

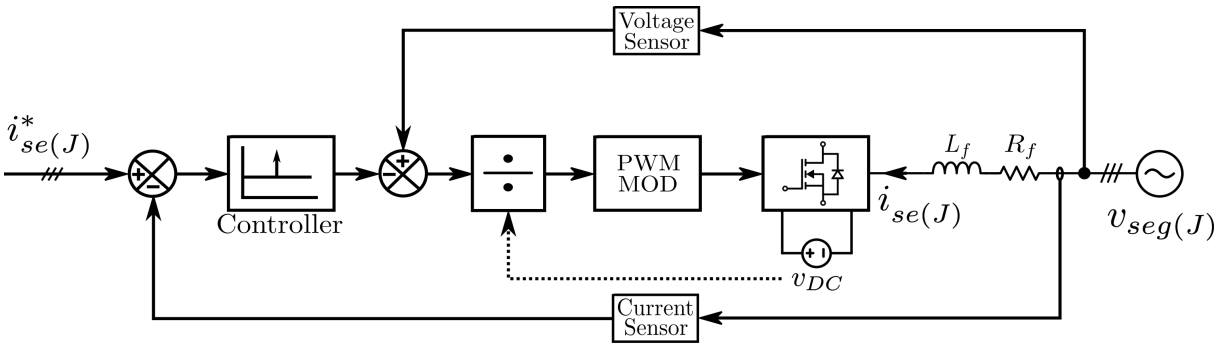
# Chapter 5

# Controller Design for Power Amplifier

As discussed in Chapter 4, the power electronic converter emulating the sending end of the transmission line, needs to be controlled in current control mode in order to track the reference currents generated by the Observer. So in this chapter we will elaborately discuss about the selection of the controller architecture and its design for achieving the required performance.

## 5.1 Controller (architecture) Selection for TLE

Control of the VSC for transmission line emulation requires regulation of the current drawn from the grid. A popular method for implementing closed loop control of such a system is based on Synchronous Reference Frame (SRF) theory, where independent control of active and reactive powers can be achieved in the '$dq$' frame.




$J \in \{a, b, c\}$

Figure 5.1: Control Loop Structure of the Converter Emulating Transmission Line

For this we need a Synchronous Reference Frame-Phase Lock Loop (SRF-PLL) to track the phase angle of the sending end grid voltage ($v_{seg(J)}$). In Chapter 3 we have seen that although the frequency of the grid voltage is 50 Hz but the sending end current drawn by the transmission line at the instant of switching has frequency components upto 500 Hz. So applying Clarke and Park Transformation on these currents with the phase obtained from the SRF-PLL will result in ac terms on the $d$ and $q$ axis. So the Proportional Integral (PI) controller which otherwise works well for tracking dc quantities will fail in this case. So we need such a controller which does not need the phase information of the grid voltage and can track current of frequency components upto 500 Hz. Proportional Resonant (PR) controller [33–36] is one such controller which can do this if the control loop bandwidth is kept more than 5 kHz.

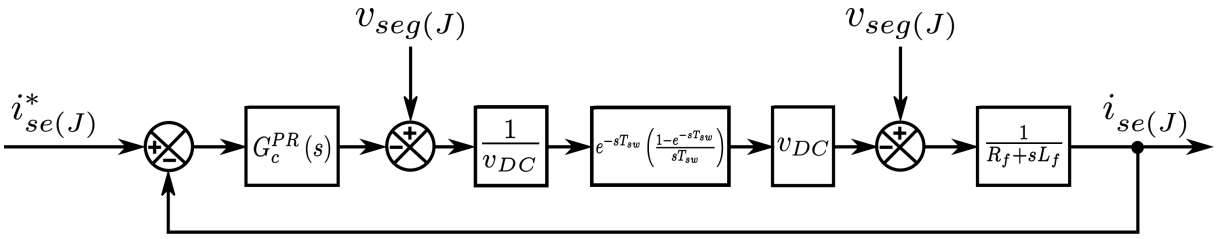
### 5.1.1 Design of PR Controller

Fig. 5.2 shows the block diagram of the current control loop in natural ($abc$) reference frame. The current controller transfer function, $G_c^{PR}(s)$ is given by,

$$G_c^{PR}(s) = K_{pr} + \frac{sK_{ir}}{s^2 + \omega_\circ^2} \tag{5.1}$$

$$\Rightarrow G_c^{PR}(s) = K_{pr}\frac{s^2 + s\frac{K_{ir}}{K_{pr}} + \omega_\circ^2}{s^2 + \omega_\circ^2} \tag{5.2}$$

Here $K_{pr}$ is the proportional gain, $K_{ir}$ is the resonant gain and $\left\{\frac{sK_{ir}}{s^2+\omega_\circ^2}\right\}$ is the Resonant Integrator (RI) part. *The resonant frequency, $\omega_\circ$ is chosen to be equal to the nominal grid frequency which is* 314.16 *rad/s since once the transient dies down, the VSC will be drawing* 50 *Hz ac currents from the connected grid.* Ideally the PR controller gives very high gain only at $\omega_\circ$. However in reality, significant gain could be provided at the vicinity of $\omega_\circ$ by changing the the ratio $\frac{K_{ir}}{K_{pr}}$ [37–39]. As shown in Fig. 5.2, the grid voltage is feed forwarded in order to reduce the controller output. $R_f$ and $L_f$ are the line filter resistance and inductance respectively.




$J \in \{a, b, c\}$

Figure 5.2: Block Diagram representation of Fig. 5.1

Denoting $T_{sw}$ as the switching time period of the VSC, the converter transfer function, $G_{conv}(s)$ can be modeled as $v_{DC}$ along with a delay of $e^{-sT_{sw}}$ due to duty update in the next switching cycle. The gain of the Pulse Width Modulation (PWM) modulator can be modeled by a Zero Order Hold (ZOH) whose transfer function is given by $\left\{\frac{1-e^{-sT_{sw}}}{sT_{sw}}\right\}$. Therefore the combined gain ($G_D(s)$) of the duty update delay and the PWM modulator can be written as,

$$G_D(s) = e^{-sT_{sw}}\left(\frac{1-e^{-sT_{sw}}}{sT_{sw}}\right) = e^{-\frac{3}{2}sT_{sw}}\left(\frac{e^{\frac{sT_{sw}}{2}}-e^{\frac{-sT_{sw}}{2}}}{sT_{sw}}\right)$$

$$\Rightarrow G_D(j\omega) = \frac{\sin\frac{\omega T_{sw}}{2}}{\frac{\omega T_{sw}}{2}}e^{-j\frac{3}{2}\omega T_{sw}}$$

In the low frequency region, i.e. $\frac{\omega T_{sw}}{2} \ll 1$, the above transfer function can be approximately written as,

$$G_D(s) \approx \frac{1-s\frac{3}{4}T_{sw}}{1+s\frac{3}{4}T_{sw}} \tag{5.3}$$

Therefore the overall open loop transfer function becomes,

$$G_{oltf}^{TLE}(s) = G_c^{PR}(s) \times \frac{1-s\frac{3}{4}T_{sw}}{1+s\frac{3}{4}T_{sw}} \times \frac{\frac{1}{R_f}}{1+\frac{L_f}{R_f}s}$$

$$\therefore G_{oltf}^{TLE}(s) = K_{pr}\frac{s^2+s\frac{K_{ir}}{K_{pr}}+\omega_\circ^2}{s^2+\omega_\circ^2} \times \frac{1-s\frac{3}{4}T_{sw}}{1+s\frac{3}{4}T_{sw}} \times \frac{\frac{1}{R_f}}{1+\frac{L_f}{R_f}s} \tag{5.4}$$

With $R_f = 0.2\ \Omega$ and $L_f = 0.5$ mH for the selected filter, the corner frequency of the filter is $\left\{\frac{R_f}{2\pi L_f} = 63.66\ Hz\right\}$. *In order to make the closed loop gain of the transfer function shown in equation* 5.4 *as zero dB for frequencies upto* 500 *Hz, we choose the gain cross-over frequency ($\omega_{gc}$) for the transfer function as* 5 *kHz. This will also ensure that there is negligible amount of phase loss for the frequency components upto* 500 *Hz.* Therefore we can write,

$$\left|G_{oltf}^{TLE}(j\omega)\right|_{\omega=\omega_{gc}} \approx \frac{K_{pr}}{L_f \times \omega_{gc}} = 1$$

$$\Rightarrow K_{pr} = L_f \times \omega_{gc} = 0.5 \times 10^{-3} \times 2\pi \times 5000 \approx 15.71 \tag{5.5}$$

$K_{ir}$ is evaluated by equating the gain of $G_{oltf}^{TLE}(s)$ to 20 dB at a frequency of 500 Hz, i.e.

$$\left|G_{oltf}^{TLE}(j\omega)\right|_{\omega=2\pi\times500} \approx \sqrt{K_{pr}^2+\left(\frac{K_{ir}}{2\pi\times500}\right)^2} \times \frac{\frac{1}{0.2}}{\sqrt{1+\left(\frac{2\pi\times500\times0.5\times10^{-3}}{0.2}\right)^2}} = 10$$

$$\Rightarrow \left(\frac{K_{ir}}{2\pi \times 500}\right)^2 = (15.83)^2 - K_{pr}^2$$

$$\Rightarrow K_{ir} = 2\pi \times 500 \times 1.945 \approx 6110$$

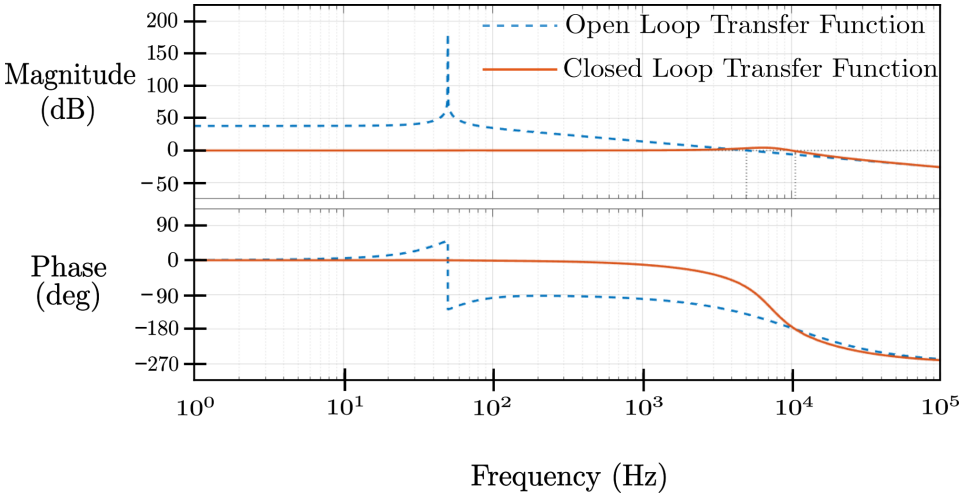



Figure 5.3: Bode Diagram of the Current Control Loop of Fig. 5.2

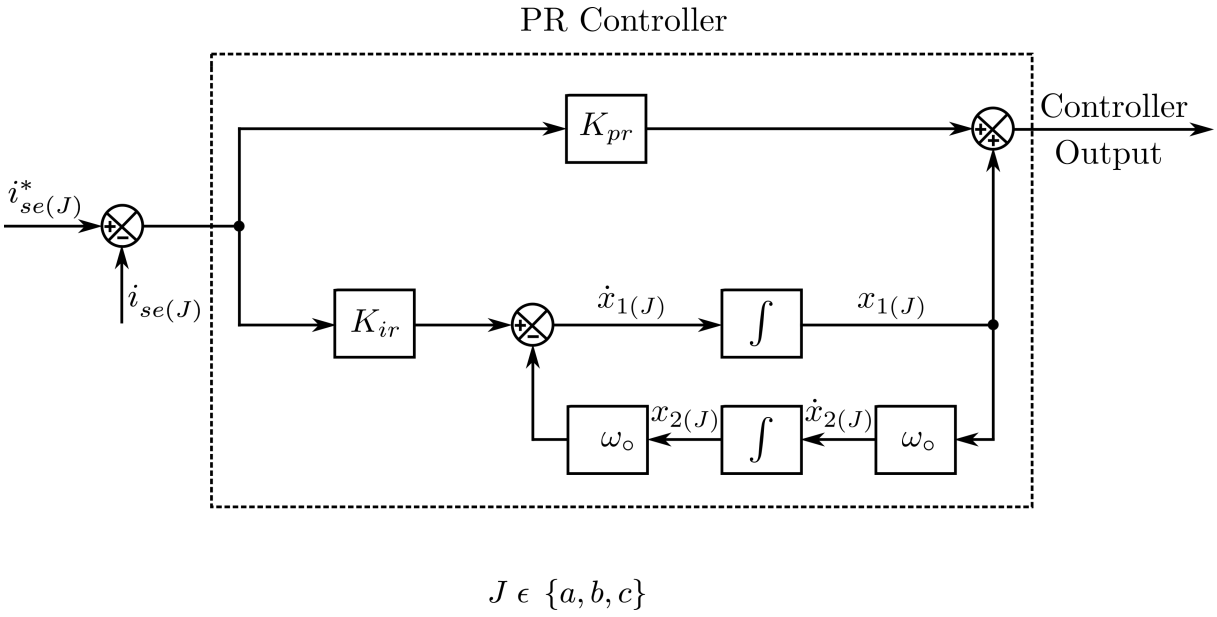
Table 5.1: Parameters of the Controller used in the VSC of the TLE

| **Sl.No.** | **Parameter** | **Value** |
|---|---|---|
| 1 | Converter switching frequency, $F_{sw}$ | 50 kHz |
| 2 | Nominal grid frequency, $F_{line}$ | 50 Hz |
| 3 | Filter inductance, $L_f$ | 0.5 mH |
| 4 | Filter resistance, $R_f$ | 0.2 Ω |
| 5 | Gain cross-over frequency, $\omega_{gc}$ | 5 kHz |
| 6 | $K_{pr}$ | 15.71 |
| 7 | $K_{ir}$ | 6110 |
| 8 | Phase margin | 39.6° |

The bode diagram of the transfer function given by equation 5.4 is plotted with the parameters of Table-5.1. From Fig. 5.3, we can see that the gain and phase of the closed loop transfer function for frequency components upto 500 Hz are zero dB and zero deg respectively, thereby ensuring accurate tracking of the current references generated by the Observer.

## 5.2 Digital Implementation of the PR Controller

For digital implementation of the PR controller, the continuous domain transfer function of RI needs to be mapped in discrete domain. Literature shows several methods of discretization for RI whose relative merits and demerits are discussed in [40]. However the two most preferred methods are Two Integrator with Forward and Backward (TIFB) Euler approximations and Tustin with Prewarping (TP) [41–43]. Discretization of RI by TP method results in trigonometric expressions as a function of resonant frequency $\omega_\circ$ in the discretized transfer function. This necessitates online calculation of trigonometric functions or maintaining a look up table. Hence the complexity in implementing along with the number of computations increases with this method. Alternatively TIFB method does not require online calculation of trigonometric function or lookup table thereby utilizing very less resources and enabling faster computation. Also the problem of shift in resonant frequency due to discretization by TIFB becomes insignificant in case the ratio of calculation frequency to resonant frequency is large [42]. Hence in this work we will use TIFB method.




$$J \in \{a, b, c\}$$

Figure 5.4: Block Diagram structure of PR Controller in Continuous Time Domain

The block diagram structure of the PR controller in continuous time domain is shown in Fig. 5.4. After discretization by TIFB, the difference equations of the RI can be expressed as,

$$x_{1(J)}[k] = x_{1(J)}[k-1] + \left\{ K_{ir} \times \left( i^*_{se(J)}[k] - i_{se(J)}[k] \right) \times T_{sw} \right\} - \left\{ x_{2(J)}[k-1] \times \omega_\circ \times T_{sw} \right\} \tag{5.6}$$

and

$$x_{2(J)}[k] = x_{2(J)}[k-1] + \left(x_{1(J)}[k] \times \omega_\circ \times T_{sw}\right) \tag{5.7}$$

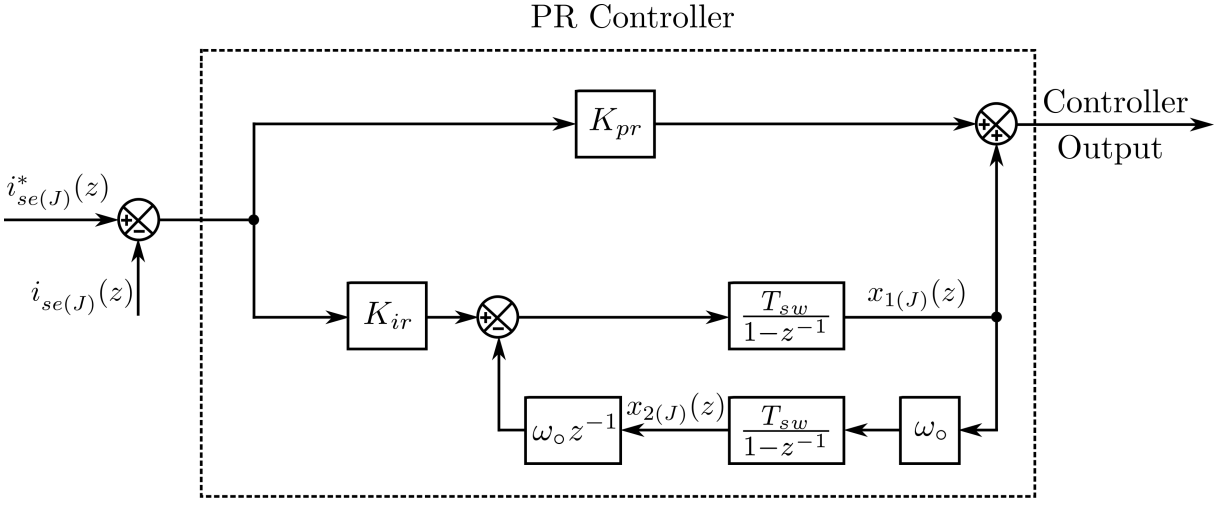
Denoting $\left(i^*_{se(J)}[k] - i_{se(J)}[k]\right)$ as $e_{(J)}[k]$ and taking Z Transform of the equations 5.6 and 5.7, we can write

$$x_{1(J)}(z) = \frac{K_{ir}T_{sw}e_{(J)}(z) - z^{-1}\omega_\circ T_{sw}x_{2(J)}(z)}{1 - z^{-1}} \tag{5.8}$$

and

$$x_{2(J)}(z) = \frac{\omega_\circ T_{sw}}{1 - z^{-1}}x_{1(J)}(z) \tag{5.9}$$

respectively. The corresponding block diagram structure of the PR controller in discrete time domain is shown in Fig. 5.5.




$$J \,\epsilon\, \{a, b, c\}$$

Figure 5.5: Block Diagram structure of PR Controller in Discrete Time Domain

Substituting equation 5.9 in 5.8, we get

$$\frac{x_{1(J)}(z)}{e_{(J)}(z)} = \frac{\left(1 - z^{-1}\right) K_{ir}T_{sw}}{1 - \left(2 - (\omega_\circ T_{sw})^2\right) z^{-1} + z^{-2}} \tag{5.10}$$

Therefore the controller transfer function implemented in the discrete time domain can be written as,

$$G_c^{PR}(z) = K_{pr} + \frac{\left(1 - z^{-1}\right) K_{ir}T_{sw}}{1 - \left(2 - (\omega_\circ T_{sw})^2\right) z^{-1} + z^{-2}} \tag{5.11}$$

Considering the duty update delay and using ZOH for incorporating the PWM modulator, the discrete domain transfer function of the overall system can be written as,

$$G_{oltf}^{TLE}(z) = G_c^{PR}(z) \times z^{-1} \times \left(1 - z^{-1}\right) \times \mathbf{Z}\left[\mathbf{L}^{-1}\left\{\frac{1}{s(R_f + sL_f)}\right\}\right]$$

$$\Rightarrow G_{oltf}^{TLE}(z) = \left[K_{pr} + \frac{\left(1 - z^{-1}\right) K_{ir} T_{sw}}{1 - \left(2 - (\omega_{\circ} T_{sw})^2\right) z^{-1} + z^{-2}}\right] \times \left[\frac{z^{-2}}{R_f}\left(\frac{1 - e^{-\frac{R_f T_{sw}}{L_f}}}{1 - z^{-1} e^{-\frac{R_f T_{sw}}{L_f}}}\right)\right] \tag{5.12}$$

Using the parameters of Table-5.1, the bode plot of the current control loop of Fig. 5.2 is shown in Fig. 5.6 for both the continuous and discrete time domain transfer functions given by equations 5.4 and 5.12 respectively.

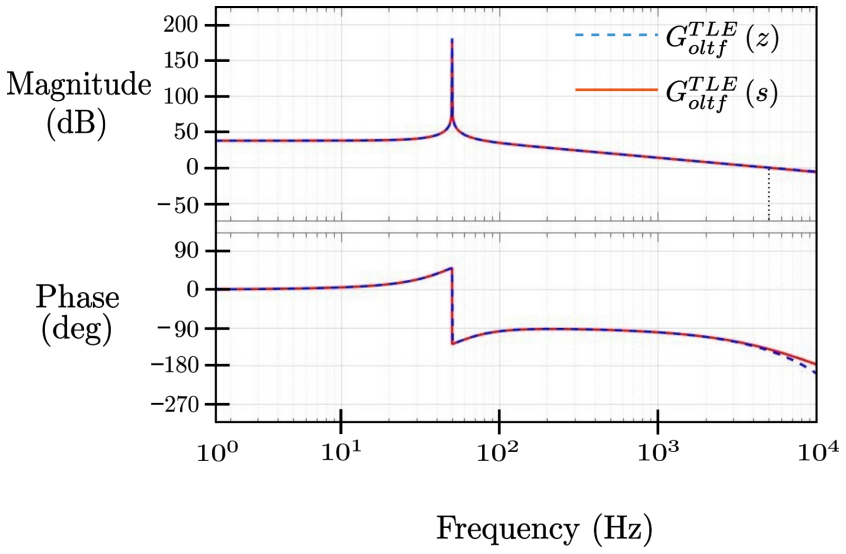



Figure 5.6: Bode Diagram of the Current Control Loop of Fig. 5.2 in both Continuous and Discrete Time Domain

From Fig. 5.6, we can see that both the magnitude and phase plots of the continuous and discrete domain transfer functions are identical for frequencies below $\omega_{gc}$, i.e. 5 kHz. Hence this justifies the controller design and implementation on a digital platform.

## 5.3 Summary

1. The line currents of the $3\phi$ VSC needs to be regulated for emulating the transmission line.

2. During the instant of switching the transmission line, the sending end line currents contain frequency components upto 500 Hz.

3. Therefore applying Clarke and Park Transformation on these currents with the phase information of the grid voltage (whose frequency is 50 Hz) will result in ac terms on the $d$ and $q$ axis.

4. So instead of using a PI controller, we choose a PR controller to track the reference currents generated by the Observer.

5. The design of the PR controller along with its implementation on a digital platform has been elaborately discussed in this chapter.

# Chapter 6

# Simulation and Experimental Results

A prototype of the TLE as shown in Fig. 6.1 has been fabricated in the laboratory to verify the proposed emulation scheme. The corresponding hardware setup of the developed TLE test bench is shown in Fig. 6.2. The Observer is implemented on a Zynq SoC XC7Z010-1CLG400C from Xilinx.

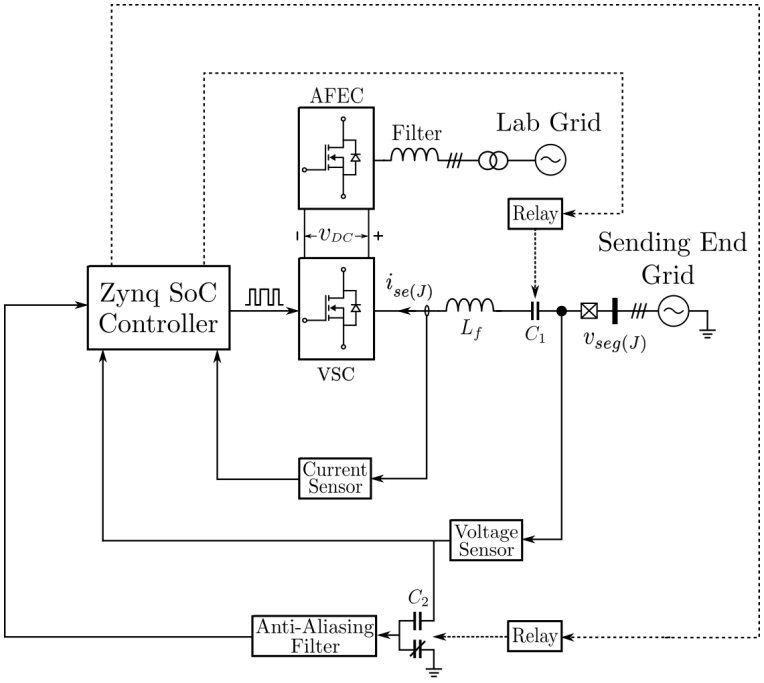



Figure 6.1: Prototype Schematic of the Transmission Line Emulator Test Bench

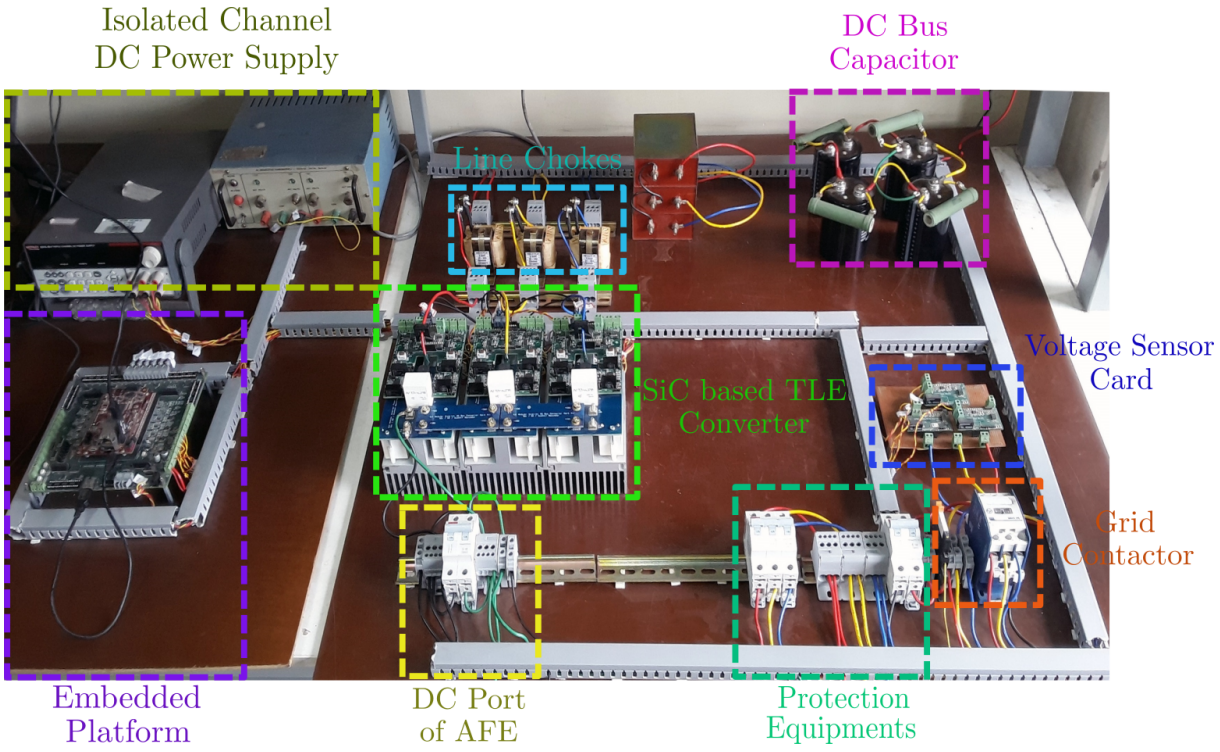



Figure 6.2: Hardware Setup of the Transmission Line Emulator Test Bench

Design of the SiC based power electronic converter has been elaborately discussed in Appendix *A*. The relevant simulation and experimental results are verified in this chapter to validate the developed TLE.

## 6.1 Parameters and Test Conditions

With constant values of line parameters, grid impedance and shunt reactor, the transients in the line currents are studied for 3 different values of line length ($l$). The system parameters of the original system and scaled down system are provided in Table-6.1 and 6.2 respectively. From equation 4.9, the travel time of the wave in the emulated transmission line is given by,

$$\tau = l \times \sqrt{LC} = l \times \sqrt{L'C'} \tag{6.1}$$

Hence considering the values of $l$ to be 300 km, 400 km and 500 km, we obtain three different values of wave travel time ($\tau$).

Table 6.1: Parameters of the Original System

| **System Parameter** | **Value** |
|---|---|
| Sending end grid voltage | $3\phi$ Line-Line (RMS) 400 kV |
| $R$ | 0.03 $\Omega$/km |
| $L$ | 1 mH/km |
| $C$ | 12.96 nF/km |
| $L_g$ | 0.25 H |
| $L_{sh}$ | 10.2 H |

Table 6.2: Parameters of the Scaled System

| **System Parameter** | **Value** |
|---|---|
| Sending end grid voltage | $3\phi$ Line-Line (RMS) 220 V |
| $R'$ | 1.063 m$\Omega$/km |
| $L'$ | 35.4375 $\mu$H/km |
| $C'$ | 0.3657 $\mu$F/km |
| $L'_g$ | 9.03 mH |
| $L'_{sh}$ | 0.36146 H |

Mentioned in Table-6.3, the values of the size of FIFO Buffer ($N$), Observer sampling period ($T_{ob}$), Observer computational time ($T_{obc}$) and the switching period of the power electronic converter ($T_{sw}$) are chosen based on the calculations proposed in Section 3.4.4 of Chapter 3. Also to verify the functionality of the Observer under different test conditions, each of the lines are switched at the zero crossing ($\Phi = 0°$) and the positive peak ($\Phi = 90°$) of '$a$' phase of the sending end grid voltage.

Table 6.3: Experimental Parameters for the Observer and Power Electronic Hardware

| $l$ (km) | $\tau$ ($\mu$s) | $N$ | $T_{ob}$ ($\mu$s) | $T_{obc}$ ($\mu$s) | $T_{sw}$ ($\mu$s) |
|---|---|---|---|---|---|
| 300 | 1080 | 27 | 40 | 4.738 | 20 |
| 400 | 1440 | 36 | 40 | 5.764 | 20 |
| 500 | 1800 | 45 | 40 | 6.79 | 20 |

## 6.2 Experimental Verification

The sending end voltage and current of the transmission line for the '$a$' and '$b$' phase are captured for each of the 6 test cases. The results of the conducted test corresponding to a particular value of line length and switching instant are shown in Figs. 6.3, 6.4, 6.5, 6.6, 6.7 and 6.8, where each of the figure again contains 4 sub-figures as described below.

**Sub-Fig. (a)** Simulation of the circuit schematic shown in Fig. 2.1 with the parameters of the original system given in Table-6.1 using FDM in PSCAD for the mentioned value of the line length and switching instant.

**Sub-Fig. (b)** Simulation of the circuit schematic shown in Fig. 2.1 with the parameters of the scaled system given in Table-6.2 using FDM in PSCAD for the mentioned value of the line length and switching instant.

**Sub-Fig. (c)** Simulation of the block diagram schematic shown in Fig. 3.7 with the parameters of the scaled system given in Table-6.2 by the Observer in MATLAB/Simulink for the mentioned value of the line length and switching instant.

**Sub-Fig. (d)** Hardware emulation of the scaled system with the parameters given in Table-6.2, as per the proposed emulation scheme shown in Fig. 4.3 for the mentioned value of the line length and switching instant.

It is observed that, on switching the transmission line of different lengths at the zero crossing of a particular phase voltage, the transient in the line currents for that phase is minimum compared to the other phases. Moreover, as the length of the line is increased the transients get damped out faster due to the increase in the effective line resistance which is also observed from the waveforms. It is also noted that the peak value of the current transient increases with increase in line length. This is due to the addition of more shunt capacitance associated with the transmission line. Hence it can be observed that the emulation performed by the developed TLE nearly matches with the PSCAD results.

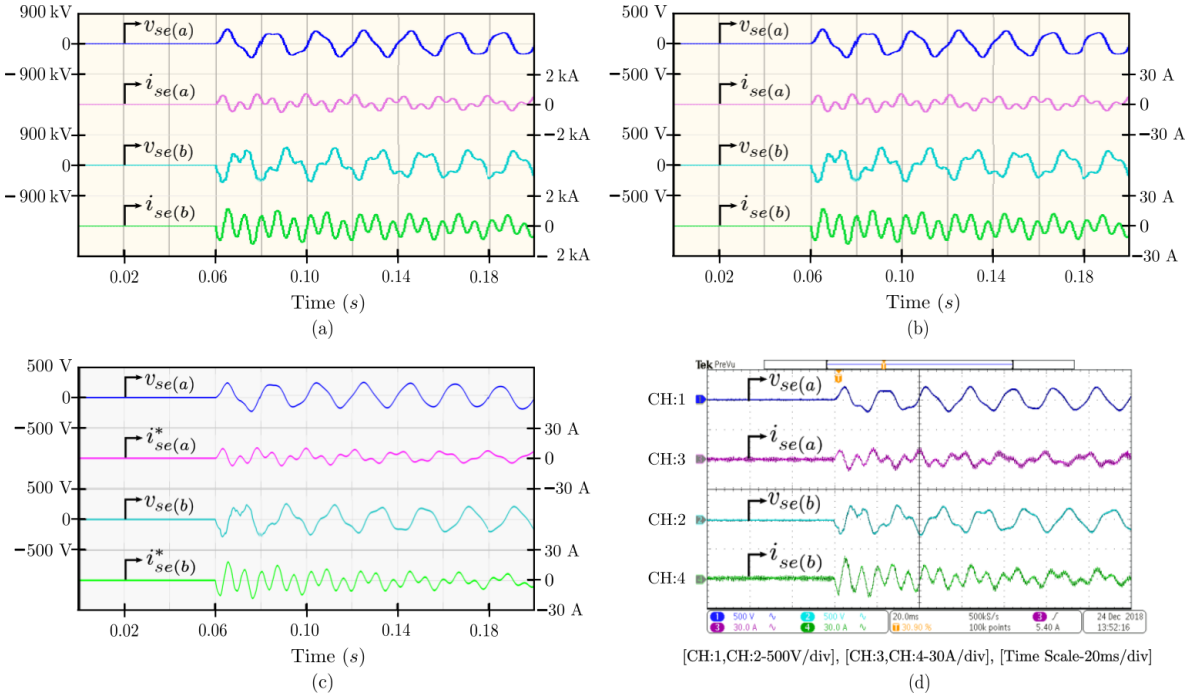



Figure 6.3: $l = 300$ km and $\Phi = 0°$

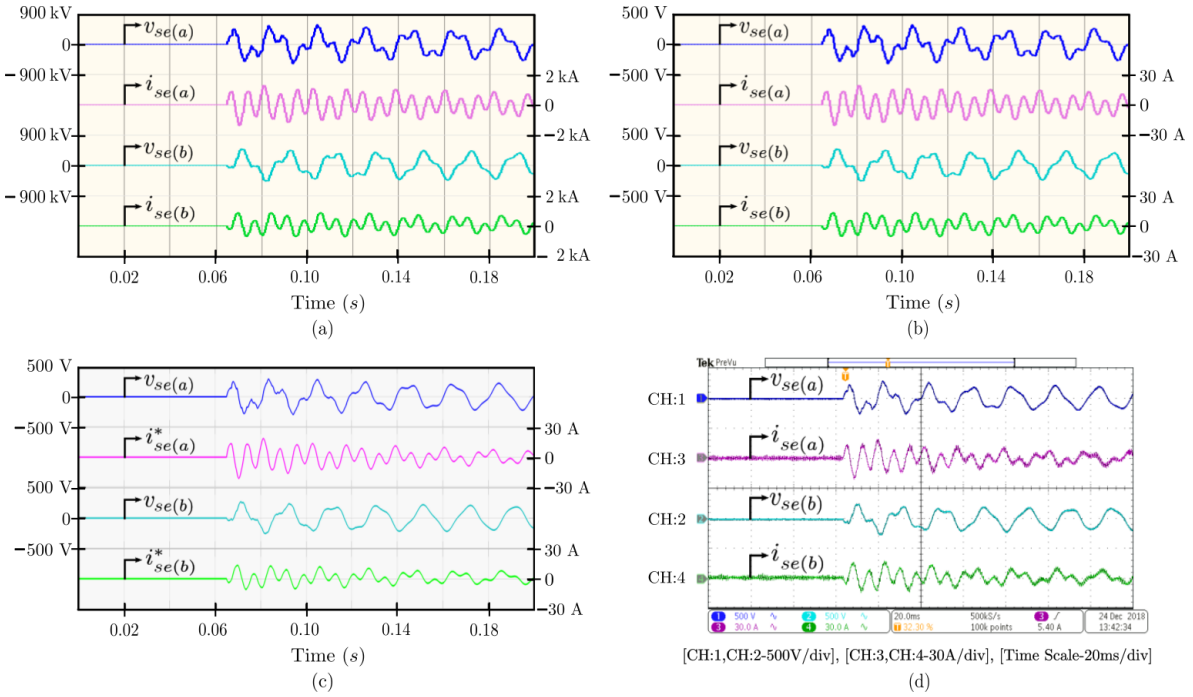



Figure 6.4: $l = 300$ km and $\Phi = 90°$

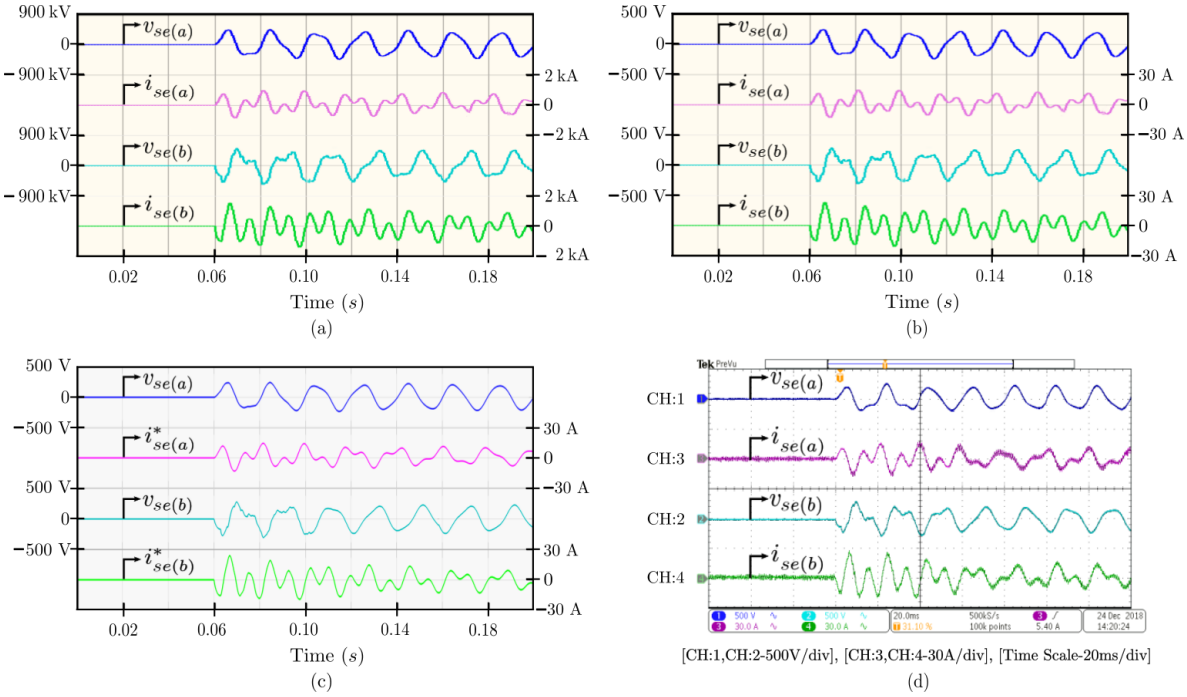



Figure 6.5: $l = 400$ km and $\Phi = 0°$

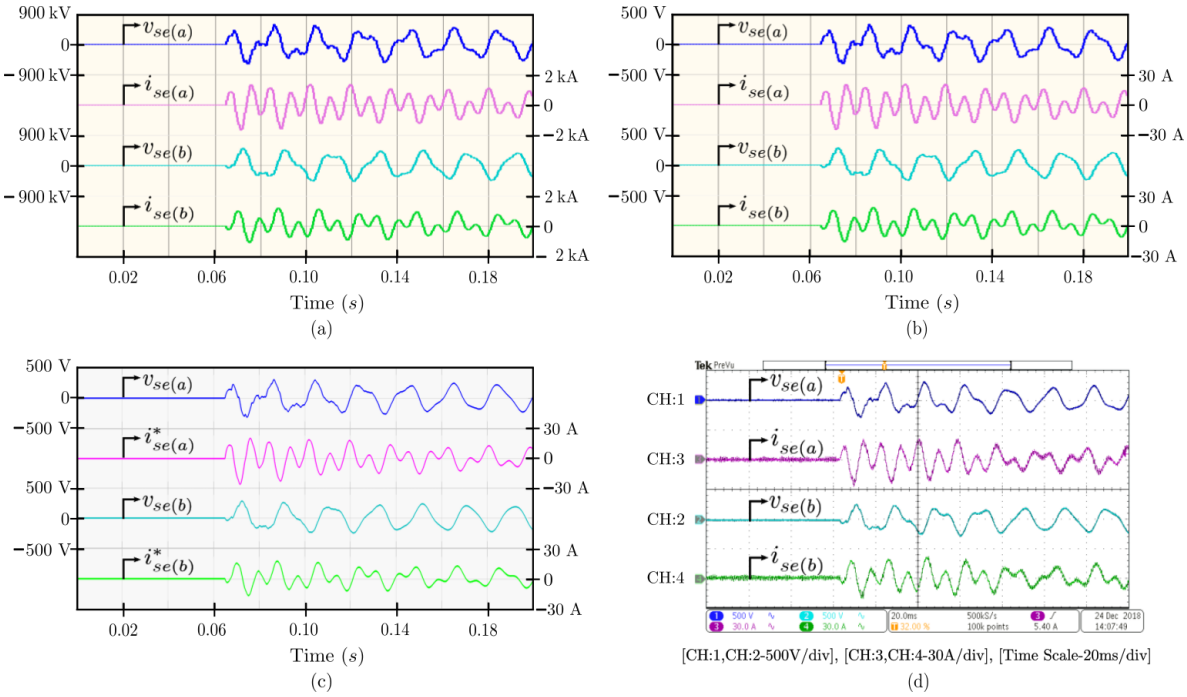



Figure 6.6: $l = 400$ km and $\Phi = 90°$

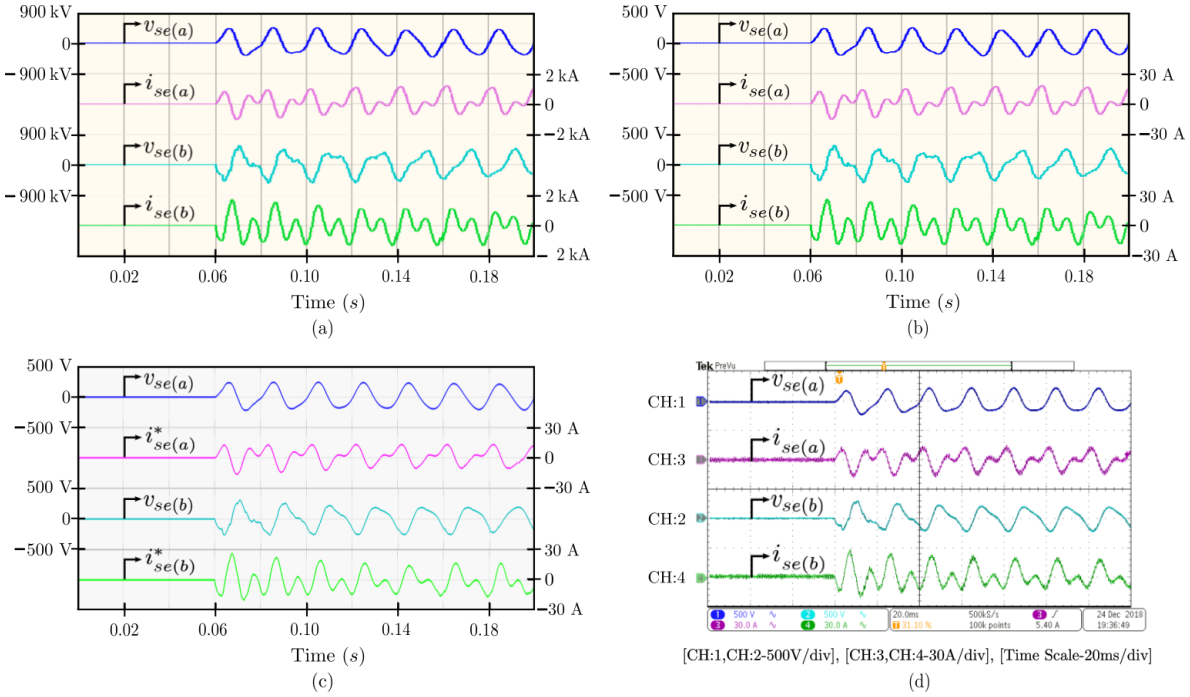



Figure 6.7: $l = 500$ km and $\Phi = 0°$

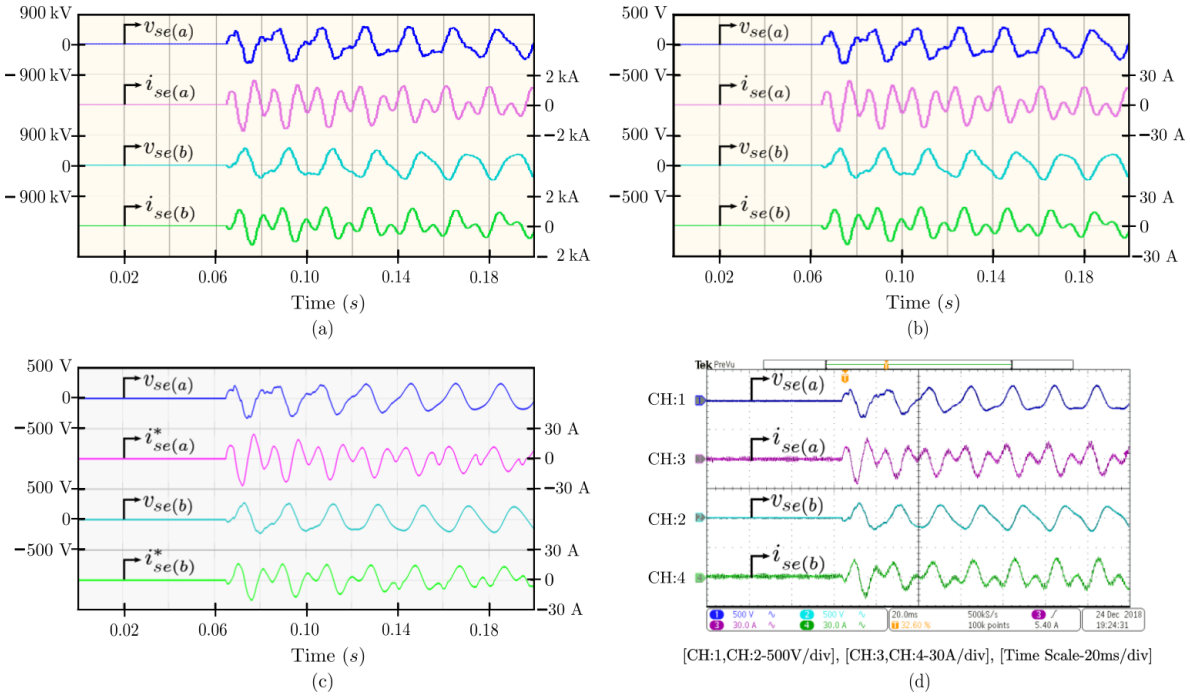



Figure 6.8: $l = 500$ km and $\Phi = 90°$

## 6.3 Summary

1. A prototype of the TLE has been fabricated in the laboratory.

2. Experiment has been conducted for three different values of line length. Also for each of the lines, the switching instant is varied to test the performance of the TLE.

3. The results of the conducted experiments have been verified both with the FDM in PSCAD and the numerical scheme in MATLAB/Simulink.

4. The dynamics captured by the TLE exhibits a high level of similarity with the simulation of the FDM in PSCAD.

# Chapter 7

# Conclusion and Future Work

The hardware emulation of energization of a long transmission line has been successfully addressed in the thesis. A hardware prototype of a programmable Transmission Line Emulator (TLE) has been developed which can emulate the high frequency current transients occurring during the instant of switching the transmission line.

Adopting a travelling wave based numerical solution (Bergeron's Model), the distributed parameter lossy transmission line is solved in real-time by the Observer. The length of the line considered for analysis is varied in between 300 km to 500 km. Hence the wave travel time in the line also changed depending on the line length and its parameters. From FFT analysis, it is found that the source end line currents have significant amount of harmonic components upto 500 Hz during the instant of switching. Therefore the sampling time period of the Observer, one of the key parameter of the transmission line emulation, is decided based on this frequency content, the wave travel time and the frequency of the selected processor of the embedded platform. To track this high frequency current, the power electronic converter needs to be switched at a relatively higher frequency (50 kHz and above). Hence a SiC based Voltage Source Converter (VSC) rated for 415 V/ 50 Hz ac, 10 kW, 800 V dc and 100 kHz switching frequency has been designed and fabricated in the laboratory. The design details of the converter has been elaborately discussed in Appendix *A* of the thesis. Moreover, after determination of the sampling frequency of the Observer, an algorithm has been proposed to select the switching frequency of the power electronic converter for the ease of embedded implementation. Further, the hardware topology for the implementation of the TLE as well as scaling of the actual transmission line to laboratory level emulator is given in the thesis. While scaling, the per unit values of the parameters were kept constant so that the system dynamics remains unaltered. The 400 kV transmission system is mapped to 220 V and the current mapping has been done so that the peak current during the switching instant can be tracked by the VSC without violating its safe current limit. The grid impedance is emulated inside the embedded platform in order to have the flexibility of varying it. The design of

the proportional resonant controller is also given in the thesis which is used by the Power Amplifier (PA) to track the currents provided by the Observer. Finally the relevant simulation and experimental results are provided for three different values of line length and two different instant of switching for each of the lines. As the length of the line emulated is increased, the transients got damped out faster due to the increase in the effective line resistance which is also observed from the experimental waveforms. Further, the peak value of the transient current increases with the line length due to the addition of more shunt capacitance associated with the transmission line. This phenomenon is also captured by the TLE. Hence from the results it can be concluded that the developed TLE exhibits a high level of similarity with the actual transmission line system results obtained from the Frequency Dependent Model (FDM) of PSCAD. This makes the developed platform an advanced and versatile TLE.

From the waveforms it is observed that the transients in the line end current is minimum when the switching is done at the zero crossing of the phase voltage. This type of switching is known as the controlled switching of transmission lines [44, 45]. But to switch each of the phase at its zero crossing, there will be a temporary phase unbalance. Hence to emulate such a phenomenon, we need to consider the zero sequence parameters of the line which is again a function of the frequency of interest [28]. So now the Frequency Dependent Model (FDM) of the transmission line needs to be solved for estimating the line end currents. Implementing this in a SoC based platform for real-time apllication can be taken as a future work. Also to emulate this with a power electronic converter, we need to use a $3\phi$, 4 wire system, the control of which is reported in [46].

# Appendix A

# Power Hardware Development

In this appendix we provide the details of the design of the power electronic converter used for the transmission line emulation. Single leg modules of half bridge topology with plug and play type gate driver card has been designed and fabricated. The modularity in the design not only allows the flexibility to adopt different converter topology but also makes easy repair and replacement. The selection of the dc bus snubber capacitors, loss estimation in the converter, thermal design of the heat sink, line filter design and the layout design for the power and the gate driver Printed Circuit Boards (PCBs) are elaborately discussed.

Table A.1: Specifications of the developed SiC MOSFET based Power Electronic Converter

| **Sl.No.** | **Parameter** | **Value** |
|---|---|---|
| 1 | Active power rating, $P_{rated}$ | 10 kW @ 0.8 pf (lag) |
| 2 | Switching frequency, $F_{sw}$ | 100 kHz |
| 3 | DC bus voltage, $V_{DC}$ | 800 V |
| 4 | $3\phi$ Line-Line (RMS) voltage, $V_{L-L(RMS)}$ | 415 V |
| 5 | Line frequency, $F_{line}$ | 50 Hz |

## A.1 Device Selection

Compared to Si, SiC has ten times the di-electric breakdown field strength, three times the bandgap, and three times the thermal conductivity which makes it an attractive material to manufacture power devices that can far exceed the performance of their Si counterparts. Resistance of high-voltage devices is predominantly determined by the width of the drift region. In theory, SiC can reduce the resistance per unit area of the drift layer to 1/300 compared to Si at the same breakdown voltage. The most popular silicon power devices for high-voltage, high-current applications are IGBT. With IGBTs, low resistance at high breakdown voltage is achieved at the cost of

switching performance. Minority carriers are injected into the drift region to reduce the conduction (ON state) resistance. When the transistor is turned off, it takes time for these carriers to recombine and dissipate, thus increasing the switching loss and time. In contrast, MOSFETs are majority carrier devices. Taking advantages of SiC's higher breakdown field and higher carrier concentration, SiC MOSFET thus can combine all three desirable characteristics of power switch, i.e., high voltage, low on-resistance and fast switching speed. The large bandgap allows the SiC devices to operate at higher temperature. The guaranteed operating temperature of the SiC devices is from 150°C - 175°C. So using these SiC MOSFETs will improve the converter efficiency and also lower the cost and size of heat sink. The device chosen is a 1200 V, 40 A N-channel SiC Power MOSFET (SCH2080KE) [47] which is co-packaged with SiC Schottky Barrier Diode (SBD). Compared to silicon Fast Recovery Diodes (FRDs), SiC SBDs have much lower reverse recovery current and recovery time, hence dramatically lowering the reverse recovery loss. The discrete device of TO-247 package has been chosen to make custom layout for better performance and also to reduce the cost.

## A.2 Selection of DC Link Snubber Capacitors

Before selecting the dc link snubber capacitor we must estimate the input current in the dc side of the converter. We have considered Conventional Space Vector Pulse Width Modulation (CSVPWM) for this analysis.

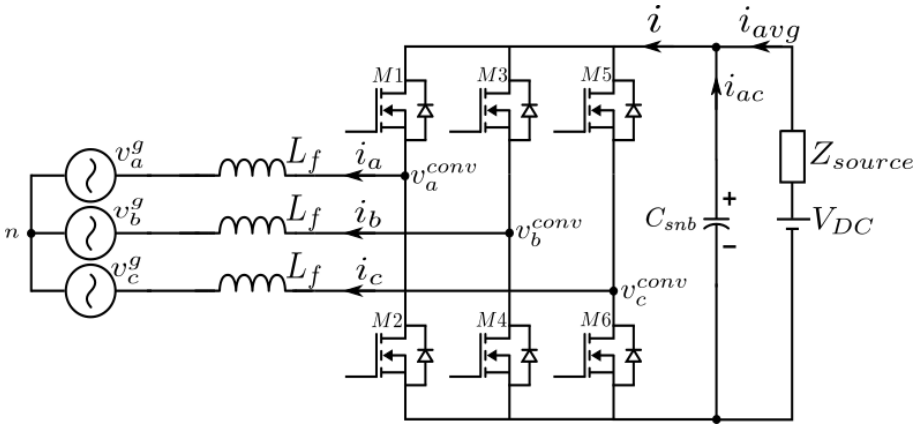



Figure A.1: $3\phi$ , 2 level Voltage Source Converter

### A.2.1 Basics of Conventional Space Vector Modulation

Fig. *A*.1 shows a $3\phi$ VSC. The load on the converter is a back electromotive force in series with the inductor. For a PWM converter, by neglecting the dc link voltage oscillations and by considering only a linear modulation range, the converter output

phase voltages averaged over the subcycle period ($T_s$) is given by :

$$\langle v_{an}^{conv} \rangle_{T_s} = MV_{DC} \cos\theta \tag{A.1}$$

$$\langle v_{bn}^{conv} \rangle_{T_s} = MV_{DC} \cos\left(\theta - \frac{2\pi}{3}\right) \tag{A.2}$$

and (A.3)

$$\langle v_{cn}^{conv} \rangle_{T_s} = MV_{DC} \cos\left(\theta - \frac{4\pi}{3}\right) \tag{A.4}$$

where we define the modulation index,

$$M = \frac{\text{Peak value of the phase voltage } (V_{pk})}{\text{DC Bus Voltage } (V_{DC})}$$

and $\theta = \omega_\circ t$ , where $\omega_\circ$ is the angular line frequency. For linear modulation, the maximum possible value of $M$ is $\frac{1}{\sqrt{3}}$ for CSVPWM. Denoting "1" as the status for which the top switch of the corresponding phase is on and the bottom is off and "0" as the status for which the bottom switch of that phase is on while the top is off, we get 8 such switching combinations. Fig. $A.2$ shows all possible eight voltage vectors that a $3\phi$ VSC may have. They are (100), (110), (010), (011), (001), (101), (111) and (000). Among the eight voltage vectors, two $(000, 111)$ are the zero voltage vectors and the rest six are the active voltage vectors. In Fig. $A.2$, the reference voltage vector ($\overrightarrow{v_{ref}} = MV_{pk}e^{j\theta}$) lies in the second sector. Hence this reference voltage vector will be generated by the nearest two active voltage vectors in the second sector, namely (110 and 010) and zero vectors namely (000 and 111). Using volt-second balance, the duty cycle of each voltage vector [48–50] can be written as :

$$D_{010} = \frac{T_{010}}{T_s} = \sqrt{3}M \sin\left(\theta - \frac{\pi}{3}\right) \tag{A.5}$$

$$D_{110} = \frac{T_{110}}{T_s} = \sqrt{3}M \sin\left(\theta + \frac{\pi}{3}\right) \tag{A.6}$$

and

$$D_{000} = D_{111} = 0.5\left(1 - D_{010} - D_{110}\right) \tag{A.7}$$

where, $T_{010}$ and $T_{110}$ are the time duration of the application of the voltage vectors 010 and 110 respectively.

### A.2.2 Input Current of the Converter

Neglecting the switching ripple, the line currents of the converter can be written as,

$$i_a = I_{pk} \cos(\theta - \phi) \tag{A.8}$$

$$i_b = I_{pk} \cos\left(\theta - \phi - \frac{2\pi}{3}\right) \tag{A.9}$$

$$i_c = I_{pk} \cos\left(\theta - \phi - \frac{4\pi}{3}\right) \tag{A.10}$$

where, $I_{pk}$ is the peak value of the line current and $\phi$ is the load power factor angle.

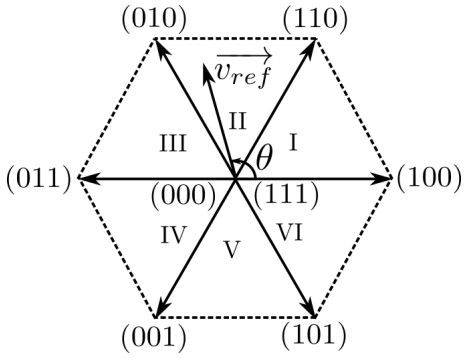



Figure A.2: 6 Active and 2 Zero Voltage Vectors for CSVPWM

**Average Value of the Input Current :**

Assuming the instantaneous value of the converter input current to be $i$, the average value of the converter input current in one subcycle (for the reference voltage vector in the second sector) can be expressed as :

$$i_{avg} = \frac{1}{T_s} \int_0^{T_s} i(\theta)\, d\theta = D_{010} i_b - D_{110} i_c \tag{A.11}$$

Since $T_s$ is very small in comparison to the fundamental time period, we can consider $i_b$ and $i_c$ to be constant within a subcycle duration. Now putting equations $A.5, A.6, A.9$ and $A.10$, in equation $A.11$, we get

$$i_{avg} = \frac{3}{2} M I_{pk} \cos\phi \tag{A.12}$$

**RMS Value of the Input Current :**

The rms value of the converter input current in one subcycle (for the reference voltage vector in the second sector) can be expressed as :

$$i_{rms}^2 = \frac{1}{T_s} \int_0^{T_s} i^2(\theta)\, d\theta = D_{010} i_b^2 + D_{110} i_c^2 \tag{A.13}$$

Therefore the rms value of the dc link current over a fundamental line cycle can be written as,

$$I_{rms}^2 = \frac{1}{\pi/3}\int_{\pi/3}^{2\pi/3} i_{rms}^2(\theta)\, d\theta \tag{A.14}$$

Substituting the equations $A.5, A.6, A.9, A.10$ and $A.13$ in equation $A.14$ we get,

$$I_{rms} = \frac{I_{pk}}{\sqrt{2}}\sqrt{\frac{4\sqrt{3}}{\pi}M\left(\frac{1}{4}+\cos^2\phi\right)} \tag{A.15}$$

### A.2.3 RMS Value of the DC Link Snubber Capacitor Current

The converter input current is composed of ac and dc component. The dc component is nothing but the average input current as derived in the equation $A.12$. So we can write the instantaneous input current, $i$ is

$$i = i_{ac} + i_{avg}$$

Now we assume that the dc link snubber capacitor reactance is much smaller than the effective series dc link impedance at the switching frequency. So the entire ac component is provided by the snubber capacitor. Therefore we can write,

$$I_{rms(capacitor)}^2 = I_{rms}^2 - i_{avg}^2 \tag{A.16}$$

Substituting equation $A.12$ and $A.15$ in equation $A.16$ , we get

$$I_{rms(capacitor)} = \frac{I_{pk}}{\sqrt{2}}\sqrt{4M\left[\frac{\sqrt{3}}{4\pi}+\cos^2\phi\left(\frac{\sqrt{3}}{\pi}-\frac{9M}{8}\right)\right]} \tag{A.17}$$

### A.2.4 Maximum Peak to Peak Voltage of the DC Link Snubber Capacitor

In [51] it is shown that at maximum value of modulation , i.e. $M = \frac{1}{\sqrt{3}}$ , the peak to peak ripple voltage ($\Delta v_{pk-pk}$) is highest when the load power factor is zero. So we will design for this case so that in all other cases the ripple is within allowable limits. It is further shown that,

$$\Delta v_{pk-pk}^{max} = \frac{I_{pk}}{4F_{sw}C_{snb}} \tag{A.18}$$

Substituting $\Delta v_{pk-pk}^{max} = 0.5$ % of $V_{DC} = 4$ V, $I_{pk} = 26$ A, $F_{sw} = 100$ kHz, we get

$$C_{snb} = \frac{26}{4\times 100000\times 4} = 16.25\times 10^{-6}\ \text{F} = 16.25\ \mu\text{F}$$

and by equation $A.17$ we get,

$$I_{rms(capacitor)} = \frac{26}{\sqrt{2}} \times \sqrt{4 \times \frac{1}{\sqrt{3}} \times \frac{\sqrt{3}}{4\pi}} = 10.37\ A$$

Now instead of choosing a single capacitor, we choose twelve thick film capacitors and connect them in parallel so that the effective capacitance is same as that required with the benefit that their net extra series inductance getting reduced. The specifications of the high frequency dc link snubber capacitors are given in Table-$A.2$.

Table A.2: Selected High Frequency DC Link Snubber Capacitor

| **Capacitance** | **Quantity** | **Voltage Rating** | **Current Rating @ 100 kHz** |
|---|---|---|---|
| 0.022 $\mu$F | 3 | 1250 V | 8 Amp |
| 0.47 $\mu$F | 3 | 1200 V | 10 Amp |
| 2.5 $\mu$F | 6 | 1200 V | 20 Amp |

## A.3 Thermal Design

Before carrying out the thermal design of the $3\phi$ VSC, we should perform a detailed loss calculation of the switches employed in the VSC. This loss has mainly two components namely conduction and switching. The loss calculation will not only help us in designing the heat sink efficiently but also ensure that the junction temperature of the switches are always less than atleast 70% of their rated values under the rated operating conditions of the VSC.

### A.3.1 Estimation of Device Conduction Loss

When a switch conducts, there will be finite amount of voltage drop across the switch due to the channel resistance of the SiC MOSFET. $r_{DS(+)}$ and $r_{DS(-)}$ are considered as the resistances offered by the channel to the flow of current from drain to source and source to drain respectively. Hence there will be power loss in the switch while it is in conduction. In this section we will evaluate the conduction loss in each phase (i.e. in the top and bottom switch of each leg) of the VSC by neglecting the dead time and the leakage current of the device when it is in blocking state.

**Case 1: The phase current $i_a$ is positive i.e. $\phi - \frac{\pi}{2} < \theta < \phi + \frac{\pi}{2}$**

The average conduction loss over a subcycle in the top MOSFET,

$$\langle p_{condM1} \rangle_{T_s} = \left( i_a^2 r_{DS(+)} \right) d_a \tag{A.19}$$

Similarly the average conduction loss over a subcycle in the bottom MOSFET,

$$\langle p_{condM2} \rangle_{T_s} = \left( i_a^2 r_{DS(-)} \right) (1 - d_a) \tag{A.20}$$

**Case 2: The phase current $i_a$ is negative i.e.** $\phi + \frac{\pi}{2} < \theta < \phi + \frac{3\pi}{2}$

The average conduction loss over a subcycle in the top MOSFET,

$$\langle p_{condM1} \rangle_{T_s} = \left( i_a^2 r_{DS(-)} \right) d_a \tag{A.21}$$

Similarly the average conduction loss over a subcycle in the bottom MOSFET,

$$\langle p_{condM2} \rangle_{T_s} = \left( i_a^2 r_{DS(+)} \right) (1 - d_a) \tag{A.22}$$

where $d_a$ is the ratio of time duration for which the top switch of the $a$ phase is on to the subcycle duration. Therefore $d_a$ for CSVPWM can be written as,

$$d_a = M \cos\theta + 0.5 + 0.5 \text{ mid} \left[ M \cos\theta, M \cos\left(\theta - \frac{2\pi}{3}\right), M \cos\left(\theta - \frac{4\pi}{3}\right) \right] \tag{A.23}$$

So the conduction loss over a fundamental line cycle in the top MOSFET,

$$P_{condM1} = \frac{1}{2\pi} \int_{-\frac{\pi}{2}+\phi}^{\frac{3\pi}{2}+\phi} \langle p_{condM1} \rangle_{T_s} \, d\theta$$

$$\Rightarrow P_{condM1} = \frac{1}{2\pi} \left( \int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi} \left( i_a^2 r_{DS(+)} \right) d_a \, d\theta + \int_{\frac{\pi}{2}+\phi}^{\frac{3\pi}{2}+\phi} \left( i_a^2 r_{DS(-)} \right) d_a \, d\theta \right)$$

Substituting the equation $A.8$ and $A.23$ in the above equation, we get

$$\begin{aligned} P_{condM1} = {} & I_{pk}^2 r_{DS(+)} \left[ \frac{1}{8} + \left( \frac{3}{2} \cos\phi - \frac{1}{6} \cos 3\phi \right) \left( \frac{M}{2\pi} + \frac{M}{4\pi} \right) - \frac{5\sqrt{3}M}{24\pi} \right] \\ & + I_{pk}^2 r_{DS(-)} \left[ \frac{1}{8} - \left( \frac{3}{2} \cos\phi - \frac{1}{6} \cos 3\phi \right) \left( \frac{M}{2\pi} + \frac{M}{4\pi} \right) + \frac{5\sqrt{3}M}{24\pi} \right] \end{aligned} \tag{A.24}$$

Considering $r_{DS(+)} = r_{DS(-)} = r_{DS}$, we get

$$\Rightarrow P_{condM1} = \frac{I_{pk}^2 r_{DS}}{4} \tag{A.25}$$

Similarly the conduction loss over a fundamental line cycle in the bottom MOSFET,

$$P_{condM2} = \frac{1}{2\pi} \int_{-\frac{\pi}{2}+\phi}^{\frac{3\pi}{2}+\phi} \langle p_{condM2} \rangle_{T_s} \, d\theta$$

$$\Rightarrow P_{condM2} = \frac{1}{2\pi} \left( \int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi} \left( i_a^2 r_{DS(-)} \right) (1 - d_a) \, d\theta + \int_{\frac{\pi}{2}+\phi}^{\frac{3\pi}{2}+\phi} \left( i_a^2 r_{DS(+)} \right) (1 - d_a) \, d\theta \right)$$

Substituting the equation $A.8$ and $A.23$ in the above equation, we get

$$P_{condM2} = I_{pk}^2 r_{DS(-)} \left[\frac{1}{8} - \left(\frac{3}{2}\cos\phi - \frac{1}{6}\cos 3\phi\right)\left(\frac{M}{2\pi} + \frac{M}{4\pi}\right) + \frac{5\sqrt{3}M}{24\pi}\right] + I_{pk}^2 r_{DS(+)} \left[\frac{1}{8} + \left(\frac{3}{2}\cos\phi - \frac{1}{6}\cos 3\phi\right)\left(\frac{M}{2\pi} + \frac{M}{4\pi}\right) - \frac{5\sqrt{3}M}{24\pi}\right] \quad \text{(A.26)}$$

Once again considering $r_{DS(+)} = r_{DS(-)} = r_{DS}$, we get

$$\Rightarrow P_{condM2} = \frac{I_{pk}^2 r_{DS}}{4} \quad \text{(A.27)}$$

Therefore the total conduction loss in each phase,

$$P_{cond(a\ phase)} = P_{condM1} + P_{condM2} = \frac{I_{pk}^2 r_{DS}}{2} = \frac{26^2 \times 0.125}{2} = 42.25\ W$$

### A.3.2 Estimation of Device Switching Loss

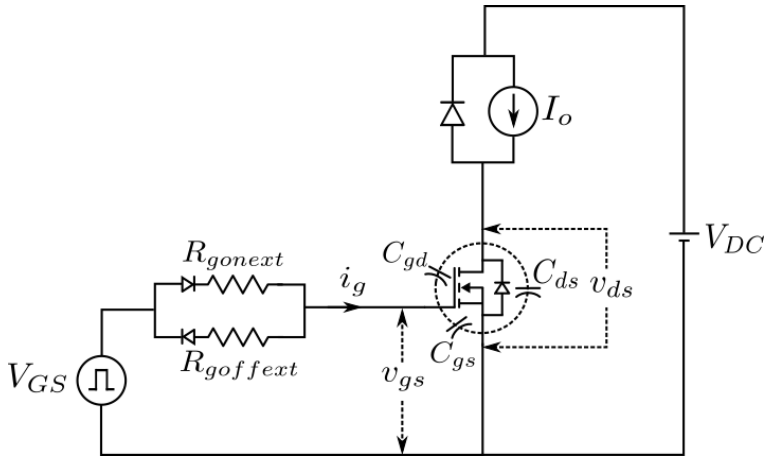



Figure A.3: Circuit for esmitation of Switching Loss of the MOSFET

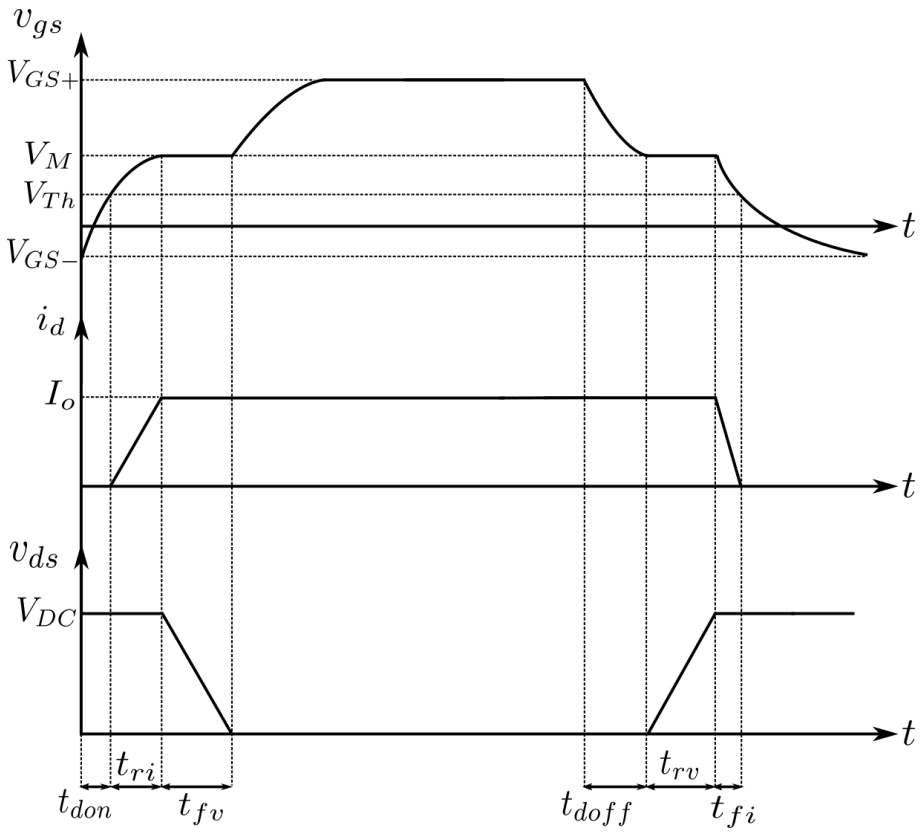



Figure A.4: Switching Characteristics of MOSFET

Gate-Charge method is used to find the switching energy loss at different values of drain current and at rated dc bus voltage. Then by curve fitting technique the analytical function relating the switching energy loss versus the drain current of the device is evaluated. The circuit shown in Fig. *A*.3 is considered to get a fundamental understanding of the switching behaviour of the MOSFET. $V_{GS+}$ and $V_{GS-}$ are the applied positive and the negative voltages to turn the MOSFET on and off respectively. Applying KCL at the gate terminal of the MOSFET, we can write

$$i_g = \frac{V_{GS} - v_{gs}}{R_G} = C_{gs}\frac{\mathrm{d}v_{gs}}{\mathrm{d}t} + C_{gd}\frac{\mathrm{d}v_{gd}}{\mathrm{d}t} \tag{A.28}$$

The uppercase subscripts refer to the rated or the applied quantities and the lowercase subscripts refer to the instantaneous quantities.

**Turn On Transient :**

Fig. *A*.4 illustrates the switching characteristics of the MOSFET. Once $v_{gs}$ crosses the gate threshold voltage ($V_{Th}$) (mentioned in the datasheet), the channel current starts increasing and once it attains the full value of the load current, the $v_{gs}$ gets

clampled at the milller plateau voltage ($V_M$). At this point of time the voltage across the device starts falling. Since $V_M$ depends on the value of the drain current, we need to find $V_M$ as per our test conditions.

**In the duration $t_{don}$ :**
We define $R_{Gon} = R_{gonext} + R_{gint}$ , where $R_{gonext}$ is the connected external gate circuit resistance and $R_{gint}$ is the device internal gate resistance specified in the datasheet. So from equation $A.28$ we can write

$$\frac{V_{GS+} - v_{gs}}{R_{Gon}} = C_{gs}\frac{\mathrm{d}v_{gs}}{\mathrm{d}t} + C_{gd}\frac{\mathrm{d}\left(v_{gs} - v_{ds}\right)}{\mathrm{d}t} = C_{gs}\frac{\mathrm{d}v_{gs}}{\mathrm{d}t} + C_{gd}\frac{\mathrm{d}v_{gs}}{\mathrm{d}t} \tag{A.29}$$

since in this duration $v_{ds} = V_{DC}$ which is constant and defining $C_{iss} = C_{gs} + C_{gd}$ we can write,

$$\int_0^{t_{don}} dt = R_{Gon}C_{iss}\int_{V_{GS-}}^{V_{Th}} \frac{dv_{gs}}{V_{GS+} - v_{gs}}$$

$$\Rightarrow t_{don} = R_{Gon}C_{iss}\ln\left|\left(\frac{V_{GS+} - V_{GS-}}{V_{GS+} - V_{Th}}\right)\right| \tag{A.30}$$

**In the duration $t_{ri}$ :**
Here the the drain current increases from zero to the full load current and $v_{ds}$ remains constant at $V_{DC}$. So we can write

$$t_{ri} = R_{Gon}C_{iss}\ln\left|\left(\frac{V_{GS+} - V_{Th}}{V_{GS+} - V_M}\right)\right| \tag{A.31}$$

Now in this region the MOSFET is in saturation. So at the end of the $t_{ri}$ duration we can write,

$$I_o = K_{SiC}\left(V_M - V_{Th}\right)^2$$

where, $K_{SiC}$ is the device constant. Also from the datasheet we have,

$$I_d^{datasheet} = K_{SiC}\left(V_M^{datasheet} - V_{Th}\right)^2$$

$$\therefore \sqrt{\frac{I_o}{I_d^{datasheet}}} = \frac{V_M - V_{Th}}{V_M^{datasheet} - V_{Th}} \tag{A.32}$$

Hence we can find $V_M$ from the above equation and put it in the equation $A.31$ to find the value of $t_{ri}$.

**In the duration $t_{fv}$ :**
In this duration, $v_{gs} = V_M$ which becomes constant and $v_{ds}$ starts falling. So from equation $A.28$ we can write,

$$\frac{V_{GS+} - V_M}{R_{Gon}} = C_{gs}\frac{\mathrm{d}v_{gs}}{\mathrm{d}t} + C_{gd}\frac{\mathrm{d}\left(v_{gs} - v_{ds}\right)}{\mathrm{d}t} = -C_{gd}\frac{\mathrm{d}v_{ds}}{\mathrm{d}t} \tag{A.33}$$

$$\therefore t_{fv} = -\frac{R_{Gon}}{V_{GS+} - V_M}\int_{V_{DC}}^{0} C_{gd}\, dv_{ds} = \frac{R_{Gon}Q_{gd}}{V_{GS+} - V_M} \tag{A.34}$$

Now $C_{gd}$ varies with $v_{ds}$. So we will use the gate charge curve given in the datasheet to find the value of the charge stored in the gate to drain capacitance ($Q_{gd}$).

$$\Rightarrow t_{fv} = \frac{R_{Gon}}{V_{GS+} - V_M}\frac{Q_{gd}^{datasheet}}{V_{DS}^{datasheet}}V_{DC} \tag{A.35}$$

Considering that the drain current linearly rises during the interval $t_{ri}$ and the drain to source voltage linearly falls in the interval $t_{fv}$ we can say that the turn on energy loss,

$$e_{on} = \frac{1}{2}I_o V_{DC}\left(t_{ri} + t_{fv}\right) \tag{A.36}$$

**Turn Off Transient :**

Now we will apply the external gate source voltage of $V_{GS-}$. Once $v_{gs}$ comes down to $V_M$, it gets clamped at this value and the voltage across the device starts building up to $V_{DC}$. When $v_{ds}$ attains the value of $V_{DC}$, the channel current starts falling. By the time $v_{gs}$ falls below $V_{Th}$ the channel current entirely becomes zero.

**In the duration $t_{doff}$ :**
We define $R_{Goff} = R_{goffext} + R_{gint}$ , where $R_{goffext}$ is the connected external gate circuit resistance and $R_{gint}$ is the device internal gate resistance specified in the datasheet. So from equation $A.28$ we can write

$$\frac{V_{GS-} - v_{gs}}{R_{Goff}} = C_{gs}\frac{\mathrm{d}v_{gs}}{\mathrm{d}t} + C_{gd}\frac{\mathrm{d}\left(v_{gs} - v_{ds}\right)}{\mathrm{d}t} = C_{gs}\frac{\mathrm{d}v_{gs}}{\mathrm{d}t} + C_{gd}\frac{\mathrm{d}v_{gs}}{\mathrm{d}t} \tag{A.37}$$

since in this duration $v_{ds} \approx 0$ which is constant and defining $C_{iss}^{*} = C_{gs} + C_{gd}$ @ $v_{ds} = 0$ we get,

$$\therefore \int_0^{t_{doff}} dt = R_{Goff}C_{iss}^{*}\int_{V_{GS+}}^{V_M}\frac{dv_{gs}}{V_{GS-} - v_{gs}}$$

$$\Rightarrow t_{doff} = R_{Goff}C_{iss}^{*}\ln\left|\left(\frac{V_{GS+} - V_{GS-}}{V_M - V_{GS-}}\right)\right| \tag{A.38}$$

**In the duration $t_{rv}$ :**
In this duration $v_{gs} = V_M$ which becomes constant and the $v_{ds}$ starts rising. So from equation $A.28$ we can write,

$$\frac{V_{GS-} - V_M}{R_{Goff}} = C_{gs}\frac{\mathrm{d}v_{gs}}{\mathrm{d}t} + C_{gd}\frac{\mathrm{d}\left(v_{gs} - v_{ds}\right)}{\mathrm{d}t} = -C_{gd}\frac{\mathrm{d}v_{ds}}{\mathrm{d}t} \tag{A.39}$$

$$\therefore t_{rv} = -\frac{R_{Goff}}{V_{GS-} - V_M}\int_0^{V_{DC}} C_{gd}\; dv_{ds} = \frac{R_{Goff}Q_{gd}}{-V_{GS-} + V_M} \tag{A.40}$$

Now $C_{gd}$ varies with $v_{ds}$. So we will use the gate charge characteristics given in the datasheet to find the value of $Q_{gd}$.

$$\Rightarrow t_{rv} = \frac{R_{Goff}}{-V_{GS-} + V_M}\frac{Q_{gd}^{datasheet}}{V_{DS}^{datasheet}}V_{DC} \tag{A.41}$$

**In the duration $t_{fi}$ :**
Here the the drain current decreases from the full load value to zero and $v_{ds}$ remains constant at $V_{DC}$ . So we can write

$$t_{fi} = R_{Goff}C_{iss}\ln\left|\left(\frac{-V_{GS-} + V_M}{-V_{GS-} + V_{Th}}\right)\right| \tag{A.42}$$

Using equation $A.32$ we can find $V_M$ and substitute it in the equation $A.42$ to find the value of $t_{fi}$. We again consider that the drain to source voltage of the device linearly rises in the interval $t_{rv}$ and the channel current linearly falls during the interval $t_{fi}$. Therefore the turn off energy loss,

$$e_{off} = \frac{1}{2}I_oV_{DC}\left(t_{rv} + t_{fi}\right) \tag{A.43}$$

Hence from the equation $A.36$ and $A.43$ we can find the total switching energy loss in a switching cycle which is given by,

$$e_{sw}\left(I_o\right) = e_{on} + e_{off} = \frac{1}{2}I_oV_{DC}\left(t_{ri} + t_{fv} + t_{rv} + t_{fi}\right)$$

Based on the parameters of the selected device, the switching energy loss for the corresponding load currents are evaluated at rated dc bus voltage for $V_{GS+} = 18.3$ V, $V_{GS-} = -3.3$ V. The corresponding values are shown in Table-$A.3$. Plotting $e_{sw}\left(I_o\right)$ vs $I_o$ and applying curve fitting in $MATLAB$ as shown in Fig. $A.5$, we get

$$e_{sw}\left(I_o\right) = \left[0.002I_o^4 - 0.04262I_o^3 + 1.671I_o^2 + 37.81I_o + 0.0322\right]\ \mu J \tag{A.44}$$

Table A.3: Switching Loss vs Switch Current

| **Sl. No.** | **Switch Current, $I_o$ in Amp** | **Switching Loss, $e_{sw}$ in $\mu J$** |
|---|---|---|
| 1 | 5 | 228.66 |
| 2 | 10 | 520 |
| 3 | 15 | 898.2 |
| 4 | 20 | 1400 |
| 5 | 25 | 2087 |
| 6 | 30 | 3075 |

Now when the pole current of a particular phase is positive, the top MOSFET of that phase is hard switched and the bottom MOSFET is soft switched due to the bottom anti-parallel diode. Substituting $I_o$ as $I_{pk}\cos(\theta-\phi)$ in the equation $A.44$, the average switching energy loss in the top MOSFET of '$a$' phase over a fundamental line cycle is

$$E_{swM1} = \frac{1}{2\pi}\int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi} e_{sw}(\theta)\ d\theta \tag{A.45}$$

Therefore the switching loss in the top MOSFET of '$a$' phase over a fundamental line cycle is

$$P_{swM1} = F_{sw} \times E_{swM1} = \frac{F_{sw}}{2\pi}\int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi} e_{sw}(\theta)\ d\theta \tag{A.46}$$

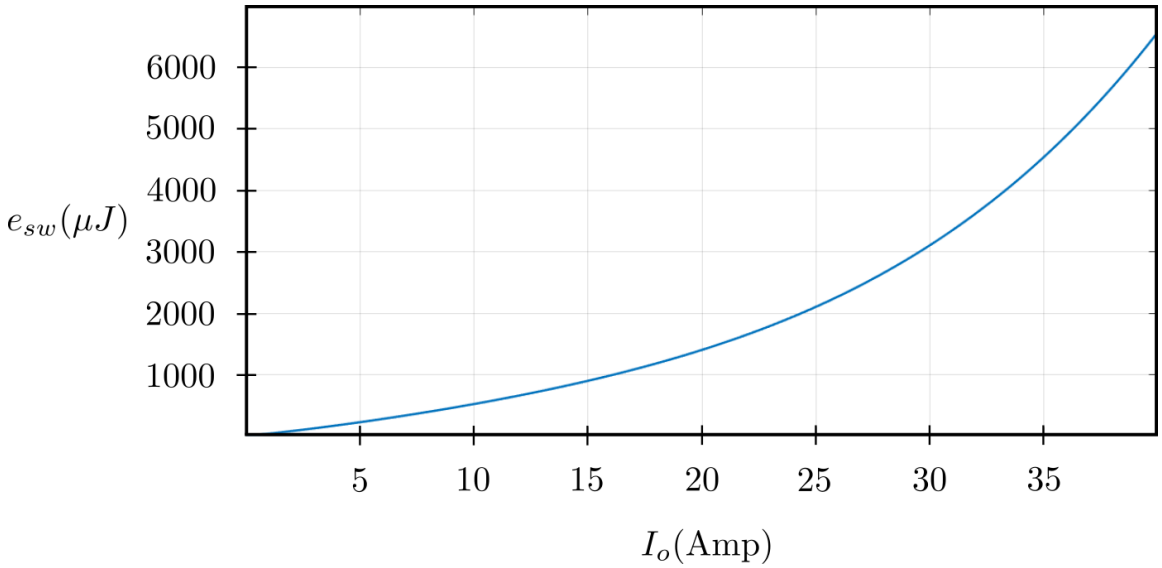



Figure A.5: Plot of Switching Energy Loss vs Drain Current

Similarly when the pole current of a particular phase is negative, the bottom MOSFET of that phase is hard switched and the top MOSFET is soft switched due

to the top anti-parallel diode. So the switching loss in the bottom MOSFET of '$a$' phase over a fundamental line cycle is

$$P_{swM2} = \frac{F_{sw}}{2\pi} \int_{\frac{\pi}{2}+\phi}^{\frac{3\pi}{2}+\phi} e_{sw}(\theta)\ d\theta \tag{A.47}$$

As the PWM used is symmetric in nature, so $P_{swM1} = P_{swM2}$. With $I_{pk} = 26$ A, the total switching loss in a particular phase,

$$P_{sw(a\ phase)} = \frac{F_{sw}}{\pi} \int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi} e_{sw}(\theta)\ d\theta$$

$$\Rightarrow P_{sw(a\ phase)} = \frac{100 \times 10^3}{\pi} \times 3818.45 \times 10^{-6} = 121.54\ W$$

### A.3.3 Heat Sink Design

The design of the heat sink is done in a modular fashion such that not only a $3\phi$ VSC but different other topology can be realized. So each leg of the VSC is built as a module and provision for connectivity between different modules is being provided. With the estimation of the losses in each phase, the heat sink module is designed such that the junction temperature of neither of the two devices (top and bottom MOSFET of a particular phase) exceeds 70 % of the rated value. The thermal model under the steady state condition is shown in the Fig. $A.6$. Since the total loss in each phase is equally contributed by the top and bottom MOSFET, therefore from the model, as shown in Fig. $A.6$, we can write,

$$\text{Junction Temerature, } T_j = \left[\left(\frac{R_{jc} + R_{cs}}{2} + R_{sa}\right) \times \left(P_{cond(a\ phase)} + P_{sw(a\ phase)}\right)\right] + T_{amb} \tag{A.48}$$

where, $R_{jc}$, $R_{cs}$ and $R_{sa}$ are the thermal resistances between junction to case, case to heat sink and heat sink to ambient respectively. The maximum possible value of the junction temperature is fixed at $T_{j(max)} = 0.7 \times 175°C = 122.5°C$. Also $(R_{jc} + R_{cs}) \approx 1°C/W$. Considering the ambient temperature, $T_{amb} = 30°C$ we get $R_{sa} \leq 0.065°C/W$. The heat sink is designed with the help of SOLIDWORKS software to achieve the desired thermal resistance. Also forced cooling technique is applied so that the volume of the heat sink can be reduced which will increase the power density of the converter. The design and the thermal simulation of the heat sink is shown in the Fig. $A.7$.

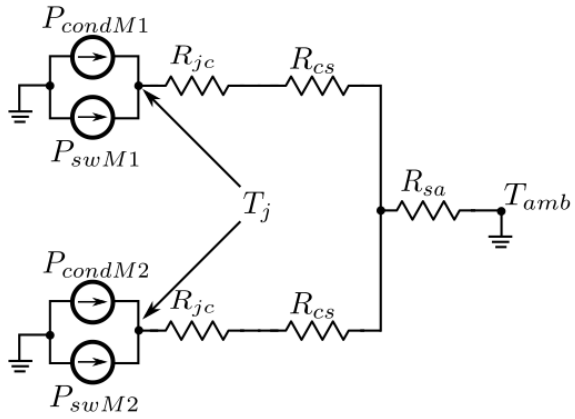



Figure A.6: Steady State Thermal Model of each leg of the VSC

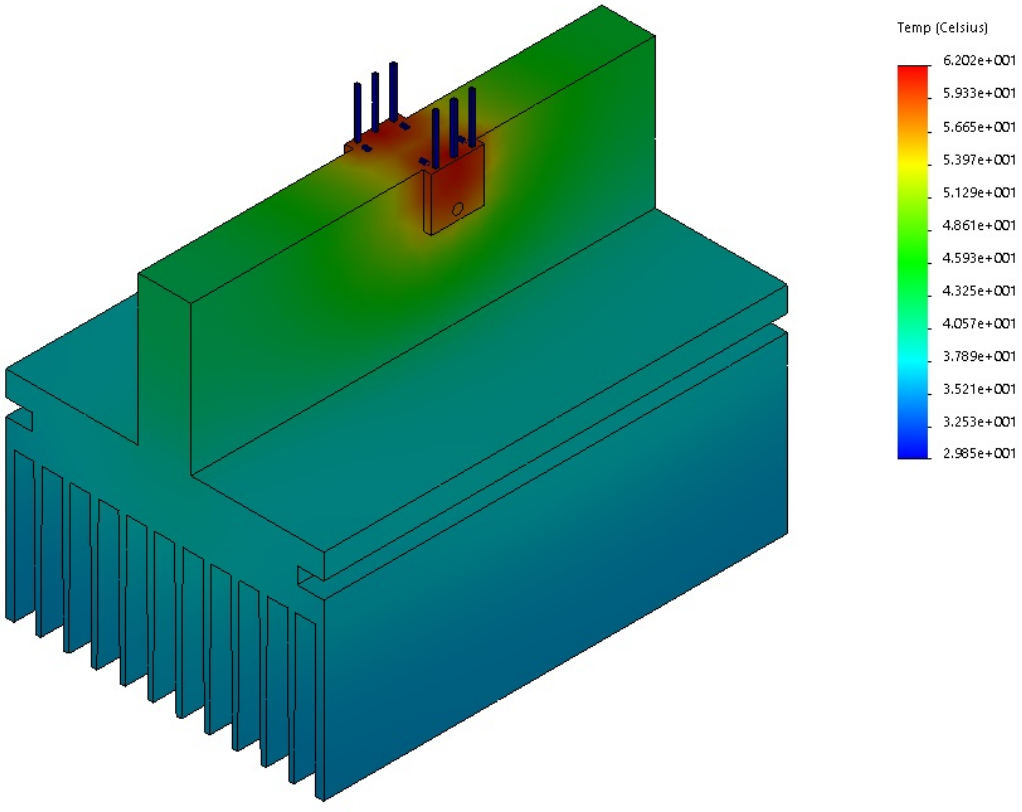



Figure A.7: Thermal Simulation of the designed Heat Sink in SOLIDWORKS

## A.4 Layout considerations of the Power PCB

Fig. *A*.8 shows the developed power PCB card. It is made of a two layer board. The source terminal of the top switch and the drain terminal of the bottom switch is placed close to each other to reduce the parasitic inductance. Sandwiching arrangement has been made in the dc bus planes.

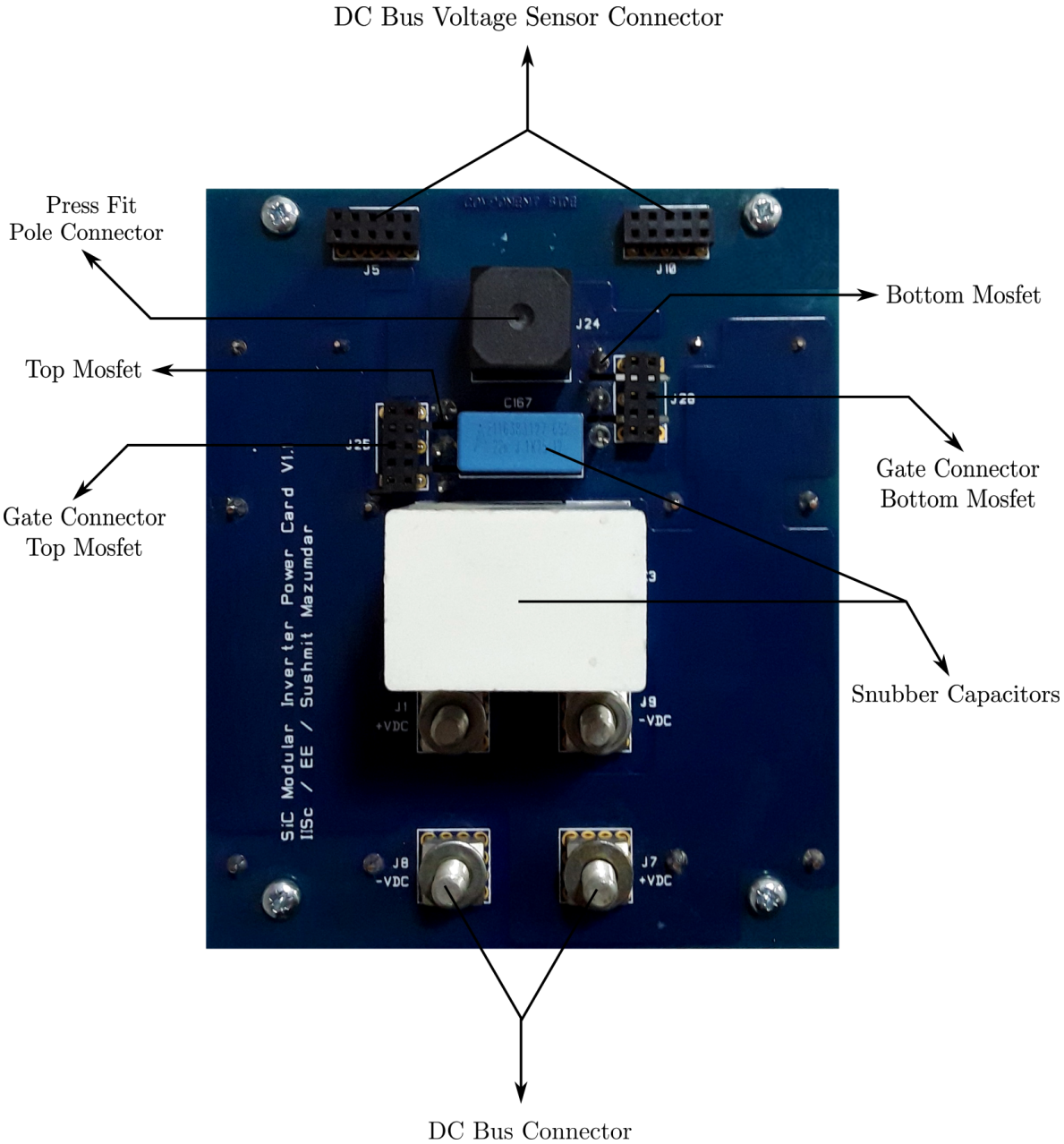



Figure A.8: Developed Power PCB Card

The snubber capacitors are packed tightly to the terminal of the switches, therby minimizing the chance of voltage spikes across the switches. Cut slot of 1 mm width has been provided in between the terminals of the switch to prevent dust accumulation. Wurth connectors has been provided for connecting the dc bus with the adjacent modules. The layout is shown in the Figs. $A.9$, $A.10$, $A.11$ and $A.12$.

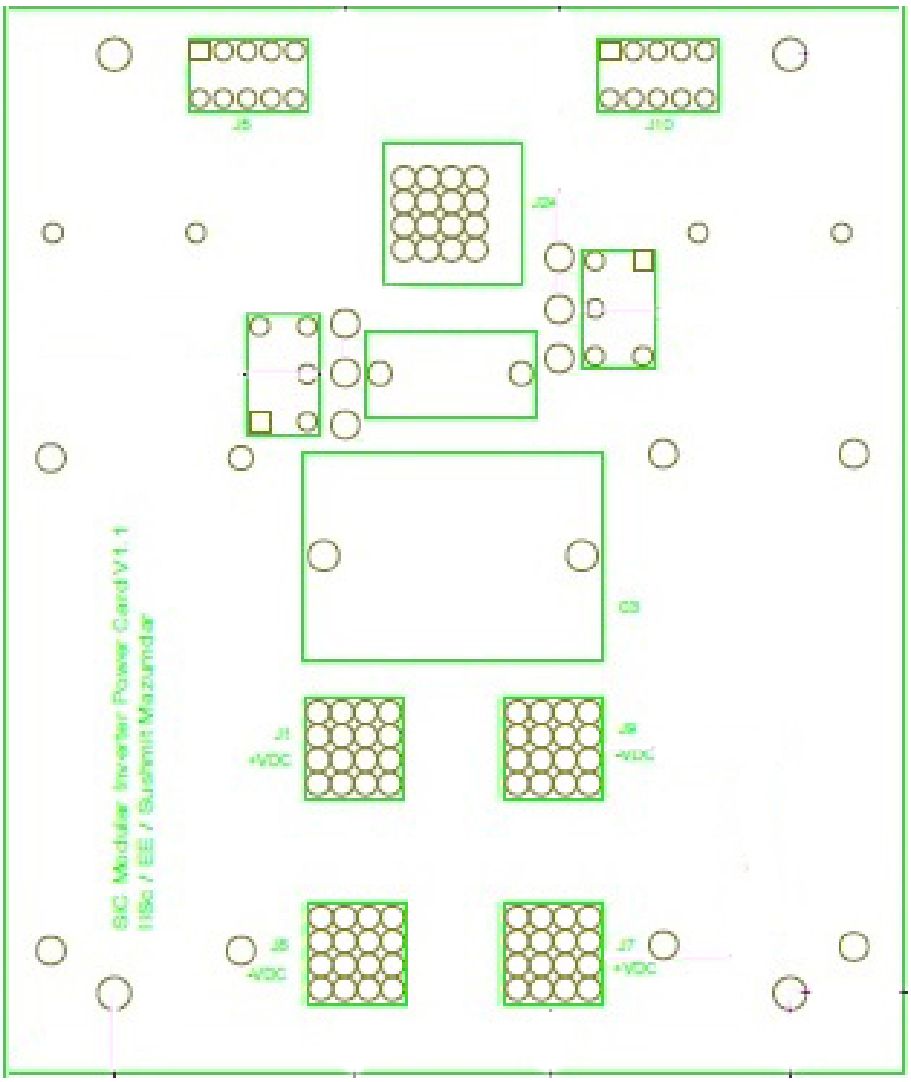



Figure A.9: Top Legend - Component Placement Details of the Power PCB Card

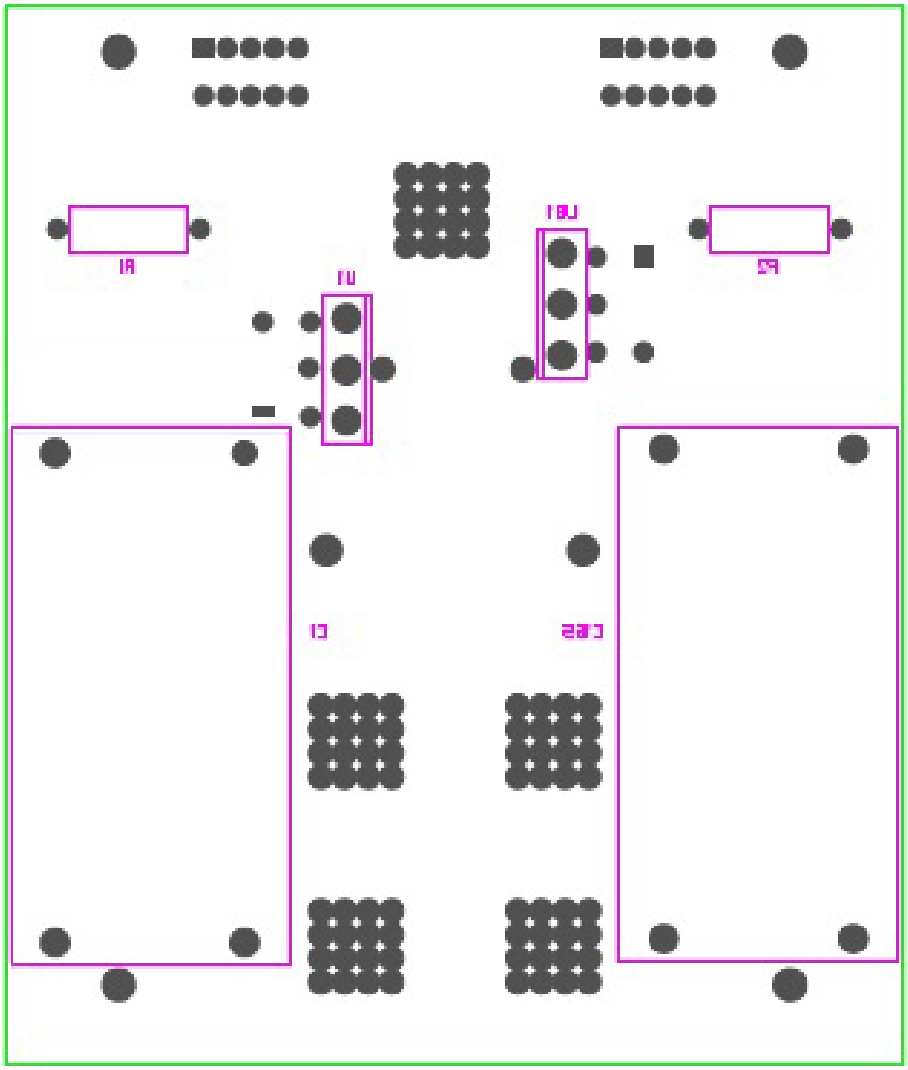


Figure A.10: Bottom Legend - Component Placement Details of the Power PCB Card

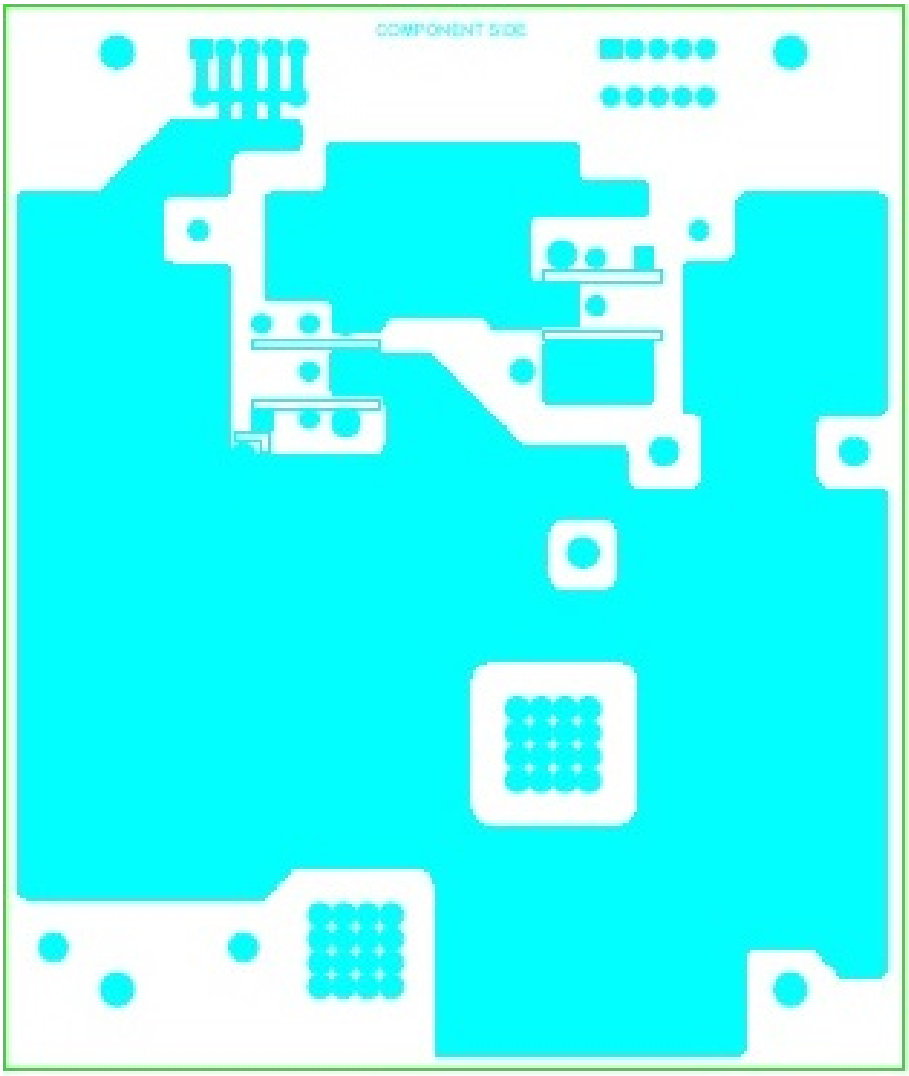



Figure A.11: Routing of First Layer of the Power PCB Card

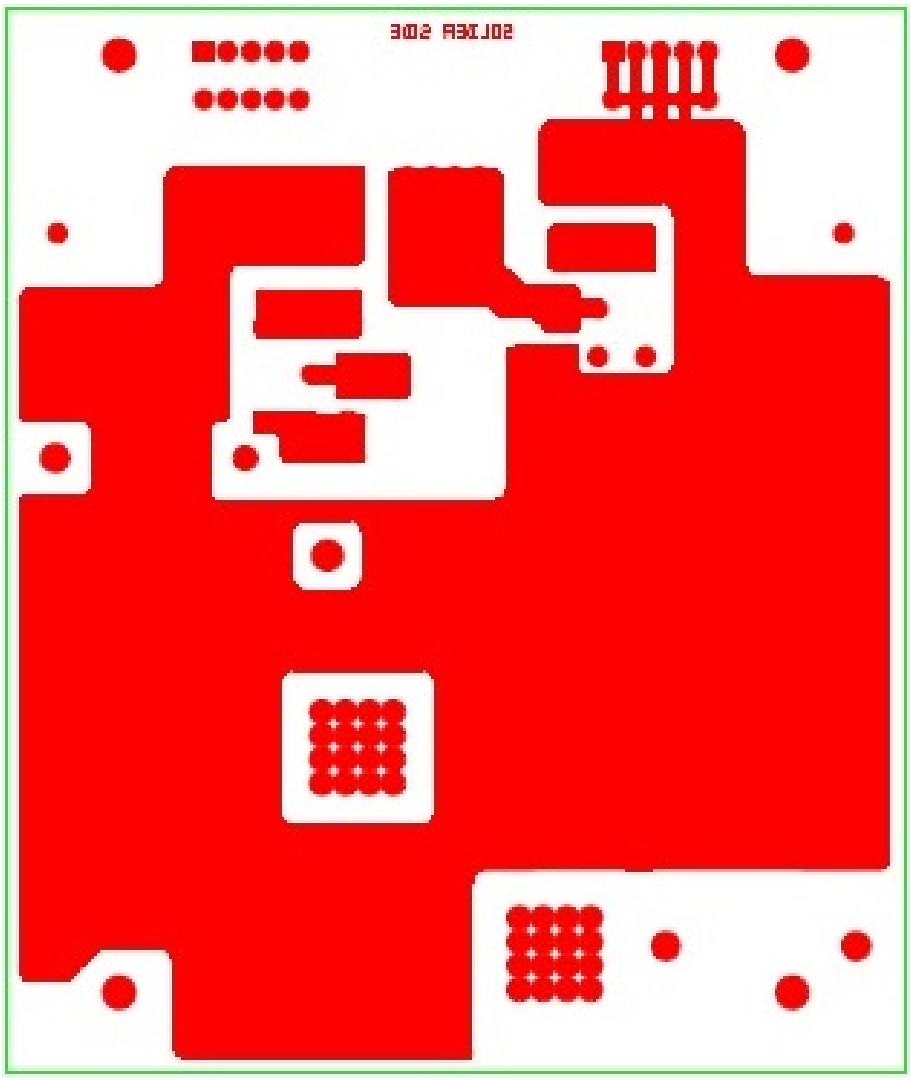


Figure A.12: Routing of Second Layer of the Power PCB Card

## A.5 Selection and Design of Line Chokes

The line choke has been designed in such a fashion so that it can be used as a part of the load for a stand alone converter application as well as can be used as a filter for grid tied application. So we will find the required value of inductance and also the peak current flowing through through the filter before designing it.

### A.5.1 Fixing the Inductance value

**Criteria 1 : Power Factor**

For the stand alone operation of the converter, if $R_L$ is the load resistance and $L_f$ is the inductance per phase and the power factor has to be greater than 0.8 we can say,

$$\frac{R_L}{\sqrt{R_L^2 + \left(\omega_\circ L_f\right)^2}} \geq 0.8$$

Putting $\omega_\circ = 2\pi \times 50$ rad/s and solving the above equation we get,

$$\frac{R_L}{L_f} \geq 419\ s^{-1} \tag{A.49}$$

**Criteria 2 : Corner Frequency**

To provide sufficient amount of attenuation to the switching frequency ripple at the converter output we should ensure that the corner frequency of the load is atleast one decade less than the switching frequency of the converter.

$$\begin{aligned} i.e.\ f_{corner} &\leq \frac{F_{sw}}{10} \\ \therefore \left(\frac{1}{2\pi}\right) \times \frac{R_L}{L_f} &\leq \frac{100000}{10} \\ \Rightarrow \frac{R_L}{L_f} &\leq 62832\ s^{-1} \end{aligned} \tag{A.50}$$

**Criteria 3 : Per unit Voltage drop**

Choosing the rated kVA and the rated line to line voltage of the converter as the base quantities, the base impedance of the converter ($Z_{Base}$) can be evaluated as,

$$Z_{Base} = \frac{415^2}{12500} = 13.778\ \Omega$$

Allowing maximum per unit voltage drop across the inductor to be 0.1, we have

$$\begin{aligned} \frac{\omega_\circ L_f}{Z_{Base}} &\leq 0.1 \\ \Rightarrow L_f &\leq 4.38\ \text{mH} \end{aligned} \tag{A.51}$$

**Criteria 4 : Percentage THD of Line Current**

Under rated operating conditions, we have the fundamental line to line rms voltage to be 415 V and output power to be 10 kW @ 0.8 pf (lag). So the rms value of the fundamental line current is,

$$I_{L(rms)} = \frac{10000}{\sqrt{3} \times 415 \times 0.8} = 17.39\ A$$

Shown in [52], the rms value of the switching ripple current flowing through the inductor for CSVPWM is given by,

$$\tilde{i}_{L(sw-rms)} = 2\frac{V_{DC}M}{F_{sw}L_f}\sqrt{\frac{1}{384}\left(1 - \frac{16}{\sqrt{3}\pi}M + \frac{9}{2}\left(1 - \frac{3\sqrt{3}}{4\pi}\right)M^2\right)} \tag{A.52}$$

Putting the maximum possible value of $M$ i.e. $\frac{1}{\sqrt{3}}$ , we get

$$\tilde{i}_{L(sw-rms)} = \frac{800 \times 0.02515}{100000 \times L_f}$$

Considering the maximum allowable THD to be 5% of the rated line current, we can write

$$\tilde{i}_{L(sw-rms)} \leq \frac{5}{100} \times 17.39$$

$$\Rightarrow \frac{800 \times 0.02515}{100000 \times L_f} \leq 0.8695$$

$$\Rightarrow L_f \geq 0.23\ \text{mH} \tag{A.53}$$

From the equations $A.51$ and $A.53$ we choose the filter inductance to be 0.5 mH. Considering star connected load we have,

$$3 \times I^2_{L(rms)} \times R_L = 10000$$

$$\Rightarrow R_L = \frac{10000/3}{17.39^2} = 11.02\ \Omega$$

$$\therefore \frac{R_L}{L_f} = \frac{11.02}{0.5 \times 10^{-3}} = 22040\ s^{-1}$$

which satisfies equations $A.49$ and $A.50$.

### A.5.2 Current Rating of the Inductor

**RMS Current Rating of the Inductor :**

Under rated operating conditions, the value of the modulation index, $M = \frac{\frac{415}{\sqrt{3}} \times \sqrt{2}}{800} = 0.4235$. Using this value of modulation and the inductance to be 0.5 mH, from equation $A.52$ we get,

$$\tilde{i}_{L(sw-rms)} = \frac{800 \times 0.02065}{0.5 \times 10^{-3} \times 100000} = 0.33\ A$$

Hence the total rms current rating of the inductor is,

$$I_{L_f(rms)} = \sqrt{17.39^2 + 0.33^2} = 17.393\ A$$

**Peak Current Rating of the Inductor :**

The peak to peak ripple current through the inductor for CSVPWM [53, 54] is given by,

$$\tilde{i}_{L(sw\ pk-pk)} = \begin{cases} \frac{M}{2}\frac{V_{DC}}{L_f F_{sw}}\left(1 - \frac{3M}{2}\right), & \text{for } 0 \leq M < 0.282 \\ \\ \frac{M}{2\sqrt{3}}\frac{V_{DC}}{L_f F_{sw}}, & \text{for } 0.282 \leq M < \frac{1}{\sqrt{3}} \end{cases}$$

With the modulation, $M = 0.4235$, we have

$$\tilde{i}_{L(sw\ pk-pk)} = \frac{0.4235}{2\sqrt{3}} \times \frac{800}{0.5 \times 10^{-3} \times 100000} = 1.956\ A$$

So the peak current rating of the inductor is given by,

$$I_{L_f(pk)} = \left(17.39 \times \sqrt{2}\right) + \frac{1.956}{2} = 25.57 \approx 25.6\ A \tag{A.54}$$

### A.5.3 Inductor Design

For the operation of the inductor under high frequency pulse width modulation, it is preferred to use Amorphous C cores to limit the core losses. The saturation flux density of Amorphous C cores is much higher than the ferrite cores, thereby enabling the weight and volume reduction of the inductor.

**Core Selection :**

The area product value of the inductor is given by,

$$\text{Area Product} = \frac{L_f I_{L_f(rms)} I_{L_f(pk)}}{B_{pk} k_w J_{L_f}} \tag{A.55}$$

where,

$$B_{pk} = \text{Peak flux density in the core}$$
$$k_w = \text{Window utilisation factor}$$
$$J_{L_f} = \text{Current density of the conductor}$$

For amorphous core, the saturation flux density is around 1.56 T. So we fix $B_{pk} = 0.8\times 1.56 = 1.248$ T. Considering natural cooling, $J_{L_f}$ is chosen as 4 A/$mm^2$. Assuming $k_w = 0.4$, the value of the area product becomes,

$$\text{Area Product} = \frac{0.5 \times 10^{-3} \times 17.393 \times 25.6}{1.248 \times 0.4 \times 4 \times 10^6} = 1.115 \times 10^{-7}\ m^4 = 11.15\ cm^4$$

So we choose the core AMCC 20 whose area product as given in the datasheet [55] is 17.6 $cm^4$

**Determination of the Turns of Inductor :**

Now we know that,

$$T = \frac{L_f I_{L_f(pk)}}{B_{pk} A_c}$$

where $T$ is the number of turns and $A_c$ is the effective cross-sectional area of the core which is $2.7 \times 10^{-4} m^2$ for AMCC 20.

$$\therefore T = \frac{0.5 \times 10^{-3} \times 25.6}{1.248 \times 2.7 \times 10^{-4}} \approx 38 \tag{A.56}$$

**Conductor Selection :**

The required conductor diameter, $d_w = \sqrt{\frac{4 I_{L_f(rms)}}{J_{L_f} \times \pi}} = 2.353$ mm. So we choose SWG 12 as the conductor, whose diameter is 2.64 mm.

Hence modified value of the window utilisation factor $= \dfrac{T \times \frac{\pi}{4} \times 2.64^2}{\text{Window Area of the Core } (A_w)}$

As $A_w = 650\ mm^2$ for the core AMCC 20,

$$\therefore k'_w = \frac{38 \times \frac{\pi}{4} \times 2.64^2}{650} = 0.32$$

**Determination of the air gap length :**

Considering that most of the energy is stored in the air gap, the length of the air gap on each side of the core,

$$l_g = \frac{T^2 \mu_\circ A_c}{2 L_f} \approx 0.5 \text{ mm}$$

## A.6 Design and Implementation of the Gate Driver Card

Before selecting the gate driver IC, we need to check the specifications so that it is compatible with the selected device (SCH2080KE). Once the IC is selected, then the various other components of the gate drive circuit needs to be selected. Having this done, we then need to address the layout considerations of the gate driver card.

### A.6.1 Selection of Gate-Source Voltage Supply

The device will be switched at a very high frequency nearly 100 kHz. So due to the parasitic inductance in the gate drive loop, there will be a spike across the gate-source terminal of the device. The maximum allowable gate-source voltage for the device SCH2080KE is $+22/-6$ V. So we put anti-parallel zener diode across the gate-source terminal to limit this spike. Again the gate-source voltage should be high enough during turn on so that the channel resistance is sufficiently low therby enabling better conduction. So we choose +18.3 V for the gate-source power supply. At the same time to provide protection against miller turn on, we provide -3.3 V to the gate-source terminal of the switch while it is off.

### A.6.2 Selection of Gate Resistance

We know that for a series R-L-C circuit, the damping factor, $\xi$ is given by,

$$\xi = \frac{R_s}{2}\sqrt{\frac{C_s}{L_s}} \tag{A.57}$$

where, $R_s$, $L_s$ and $C_s$ are the circuit resistance, inductance and capacitance respectively. Drawing an analogy with the gate drive loop, we should make $\xi \geq 1$ in order to suppress the oscillation across the gate-source terminal of the device. With the input capacitance of the device to be 1850 pF (from the datasheet of SCH2080KE) and ensuring that the parasitic inductance in the gate drive loop is less than 10 nH, we get

$$R_s \geq 2 \times \sqrt{\frac{10 \times 10^{-9}}{1850 \times 10^{-12}}} = 4.65\ \Omega$$

Now the device SCH2080KE has an internal gate resistance of 6.3 Ω. In order to limit the peak value of the gate current (which is provided by the gate driver IC), we provide an external gate resistance of 4.7 Ω during turn on of the switch. Also to ensure that the device is turned off very quickly we provide external gate resistance of 1.1 Ω during turn off of the switch. So the effective gate resistance during turn on process is 11 Ω and that during turn off process is 7.4 Ω.

### A.6.3 Peak Gate Drive Current Requirement

The internal gate resistance of the device SCH2080KE is 6.3 Ω. So during turn on, the peak gate current required is,

$$I_{Gpk(TurnOn)} = \frac{18.3 + 3.3}{6.3 + 4.7} = 1.96 \text{ Amp}$$

Similarly during turn off, the peak gate current required is,

$$I_{Gpk(TurnOff)} = \frac{18.3 + 3.3}{6.3 + 1.1} = 2.92 \text{ Amp}$$

### A.6.4 Selection of Gate Driver IC

Considering the above factors we choose ADuM4135 [56] from Analog Devices as the gate driver IC. The important features of the gate driver are provided in Table- *A*.4.

Table A.4: Features of ADuM4135 Gate Driver IC

| Sl. No. | Parameters | Value |
|---|---|---|
| 1 | Maximum possible output voltage | 30 V |
| 2 | Peak drive output capability | 4 Amp |
| 3 | Input voltage range | 2.3 V to 6 V |
| 4 | Over current protection | Soft shut down |
| 5 | Miller clamp | During turn off |
| 6 | Output power device resistance | $< 1\ \Omega$ |
| 7 | Propagation delay | $< 55$ ns |
| 8 | Common mode transient immunity | 100 kV/$\mu$s |
| 9 | Resistance between input side to output side | $10^6$ MΩ |

### A.6.5 Power Dissipation in Gate Driver IC

During driving the MOSFET gate, there is power loss inside the driver IC. This power is not insignificant and can lead to thermal wear out if considerations are not made. The gate of a MOSFET can be roughly simulated as a capacitive load. Due to Miller capacitance and other non-linearities, it is common practice to take the stated input capacitance, $C_{iss}$, of a given MOSFET, and multiply it by a factor of 5 to arrive at a conservative estimate to approximate the load being driven. With this value, the estimated total power dissipation $P_{Diss}$ due to switching action is given by,

$$P_{Diss} = C_{est} \left(V_{GS+} - V_{GS-}\right)^2 F_{sw} \tag{A.58}$$

$$\Rightarrow P_{Diss} = 5 \times 1850 \times 10^{-12} \times (18.3 + 3.3)^2 \times 100 \times 10^3$$

$$\Rightarrow P_{Diss} = 0.43\ W$$

This power dissipation is shared between the on state resistances of the switches inside the gate driver IC ($R_{DSON-P}$ and $R_{DSON-N}$) and the external gate resistances, ($R_{Gon}$ and $R_{Goff}$). The ratio of the internal gate resistances to the total series resistance allows the calculation of losses seen within the ADuM4135 chip.

$$P_{Diss}^{ADuM4135} = \frac{1}{2} P_{Diss} \left[ \frac{R_{DSON-P}}{R_{Gon} + R_{DSON-P}} + \frac{R_{DSON-N}}{R_{Goff} + R_{DSON-N}} \right] \tag{A.59}$$

Putting the corresponding values from the datasheet of ADuM4135 IC, we get

$$P_{Diss}^{ADuM4135} = \frac{1}{2} \times 0.43 \times \left[ \frac{0.975}{4.7 + 6.3 + 0.975} + \frac{0.625}{1.1 + 6.3 + 0.625} \right] = 0.0342\ W$$

Taking the power dissipation found inside the chip and multiplying it by the thermal resistance between the IC junction and ambient, gives the rise above ambient temperature that the ADuM4135 experiences.

$$T_j^{ADuM4135} = T_{amb} + P_{Diss}^{ADuM4135} R_{ja}^{ADuM4135} \tag{A.60}$$

$$\Rightarrow T_j^{ADuM4135} = 30 + 0.0342 \times 75.4 = 32.58^{\circ}C$$

For the device to remain within specification, $T_j^{ADuM4135}$ must not exceed $125^{\circ}C$. If $T_j^{ADuM4135}$ exceeds $155^{\circ}C$ (typical), the device enters thermal shutdown mode.

### A.6.6 Features of the Designed Gate Driver Card

The Gate Driver Card has been designed such that it can be used in a plug and play fashion with the following features :

- PWM signal conditioning and providing required hardware delay.
- Provision for accepting both analog and optical pwm signals.
- Fault latching and feedback to the controller.
- Provision for manual reset or automatic reset of the fault.
- Pole current sensing and feedback to the controller.
- Annunciation of various conditions for monitoring.
- Gate power supply under-voltage lockout.

### A.6.7 Layout Considerations

Fig. $A.13$ shows the developed gate driver card. A four layer board is used for the gate driver card. The PCB layout of the gate driver card is being shown in the Figs. $A.14$, $A.15$, $A.16$, $A.17$, $A.18$ and $A.19$. The routing is explained as follows.

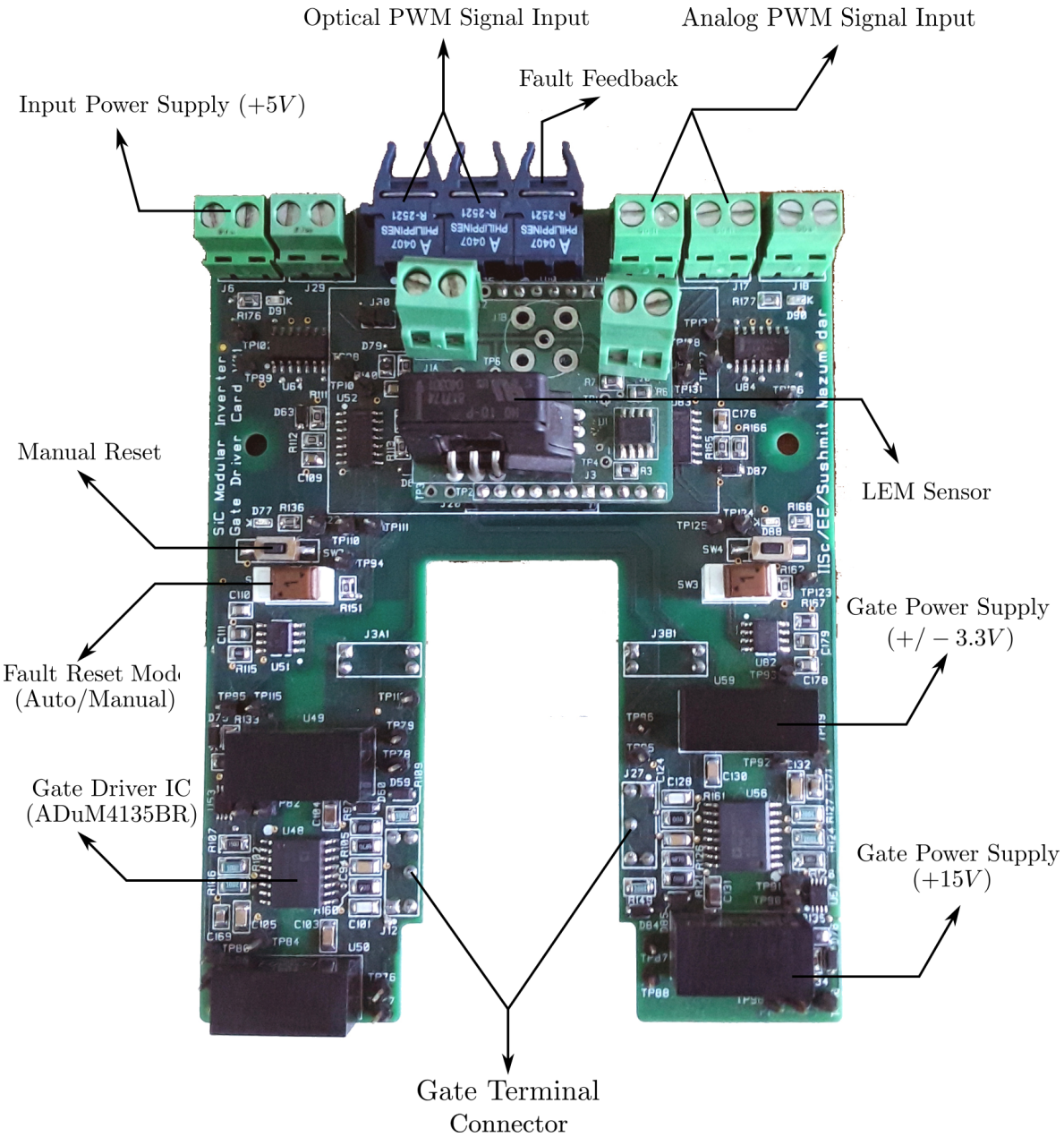



Figure A.13: Developed Gate Driver Card

**Signal Side :**

The top layer contains all the PWM signals coming from the micro-controller. Then the second layer contains the common ground. The third layer contains the +5 V power supply for the gate driver input. So there is sandwiching effect in the first and the second layer as well as the second and third layer. The fourth layer contains fault feedback signal.

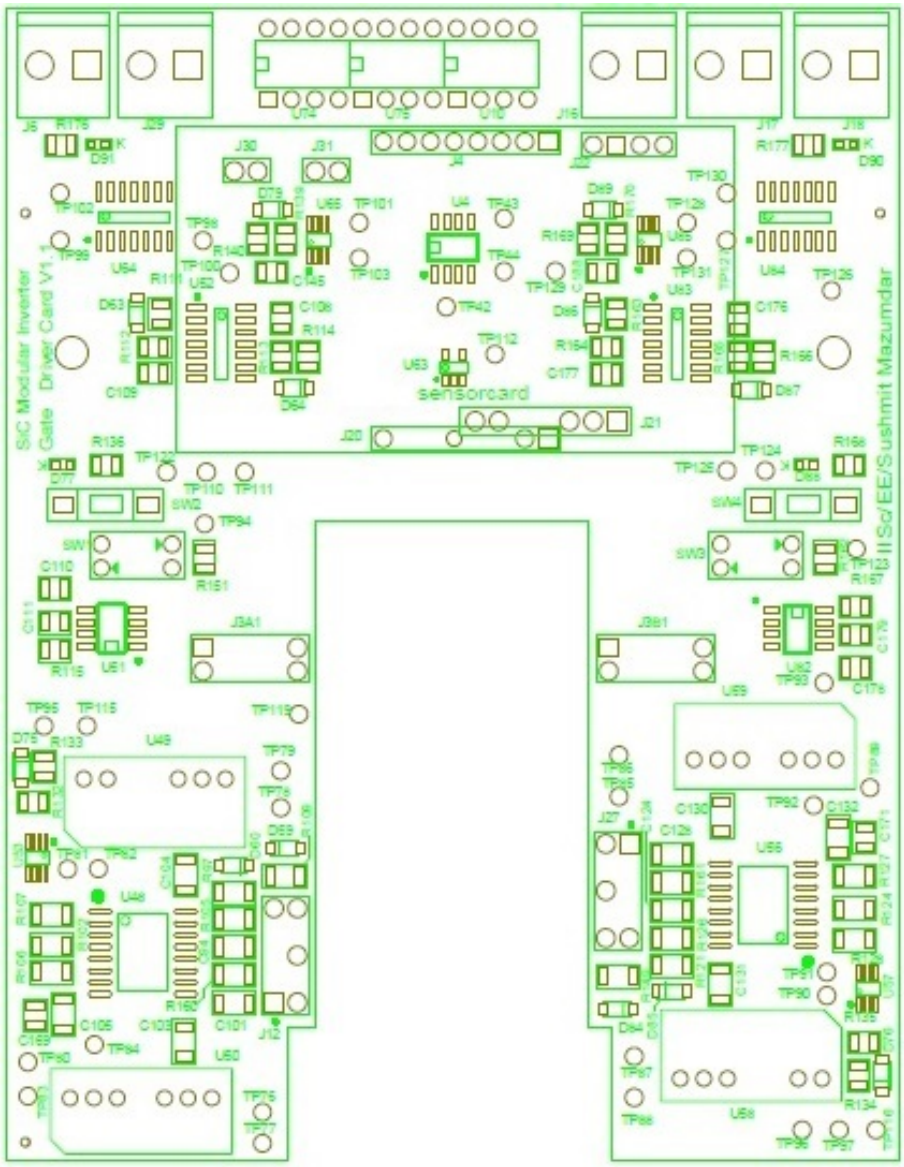



Figure A.14: Top Legend - Component Placement Details of the Gate Driver Card

**Power Side :**

The top layer contains the plane for the gate connections. In the second layer the source plane is expanded to minimize the gate drive loop parasitic inductance. The third layer contains the +18.3 V plane and the fourth layer contains the -3.3 V plane. Decoupling capacitors have been put across the gate drive power supply to momentarily support the peak current requirement.

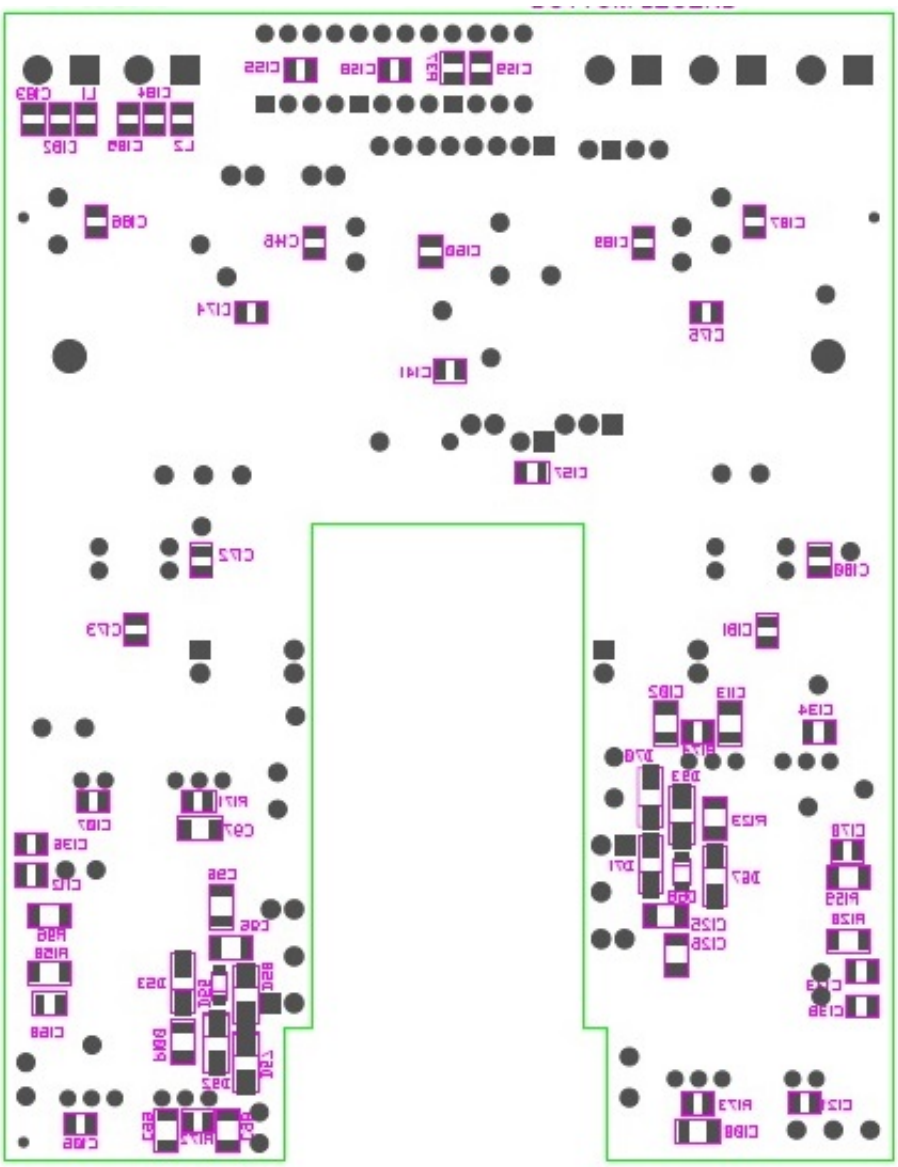


Figure A.15: Bottom Legend - Component Placement Details of the Gate Driver Card

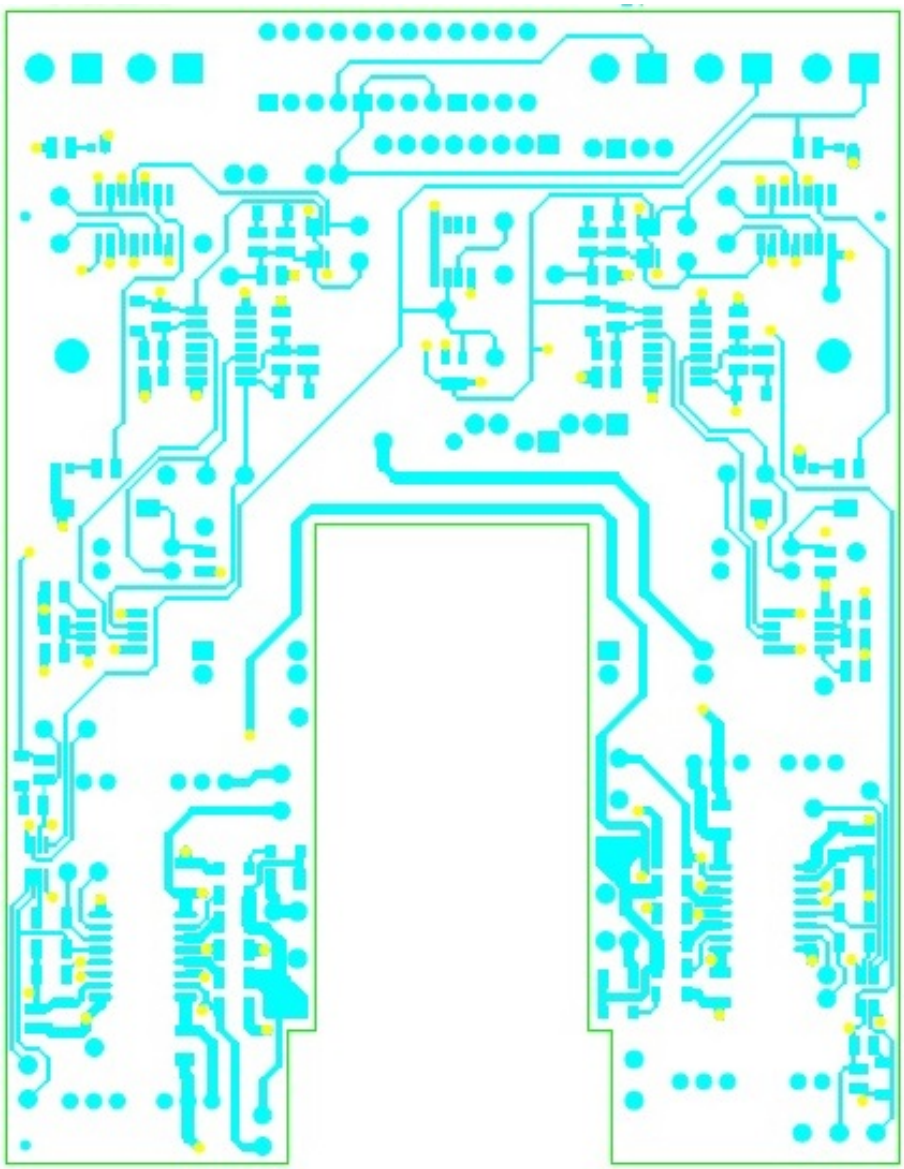


Figure A.16: Routing of First Layer of the Gate Driver Card

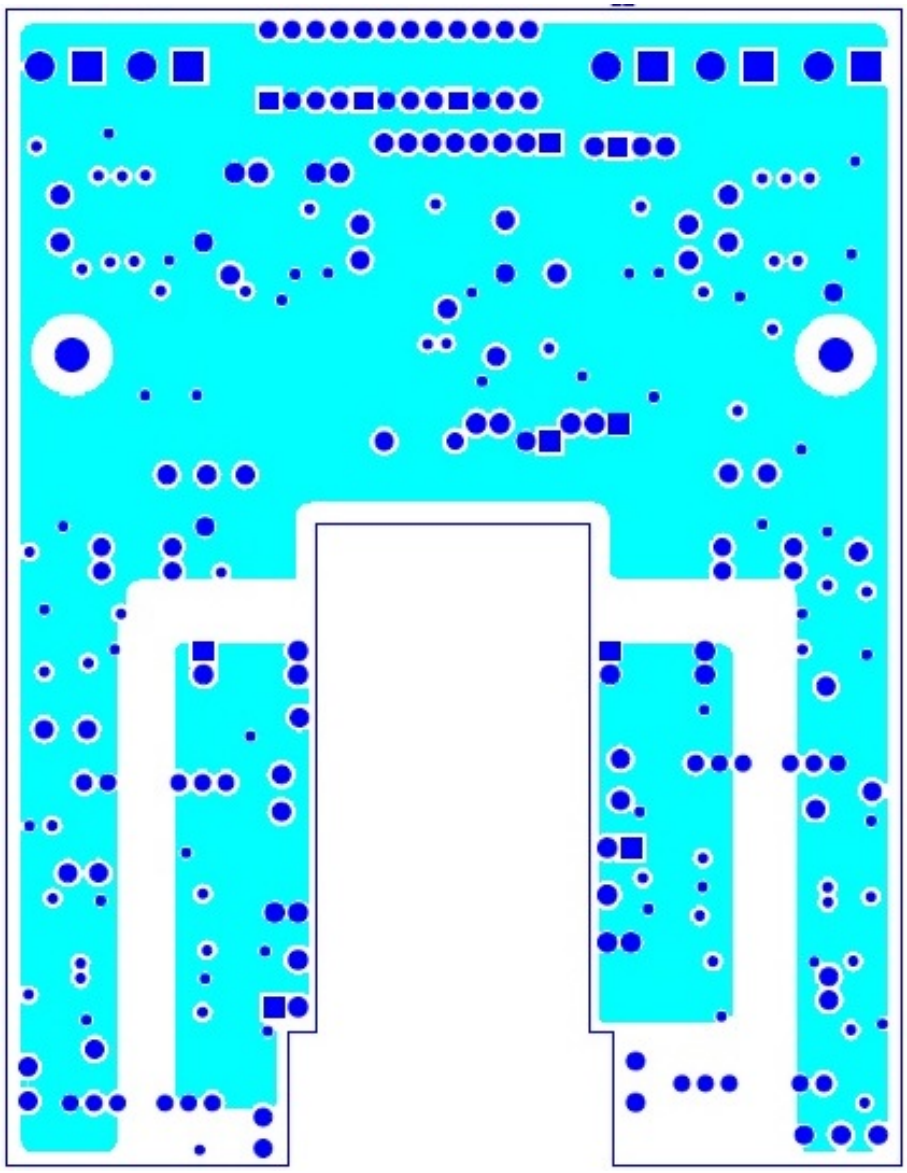


Figure A.17: Routing of Second Layer of the Gate Driver Card

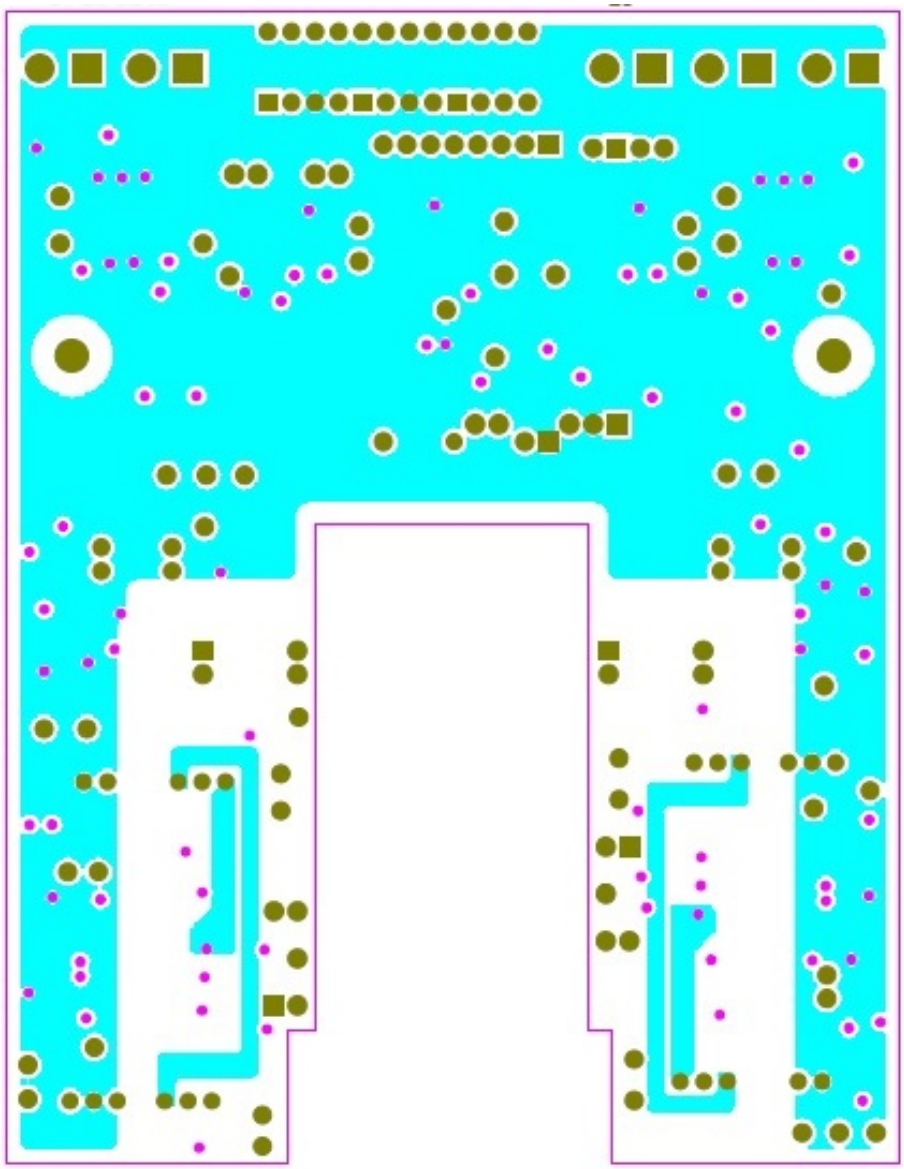


Figure A.18: Routing of Third Layer of the Gate Driver Card

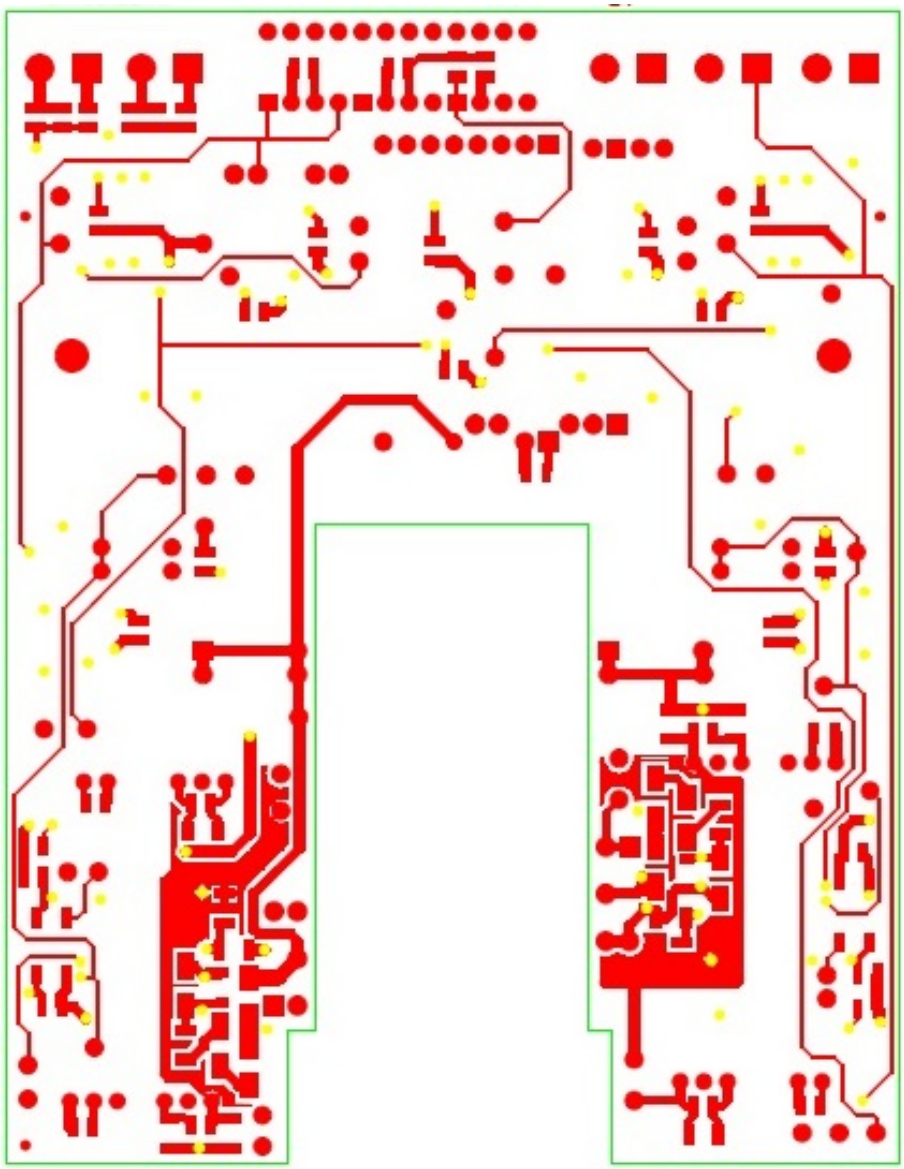


Figure A.19: Routing of Fourth Layer of the Gate Driver Card

## A.7 Testing of Power Converter

### A.7.1 Module Operation as a Buck Converter

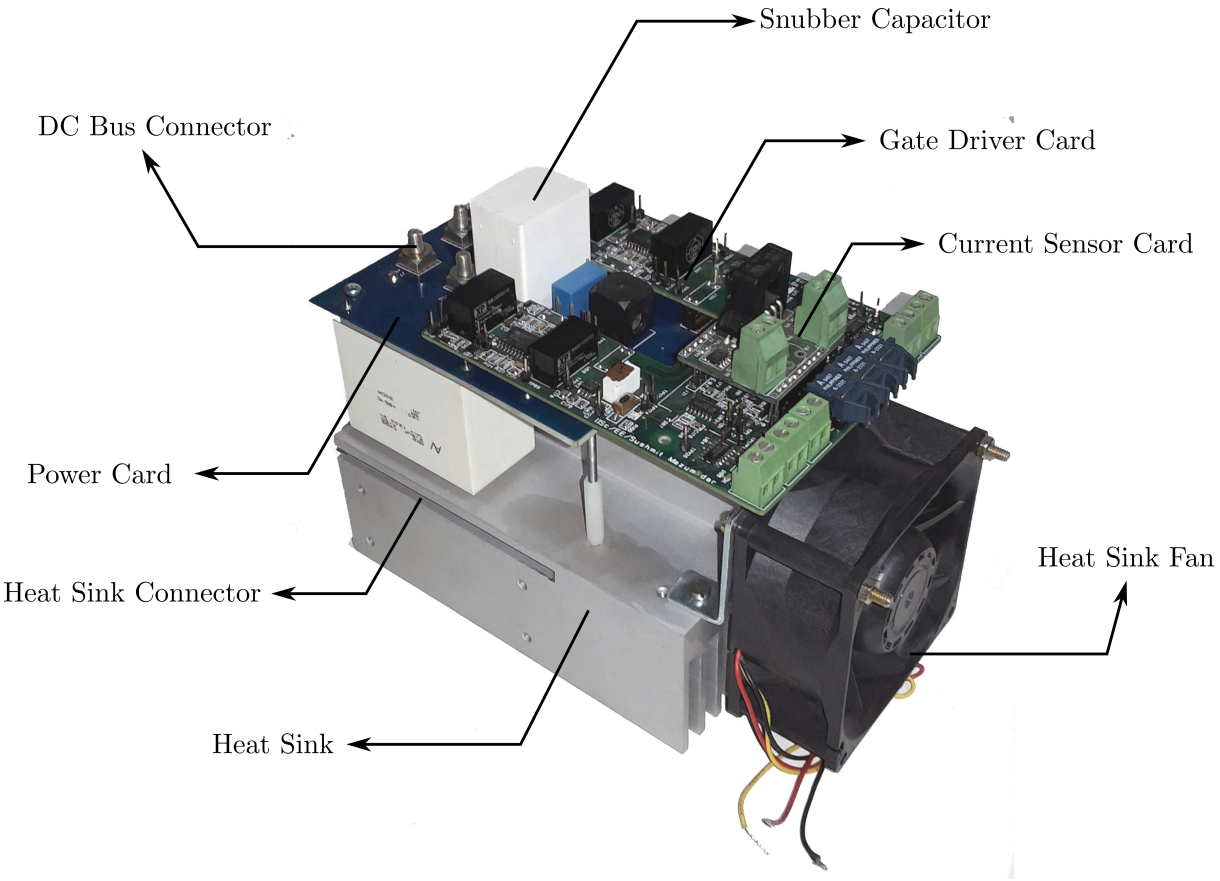


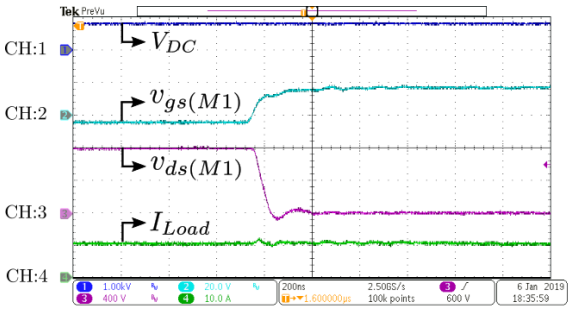

Figure A.20: Module of the developed Converter

Each of the developed module (leg) as shown in Fig. $A.20$ is operated at rated conditions as a buck converter. With the assumption that the positive and the negative channel resistances of the MOSFET are equal and neglecting the dead time, the conduction losses in the top MOSFET is $\left\{\left(I_{Load}\sqrt{D}\sqrt{1+\frac{1}{3}\left(\frac{\Delta i_{L(pk-pk)}}{2I_{Load}}\right)^2}\right)^2 r_{DS}\right\}$ and in the bottom MOSFET is $\left\{\left(I_{Load}\sqrt{1-D}\sqrt{1+\frac{1}{3}\left(\frac{\Delta i_{L(pk-pk)}}{2I_{Load}}\right)^2}\right)^2 r_{DS}\right\}$, where $D$, $I_{Load}$ and $\Delta i_{L(pk-pk)}$ are the duty ratio, load current and the peak to peak inductor ripple current of the buck converter. Now with reference to the equations $A.25$ and $A.27$, to equalize the conduction losses in the top and the bottom MOSFET, we select

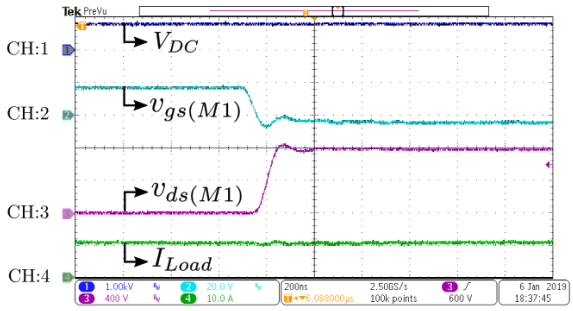
$D$ as 0.5. Therefore the load current of the converter is,

$$I_{Load} = \frac{P_{rated}/3}{DV_{DC}} = \frac{10000/3}{0.5 \times 800} = 8.33 \text{ Amp} \tag{A.61}$$

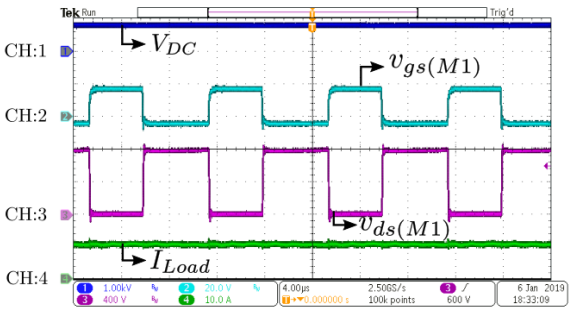
The drain to source voltage of the top MOSFET ($v_{ds(M1)}$) along with its gate to source voltage ($v_{gs(M1)}$) for the rated value of dc bus voltage and load current is shown in Fig. $A.21$. The zoomed in view during the turn on and turn off of the top MOSFET are shown in Figs. $A.21$(a) and $A.21$(b) respectively while the zoomed out view is shown in Fig. $A.21$(c).




(a)
[Time Scale-200ns/div]




(b)
[Time Scale-200ns/div]




(c)
[Time Scale-4$\mu$s/div]

Figure A.21: Module shown in Fig. $A.20$ operating as a Buck Converter [CH:1-1kV/div], [CH:2-20V/div], [CH:3-400V/div], [CH:4-10A/div]

### A.7.2 Open Loop Operation of the $3\phi$ VSC

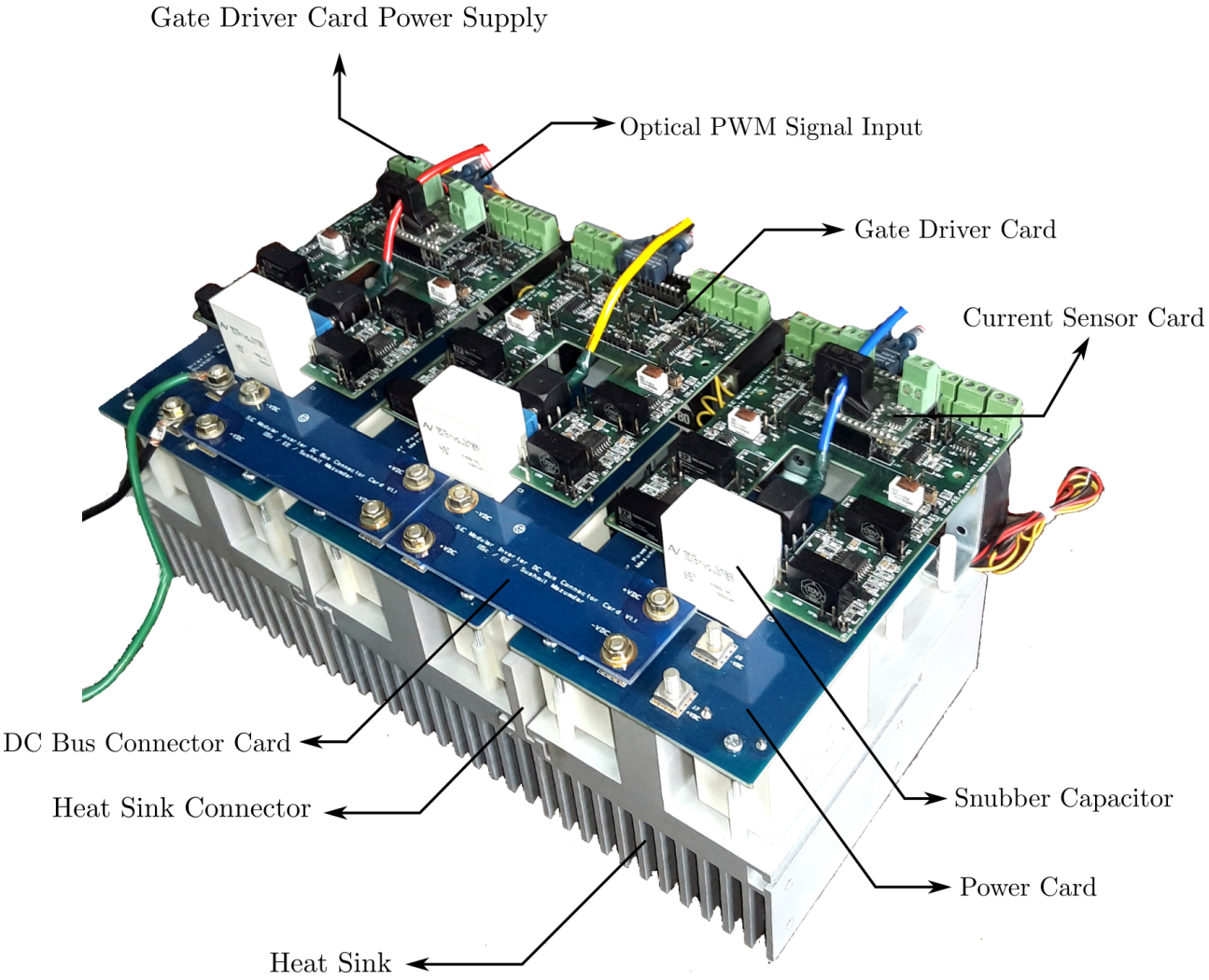



Figure A.22: The developed $3\phi$ SiC based Power Electronic Converter

The $3\phi$ VSC shown in Fig. $A.22$, is operated at rated conditions provided in Table-$A.1$ in open loop mode, feeding a passive R-L load. The relevant waveforms are shown in Fig. $A.23$.

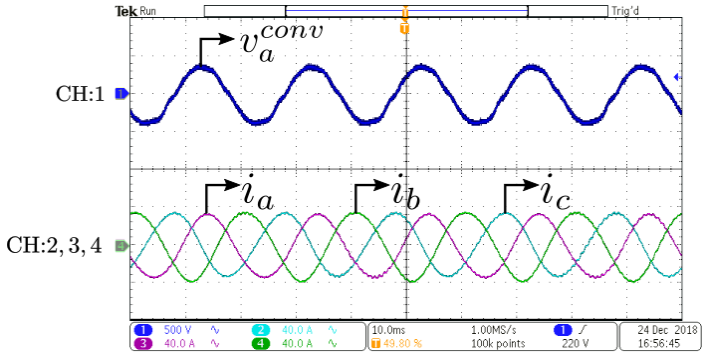



Figure A.23: $3\phi$ VSC feeding a Passive R-L Load [CH:1-500V/div], [CH:2,CH:3,CH:4-40A/div], [Time Scale-20ms/div]

### A.7.3 Grid Tied Operation of the $3\phi$ VSC

Before connecting the converter to the grid, the output line voltages of the converter are properly synchronized with the grid voltages. The following steps are adopted for the grid synchronization :

**Step 1 :**

The grid voltages are sensed and proper modulating signals are generated inside the embedded platform for required control action.

**Step 2 :**

Having this done, the output line voltages of the converter are slowly build up to match the grid voltage which is shown in Fig. *A*.24(a).

**Step 3:**

Once the magnitude of the converter output voltage becomes nearly equal to the grid voltage, the contactor $C_1$, shown in Fig. 4.3 is being closed and the converter now starts operating in zero current control mode. The relevant waveforms are shown in Fig. *A*.24(b).

**Step 4:**

A step change in the current reference is then given to observe the performance of the current controller whose architecture is shown in Chapter 5. The results are shown in Fig. *A*.24(c).

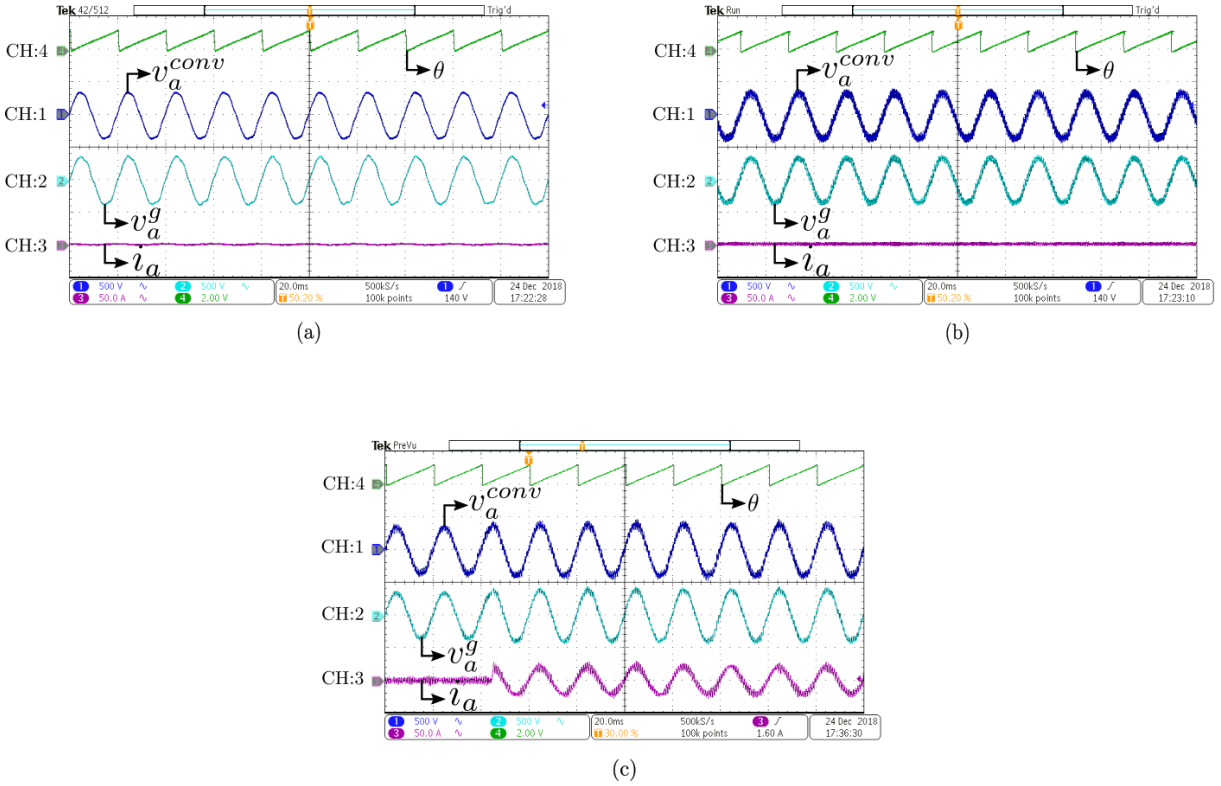



Figure A.24: $3\phi$ VSC operating in Grid Connected mode [CH:1,CH:2-500V/div], [CH:3-50A/div], [CH:4-2V/div], [Time Scale-20ms/div]

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# Appendix B

# Controller Design for Active Front End Converter

The design algorithm for the Synchronous Reference Frame-Phase Lock Loop (SRF-PLL) is provided in this appendix. Also as proposed in Chapter 4, the controller design methodology for the Active Front End Converter (AFEC) has been elaborately discussed here.

## B.1 Synchronous Reference Frame - Phase Lock Loop

In order to transform any state variables from its natural frame ($abc$) of reference to the synchronous frame ($dq0$) of reference we need a SRF-PLL to estimate the instantaneous phase information of the corresponding state variables. The advantage of controlling in '$dq$' frame is that the 50 Hz state variables in the natural frame of reference gets transformed into the dc quantities in the synchronous frame of reference. So then we can use a PI controller to track the reference quantities since it provides infinite gain at dc, thereby providing zero steady state error.

### B.1.1 Basics of Space Phasor

The $3\phi$ grid voltages ($v_a^g$, $v_b^g$, $v_c^g$) can be converted from natural frame of reference to stationary two phase reference frame ($\alpha\beta$) by applying Clarke's Transformation as shown in the equation $B.1$.

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos 0 & \cos \frac{2\pi}{3} & \cos \frac{4\pi}{3} \\ \sin 0 & \sin \frac{2\pi}{3} & \sin \frac{4\pi}{3} \end{bmatrix} \begin{bmatrix} v_a^g \\ v_b^g \\ v_c^g \end{bmatrix} \tag{B.1}$$

The factor $\frac{2}{3}$ is used to maintain power equivalence in each phase either in '$abc$' frame of reference or in '$\alpha\beta$' frame of reference. Let us consider

$$v_a^g = V_{pk}\cos\left(\omega_\circ t + \theta_\circ\right) \tag{B.2}$$

$$v_b^g = V_{pk}\cos\left(\omega_\circ t + \theta_\circ - \frac{2\pi}{3}\right) \tag{B.3}$$

and

$$v_c^g = V_{pk}\cos\left(\omega_\circ t + \theta_\circ - \frac{4\pi}{3}\right) \tag{B.4}$$

where, $V_{pk}$ is the peak value of the phase voltage and $\omega_\circ$ is the nominal value of the grid frequency. Substituting equations $B.2$, $B.3$ and $B.4$ in the equation $B.1$ we get,

$$v_\alpha = V_{pk}\cos\left(\omega_\circ t + \theta_\circ\right) \tag{B.5}$$

and

$$v_\beta = V_{pk}\sin\left(\omega_\circ t + \theta_\circ\right) \tag{B.6}$$

Now we will transform the state quantities from stationary two phase reference frame $(\alpha\beta)$ to the synchronous revolving reference frame $(dq)$ using Park's Transformation as shown in the equation $B.7$.

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos\theta_e & \sin\theta_e \\ -\sin\theta_e & \cos\theta_e \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{B.7}$$

where $\theta_e$ is the estimated angular position of the $d$ axis with respect to the $\alpha$ axis. Putting equations $B.5$ and $B.6$ in equation $B.7$ we get,

$$v_d = V_{pk}\cos\left(\omega_\circ t + \theta_\circ - \theta_e\right) \tag{B.8}$$

and

$$v_q = V_{pk}\sin\left(\omega_\circ t + \theta_\circ - \theta_e\right) \tag{B.9}$$

### B.1.2 Operation of the $3\phi$ SRF-PLL

To estimate the phase angle of the grid voltage by SRF-PLL, we will use a feedback control system with a PI regulator as shown in Fig. $B.1$. The nominal frequency of the grid is feed forwarded for faster response of the PLL. Now from the equation $B.9$ we can write,

$$v_q = V_{pk}\sin\left(\omega_\circ t + \theta_\circ - \left(\omega_\circ + \Delta\omega\right)t\right)$$

$$\Rightarrow v_q \approx V_{pk}\left(\theta_\circ - \Delta\omega t\right) \tag{B.10}$$

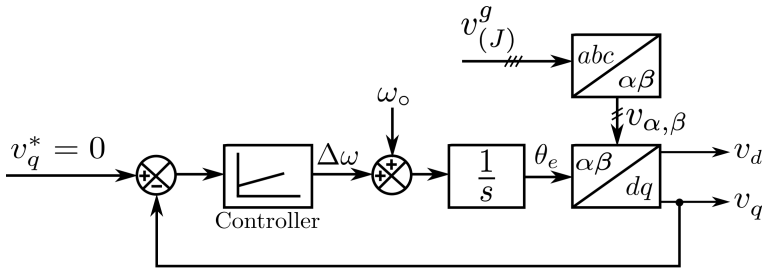


Figure B.1: Operation of the SRF-PLL

The control loop structure is redrawn as shown in the Fig. $B.2$. The plant transfer function, $G_p^{PLL}(s)$ can be written as,

$$G_p^{PLL}(s) = -\frac{V_{pk}}{s}$$

With the controller transfer function, $G_c^{PLL}(s) = -K_p^{PLL} - \frac{K_i^{PLL}}{s}$, the open loop transfer function becomes

$$G_{oltf}^{PLL}(s) = \frac{V_{pk}}{s}\left(K_p^{PLL} + \frac{K_i^{PLL}}{s}\right) = \frac{V_{pk}K_i^{PLL}}{s^2}\left(1 + s\frac{K_p^{PLL}}{K_i^{PLL}}\right)$$

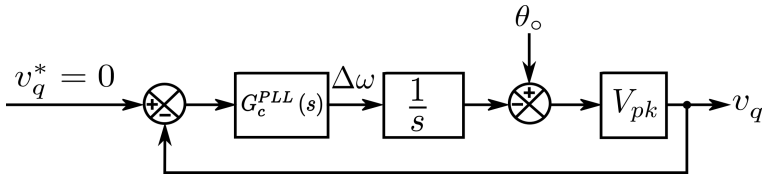


Figure B.2: Simplified Small Signal Block Diagram of the SRF-PLL

In order to obtain the maximum possible phase margin, the bode magnitude plot of the above transfer function is made to cross the 0 dB line at a slope of $-20$ dB/decade. Hence we place the zero, one decade before the desired gain cross-over frequency. Choosing the gain cross-over frequency as 60 Hz, we can write

$$\frac{K_i^{PLL}}{K_p^{PLL}} = \frac{1}{10} \times 2\pi \times 60 = 12\pi$$

Equating the gain of the open loop transfer function to unity at the gain cross-over frequency, we get

$$\left|G_{oltf}^{PLL}(j\omega)\right|_{\omega=\omega_{gc}} = \frac{V_{pk}K_i^{PLL}}{(2\pi \times 60)^2}\sqrt{1 + \left(\frac{2\pi \times 60}{12\pi}\right)^2} = 1$$

Considering the line to line rms voltage to be 415 V we get, $V_{pk} = \frac{\sqrt{2}\times 415}{\sqrt{3}} \approx 339$ V. Therefore,

$$K_i^{PLL} \approx \frac{(2\pi \times 60)^2}{10 \times 339} \approx 42$$

and

$$K_p^{PLL} = \frac{K_i^{PLL}}{12\pi} = \frac{42}{12\pi} = 1.114$$

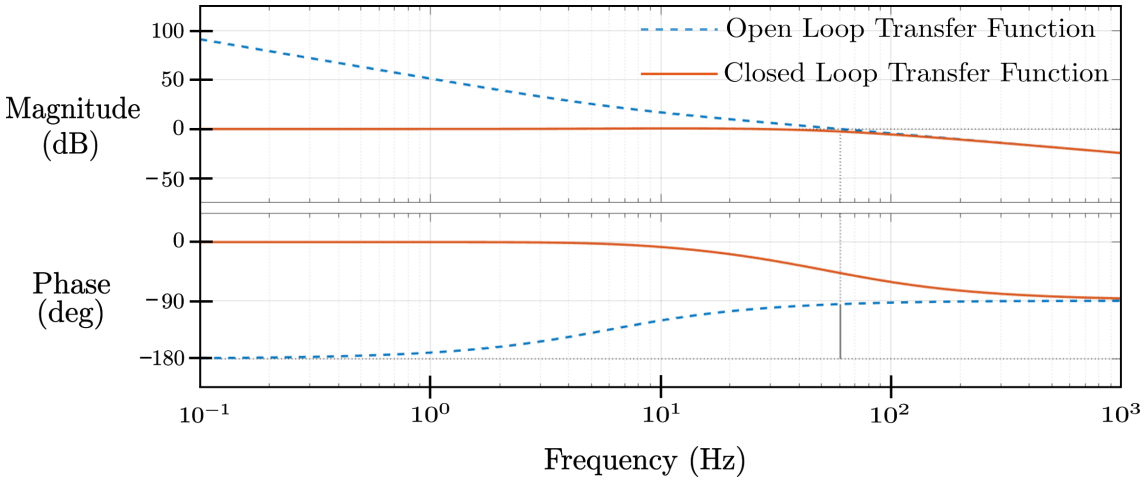


Figure B.3: Bode Diagram of the SRF-PLL Control Loop

Table B.1: Parameters of the Controller used in SRF-PLL

| Sl.No. | Parameter | Value |
|---|---|---|
| 1 | Peak value of phase to neutral voltage, $V_{pk}$ | 339 V |
| 2 | Gain cross-over frequency | 60 Hz |
| 3 | $K_p^{PLL}$ | 1.114 |
| 4 | $K_i^{PLL}$ | 42 |
| 5 | Phase Margin | 84.3° |

## B.2 Controller Design of AFEC

A $3\phi$ ac to dc conversion is an essential part of power electronic system. The thyristor based rectifiers are incapable of bi-directional power flow and also behave as a non linear load thereby drawing currents containing a fundamental (line frequency) as well as harmonic components. Therefore the main supply voltage (feeding other parallel connected loads) gets distorted due to the drop in the line filter inductance by the harmonic currents. To mitigate this problem we will use a pulse width modulated rectifier as the AFEC. These rectifier will draw near sinusoidal currents from the

mains and also regulate the dc output voltage at the same time [57–59]. The voltage at the mid-point of the leg contains a fundamental component at line frequency and also harmonic components near the switching frequency and its multiple. As the switching frequency is very high, therefore these components get easily filtered out by the line inductor. Hence the current drawn from the supply is near sinusoidal.

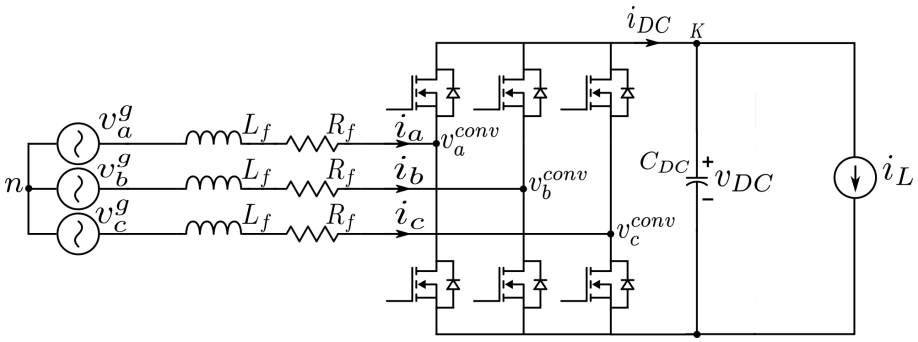


Figure B.4: Active Front End Converter

### B.2.1 Plant Equations of Inner Current Loop

The state equations from the Fig. $B.3$ can be written as,

$$v_a^g = v_a^{conv} + R_f i_a + L_f \frac{\mathrm{d}i_a}{\mathrm{d}t} \tag{B.11}$$

$$v_b^g = v_b^{conv} + R_f i_b + L_f \frac{\mathrm{d}i_b}{\mathrm{d}t} \tag{B.12}$$

and

$$v_c^g = v_c^{conv} + R_f i_c + L_f \frac{\mathrm{d}i_c}{\mathrm{d}t} \tag{B.13}$$

Applying Clarke and Park Transformations on the above state equations, we get

$$v_q = v_q^{conv} + R_f i_q + L_f \frac{\mathrm{d}i_q}{\mathrm{d}t} + \omega_\circ L_f i_d \tag{B.14}$$

and

$$v_d = v_d^{conv} + R_f i_d + L_f \frac{\mathrm{d}i_d}{\mathrm{d}t} - \omega_\circ L_f i_q \tag{B.15}$$

Due to frame transformation the cross coupling terms appear in the above equations. Now applying Laplace Transformation on the equations $B.14$ and $B.15$ we get,

$$v_q(s) = v_q^{conv}(s) + R_f i_q(s) + sL_f i_q(s) + \omega_\circ L_f i_d(s) \tag{B.16}$$

and

$$v_d(s) = v_d^{conv}(s) + R_f i_d(s) + sL_f i_d(s) - \omega_\circ L_f i_q(s) \tag{B.17}$$

Therefore the plant equations governing the inner current loop are :

$$i_q(s) = \frac{1}{R_f + sL_f}\left(v_q(s) - v_q^{conv}(s) - \omega_\circ L_f i_d(s)\right) \tag{B.18}$$

and

$$i_d(s) = \frac{1}{R_f + sL_f}\left(v_d(s) - v_d^{conv}(s) + \omega_\circ L_f i_q(s)\right) \tag{B.19}$$

where, the converter output voltages in the '$dq$' reference frame, $v_d^{conv}(s)$ and $v_q^{conv}(s)$ acts as the input to the inner loop system. The disturbance inputs $v_d(s)$ and $v_q(s)$ along with the cross coupling terms like $\omega_\circ L_f i_d(s)$ and $\omega_\circ L_f i_q(s)$ is feed forwarded to reduce the output of the current controller. So the plant transfer function of the inner current loop becomes,

$$G_p^{CC}(s) = \frac{1}{R_f + sL_f} \tag{B.20}$$

### B.2.2 Plant Equations of Outer Voltage Loop

The variable load on the dc side is modeled as a current source $i_L$. Neglecting losses in the converter bridge and applying KCL at node $K$, we can write

$$C_{DC}\frac{\mathrm{d}v_{DC}}{\mathrm{d}t} + i_L = i_{DC} = \frac{p}{v_{DC}} \tag{B.21}$$

where, $p$ is the instantaneous active power drawn from the grid. Equation $B.21$ shows that the dc side of the AFEC acts as a non linear system. Hence to design the controller we need to linearize the system. We will do this by applying small signal perturbation and neglecting the higher order terms. So in the equation $B.21$ we will substitute the following quantities.

$$\begin{aligned} v_{DC} &= V_{DC} + \tilde{v_{DC}} \\ i_L &= I_L + \tilde{i_L} \\ p &= P + \tilde{p} \end{aligned}$$

where $V_{DC}$, $I_L$ and $P$ are the nominal values of the dc bus voltage, load current and active power drawn from the grid, while $\tilde{v_{DC}}$, $\tilde{i_L}$ and $\tilde{p}$ are the ripple quantities. Therefore we have,

$$C_{DC}\frac{\mathrm{d}\left(V_{DC} + \tilde{v_{DC}}\right)}{\mathrm{d}t} + I_L + \tilde{i_L} = \frac{P + \tilde{p}}{V_{DC} + \tilde{v_{dc}}}$$

$$\Rightarrow \left(V_{DC} + \tilde{v_{DC}}\right) C_{DC}\frac{\mathrm{d}\left(V_{DC} + \tilde{v_{DC}}\right)}{\mathrm{d}t} + \left(V_{DC} + \tilde{v_{DC}}\right)\left(I_L + \tilde{i_L}\right) = P + \tilde{p}$$

Neglecting the higher order terms we get,

$$V_{DC}C_{DC}\frac{\mathrm{d}\tilde{v_{DC}}}{\mathrm{d}t} + V_{DC}I_L + V_{DC}\tilde{i_L} + \tilde{v_{DC}}I_L = P + \tilde{p}$$

Separating the dc and the ac quantities, we can write

$$V_{DC}I_L = P \tag{B.22}$$

$$\Rightarrow I_L = \frac{P}{V_{DC}} = \frac{P_{rated}}{V_{DC}} = \frac{10000}{800} = 12.5 \text{ Amp}$$

and

$$V_{DC}C_{DC}\frac{\mathrm{d}\tilde{v_{DC}}}{\mathrm{d}t} + V_{DC}\tilde{i_L} + \tilde{v_{DC}}I_L = \tilde{p} \tag{B.23}$$

Applying Laplace Transformation to the above equation, we get

$$\tilde{v_{DC}}(s) = \frac{1}{I_L + sC_{DC}V_{DC}}\left[\tilde{p}(s) - V_{DC}\tilde{i_L}(s)\right]$$

Neglecting the ripple in the load current of dc side, the above equation can be simplified as,

$$\tilde{v_{DC}}(s) = \frac{\tilde{p}(s)}{I_L + sC_{DC}V_{DC}} \tag{B.24}$$

So the plant transfer function of the outer voltage loop becomes,

$$G_p^{VC}(s) = \frac{1}{I_L + sC_{DC}V_{DC}} \tag{B.25}$$

Now the active power drawn from the grid can be written as,

$$p = \frac{3}{2}\left(v_d i_d + v_q i_q\right) \tag{B.26}$$

Since $v_d$ is alligned with $V_{pk}$ by the SRF-PLL, we have $v_q = 0$. Therefore the equation $B.26$ can be re-written as,

$$p = \frac{3}{2}\left(V_{pk} i_d\right)$$

$$\Rightarrow i_d = \frac{2}{3}\frac{p}{V_{pk}} \tag{B.27}$$

### B.2.3 Design of PI Controller

We will use nested control structure, where in the inner loop the line current drawn by the converter will be controlled and in the outer loop the dc bus voltage will be controlled. The power reference will be given by the dc voltage controller and the inner loop will track the current corresponding to this power.

**Current Controller :**

Here the plant is a first order system with the transfer function,

$$G_p^{CC}(s) = \frac{1}{R_f + sL_f} = \frac{\frac{1}{R_f}}{1 + s\frac{L_f}{R_f}}$$

The PI controller used has the transfer function,

$$G_c^{CC}(s) = \frac{K_i^{CC}}{s}\left(1 + s\frac{K_p^{CC}}{K_i^{CC}}\right)$$

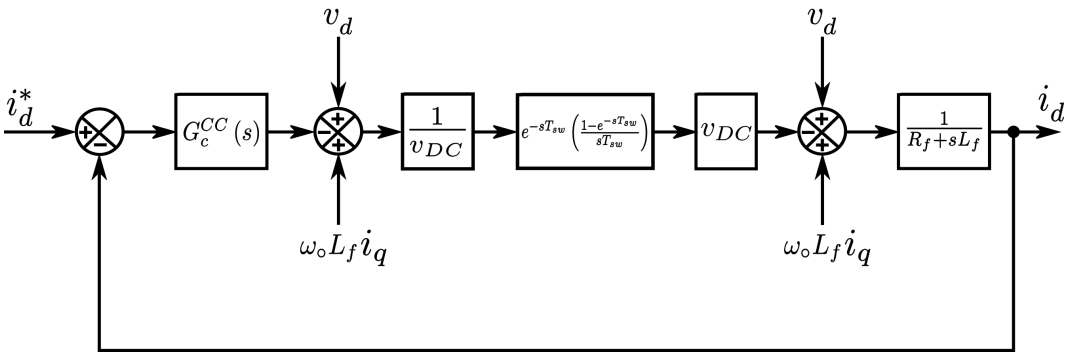


Figure B.5: Block Diagram of Inner $d$ Axis Current Loop

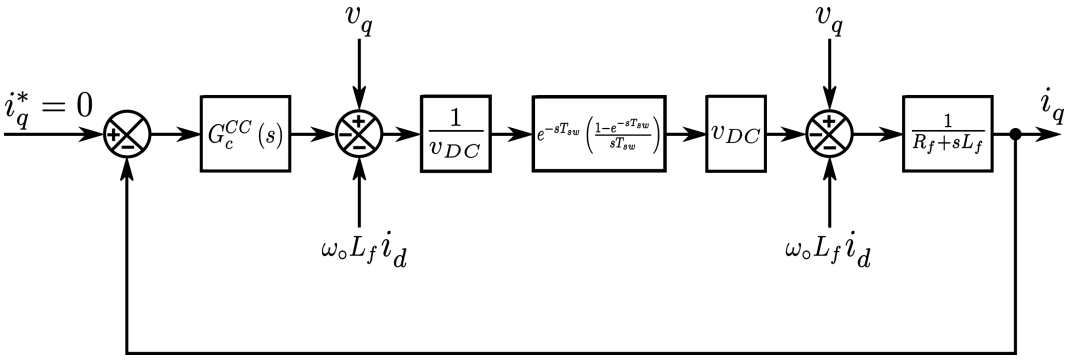


Figure B.6: Block Diagram of Inner $q$ Axis Current Loop

The controller design has been done by canceling the plant pole with the zero of the controller. So we have

$$\frac{K_p^{CC}}{K_i^{CC}} = \frac{L_f}{R_f}$$

The converter transfer function, $G_{conv}(s)$ can be modeled as $v_{DC}$ along with a delay of $e^{-sT_{sw}}$ due to duty update in the next switching cycle. The gain of the Pulse Width Modulation (PWM) modulator can be modeled by a ZOH whose transfer function is given by $\left\{\frac{1-e^{-sT_{sw}}}{sT_{sw}}\right\}$. Therefore using equation 5.3, the open loop transfer function of the inner current loop can be written as,

$$G_{oltf}^{CC}(s) = \frac{K_i^{CC}}{sR_f} \times \frac{1 - s\frac{3}{4}T_{sw}}{1 + s\frac{3}{4}T_{sw}}$$

With 100 kHz as the switching frequency of the converter, the gain cross-over frequency is chosen to be 10 kHz. Hence we can write,

$$K_i^{CC} = \omega_{gc} \times R_f = 2\pi \times 10 \times 10^3 \times 0.2 \approx 12566$$

$$\therefore K_p^{CC} = K_i^{cc} \times \frac{L_f}{R_f} = 12566 \times \frac{0.5 \times 10^{-3}}{0.2} = 31.415$$

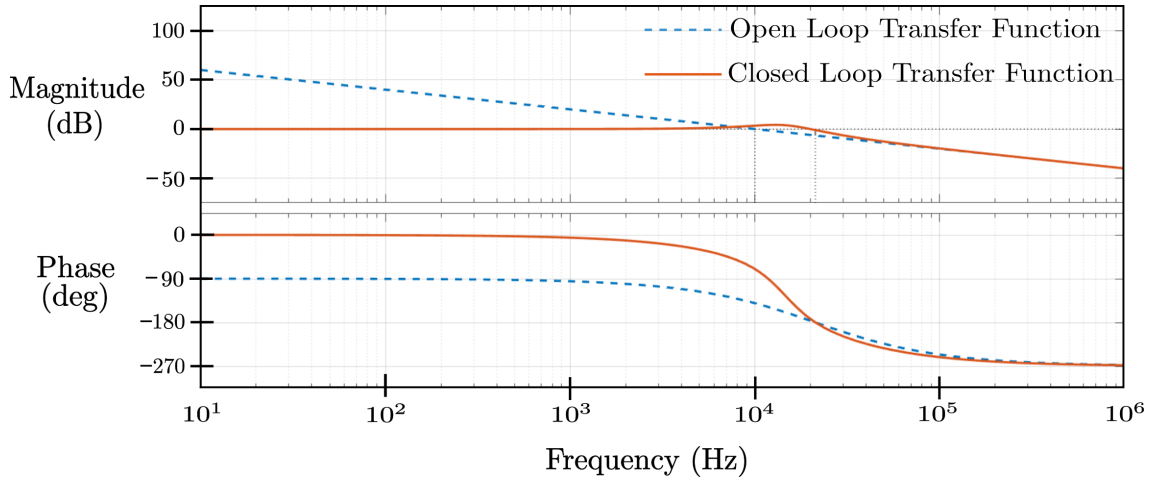


Figure B.7: Bode Diagram of the Inner Current Loop of the AFEC

**Voltage Controller :**

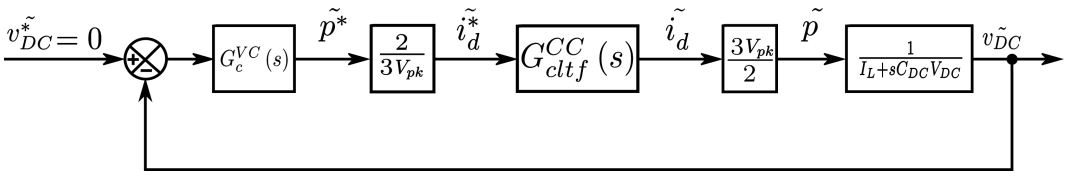


Figure B.8: Block Diagram of Outer Voltage Loop

Now for the outer voltage loop to work properly, it should be atleast ten times slower than the inner current loop. So we choose the gain cross-over frequency of the outer voltage loop transfer function to be 1 kHz. At this frequency the closed loop gain of the inner current loop ($G_{cltf}^{CC}$) can be taken as unity. Since the plant is a first order system, we choose a PI controller with the transfer function, $G_c^{VC}(s) = \frac{K_i^{VC}}{s}\left(1 + s\frac{K_p^{VC}}{K_i^{VC}}\right)$. Therefore the open loop transfer function of the outer voltage loop becomes,

$$G_{oltf}^{VC}(s) = \frac{K_i^{VC}}{s}\left(1 + s\frac{K_p^{VC}}{K_i^{VC}}\right) \times G_{cltf}^{CC}(s) \times \frac{\frac{1}{I_L}}{1 + s\frac{C_{DC}V_{DC}}{I_L}} \tag{B.28}$$

The controller design has been done by canceling the plant pole with the zero of the controller. So we have

$$\frac{K_p^{VC}}{K_i^{VC}} = \frac{C_{DC}V_{DC}}{I_L} = \frac{1.5 \times 10^{-3} \times 800}{12.5} = 0.096$$

Therefore,

$$\left|G_{oltf}^{VC}(s)\right|_{\omega=2\pi\times1000} = \frac{K_i^{VC}}{2\pi \times 1000 \times I_L} = 1$$

$$\Rightarrow K_i^{VC} = 2\pi \times 1000 \times 12.5 \approx 78540$$

and

$$K_p^{VC} = 0.096 \times 78540 \approx 7540$$

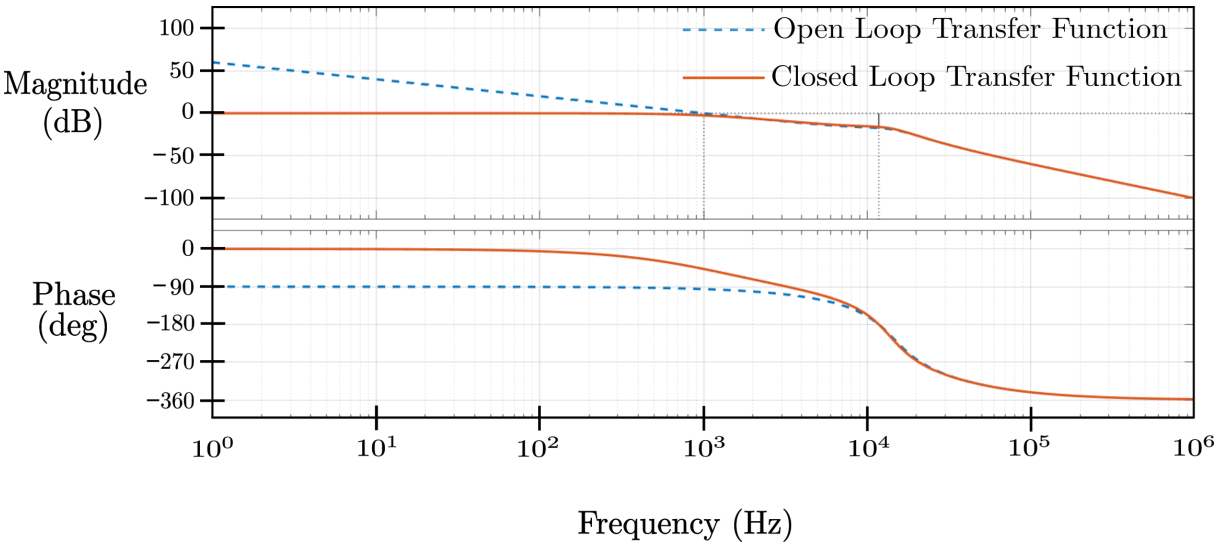


Figure B.9: Bode Diagram of the Outer Voltage Loop of the AFEC

Table B.2: Parameters of the Controller used in AFEC

| **Sl.No.** | **Parameter** | **Value** |
|---|---|---|
| 1 | Converter switching frequency, $F_{sw}$ | 100 kHz |
| 2 | DC bus voltage, $V_{DC}$ | 800 V |
| 3 | Active power rating, $P_{rated}$ | 10 kW |
| 4 | DC bus capacitance, $C_{DC}$ | 1.5 mF |
| 5 | Line filter inductance, $L_f$ | 0.5 mH |
| 6 | Line filter resistance, $R_f$ | 0.2 Ω |
| 7 | Gain cross-over frequency of inner current loop | 10 kHz |
| 8 | $K_p^{CC}$ | 31.415 |
| 9 | $K_i^{CC}$ | 12566 |
| 10 | Phase margin of inner current loop | 39.6° |
| 11 | Gain cross-over frequency of outer voltage loop | 1 kHz |
| 12 | $K_p^{VC}$ | 7540 |
| 13 | $K_i^{VC}$ | 78540 |
| 14 | Phase margin of outer voltage loop | 84.2° |

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# Appendix C

# Implementation of Observer based upon Method Of Characteristics

As mentioned in Subsection 2.1.2 of Chapter 2, there is another model known as Method of Characteristics (MoC), which can effectively capture the distributed nature of the transmission line. In this appendix we provide a quantitative comparison of the computational burden involved with Bergeron's Model and MoC for a processor based real-time implementation.

## C.1 Numerical Solution of a Long Transmission Line by Method Of Characteristics

The MOC converts the hyperbolic partial differential equations 2.3 and 2.6 of Chapter 2 into ordinary differential equations on the characteristic curves. In order to evaluate this curve, we use a Lagrange Multiplier ($\lambda$) and form an auxiliary equation as shown in $C.1$.

$$\left(Ri + L\frac{\partial i}{\partial t} + \frac{\partial v}{\partial x}\right) + \lambda\left(Gv + C\frac{\partial v}{\partial t} + \frac{\partial i}{\partial x}\right) = 0 \tag{C.1}$$

$$\Rightarrow \lambda C\left(\frac{\partial v}{\partial t} + \frac{1}{\lambda C}\frac{\partial v}{\partial x}\right) + L\left(\frac{\partial i}{\partial t} + \frac{\lambda}{L}\frac{\partial i}{\partial x}\right) + (Ri + \lambda Gv) = 0 \tag{C.2}$$

Equating $\frac{1}{\lambda C} = \frac{\lambda}{L} = \frac{\mathrm{d}x}{\mathrm{d}t}$, the partial differential equation $C.2$ gets converted into an ordinary differential equation given by $C.3$.

$$\lambda C\frac{\mathrm{d}v}{\mathrm{d}t} + L\frac{\mathrm{d}i}{\mathrm{d}t} + Ri + \lambda Gv = 0 \tag{C.3}$$

Solving for $\lambda$, we can write,

$$\lambda^2 = \frac{L}{C}$$

$$\Rightarrow \lambda = \pm\sqrt{\frac{L}{C}}$$

$$\text{Therefore, } \frac{\mathrm{d}x}{\mathrm{d}t} = \frac{\lambda}{L} = \pm\frac{1}{\sqrt{LC}} = \pm c_{TL} \tag{C.4}$$

As shown in Fig. $C.1$, $\frac{\mathrm{d}x}{\mathrm{d}t} = c_{TL}$ gives family of straight lines with positive slope, whereas, $\frac{\mathrm{d}x}{\mathrm{d}t} = -c_{TL}$ gives family of straight lines with negative slope. Substituting $\lambda = +\sqrt{\frac{L}{C}}$ in equation $C.3$, we get

$$\sqrt{LC}\frac{\mathrm{d}v}{\mathrm{d}t} + L\frac{\mathrm{d}i}{\mathrm{d}t} + Ri + \sqrt{\frac{L}{C}}Gv = 0 \tag{C.5}$$

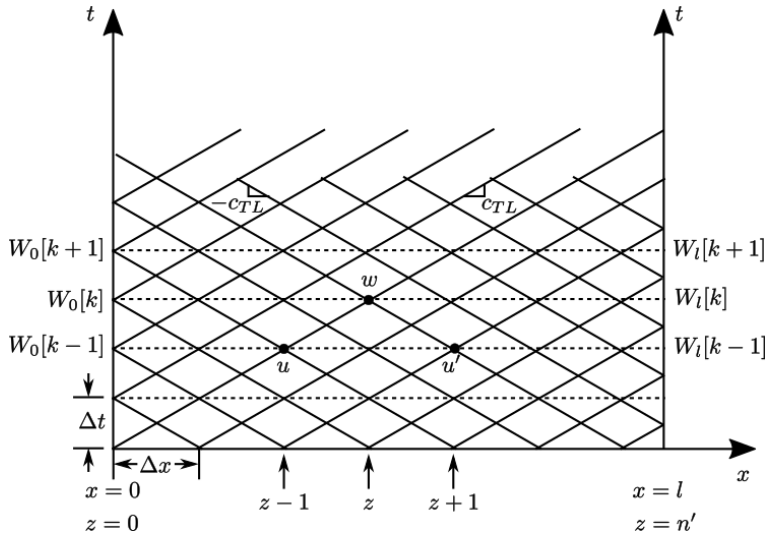


Figure C.1: Numerical Scheme for Method Of Characteristics

Integrating equation $C.5$ from point $u$ to $w$ along the positive characteristic line, we get

$$\sqrt{LC}\,(v_w - v_u) + L\,(i_w - i_u) + \frac{R}{2}\,(i_w + i_u)\,\Delta t + \frac{G}{2}\sqrt{\frac{L}{C}}\,(v_w + v_u)\,\Delta t = 0$$

$$\Rightarrow C_{19}v_w + C_{20}i_w = C_{21}v_u + C_{22}i_u$$

$$\Rightarrow C_{19}v\,(x,t) + C_{20}i\,(x,t) = C_{21}v\,(x - \Delta x, t - \Delta t) + C_{22}i\,(x - \Delta x, t - \Delta t) \tag{C.6}$$

where the constants $C_{19-22}$ are provided in Table-$C.1$. Similarly substituting $\lambda = -\sqrt{\frac{L}{C}}$ in equation $C.3$ and integrating from point $u'$ to $w$ along the negative characteristic line, we get

$$C_{19}v\,(x,t) - C_{20}i\,(x,t) = C_{21}v\,(x + \Delta x, t - \Delta t) - C_{22}i\,(x + \Delta x, t - \Delta t) \tag{C.7}$$

Solving for $v(x,t)$ and $i(x,t)$ from equations $C.6$ and $C.7$, we get

$$v(x,t) = \frac{C_{21}}{2C_{19}}\left\{v(x-\Delta x, t-\Delta t) + v(x+\Delta x, t-\Delta t)\right\} + \frac{C_{22}}{2C_{19}}\left\{i(x-\Delta x, t-\Delta t) - i(x+\Delta x, t-\Delta t)\right\} \quad \text{(C.8)}$$

and

$$i(x,t) = \frac{C_{21}}{2C_{19}}\left\{v(x-\Delta x, t-\Delta t) - v(x+\Delta x, t-\Delta t)\right\} + \frac{C_{22}}{2C_{19}}\left\{i(x-\Delta x, t-\Delta t) + i(x+\Delta x, t-\Delta t)\right\} \quad \text{(C.9)}$$

respectively. Shown in equations $C.10$ and $C.11$, $i(0,t)$ and $i(l,t)$ are evaluated by putting $x = 0$ and $x = l$ in equations $C.7$ and $C.6$ respectively .

$$i(0,t) = \frac{1}{C_{20}}\left\{C_{19}v(0,t) - C_{21}v(\Delta x, t-\Delta t) + C_{22}i(\Delta x, t-\Delta t)\right\} \quad \text{(C.10)}$$

$$i(l,t) = \frac{1}{C_{20}}\left\{-C_{19}v(l,t) + C_{21}v(l-\Delta x, t-\Delta t) + C_{22}i(l-\Delta x, t-\Delta t)\right\} \quad \text{(C.11)}$$

Table C.1: Constants for Observer based on MOC

| | | | |
|---|---|---|---|
| $C_{19} = \sqrt{LC} + \frac{G}{2}\sqrt{\frac{L}{C}}$ | $C_{24} = \frac{C_{22}}{2C_{19}}$ | $C_{29} = \frac{C_{22}}{C_{20}}$ | $C_{32} = -\frac{C_{28}}{K_3}$ |
| $C_{20} = L + \frac{R\Delta t}{2}$ | $C_{25} = \frac{C_{21}}{2C_{20}}$ | $K_3 = 1 + C_{27}\frac{L_g}{T_{ob}}$ | $C_{33} = \frac{C_{29}}{K_3}$ |
| $C_{21} = \sqrt{LC} - \frac{G}{2}\sqrt{\frac{L}{C}}$ | $C_{26} = \frac{C_{22}}{2C_{20}}$ | $K_4 = 1 + C_{27}\frac{L_{sh}}{T_{ob}}$ | $C_{34} = \frac{C_{27}\frac{L_{sh}}{T_{ob}}}{K_4}$ |
| $C_{22} = L - \frac{R\Delta t}{2}$ | $C_{27} = \frac{C_{19}}{C_{20}}$ | $C_{30} = \frac{C_{27}}{K_3}$ | $C_{35} = -\frac{C_{28}}{K_4}$ |
| $C_{23} = \frac{C_{21}}{2C_{19}}$ | $C_{28} = \frac{C_{21}}{C_{20}}$ | $C_{31} = \frac{C_{27}\frac{L_g}{T_{ob}}}{K_3}$ | $C_{36} = -\frac{C_{29}}{K_4}$ |

## C.2 Digital Implementation Of Observer based upon Method Of Characteristics on Embedded Platform

We discretize the continuous quantity $w \,\epsilon\, \{v, i\}$ in space and time as,

$$w(x,t) = w(z\Delta x, k\Delta t) = W_z[k] \text{ where, } W \,\epsilon\, \left\{v_{(J)}, i_{(J)}\right\} \quad \text{(C.12)}$$

In this particular case, $J \,\epsilon\, \{a, b, c\}$, $\Delta t = T_{ob}$, $\Delta x = c_{TL}T_{ob}$ and $z = 0, 1, 2, ...n'$ where, $l = n'\Delta x$. At every $k^{\text{th}}$ time step, to solve $W_z[k]$ at any internal point on the line,

the Observer solves equations $C.13$ and $C.14$ using the previous step information at two adjacent points $W_{z-1}[k-1]$ and $W_{z+1}[k-1]$.

$$\text{For } 1 \leq z \leq n' - 1,$$

$$v_{z(J)}[k] = C_{23}\left(v_{z-1(J)}[k-1] + v_{z+1(J)}[k-1]\right) + C_{24}\left(i_{z-1(J)}[k-1] - i_{z+1(J)}[k-1]\right) \tag{C.13}$$

$$i_{z(J)}[k] = C_{25}\left(v_{(z-1(J)}[k-1] - v_{z+1(J)}[k-1]\right) + C_{26}\left(i_{z-1(J)}[k-1] + i_{z+1(J)}[k-1]\right) \tag{C.14}$$

With the constants of Table-$C.1$, and denoting $i(0,t)$ and $i(l,t)$ as $i^{**}_{se}(t)$ and $-i^{**}_{re}(t)$ respectively, the equations $C.10$ and $C.11$ can be discretized as,

$$i^{**}_{se(J)}[k] = C_{27}v_{se(J)}[k] - C_{28}v_{1(J)}[k-1] + C_{29}i_{1(J)}[k-1] \tag{C.15}$$

and

$$i^{**}_{re(J)}[k] = C_{27}v_{re(J)}[k] - C_{28}v_{n'-1(J)}[k-1] - C_{29}i_{n'-1(J)}[k-1] \tag{C.16}$$

respectively. From equations 3.6 and 3.7 of Chapter 3, we can write,

$$v_{se(J)}[k] = v_{seg(J)}[k] - \frac{L_g}{T_{ob}}\left(i^{**}_{se(J)}[k] - i^{**}_{se(J)}[k-1]\right) \tag{C.17}$$

and

$$v_{re(J)}[k] = -\frac{L_{sh}}{T_{ob}}\left(i^{**}_{re(J)}[k] - i^{**}_{re(J)}[k-1]\right) \tag{C.18}$$

Substituting equations $C.17$ and $C.18$ in equations $C.15$ and $C.16$ respectively, the currents at the sending and receiving end of the line generated by the Observer can be written as,

$$i^{**}_{se(J)}[k] = C_{30}v_{seg(J)}[k] + C_{31}i^{**}_{se(J)}[k-1] + C_{32}v_{1(J)}[k-1] + C_{33}i_{1(J)}[k-1] \tag{C.19}$$

and

$$i^{**}_{re(J)}[k] = C_{34}i^{**}_{re(J)}[k-1] + C_{35}v_{n'-1(J)}[k-1] + C_{36}i_{n'-1(J)}[k-1] \tag{C.20}$$

To find out currents at the sending and receiving end of the line, equations $C.19$ and $C.20$ are solved using previous step data at one adjacent point and sampled value of the grid voltages. The solved $k^{\text{th}}$ step data are stored and used to solve the $(k+1)^{\text{th}}$ step in the next computation cycle and in this way the numerical scheme advances in real-time. The constants $C_{23-36}$ are defined in Table-$C.1$.

### C.2.1 Compuations to be done by the Observer in each Computational Cycle :

We consider that the $3\phi$ transmission line is balanced and transposed throughout its length. So we calculate the line end currents for two phases and the third one

is taken as the negative sum of the other two phases. This will slightly reduce the computational burden for real-time implementation. Two voltage and two current buffers of length $n'$ are used to store the present $\left(k^{\text{th}}\right)$ and past $\left((k-1)^{\text{th}}\right)$ values for each $a$ and $b$ phase. The instructions to be executed in every computational cycle are as follows :

i. Feed the latest sending end voltage of the $a$ and $b$ phase of the transmission line. $[2 \times n_{ls}]$

ii. Referring equation $C.19$, four multiplication and three addition are involved for calculating the sending end current for each $a$ and $b$ phase. $[8 \times n_{mul}\ ,\ 6 \times n_{add}]$

iii. Referring equation $C.20$, three multiplication and two addition are involved for calculating the receiving end current for each $a$ and $b$ phase. $[6 \times n_{mul}\ ,\ 4 \times n_{add}]$

iv. Referring equation $C.17$, one multiplication and two subtraction are involved for calculating the sending end line voltage for each $a$ and $b$ phase. $[2 \times n_{mul}\ ,\ 4 \times n_{sub}]$

v. Referring equation $C.18$, one multiplication and one subtraction are involved for calculating the receiving end line voltage for each $a$ and $b$ phase. $[2 \times n_{mul}\ ,\ 2 \times n_{sub}]$

vi. Referring equation $C.13$, two multiplication, two addition and one subtraction are involved for calculating the voltage at each of the $n'-1$ points for each $a$ and $b$ phase. $\left[4\left(n'-1\right) \times n_{mul}\ ,\ 4\left(n'-1\right) \times n_{add}\ ,\ 2\left(n'-1\right) \times n_{sub}\right]$

vii. Referring equation $C.14$, two multiplication, two addition and one subtraction are involved for calculating the current at each of the $n'-1$ points for each $a$ and $b$ phase. $\left[4\left(n'-1\right) \times n_{mul}\ ,\ 4\left(n'-1\right) \times n_{add}\ ,\ 2\left(n'-1\right) \times n_{sub}\right]$

viii. $n'+1$ number of moving operations in the voltage and current memory buffers of $a$ and $b$ phase, so that it can be recycled and used. $\left[4 \times \left(n'+1\right) \times n_{mov}\right]$

ix. Sending end current calculation for the $c$ phase. $[2 \times n_{sub}]$

The moving operation in the memory buffers is done by a counter , which needs to be incremented and compared with the reference value. Denoting the instruction clock period of the PS as $T_{clk(PS)}$ and referring Table-3.2 of Chapter 3, the total computational time required by the Observer ($T_{obc}$) can be written as,

$$\begin{aligned} T_{obc} = T_{clk(PS)}[&(2 \times n_{ls}) + (18 \times n_{mul}) + (10 \times n_{add}) + (6 \times n_{sub}) + (8n' \times n_{mul}) \\ &- (8 \times n_{mul}) + (8n' \times n_{add}) - (8 \times n_{add}) + (4n' \times n_{sub}) - (4 \times n_{sub}) \\ &+ \Big(\left(n'+1\right)\left(4 \times n_{mov} + n_{add} + n_{cmp}\right)\Big) + (2 \times n_{sub})] \end{aligned}$$

$$\Rightarrow T_{obc} = T_{clk(PS)}[(2\times 3)+(10\times 5)+(2\times 4)+(2\times 4)+(8n'\times 5) + (8n'\times 4)+(4n'\times 4)+(n'\left((4\times 2)+4+3\right))+((4\times 2)+4+3)+(2\times 4)]$$

$$\Rightarrow T_{obc} = T_{clk(PS)}\left[95+103n'\right]$$

For floating point operation in the selected Zynq PS, $T_{clk(PS)}$ is approximately 6 ns.

$$\therefore T_{obc} \approx \left(0.57+\frac{618}{1000}n'\right)\mu s \tag{C.21}$$

Since $n' = \frac{l}{\Delta x} = \frac{c_{TL}\tau}{\Delta x} = \frac{\tau}{T_{ob}}$, the equation $C.21$ can be further written as,

$$T_{obc} = \left(0.57+\frac{618}{1000}\frac{\tau}{T_{ob}}\right)\mu s \tag{C.22}$$

Whereas for Bergeron's Model the computation required was $\left(1.66+\frac{114}{1000}\frac{\tau}{T_{ob}}\right)\mu s$. For long lines with high $\tau$, the ratio of computational burden for both the models can be written as,

$$\frac{T_{obc(\text{MoC})}}{T_{obc(\text{Bergeron's Model})}} \approx \frac{618}{114} = 5.42 \tag{C.23}$$

Therefore as mentioned in Chapter 2, it is observed that with increase in the number of line sections, the computational burden enhances thereby putting an upper limit to the sampling frequency of the Observer.

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