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8 A, 200 V Normally-off Cascode GaN-on-Si HEMT: From Epitaxy to Double Pulse Testing

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Abstract—
In this paper, we provide a comprehensive study on all aspects of development of normally-off multi-finger III-nitride HEMT on Silicon in cascode configuration. AlGaN/GaN HEMT epi-stack with *in situ* SiN cap was grown on 2-inch Silicon (111) using MOCVD, utilizing a 2-step AlN nucleation, step-graded AlGaN transition layer and C-doped GaN buffer. Depletion-mode HEMTs in winding gate geometry with a gate width of 30 mm were fabricated with thick electroplated metal contacts and an optimized bilayer SiN passivation. Devices were diced and packaged in TO254 with conducting epoxy and Au-coated ceramic substrate. These packaged D-mode HEMTs exhibited a threshold voltage (V_{th}) of -12 V, maximum ON current of 10 A, and a 3-terminal hard breakdown in excess of 400 V. Bare dies of D-mode HEMTs were then integrated with commercially procured silicon MOSFET in a TO254 package in cascode configuration to achieve V_{th} > 2 V, ON current of 8 A, and breakdown > 200 V. The normally-off cascaded GaN HEMTs were subjected to various gate and drain stress measurements and were found to exhibit a V_{th} shift of 10 mV after 1000 seconds of positive gate (+5 V) stress. The input and output capacitances of the cascode devices were measured to be 1 nF and 0.8 nF, respectively. The 3rd quadrant operation was checked at 8 A on-state current level to reveal a lower voltage drop of 0.7V. Finally, cascode HEMTs were subjected to double pulsed testing (DPT) using a half-bridge evaluation board. On and off rise times of 52 ns and 59 ns were obtained along with energy loss of 25 µJ and 20 µJ, respectively, for devices switched at 8 A, 100 V.

Index Terms—AlGaN/GaN on Silicon, large periphery device fabrication, cascoded -normally-off HEMT, double pulse switching

I. INTRODUCTION

Gallium Nitride-High Electron Mobility Transistors (HEMT), owing to their superior ON current, faster-switching capability, and higher breakdown voltages, are preferred over conventional silicon-based power FETs for applications such as ultrafast chargers in mobile phones and laptops, On-board chargers in electric vehicles(EV's) [1]. Normally-off AlGaN/GaN HEMTs on a silicon substrate, either in cascode configuration or using p-GaN, are fast penetrating the 200-650 V power electronics market [2][3]. The advantage of cascode devices over p-GaN e-mode HEMTs is the lower cut-off voltage at third quadrant operation, which reduces the reverse recovery charge and allows for a +/- 20 V positive gate swing [4]. Although cascode GaN HEMTs with ratings up to 60 A and 1200 V are now commercially available, indicating their maturity, most of the know-how of device process and materials growth is proprietary and rests with the respective industry players and are not often published. Only reliability studies or systems development [5] [6] using such commercially available GaN HEMTs are reported in the literature, either by the industry or by academic groups. Multi-finger GaN HEMTs are extremely difficult to realize in any academic cleanroom. This is why it is rare to find any published paper with fabrication details and device analysis from academic groups on GaN devices with higher current ratings [7]–[10]. As far as processing and device analysis is concerned, almost all GaN HEMT papers to date, excluding a few from industry [11][12], are on small gate periphery (100-200 µm) devices. Thus, there is a need to present and discuss all aspects of developing high-power carrying GaN HEMTs, including epi-growth, device design and associated process challenges, characterization, packaging, and testing of switching performance. This work seeks to fill this vacuum in literature. We have fabricated depletion mode (D-mode) HEMTs with 30 mm gate width on Metal Organic Chemical Vapour Deposition (MOCVD)-grown GaN HEMT epi-stack, which exhibits 10 A of ON current with off-state breakdown exceeding 400 V. These devices were diced, packaged and integrated with bought-out Silicon MOSFET to realize normally-off operation. Cascoded GaN HEMTs are then characterized for stress measurements, capacitance and finally put in a half-bridge board to evaluate the performance when switched at 8 A, 100 V.

II. MATERIAL AND DEVICE FABRICATION

A. Material growth

The HEMT epi-stack was grown on a 2" Si (111) substrate using MOCVD. The details of the growth have been published earlier[13], wherein a two-step AlN layer is first deposited on the Si substrate to reduce threading dislocation density and to achieve a smooth growth front for subsequent layer deposition. Then, three AlGaN layers were deposited in sequence with a

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gradual increase in GaN-fraction: $Al_{0.75}Ga_{0.25}N$, $Al_{0.50}Ga_{0.50}N$, and $Al_{0.25}Ga_{0.75}N$, with thicknesses of 250 nm, 250 nm, and 500 nm, respectively. A C-doped GaN buffer layer (500 nm) and nominally undoped GaN channel layer (150 nm) were then grown on the AlGaN buffer stack. An AlN spacer layer (1 nm), $Al_{0.25}Ga_{0.75}N$ barrier layer (25 nm), and in-situ Si_3N_x cap layer (3 nm) were then deposited sequentially to achieve a stable 2DEG at the top of the GaN channel layer. Except for the cap layer at the top of the stack, it is similar to the reference stack used by Remesh et al.[14]. The surface morphology of the stack was investigated using Atomic Force Microscopy (AFM), revealing an RMS roughness of 0.4 nm over a surface area of 5 microns x 5 microns, as illustrated in Fig. 1 (a). Rigaku Smartlab high-resolution X-ray diffractometer was used for obtaining the symmetric (002) and asymmetric (102) rocking curves with FWHMs of 0.22 deg. and 0.36 deg., respectively, for the GaN layer, as shown in Fig. 1(b). Fig.2 (a) shows an image of the 2-inch MOCVD-grown GaN on a Silicon wafer.

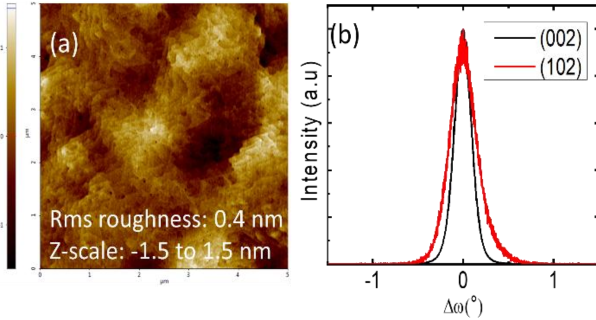

Fig.1. (a)AFM image of in-situ SiN_x, (b) XRD- ω scan for GaN grown on Silicon.

B. Device fabrication:

HEMTs under study were designed with a meandering gate geometry for medium-voltage applications. Ohmic contacts were formed by an e-beam evaporating a Ti/Al/Ni/Au metal stack (20/120/30/50 nm) which was annealed at 850^0 C in an N_2 atmosphere for 45 sec. A BCl_3/Cl_2-based dry etch chemistry using a reactive ion etch (RIE) chamber was used to define mesa isolation of HEMTs. The mesa etch depth was 400 nm so that subsequent gate pad and metal bus bars would 'sit' on the high resistive C-doped GaN buffer. An optimized bilayer SiN_x was then used for acting as a gate dielectric and passivation layer [15]. First, SiN_x (20 nm) was deposited using plasma-enhanced chemical vapour deposition (PECVD) under high-frequency (HF-13.56 MHz) conditions as gate dielectric and annealed at 700^0C in an N_2 ambient for 10 minutes. This was followed by e-beam evaporation of Schottky gate metal stack (Ni/Au- 30/100 nm). Next, the active area was passivated with PECVD SiN_x of thickness 150 nm, which was deposited using a combination of HF,13.5 MHz and low frequency (LF, 300 kHz) conditions. Gate-connected field plates (Ni/Au, 30/100 nm) were implemented to improve field management at the gate edge. The field plate had a 1 µm extension from the gate edge toward the drain. Post field plate, the devices were passivated by PECVD SiN_x (200 nm) deposited with a low-frequency recipe at 300^0C. The SiN_x was selectively removed to expose source-drain fingers and gate pad. Next, 2 µm thick Au was electroplated to thicken the Ohmic contact fingers and bond pads.

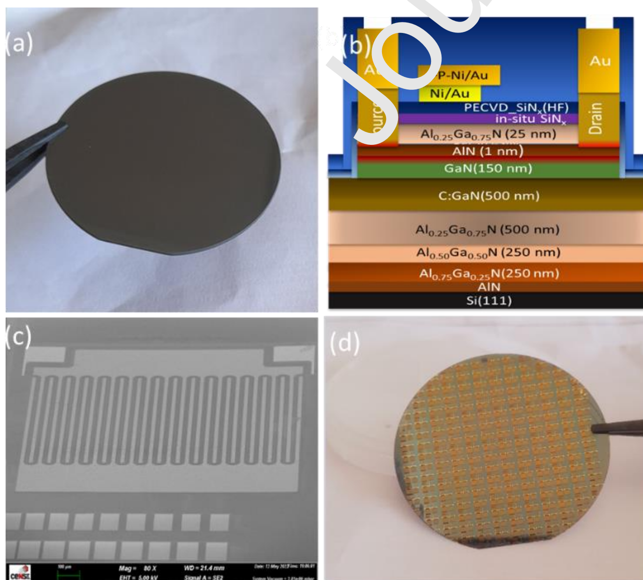

Fig.2. (a) MOCVD-grown HEMT stack on GaN, (b) schematic of a processed device, (c) SEM image of a fabricated device and (d) fabricated 2-inch wafer

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The metal resistance of electroplated Au was measured and was found to be negligible. Finally, PECVD-SiN_x of 100 nm thickness was blanket deposited to protect the active device area from particles produced during the dicing of the wafer. Bond pads were opened using selective dry etching of the last layer of SiN_x to enable wire bonding. A device schematic, an SEM image of a representative HEMT and an image of the 2-inch wafer post-processing are shown in Fig. 2 (b), (c) and (d), respectively. The fabricated device has source-to-gate spacing L_{SG} =6 µm, gate length L_G=3 µm and gate-to-drain spacing L_{GD}= 12 µm, respectively.

C. Design parameters for cascoded GaN HEMT

The primary concern in choosing a Si-MOSFET is ensuring that its breakdown voltage exceeds the threshold voltage (V_{th}) of the D-mode HEMT but is less than its gate voltage rating. One method to achieve this is using a cascode mode with a Si-MOSFET, which allows for low R_{on}, positive V_{th}, high breakdown voltage, and low reverse recovery loss. In our process, the Si-MOSFET had R_{on} =30 mΩ, V_{th} = +1.8V, V_{DS}=30 V (I_D=250 µA), V_{GS}=20 V (at I_{GS}=100 nA), reverse capacitance ($C_{rss} = C_{gd}$) =100 pF, input capacitance (C_{iss}=$C_{gd+}C_{gs}$) = 860 pF, and output capacitance (C_{oss}=$C_{ds+}C_{gs}$) = 120 pF (capacitance measured at 15 V with 1 MHz).

D. TO254 packaging D-Mode and cascoded GaN HEMT

D-mode HEMTs were diced and then packaged in a three-lead pin TO-254 package. The insulation leak test was measured up to 1 kV, and the bare package was able to withstand 1 kV with 900 MΩ resistance. First, HEMTs were soldered on gold-coated ceramic substrates using NAMICS epoxy: the ceramic substrate was then soldered to the body of the package, once again using NAMICS epoxy, which was then used to connect to the drain lead of the package. The devices were wire-bonded using 1 ml Au wires with the ball bonding method: while the gate and source were wire-bonded to the respective leads of the package, the drain pad was wire bonded to the Au-coated ceramic substrate as shown in Fig. 3 (a). The first bond is on the device, and the second is on the package leads. The lead configuration is Gate, Drain, and Source, respectively. For normally-off cascode operation, bare dies of D-mode HEMTs are cascode-connected with commercially available Silicon MOSFET wafer dies in the TO254 package, where Au wire bonding is used to connect the devices (Fig. 3 (b)).

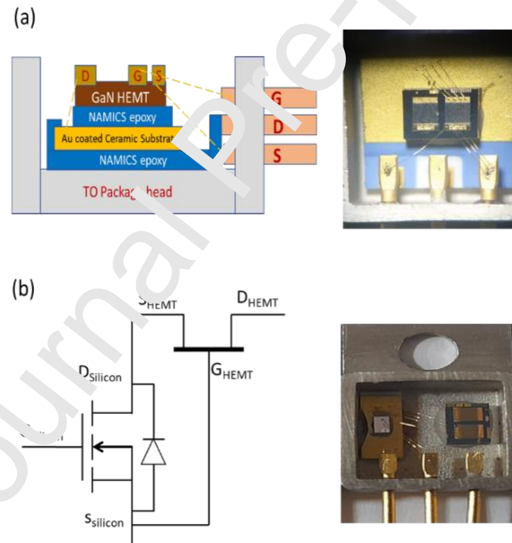

Fig.3. (a) Schematic and photograph of TO254-packaged D-MODE device (b) Circuit diagram of a cascode device and a photograph of the same realized in this work in the TO254 package

The drain of the MOSFET is located on the bottom of the device, and the source and gate are on the top sides. To connect the drain of the MOSFET and the source of the HEMT, a silicon MOSFET is placed on a gold-coated ceramic, and the source of the HEMT is connected from the gold plate. The HEMT is then attached to the substrate with thermal epoxy (Able Stik-8700K). The lead configuration on the cascode device is a gate, source, and drain. The drain of the HEMT is connected to the body of the TO-254 package using a wire bond. The G-S-D lead configuration reduces the Miller effect in the transistor performance.

E. Cascode-HEMT Double Pulse Testing (DPT)

A double pulse test (DPT) experiment is conducted to capture the switching dynamics of the fabricated cascode GaN device for different operating conditions. Fig. 4 (a) represents the circuit schematic of the DPT. Q1 and Q2 are cascode GaN devices connected in a half-bridge configuration. V_{DS} is the applied DC voltage. L represents the inductive output load connected across Q1. Two pulses of different widths are applied to Q2 (see Fig. 4 b). Initially, current through the inductor (i_L) is zero. Q2 is gated for a time duration of T1 to build the current through L to the required current level. I_0 $(= V_{DS}T_1/L)$. At time $t = T1$, Q2 is gated off, and the inductor current I_0 commutates from Q2 to Q1. This is termed as a hard turn-off transition of Q2. After the transition, it freewheels through the reverse channel of Q1. At t=(T1+T2), Q2 is gated again and i_L transfers from the reverse channel of Q1 to the forward channel of Q2. This is termed a hard turn-on transition. Finally, Q2 is turned off after a small-time interval T3.

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Using DPT, hard turn-on and off transitions can be captured for the operating conditions V_{DS}, Io.

The gate and source terminals of the Q1 are shorted externally (Fig. 4 a). Consequently, the low voltage Si MOSFET of Q1 is in the off state. When a positive drain-to-source voltage is applied across Q1, the gate-source voltage of the D-mode device becomes negative. Thus, the D-mode GaN device is in the cut-off region. Note: the gate-source voltage of the D-mode device is the same as the source-drain voltage of the Si MOSFET. However, when current flows from the source to the drain of Q1, the body diode of Si MOSFET conducts, and a small positive voltage appears across the gate source of the D-mode device (equal to the voltage drop across the antiparallel diode of the Si MOSFET). So, the channel of the D-mode device is on and offers a low-impedance path for the current to freewheel.

The image of the experimental set-up is given in Fig. 5. The DPT set-up is designed for 150 V DC bus voltage and 20 A load current. An air core inductor with 150 µH is used as the inductive load. Isolated gate driver 1EDB8275F from Infineon is used to drive the devices. The gate voltage levels are 15V and 0V, respectively. A 10 Ω is used as both turn on and off gate resistances. An oscilloscope, voltage and current probes are used to measure these signals correctly. Oscilloscope MDO3104 from Tektronix with 1 GHz bandwidth is used. Passive probe TPP1000 of 1GHz bandwidth (from Tektronix) is used for drain-source voltage measurement. Coaxial current shunt SSDN-10 from T&M research is used to measure device current. Matching propagation delay between voltage and current signals is done using a matching delay instrument from Tektronix (067-1686-00, Power Measurement De-skew and Calibration Fixture).

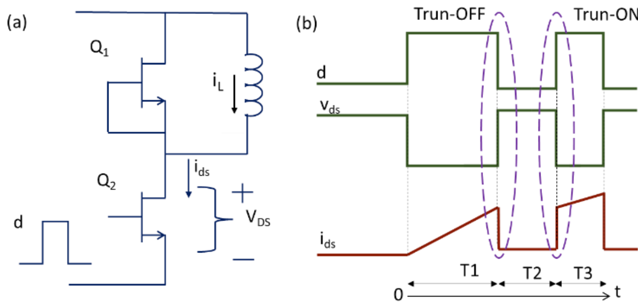

Fig. 4. (a) Schematic circuit and (b) pulse timing diagram of DPT evaluation board

Fig. 5. Half bridge evaluation DPT board with fabricated HEMT

III. RESULTS AND DISCUSSION

A. Characterization of D-mode device

First, D-mode HEMTs with 100 µm gate width were measured using an Agilent B1500A set-up to understand the basic characteristics of the fabricated devices. Fig. 6 (a&b) shows the static characteristics of the same: gate leakage was found to be 300 nA/mm at -20 V with $V_D = V_S$ grounded, while I_D-V_G revealed a V_{th} ~ -16 V with an On/Off ratio close to 10^7. The ON current was measured to be about 670 mA/mm at 0 V gate bias, while R_{on} was found to be 9.8 Ω.mm. It is noteworthy that there was no observable difference in the performance of 100 µm gate-width HEMTs with and without field plates as far as gate leakage and ON current were concerned.

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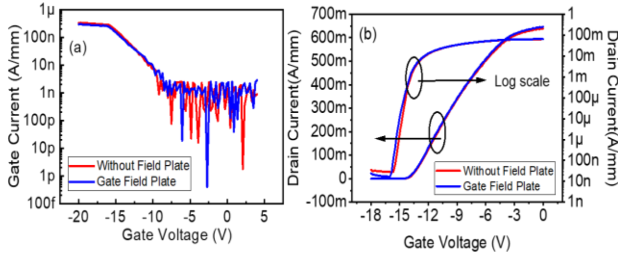

Fig.6. comparison of 100 µm (a) gate leakage(b) $I_D V_G$

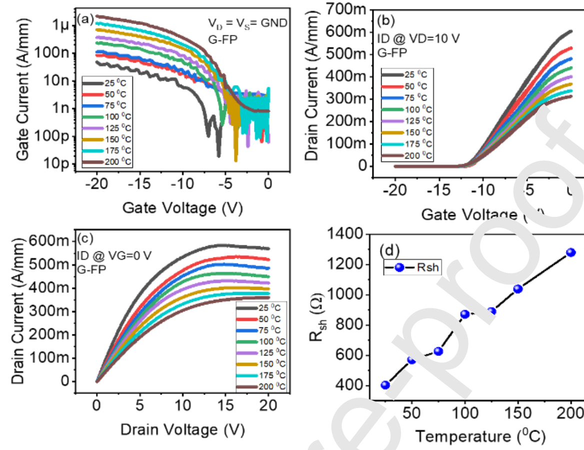

Fig.7. Temperature-dependent $I_G V_G$, $I_D V_G$, $I_D V_D$ and sheet resistance of 100 µm device and van der Pau structure.

Further, we performed temperature-dependent *I-V* characteristics for devices with 100 µm gate width, as shown in Fig. 7. The gate leakage was found to increase from 100 nA/mm to 5 µA/mm at -20 V bias while going from room temperature to 200°C (Fig.7 (a)); similar increase in gate leakage with temperature had been reported [16]. The ON current was found to drop by nearly ½ from 600 mA/mm to 300 mA/mm at 0 V on the gate for the same range of temperature (Fig. 7(b)). From the output characteristics (Fig. 7(c)), the ON resistance was found to increase from 11.28 Ω.mm to 24.15 Ω.mm with increase in temperature which correlates well with the 3x increase in the sheet resistance measured as a function of temperature, as shown in Fig. 7(d).

The packaged devices with 30 mm gate width were measured using an Agilent 1505A semiconductor analyzer. Fig. 8 (a) shows the transfer characteristics of a device with different drain biases and the corresponding Fig. 8 (b) gate leakage. The measurements were done in pulsed mode with a pulse period of 350 µs and a width of 480 µs. The device had less than 1 mA gate leakage at V_D= 10 V. With a drain voltage of 15 V, the devices exhibited an ON current of 10 A (Fig.8.c) with a R_{on} 776 mΩ at 5A. The 30 mm gate width devices should have exhibited 18 A considering that 600 mA/mm was measured for 100 µm gate width HEMT. The reduction of the 30 mm gate width device current is perhaps due to the increase in junction temperature. It can be seen from Fig.7.c that as the temperature increases, the current drops considerably. The correlation between the substrate temperature and junction temperature was reported [17]. In the present packaging scheme, there are several interfaces which could result in 190 ◦C/W to 310 ◦C/W thermal resistance leading to poor thermal dissipation[18]. The three-terminal breakdown of the devices was measured at V_G=-18 V. At 430 V, a sharp increase in the drain current of 3 mA and a gate current of 1.2 mA was observed (Fig. 8 (b)).

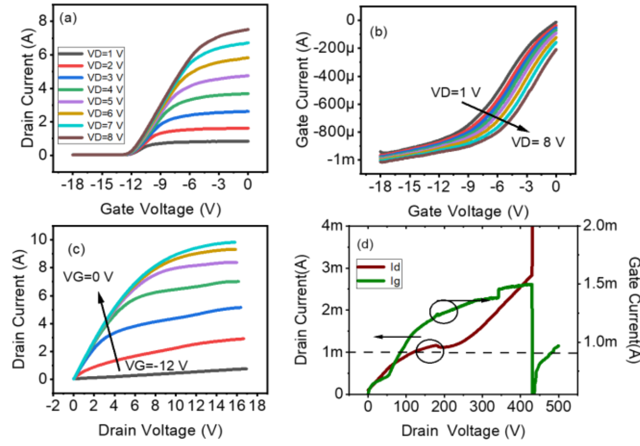

Fig.8. I-V characteristics of 30 mm gate width D-mode device; (a) transfer characteristics, (b) corresponding gate leakage, (c) output characteristics, (d) and breakdown voltage.

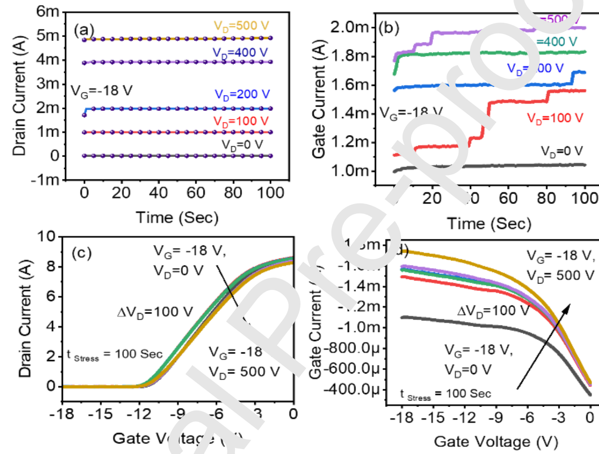

Fig.9. (a) Drain and (b) gate leakage with different stress voltage and time. (c) transfer characteristics with different drain voltage stress, (d) corresponding gate leakage

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Time-voltage-dependent stress measurements were performed on these devices. The devices were stressed at different off-state conditions for 100 seconds and then measured after each set of conditions. The off-state condition was V_G= -18 V, and V_D was varied from 0 V to 500 V in steps of 100 V. The stress-induced degradation of the drain and gate current were monitored for 100 sec (Fig. 9 (a & b)). Although the off-state drain leakage increased from 1mA to 5mA with 100V -500V drain voltage stress, there was no significant change with time. That indicated the drain did not see field-dependent degradation, and leakage was stable. However, as shown in Fig. 9 (b), an increase of 1mA to 2mA leakage current was observed in the gate with time, indicating that the gate eventually experienced degradation under off-state stress. Fig. 9 (c) & (d) show the I_D-V_G measured and gate leakage, respectively, after each stress condition. Transfer characteristics exhibited negligible change with the off-state stress.

B. Cascode Si-MOSFET with GaN D-HEMT

The fabricated D-mode HEMT was connected in a cascode with a Si-MOSFET. The source and drain of the Si-MOSFET were connected to the gate and the drain of the HEMT, respectively, as shown in Fig.3 (b). The three terminals of the package are the gate of the MOSFET, the source of the MOSFET, and the drain of the D-mode GaN HEMT. Fig.10 (a) shows that the floating gate leakage is less than 30 nA for +/-30 V gate sweep, which is better than many commercial cascode devices as quoted in their datasheets [19][20]. This holds promise for these fabricated devices to be useful as +12 V silicon-based gate drivers. The transfer and output characteristics and the breakdown voltage of the devices are shown in Fig. 10 (b), (c), and (d), respectively. The device exhibits an 8 A current in the saturation region, which is limited by R_{on} (776 mΩ) of the GaN HEMT. The buffer blocks more than 250 V with V_G=0 V in these devices.

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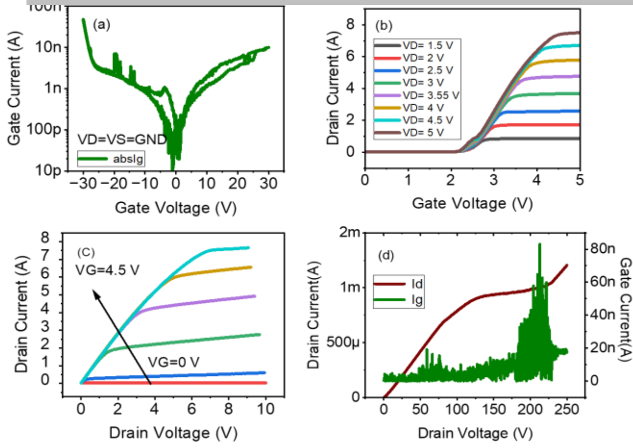

Fig.10. *I-V* characteristics of 30 mm gate width cascode connected device: (a) gate leakage, (b) transfer characteristics, (c) output characteristics and (d) breakdown voltage

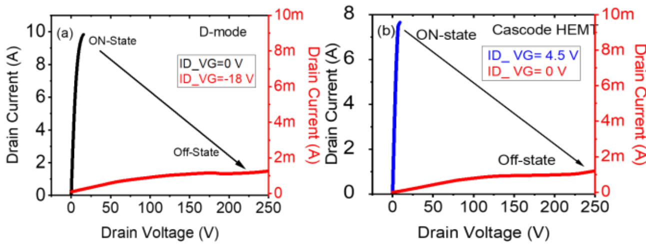

Fig.11. (a) D-mode HEMT and (b) cascode HEMT on/off drain current comparison

Fig. 11 (a) and (b) show the on/off performance of the D-mode HEMT and the cascode device, respectively. The buffer leakage at 250 V is about 1 mA, which can be reduced with an optimized buffer design. The cascode device is then subjected to a V_{th} reliability study: V_G= +5V and V_D = 0.1V were applied for 1000 sec. The I_D-V_G characteristic was measured at V_D=0.1 V at particular intervals (Fig. 12 (a)). The positive gate voltage stress induced a hole injection to the Si-MOSFET in the cascode device [21]. The V_{th} shift was observed to be minimal, as shown in Fig. 12 (b). It is to be noted that we have defined V_{th} at I_D = 0.1 mA.

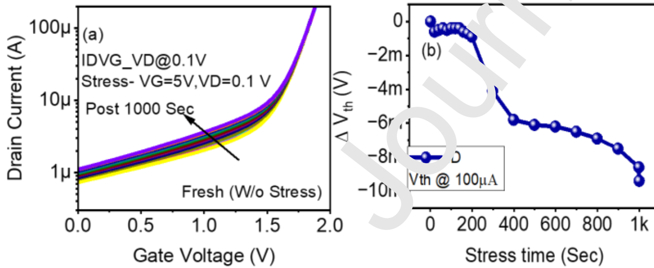

Fig.12. casocode GanHEMT (a) $I_D V_D$ plot for a different time with the stress of V_G=5V and V_D=0.1V different stress time (b) corresponding threshold voltage shift

Third-quadrant operation of the device is important when used in voltage source-based power electronic converter applications. Cascode GaN devices exhibit a lower voltage drop of 0.7 V @ V_G=0 V compared to similarly rated enchancement mode (E-mode) GaN devices (Fig. 13). Drop across the device remains almost unaffected by the change in negative gate-source voltage. This is unlike the case for E-mode GaN devices, where the drop increases with negative gate-source bias [21]. This will reduce the loss of the device during the dead time.

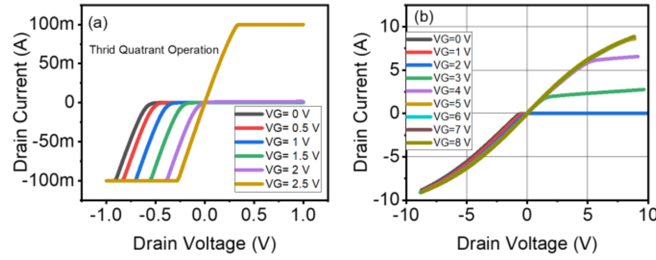

Fig.13. (a) third quadrant operation of the cascode device (a) with a small current level and (b) with higher current levels

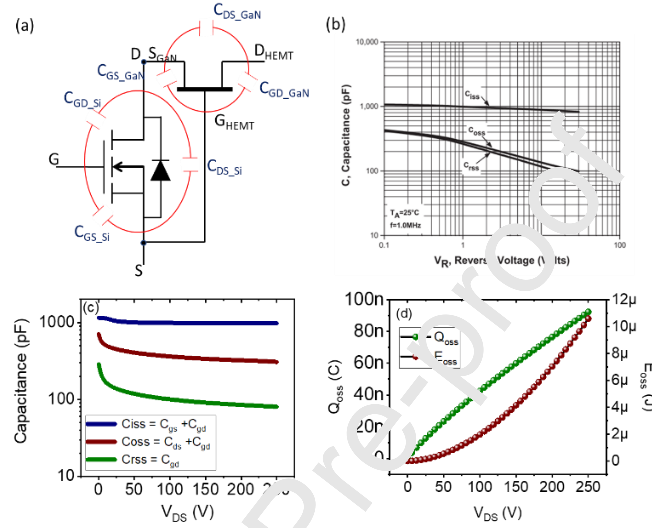

Fig.14. (a) the capacitance of the commercial Silicon MOSFET from the datasheet, (b) the measured capacitance of the cascaded GaN HEMT, (c) intrinsic capacitances and (d) Q_{oss}-V_{DS}

The overall schematic of the cascode GaN device, along with its intrinsic parasitic capacitances, is given in Fig. 14 (a). C_{gs}, C_{gd} and C_{ds} represent gate-source, gate-drain and drain-source capacitances, respectively. GaN and Si are used to differentiate between the capacitances of D-mode GaN devices and low-voltage Si MOSFET. Externally, terminals g, d and s are available, directly connected to the gate of Si MOSFET, D-mode GaN device drain and Si MOSFET source, respectively. The intrinsic capacitances of the commercial MOSFET (Fig. 14.b) and the cascode-connected GaN device were measured as a function of V_{DS} in the range of zero to 250 V (Fig.14 (c). The gate voltage V_G is kept at 0 V, and the measurement frequency is 1 MHz. C_{iss}, C_{rss} and C_{oss} are the input, reverse transfer and output capacitances of the overall cascode device. C_{iss} has measured at around 1000 pF and remains almost constant with V_{DS}. It is to be noted that the value of C_{iss} for the fabricated cascode device is mostly contributed by the C_{iss} of the low voltage Si MOSFET (C_{iss}_Si).

On the other hand, both C_{rss} and C_{oss} are monotonically decreasing functions of V_{DS}. C_{rss} and C_{oss} vary in the range of 300-100pF and 900-500pF, respectively, for V_{DS} in the range of zero to 250 V. It is noteworthy that C_{rss} of the cascode device is the series combination of output capacitance of D-mode GaN device (C_{oss}_GaN) and reverse transfer capacitance of the Si MOSFET (C_{rss}_Si). The C_{oss} of the cascode device is the series combination of C_{oss}_GaN and C_{oss}_Si (the Si MOSFET output capacitance). The equivalent charge (Q_{oss}) and energy stored in the C_{oss} (E_{oss}) were plotted as a function of vds in Fig. 14 (d), and the values are calculated to be Q_{oss}= 90 nC and E_{oss} = 11 µJ for V_{DS}=250 V.

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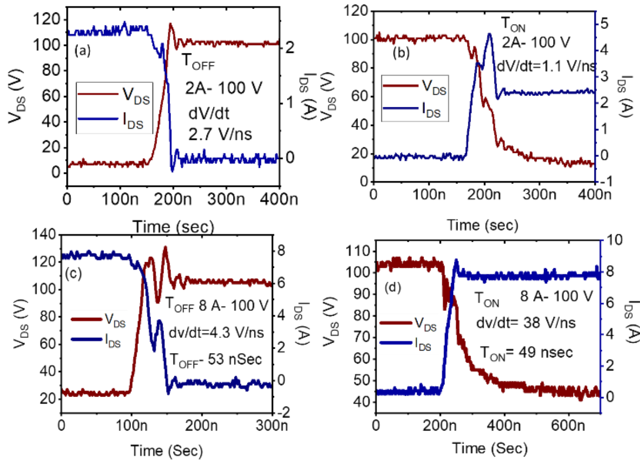

Fig.15. double pulse switching waveforms at V_{DS} 100 V-2A (a) turn-off, (b) turn-on and V_{DS} 100V-8A (c) turn-off, (d) turn-on.

To capture the switching transient waveforms of the fabricated cascode device for different operating conditions, DPT was performed for different values of V_{DS} and Io. V_{DS} =20V, 30V, 50V and 100V are used with Io=1A, 2A, 6A and 8A. This makes 16 different operating conditions. In Fig. 15 (a) to (d), experimentally obtained turn-on and off waveforms (v_{ds} & i_d) are plotted for V_{DS} =100V and Io=2A, 8A. Smooth transitions of v_{ds} and i_d with minimal high-frequency oscillations are observed for all the operating conditions.

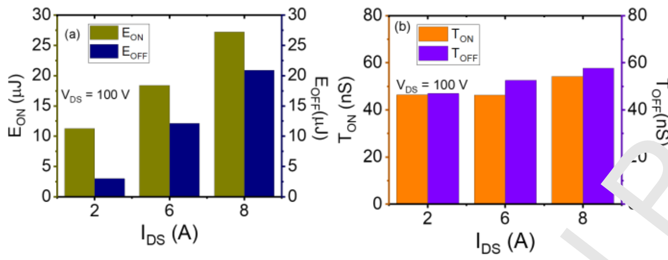

Fig.16. Energy loss comparison at (a) V_{DS} =100V and I_{DS} =2A, 6,8 A. Comparison of switching time at (b) V_{DS} =100V and I_{DS} =2,6,8 A.

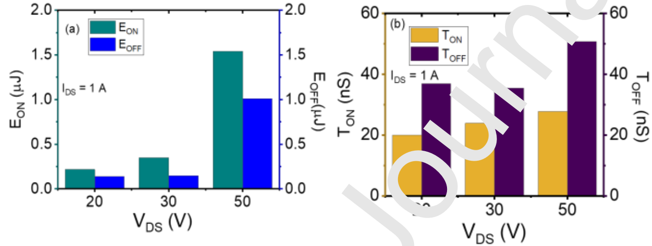

Fig.17. Energy loss comparison at (a) I_{DS} =1 A and V_{DS} =20 V, 30V,50 V. Comparison of switching time at (b) I_{DS} =1 A and V_{DS} =20 V, 30V,50 V.

After obtaining the switching transient waveforms experimentally, turn-on and off loss (E_{on} and E_{off}, respectively) are plotted in Fig. 16 (a) for V_{DS} =100 and Io=2A, 6A and 8A. It can be observed that E_{on} is increased from 11 µJ to 27 µJ for 2A to 8A Io, respectively. And corresponding E_{off} was calculated as 0.25 µJ to 20 µJ. Also, the difference between E_{on} and E_{off} are noticeable in low Io (for example, Io=1A). Similarly, turn-on and off transition times (T_{on} and T_{off}, respectively) are plotted in Fig. 16(b) for the same operating conditions. It can be observed that both T_{on} and T_{off} are similar for a given operating condition (V_{DS} and Io value) and increases slightly as Io increases for a given V_{DS}. To understand the variation of E_{on} and E_{off} with respect to V_{DS}, both of these quantities are plotted as a function of V_{DS} in the range 20V to 50V and Io=1A. It can be observed that both E_{on} and E_{off} increase with V_{DS} (Fig.17 (a)). Similarly, T_{on} and T_{off} are plotted for the same operating conditions (Fig.17 (b)). Similar to E_{on} and E_{off}, both T_{on} and T_{off} also increase with V_{DS}. Also, T_{off} is observed to be large compared to T_{on} for low V_{DS} values.

CONCLUSION

This work is a comprehensive study on developing normally-off multi-finger III-nitride HEMT on Silicon in cascode configuration. The resulting D-mode HEMTs had a gate width of 30 mm, thick electroplated metal contacts, and an optimized bilayer SiN_x passivation. These devices were diced and packaged in TO254 with conducting epoxy and Au-coated ceramic substrate. The fabricated D-mode HEMTs had a threshold voltage (V_{th}) of -12 V, a maximum ON current of 10 A, and a 3-terminal hard breakdown in excess of 400 V. We then integrated the bare dies of D-mode HEMTs with commercially procured silicon

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MOSFET in a TO254 package in cascode configuration. Thus, the cascoded GaN HEMTs obtained had a $V_{th} > 2$ V, an ON current of 8 A, and a breakdown of > 200 V. The normally-off cascaded GaN HEMTs were subjected to various gate and drain stress measurements, and they exhibited a V_{th} shift of 10 mV after 1000 seconds of positive gate (+5 V) stress. The input and output capacitances of the cascode devices were measured to be 1 nF and 0.8 nF, respectively. We also tested the 3rd quadrant operation of the cascode devices at 100 mA and 8 A on-state current levels, revealing a lower voltage drop of 0.7 V. Finally, the cascode HEMTs were subjected to DPT using an evaluation board. The devices switched at 8 A and 100 V showed on and off rise times of 52 ns and 59 ns, respectively, with 25 µJ and 20 µJ energy loss.

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Credit Author Statement

Rijo Baby: Idea, design, fabrication and testing

Manish Mandal : Circuit design and testing

Shamibrota K.Roy: DPT Circuit design and testing

Abheek Bardhan: Wafer growth MOCVD

R. Muralidharan: Guidance and paper correction

Kaushik Basu: Guidance and paper correction

S. Raghavan: Guidance and paper correction

Digbijoy N. Nath: Guidance and paper correction

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Declaration of interests

☐The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

☒The authors declare the following financial interests/personal relationships which may be considered as potential competing interests:

Digbijoy N Nath reports financial support was provided by Indian Space Research Organisation. Digbijoy N Nath reports a relationship with MHRD that includes:.

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Highlights

Title: 8 A, 200 V Normally-off Cascode GaN-on-Si HEMT: From Epitaxy to Double Pulse Testing

- Indigenously grown AlGaN/GaN HEMT stack on silicon using MOCVD with in-situ SiN_x cap layer. The GaN layer shows the symmetric (002) and asymmetric (102) rocking curves with FWHMs of 0.22 deg. and 0.36 deg. Which is comparable with best-in-literature values
- We are implementing a bi-layer SiN_x process to improve off-state performance with a single field plate blocked ~500V with an absolute on-state current of 10A. Most scientific reports have higher breakdowns with normalized current values and multi-field plates. Scaling the device is an extensive process challenge.
- Commercial Silicon MOSFET transistor cascoded with GaN HEMT and packaged in TO-254 with NAMIC epoxy. The tested device gate swings between +/-30 V with less than 100nA leakage current. On-current measured up to 8A-250V.
- Double pulse testing was performed for fabricated cascoded. The energy loss was measured. On and off rise times of 52 ns and 59 ns were obtained along with energy loss of 25 µJ and 20 µJ, respectively, for devices switched at 8 A, 100 V.

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