Measurement of Circuit Parasitics of SiC MOSFET in a Half-Bridge Configuration

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***Abstract*—Fast switching transient of SiC MOSFET reduces switching loss. However, it excites device and circuit parasitics resulting in prolonged oscillation, high device stress, spurious turn ON, EMI related issues, and higher switching loss. Behavioral or analytical models are used to estimate switching loss (dv/dt), (di/dt) rates, etc., and it requires the value of circuit parasitics as input. Measurement is the only way to accurately estimate some device package-dependent circuit parasitics when the internal package geometry is unknown. Hence, measurement of circuit parasitic is essential for optimal design. This article presents a set of simple experimental measurement techniques to determine circuit parasitic inductance and capacitances relevant for switching transient study of SiC MOSFET in a half-bridge configuration. The accuracy of the proposed technique is verified through simulation and experimental results of the hard turn OFFand capacitor assisted soft turn-OFF dynamics of SiC MOSFET over a range of operating conditions for two 1.2-kV discrete SiC MOSFET of different current ratings and two different PCB layouts. Furthermore, the proposed technique is also validated with the existing frequency response analysis-based impedance measurement.**

***Index Terms*—Dead-time, double pulse test, hard switching, modeling, parasitic measurement, SiC MOSFET, ZVS.**

I. Introduction

Fast switching dynamics of SiC MOSFET reduces switching loss. However, it excites device and circuit parasitics that may result in prolonged oscillation, high device stress, spurious turn ON, EMI-related issues, and higher switching loss [1], [2]. The influence of parasitic also results in a mismatch between actual switching loss and experimentally measured loss [3].

Device parasitics are contributed by the internal capacitances of the SiC MOSFET (i.e., output capacitance) and their values as a function of voltage are given in the device datasheet [3]. On the other hand, circuit parasitic inductances are dependent on both device package (device lead, wire bond, etc.) and circuit layout (PCB layout) whereas circuit parasitic capacitances are contributed solely by the circuit layout and the values are not available from device datasheet [1], [3]. This article is concerned with measuring circuit parasitics of SiC MOSFET in a half-bridge configuration.

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A. Importance of Experimental Estimation of Circuit Parasitics

Fig. 1(a) gives an overview of power converter design. One of the significant parts of converter development is the design of the power stack, which consists of power devices, dc bus capacitor, gate driver circuit, gate, and power circuit layout. In the design process, the power stack is first designed and validated. This process helps to select suitable power device for a given application. It is also useful to accurately obtain switching transition time, loss, (dv/dt), (di/dt), and transient over voltage for a wide range of operating conditions. The obtained switching loss is used to select the switching frequency, which further dictates the design of heatsink and differential mode filter. On the other hand, obtained (dv/dt), (di/dt) values are used to design the common mode filter. Converter design also includes the design of embedded controller and sensor circuitry. An iterative process is followed until all the design requirements are satisfied.

Steps of power stack design are given in Fig. 1(b). The design stage starts with the topology and device selection followed by gate driver design, dc bus capacitor selection and gate and power circuit layout design. Simulation or analytical approaches are used in this stage to extract the circuit parasitics [4]. The extracted values are then used in switching transient models (behavioral models like Spice simulation or analytical model) to compute transition time, (dv/dt), (di/dt) rates, loss etc., where the device and gate driver parameters are obtained from the datasheet [1]. The initial design (for example, gate and power circuit layouts) are optimized using these estimated results to keep (dv/dt), (di/dt) rates, loss, etc., within specified limits.

However, the design cannot be finalized in this stage as the simulation or analytical approaches for parasitic estimation have the following limitations:

1) Simulation approaches are based on finite element analysis (FEA) [4], [5] or partial element equivalent circuit (PEEC) method [6]. Though accurate, this approach requires expensive software tools, long computation time, and may suffer from the convergence problem when the physical structure is complex. Also, the estimated parasitics are functions of frequency and there is ambiguity about the selection of frequency.

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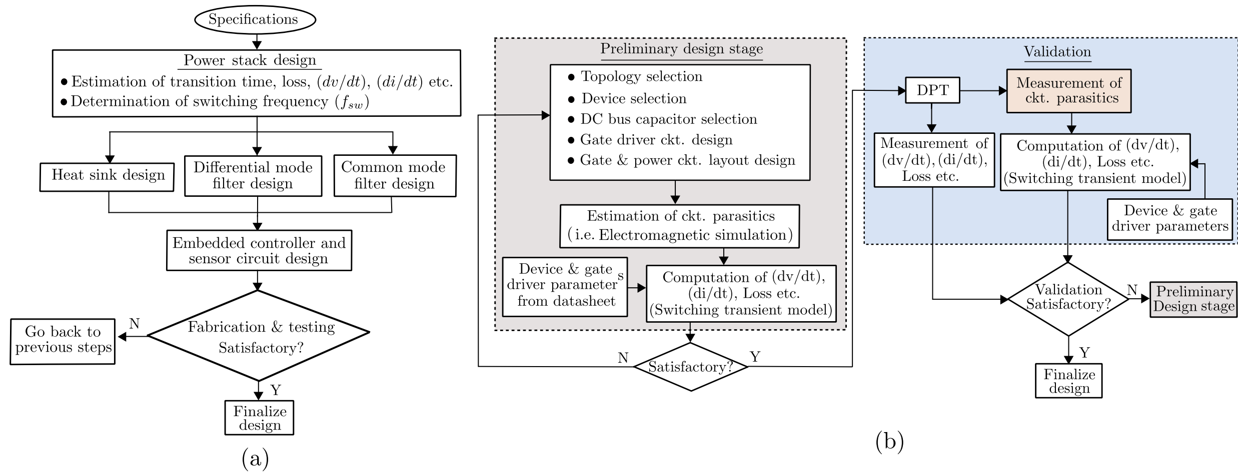

Fig. 1. (a) Overall steps of power converter design. (b) Steps of power stack design.

2) The analytical approach relies on the closed-form expressions of parasitic inductance and capacitances for an approximate simplified geometry of a complex structure [7]. Though it requires less computation time, the estimated parasitics are less accurate when the geometry is complex.
3) Both of the simulation and analytical approaches require the proprietary information of the internal geometrical structure of the device package (i.e., wire bond structure, the dielectric material used, etc.) that may not be available to a converter designer [5].

After the initial design stage, a double pulse test (DPT) setup is designed and fabricated to validate the design experimentally. The circuit parasitics are measured and compared with the parasitic values obtained in the preliminary design stage using simulation or analytical approach. Please note, measurement is the only way to estimate some device package-dependent circuit parasitics accurately when the internal package geometry is unknown. Also, the switching transient waveforms are captured for different operating conditions and validated using the waveforms obtained from the switching transient models with experimentally measured circuit parasitic values. The design is finalized if the results match closely. Otherwise, the initial design is modified accordingly to meet the requirements. The usefulness of the measured parasitic values in accordance with the switching transient model is given below:

1) Fast switching transient of SiC MOSFET makes it challenging to design the gate and power circuit layout and it may lead to sustained oscillation, spurious turn ON, high device stress [1], [2], etc. Switching transient model along with the measured circuit parasitics will help to mitigate the problem through better layout design, optimal gate resistance selection [8] or snubber circuit design, etc. [9].
2) This is well established that the experimentally measured switching loss is different from the actual switching loss and there can be significant difference between actual and experimental losses for SiC MOSFET [8]. Behavioral model along with the measured parasitics help in estimating actual switching loss which is important, especially for soft switched converter design [10].
3) Often it is difficult to measure all the required waveforms accurately due to the limitations of the measurement probes. For example, accurate measurement of gate source and drain source voltages of the high side device in a half-bridge configuration is difficult as the differential probes connected across the respective nodes experience high-frequency common mode voltage. Generally, the common mode rejection ratio of differential probe reduces with frequency [11] and it leads to measurement error.
4) Generally, the experimental switching transient waveforms can be captured for a limited number of operating conditions. However, in practical scenarios, power converter may encounter a wider operating range due to the line and load variations. To understand the switching transient performance for a wider range of operating conditions (for example, load current, temperature, etc.), switching transient model in accordance with circuit parasitics are important.
5) Switching transient model in accordance with measured circuit parasitics can help in designing active gate driving schemes to optimize switching transition time, loss, (dv/dt), (di/dt), transient over voltage, etc., [12].

B. Literature on Measurement of Circuit Parasitics

The experimental approach of measuring circuit parasitics can be conventionally divided into two categories: time domain reflectometry (TDR) and frequency response analysis (FRA). TDR measurement is based on transmission line theory [13]. Though accurate, it requires expensive measurement equipment and software. Also, TDR measurement method is generally developed for 50 Ω connector impedance and suffers from a lack of accuracy when the characteristic impedance of the device under test (DUT) deviates significantly from 50 Ω [14].

FRA based measurement can be divided into one port [15]–[17] or two port [14] measurement. In one port measurement, the impedance between two ports are measured as

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a function of frequency using an impedance analyzer. On the contrary, two port measurement requires vector network analyzer (VNA) where two ports of the DUT are connected to two excitation sources and the third node is connected to the reference. Z-parameter or S-parameter measurements are performed to obtain the parasitic inductance and capacitances. However, FRA based measurement techniques suffer from the following challenges/limitations:

1) The parasitics impact the switching transient of SiC MOSFET are of small values (inductances in the range of few nHs to 10's of nHs and capacitance in the range of 10–100 pF). In general, the DUT is connected to the VNA/impedance analyzer with basic cable type connectors and it may severely affect the measurement accuracy at higher frequencies; especially the measurement of inductances. There are special fixtures provided by the manufacturer to measure low value inductances at higher frequencies (for example, IAI kelvin fixture is available with an impedance analyzer PSM3750 from Newtons4th). However, these fixtures are not suitable to measure PCB layout dependent parasitic inductances due to difficulty in connections. To solve this problem, a special PCB structure is made in [4] to connect the DUT with VNA/impedance analyzer. This may help in the accurate measurement of PCB related inductances but requires specially designed PCBs.
2) In this measurement technique, the circuit elements are considered constant and independent of the excitation frequency [14]–[17]. However, in practical scenarios, the parasitic inductances are strong functions of excitation frequency and generally, the values reduce as the frequency increases [18]. Also, in reality, some of the internal device capacitances are highly nonlinear functions of voltage. So, frequency domain impedance measurement based on linear circuit theory may give erroneous results if the excitation voltage amplitude is relatively high. Please note, nonlinearity of the device capacitance are more pronounced around the zero bias region.
3) In case of one port impedance measurement, the other device terminals are kept floating and this may cause measurement error at higher frequencies if the floating node is in the vicinity of any external object [14].
4) In case of two port measurement technique proposed in [14] to extract parasitics of a half bridge configuration, some of the nodes need to be shorted externally. However, these external connections may introduce extra parasitics which will result in measurement error.
5) Careful calibrations are required (open and short) to measure low values of parasitic inductance and capacitance measurement [19]. If the measurement setup is not calibrated properly, it may lead to measurement error.

However, some of the internal device capacitances are nonlinear functions of voltage, so it is difficult to find circuit parasitic inductances from frequency domain impedance measurement as the estimation procedure is based on linear circuit theory. Also, in the case of one port impedance measurement, generally, the other device terminals are kept floating and this may cause measurement error [14].

There is another experimental approach explicitly developed for the measurement of circuit parasitic relevant in the switching dynamic study of power semiconductor devices, [10], [19]–[21]. This approach does not require specialized expensive measuring instruments used for TDR or FRA. The measurements are done with the oscilloscope and voltage/current probes, routinely used for converter development and testing. Trivedi and Shenai [20] proposed an experimental procedure to extract parasitic inductances for Si IGBT and it is not directly applicable for SiC MOSFET due to different device characteristics. Umetani *et al.* [19] presented a technique to estimate the value of common source inductance but no test procedure is given to obtain other circuit parasitics important for switching dynamics. Similarly, in [21], only the parasitic inductance of the busbar is estimated from the dominant frequency content of turn-OFF voltage oscillation of SiC MOSFET. Note that all the previous literature does not consider the effect of circuit parasitic capacitances which plays an important role in switching dynamics [3], [8]. In [10], circuit parasitics related to the switching transient study of SiC MOSFET and Schottky diode pair are extracted through a simple measurement technique. However, this technique cannot be applied directly for SiC MOSFET in a half-bridge configuration as it ignores the effect of some of the important circuit parasitic inductance and capacitances relevant for switching transient study.

C. Contribution

This article presents a set of experimental techniques for parasitic measurement of SiC MOSFET in a half-bridge configuration. A half-bridge configuration is taken as it is a basic building block of most of the power converters. The proposed technique is based on the behavioral model of SiC MOSFET. It is especially useful for designers who do not have the internal architecture of the packaged device and hence cannot use simulation-based approaches for extraction of circuit parasitics. Circuit parasitic inductances (gate, drain, power loop, and common source inductances) and external parasitic capacitances (parasitic capacitance between gate-drain and drain-source nodes) are estimated using a series of experiments. The proposed technique is validated through simulation and experiment results of the hard turn OFF and capacitor assisted soft turn-OFF dynamics of SiC MOSFET. Two 1.2-kV SiC MOSFET of different current ratings and two different PCB layouts are used for validation.

The rest of the article is arranged in the following order. In Section II, the behavioral model for switching transient study is discussed. The measurement procedure of circuit parasitics is given in Section III. Details of the experimental setup are provided in Section IV and experimental results are given in Section V. Section VI discusses the verification of the proposed measurement technique. Comparison between the proposed parasitic estimation technique and other exiting methods are given in Section VII. Section VII draws the conclusion.

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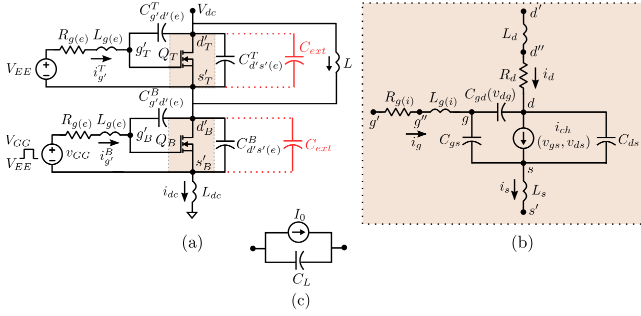

Fig. 2. Circuit configuration for soft turn-OFFswitching transient analysis. (a) Half-bridge configuration with circuit parasitics. (b) SiC MOSFET model. (c) High-frequency model of inductive load L.

II. Behavioral Model

To study the switching transient of SiC MOSFET, a half-bridge configuration is considered [see Fig. 2(a)], where both Q_T and Q_B are SiC MOSFETs. Q_T and Q_B are modeled as three-terminal devices with terminals gate (g'), drain (d'), and source (s'). Input of the half-bridge pair is connected to a dc voltage source V_{dc} and output side connected to an inductive load L. During switching transition, current through L remains almost constant and hence, it can be modeled as a constant current sink I_0 [see Fig. 2(c)]. Also, parasitic capacitance of L (C_L) affects the switching transient [4].

The gate of SiC MOSFET is driven by the voltage source v_{GG}, and it has two levels V_{GG} and V_{EE}, respectively. $R_{g(e)}$ represents the external gate resistance and it includes the internal resistance of the gate driver. $L_{g(e)}$ represents the external gate inductance contributed by the gate driver IC pin inductance and the PCB trace inductance connecting the gate and source pins of the SiC MOSFET to the gate driver. It is considered equal for both Q_T and Q_B as the gate loop for both the MOSFETs are alike.

$C_{g'd'(e)}$ and $C_{d's'(e)}$ are the external gate-drain and drain-source parasitic capacitances contributed by the gate and power circuit routed in the PCB. $C_{g'd'(e)}$ affects the switching transient for both hard and soft switching conditions [8], [22], whereas $C_{d's'(e)}$ impacts the hard switching transient [23]. There are external parasitic capacitances present across g' and s' nodes of both the MOSFETs. However, its value is small compared to the internal gate-source capacitance (C_{gs}) and has a negligible impact on switching transient. In most of the practical scenarios, the PCB layout of the power loop is not symmetric with respect to the midpoint connection (the connection between s'_T and d'_B). So, the value of $C_{g'd'(e)}$ is different for Q_T and Q_B and represented as $C^T_{g'd'(e)}$ and $C^B_{g'd'(e)}$. The same is true for $C_{d's'(e)}$. Parasitic capacitance of the inductive load L (C_L) is considered to be in parallel with $C^T_{d's'(e)}$. C_{ext} is an external capacitor connected across the d' and s' nodes of both the SiC MOSFETs (Q_T and Q_B, respectively) to achieve capacitor assisted soft turn OFFin zero-voltage switching converters [22]. L_{dc} represents the fraction of parasitic inductance of the power loop, which excludes the lead inductances of the SiC MOSFET.

A detailed model of SiC MOSFET is given in Fig. 2(b). $R_{g(i)}$ represents the internal gate resistance. $L_{g(i)}$, L_d, and L_s are the gate, drain, and source inductances, respectively. These are contributed by the lead and wire-bond inductance of the respective pins. Values of $L_{g(i)}$, L_d, and L_s are considered to be equal for both Q_T and Q_B. To model i_{ch} accurately in ohmic and saturation regions, detailed nonlinear functions are used as described in [24]. A single channel approximation is considered for simplicity. In cut off region, $v_{gs} < V_{th}$ and $i_{ch} = 0$. V_{th} is the threshold voltage of the MOSFET. For $v_{ds} < (v_{gs} - V_{th})/P_{vf}$ and $v_{gs} > V_{th}$, SiC MOSFET is in ohmic region and i_{ch} is modeled as (1). y is defined as $(K_f/(K_f - 0.5P_{vf}))$. For $v_{ds} > (v_{gs} - V_{th})/P_{vf}$ and $v_{gs} > V_{th}$, MOSFET is in saturation and i_{ch} is modeled as (2). R_d represents the drift region resistance. This model does not incorporate the effect of parameter variation with temperature. Parameters R_d, K_p, K_f, V_{th}, θ, and P_{vf} are obtained from the transfer characteristics (in saturation region) and output characteristics (in ohmic region) of the SiC MOSFET for a given temperature (provided in the datasheet). All the parameters are temperature dependent and these are extracted for 25 °C

$$i_{ch} \approx \frac{K_p K_f \left((v_{gs} - V_{th})\, v_{ds} - \left(\frac{P_{vf}^{y-1}}{y} \right) (v_{gs} - V_{th})^{2-y}\, v_{ds}^{y} \right)}{(1 + \theta(v_{gs} - V_{th}))} \quad (1)$$

$$\approx \frac{K_p\,(v_{gs} - V_{th})^2}{2(1 + \theta(v_{gs} - V_{th}))}. \quad (2)$$

C_{gs}, $C_{gd}(v_{dg})$, and $C_{ds}(v_{ds})$ are the internal device capacitances. C_{gs} is considered as constant, whereas $C_{gd}(v_{dg})$ and $C_{ds}(v_{ds})$ are nonlinear functions of v_{dg} (3) and v_{ds} (4), respectively. Input capacitance (C_{iss}), reverse transfer capacitance (C_{rss}) and the output capacitance (C_{oss}) as a function of v_{ds} is given in the device datasheet. $C_{gs} \approx C_{iss}$ for high values of v_{ds}, $C_{gd}(v_{dg}) \approx C_{rss}(v_{ds})$ as $v_{dg} \approx v_{ds}$ during the measurement of C_{rss} [3] and $c_{ds}(v_{ds}) = (C_{oss} - C_{rss})$. Parameters $k_1 - k_6$ are obtained through curve fitting using plots given in the datasheet

$$C_{gd}(v_{dg}) = \begin{cases} C_{oxd} = \dfrac{k_1}{k_3}, & v_{dg} \in (-\infty, 0) \\ \dfrac{k_1}{\left(1 + \dfrac{v_{dg}}{k_2}\right)^{1/2} + k_3}, & v_{dg} \in [0, V_{td}) \\ \dfrac{k_4}{\left(1 + \dfrac{v_{dg} - V_{td}}{k_5}\right)^{1/4}}, & v_{dg} \in [V_{td}, \infty) \end{cases} \quad (3)$$

$$C_{ds}(v_{ds}) = \frac{k_6}{\left(1 + \dfrac{v_{ds}}{k_7}\right)^{1/2}}. \quad (4)$$

The parameters related to channel current i_{ch}, device internal capacitance (C_{gs}, C_{gd} and C_{ds}), and $R_{g(i)}$ can be obtained directly from the device datasheet. Parasitic inductances ($L_{g(e)}$, $L_{g(i)}$, L_d, L_s, L_{dc}) and capacitances ($C^T_{g'd'(e)}$, $C^T_{d's'(e)}$, $C^B_{g'd'(e)}$,

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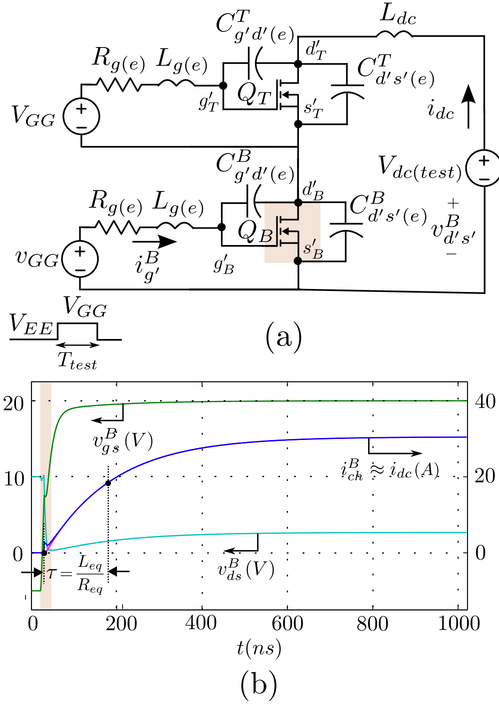

Fig. 3. (a) Circuit configuration. (b) simulation waveforms of Test 1 (SiC MOSFET C2M0080120D, $V_{dc(test} = 10\,V$, $R_{g(e)} = 3.5\,\Omega$).

$C^B_{d's'(e)}$) are layout dependent and has significant impact on switching transient.

III. Circuit Parasitic Measurement

The objective of this section is to obtain the values of circuit parasitics (($L_{g(e)}$, $L_{g(i)}$, L_d, L_s, L_{dc}, $C^T_{g'd'(e)}$, $C^T_{d's'(e)}$, $C^B_{g'd'(e)}$, $C^B_{d's'(e)}$) through experimental measurement. The experimental measurement procedure is classified into two parts: 1) parasitic inductance measurement, 2) layout dependent parasitic capacitance measurement.

A. Parasitic Inductance Measurement

Circuit related parasitic inductances are $L_{g(e)}$, $L_{g(i)}$, L_d, L_s, L_{dc}. The following series of tests are conducted to estimate these parameters.

1) Test 1: To conduct Test 1, the circuit configuration shown in Fig. 3(a) is used. Both Q_T and Q_B are placed in the circuit. The input side is connected to a dc voltage source V_{dc} and output inductive load is not connected. C_{ext} is also not present across any of the devices. V_{GG} is applied across the gate-source of Q_T and it remains in on-state. On the other hand, V_{EE} is applied across the gate-source of Q_B initially and it is blocking the dc bus voltage $V_{dc(test)}$.

As Q_T is gated, it remains in the ohmic region. Current through the internal capacitances of the MOSFET Q_T ($C_{gd}(v^T_{dg})$ and $C_{ds}(v^T_{ds})$) are negligible and it can be modeled as ON-state resistance R_{on} in series with the inductance $(L_d + L_s)$ [see Fig. 4(a)]. R_{on} denotes the ON-state resistance of the SiC MOSFET @$v^T_{gs} = V_{GG}$. As the rate of change of voltage $v^T_{g's'}$ is negligible,

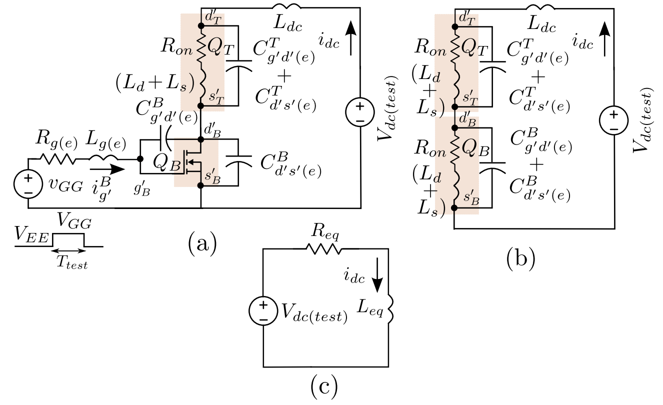

Fig. 4. (a) Equivalent circuit. (b) approximate equivalent circuit 1 and (c) approximate equivalent circuit 2 for Test 1.

the equivalent layout dependent parasitic capacitance across d'_T and s'_T can be represented as $(C^T_{g'd'(e)} + C^T_{d's'(e)})$. Applied dc bus voltage $V_{dc(test)}$ (5–10 V) is small compared to the rated dc bus voltage (≈800 V).

Initially, Q_B is in OFF state and $v^B_{ds} = v^B_{d's'} = V_{dc(test)}$ [see Fig. 3(b)]. Single gate pulse of duration T_{test} is applied across the gate-source of Q_B and v^B_{gs} starts increasing from its initial value V_{EE}. Until $v^B_{gs} = V_{th}$, $i^B_{ch} = i_{dc} = 0$. After $v^B_{gs} > V_{th}$, i^B_{ch} starts increasing. However, due to the presence of parasitic inductance in the power loop, i_{dc} cannot change fast and i^B_{ch} is supported by the discharge of output capacitance of Q_B. As the voltage $V_{dc(test)}$ is small and no load is present, the turn ON transition time of Q_B is small compared to T_{test} [see highlighted portion of Fig. 3(b)].

After the small transient, v^B_{gs} approximately settles to V_{GG} [see Fig. 3(b)] and Q_B remains in on-state (ohmic region) for the rest of the T_{test} period. So, similar to Q_T, Q_B can be modeled as ON-state resistance $R_{on}(@V_{GG})$ in series with the inductance $(L_d + L_s)$. Also, using a similar argument as given for Q_T, the equivalent layout dependent parasitic capacitance across d'_B and s'_B can be represented as $(C^B_{g'd'(e)} + C^B_{d's'(e)})$. Then, the equivalent circuit of Fig. 4(a) can be reduced to Fig. 4(b). Now, the total impedance across d'_T and s'_B of the circuit [see Fig. 4(b)] is given as Z_{eq} and can be approximated as (5) for practical values of different parameters. Detailed calculations are given in the Appendix

$$Z_{eq} \approx 2 \times (R_{on} + s(L_d + L_s))\,. \tag{5}$$

Using the above-mentioned approximation, equivalent circuit Fig. 3(b) can be approximated as Fig. 3(c) where $L_{eq} = (2 \times (L_d + L_s) + L_{dc})$ and $R_{eq} = (2 \times R_{on} + R_{dc})$. R_{dc} represents high-frequency resistance of the power loop and it excludes the ON-state resistance of SiC MOSFETs. The time evolution of $i^B_d \approx i_{dc}$ is given by

$$i_{dc}(t) \approx i^B_d(t) = \left(\frac{V_{dc(test)}}{R_{eq}}\right)\left(1 - e^{-(R_{eq}/L_{eq})t}\right). \tag{6}$$

To perform Test 1, values of T_{test} and $V_{dc(test)}$ need to be selected properly. The value of T_{test} should be in the order of

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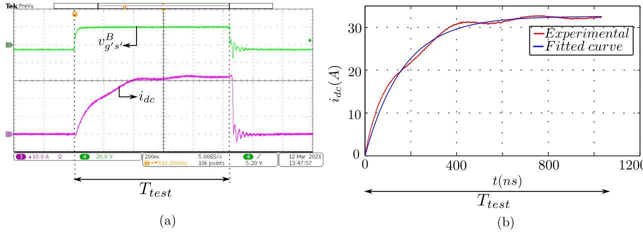

Fig. 5. Measured waveforms of Test 1 (SiC MOSFET C2M0080120D, $V_{dc(test} = 10\,V$, $R_{g(e)} = 3.5\,\Omega$): (a) Experimental waveforms ($v^B_{g's'}$: 20 V/div, i_{dc}: 10 A/div), (b) Fitted curve.

five times the time constant of *RL* circuit given in Fig. 4(c). Note, the steady-state value of $i^B_d \approx i_{dc}$ is given as $(V_{dc(test)}/R_{eq})$. For large values of $i^B_d \approx i_{dc}$, ON-state resistance of both Q_T and Q_B can increase from R_{on}. Thus, $V_{dc(test)}$ is selected from the constrain that both Q_T and Q_B should remain deep into the ohmic region with constant ON-state resistance R_{on} for $i^B_d \approx i_{dc} \in (0, V_{dc(test)}/R_{eq})$. Also, in the worst-case scenario, the entire charge required to build the current i_{dc} will be supplied from the input dc bus capacitor. Assuming i_{dc} is fully supplied by the dc bus capacitor C_{dc}, the condition given in (7) needs to be satisfied

$$\int_0^{T_{\text{test}}} i_{\text{dc}}(\tau)\, d\tau \ll C_{\text{dc}} V_{\text{dc(test)}}. \tag{7}$$

Fig. 5(a) shows a sample experimental result of Test 1. Values of L_{eq} and R_{eq} are estimated by fitting (6) in $i_{dc}(t)$ obtained from Test 1 [see Fig. 5(b)]. A similar test procedure is used in [10] for SiC MOSFET and Schottky diode pair in a buck chopper configuration. It is noteworthy that with the increase in device temperature, value of R_{on} of SiC MOSFET increases. However, values of device package and layout dependent parasitic inductances should remain invariant with temperature. Hence, with the increase in temperature, time constant of *RL* circuit will reduce. Also, the steady-state value of i_{dc} reduces with the increase in device temperature.

2) Test 2: This test is conducted to estimate the value of L_{dc} separately. For Test 2, the circuit configuration given in Fig. 6(a) is used. Both Q_T and Q_B are placed in the circuit. The input side is connected to a dc voltage source V_{dc} and inductive load is connected at the output and it is modeled as a constant current sink I_0. C_{ext} is connected across drain and source terminals of both devices. Double pulse test is conducted to obtain the soft turn-OFFswitching transient waveforms of SiC MOSFET Q_B.

Initially, Q_B is in ON state and load current I_0 is flowing through it. Q_T is reversed biased and it is blocking the entire dc bus voltage V_{dc}. When the gate voltage of Q_B (v_{GG}) is changed from V_{GG} to V_{EE}, the circuit configuration given in Fig. 6(a) goes through a turn OFFtransition called as capacitor assisted soft turn OFF. The waveforms of this transition obtained from the behavioral model for low values of I_0 and $R_{g(e)}$ are given in Fig. 6(b). During the voltage rise period of the soft turn-OFFswitching transient, channel current of Q_B (i^B_{ch}) collapses to zero and oscillatory behavior in i_{dc} can be observed [see the highlighted portion of Fig. 6(b)]. As i^B_{ch} is zero, gate

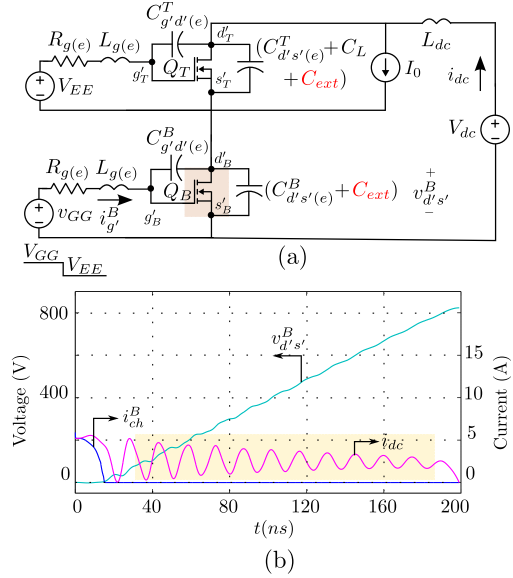

Fig. 6. (a) Circuit configuration and (b) Simulation waveforms (SiC MOSFET C2M0160120D), $V_{dc} = 800\,\text{V}$, $I_0 = 5\,\text{A}$, $R_{g(e)} = 3.3\,\Omega$, $C_{ext} = 470\,\text{pF}$).

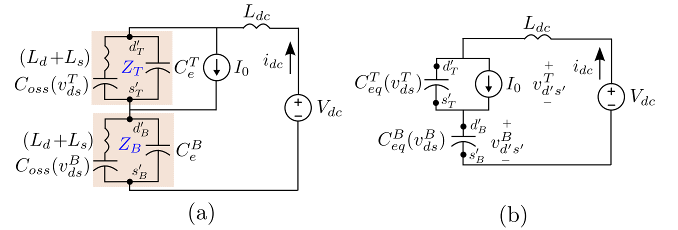

Fig. 7. (a) Equivalent circuit and (b) approximate equivalent circuit for Test 2.

of Q_B looses its control over power circuit state variables and hence, gate circuit dynamics can be neglected for the analysis of the power circuit dynamics [22]. As the channel of both the devices are OFF(both Q_T and Q_B) and the rate of change of gate source voltage is negligible compared to drain source voltage, then devices can be modeled as output capacitances $C_{oss}(v^T_{ds})$ and $C_{oss}(v^B_{ds})$, respectively, in series with parasitic inductances $(L_d + L_s)$. The equivalent capacitances across d'_T, s'_T and d'_B, s'_B are given as C^T_e (8) and C^B_e (9), respectively. Then, the circuit configuration of Fig. 6(a) can be reduced to Fig. 7(a)

$$C^T_e = \left(C^T_{g'd'(e)} + C^T_{d's'(e)} + C_{ext} + C_L\right) \tag{8}$$

$$C^B_e = \left(C^B_{g'd'(e)} + C^B_{d's'(e)} + C_{ext}\right). \tag{9}$$

The impedance between d'_T and s'_T of Fig. 7(a) is given as Z_T (10). The selected value of C_{ext} is large such that $C^T_e \gg C_{oss}(v^T_{ds})$ and Z_T can be approximated as (11). Similarly, $C^B_e \gg C_{oss}(v^B_{ds})$ and using the same argument, Z_B can be represented as (12). Also, $v^T_{d's'} \approx v^T_{ds}$ and $v^B_{ds} \approx v^B_{ds}$. Then, the equivalent circuit of Fig. 7(a) can be reduced to Fig. 7(b) [22]. It can be observed that the effect of lead inductances L_d and L_s of both the MOSFETs are negligible during voltage rise period

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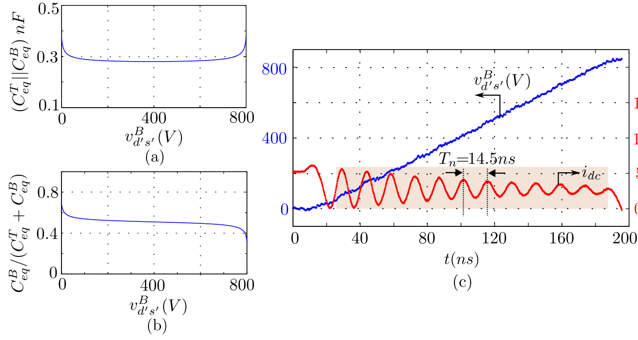


Fig. 8. (a) $(C_{eq}^{T}||C_{eq}^{B})$-$v_{d's'}^{B}$ plot. (b) $(C_{eq}^{B}/(C_{eq}^{T}+C_{eq}^{B}))$-$v_{d's'}^{B}$ plot for C2M0160120D. (c) Experimental waveforms of Test 2 (SiC MOSFET C2M0160120D), $V_{dc} = 800\,\text{V}$, $I_0 = 5\,\text{A}$, $R_{g(e)} = 3.3\,\Omega$, $C_{ext} = 470\,\text{pF}$).

because of the presence of high-value C_{ext}

$$Z_T = \left(s\left(L_d + L_s\right) + \frac{1}{sC_{oss}(v_{ds}^{T})}\right) \parallel \frac{1}{sC_e^{T}} \tag{10}$$

$$\approx \frac{1}{s\left(C_{eq}^{T}(v_{ds}^{T}) + C_e^{T}\right)} = \frac{1}{sC_{eq}^{T}(v_{ds}^{T})} \tag{11}$$

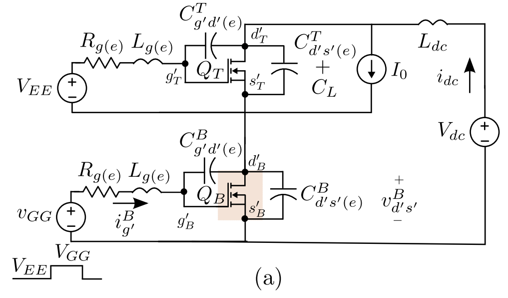
$$Z_B \approx \frac{1}{s\left(C_{eq}^{B}(v_{ds}^{B}) + C_e^{B}\right)} = \frac{1}{sC_{eq}^{B}(v_{ds}^{B})}. \tag{12}$$

Solving the equivalent circuit given in Fig. 7(b), a differential equation of i_{dc} can be found as given in (13). During most of the voltage rise period, v_{ds}^{T} and v_{ds}^{B} are large compared to the voltage drop across L_{dc} resulting $v_{ds}^{T} \approx (V_{dc} - v_{ds}^{B})$. Considering this fact, $(C_{eq}^{T}||C_{eq}^{B})$ and $(C_{eq}^{B}/(C_{eq}^{T} + C_{eq}^{B}))$ are plotted as a function of v_{ds}^{B} in Fig. 8(a) and Fig. 8(b), respectively. It can be observed that both of these quantities remain almost constant for most values of v_{ds}^{B}. So, $(C_{eq}^{T}||C_{eq}^{B})$ is replaced with a constant charge related capacitance C_Q, calculated in the range $(0, V_{dc})$ (14). Note, C_Q represents the average capacitance and it is approximately equal to the flat portion of $(C_{eq}^{T}||C_{eq}^{B})$-$v_{d's'}^{B}$ plot in Fig. 8(a). Also, $(C_{eq}^{B}/(C_{eq}^{T} + C_{eq}^{B}))$ remains almost constant with v_{ds}^{B}. So, (13) can be approximated as a second-order underdamped equation with oscillation time period $T_n = 2\pi\sqrt{L_{dc}C_Q}$

$$L_{dc}\left(C_{eq}^{T}||C_{eq}^{B}\right)\frac{di_{dc}^{2}}{dt^{2}} + i_{dc} = I_0\left(\frac{C_{eq}^{B}}{C_{eq}^{T} + C_{eq}^{B}}\right) \tag{13}$$

$$C_Q = \frac{1}{V_{dc}}\int_0^{V_{dc}} \left(C_{eq}^{T}||C_{eq}^{B}\right) dv_{d's'}^{B}. \tag{14}$$

To estimate the value of L_{dc}, the oscillation time period of i_{dc} during the voltage rise period (T_n) is obtained experimentally [see Fig. 8(c)]. Then, L_{dc} is estimated using the expression $L_{dc} = T_n^2/(4\pi^2 C_Q)$. C_Q has terms like $C_{g'd'(e)}^{T}$, $C_{d's'(e)}^{T}$, $C_{g'd'(e)}^{B}$, and $C_{d's'(e)}^{B}$, which are obtained separately using Test 5 and estimated values are used here. It is also noteworthy that for low values of I_0 and $R_{g(e)}$, i_{ch}^{B} collapses fast and the voltage rise period is prolonged with several peaks and valleys in i_{dc}. This results in a better estimation of L_{dc}. Also, the internal device capacitances and device package and layout dependent inductance and capacitances are weak functions of temperature,



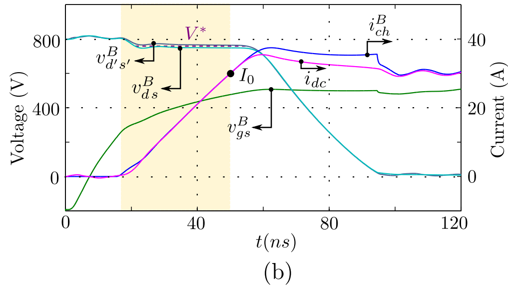


Fig. 9. (a) Circuit configuration and (b) Simulation waveforms (C2M0080120D, $V_{dc} = 800\,V$, $I_0 = 30\,A$, $R_{g(e)} = 21\,\Omega$) of Test 3.

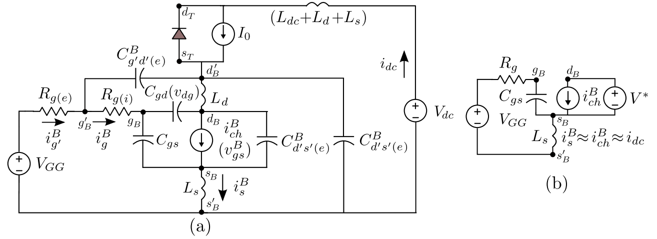


Fig. 10. (a) Equivalent circuit and (b) approximated equivalent circuit of Test 3.

implying the values of C_Q and L_{dc} are expected to be weak functions of temperature [25]. Thus, the value of T_n should not vary with the change in temperature.

3) Test 3: This test is conducted to estimate the value of L_s. Fig. 9(a) represents the circuit configuration of Test 3. Both Q_T and Q_B are placed in the circuit. The input side is connected to a dc voltage source V_{dc}. The inductive load is connected at the output and it is modeled as a constant current sink I_0. No C_{ext} is present across any of the devices. Double pulse test is conducted to obtain the turn-ON switching transient waveforms of SiC MOSFET Q_B.

The hard turn-ON waveforms obtained from the behavioral simulation for moderately high values of $R_{g(e)}$ is given in Fig. 9(b). During the current rise period [see the highlighted portion of Fig. 9(b)], both i_{dc} and i_{ch}^{B} are approximately equal and less than I_0 and the rest of the load current is flowing through the body diode of Q_T. So, L_d and L_s of Q_T can be lumped with L_{dc} in the power loop. The value of $R_{g(e)}$ is large and the gate circuit is over damped. So, the effect of $L_{g(e)}$ and $L_{g(i)}$ are negligible. Fig. 10(a) represents the equivalent circuit of Test 3.

KCL at nodes g_B and g_B' of Fig. 10(a) results in (15) and (16), respectively. Also, applying KVL in the loop formed by g_B, d_B,

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s_B and g'_B, d'_B, s'_B, we get (17) and (18). KVL in the gate loop of Q_B results in (19)

$$i_g^B = C_{gs}\frac{dv_{gs}^B}{dt} + C_{gd}\frac{dv_{gd}^B}{dt} \tag{15}$$

$$i_{g'}^B = i_g + C_{g'd'(e)}^B \frac{dv_{g'd'}^B}{dt} \tag{16}$$

$$v_{gs}^B = v_{gd}^B + v_{ds}^B \tag{17}$$

$$v_{g's'}^B = v_{g'd'}^B + v_{d's'}^B \tag{18}$$

$$V_{GG} = i_{g'}^B R_{g(e)} + i_g^B R_{g(i)} + v_{gs}^B + L_s\frac{di_s^B}{dt}. \tag{19}$$

It can be observed from Fig. 9(b) that $v_{ds}^B \approx v_{d's'}^B$ and remain almost constant to V^* implies $(dv_{ds}^B/dt) \approx (dv_{d's'}^B/dt) \approx 0$. For most of the current rise period, $i_{\rm dc}$ and i_{ch}^B are approximately equal. Also, gate current $i_{g'}^B \ll i_{dc}$ implies $i_{dc} \approx i_d^B \approx i_s^B \approx i_{ch}^B$ [3]. V^* is close to $V_{\rm dc}$ and the value of $C_{gd}(v_{dg}) \ll C_{gs}$. Also, in practical scenarios, the value of $C_{g'd'(e)}^B \ll C_{gs}$. As an example, for C2M0080120D SiC MOSFET from Wolfspeed (1200 V, 36 A), $C_{gs} = 950$ pF and $C_{gd}(v_{dg}) = 7.6$ pF @$v_{dg} =$ 800 V. Also, the value of $C_{g'd'(e)}^B \approx 5.5$ pF. This implies current through $C_{gd}(v_{dg})$ and $C_{g'd'(e)}$ are small compared to the current flowing through C_{gs}.

Now, replacing the values of i_g^B and $i_{g'}^B$ from (15) and (16), respectively, in (19) and using (17), (18) along with above-mentioned approximations, we obtain (20), where $R_g = (R_{g(e)} + R_{g(i)})$. As $\theta(v_{gs}^B - V_{th}) \ll 1$, so (2) can be approximated as (21). Using (20) and (21), $(di_{\rm dc}/dt)$ for SiC MOSFET during the current rise period can be represented using (22). At $i_{\rm dc} = I_0$, the value of $v_{gs}^B = V_m$ and it is given by (23). It is well established that L_s heavily impacts the current rise period of turn-ON switching transient of SiC MOSFET [3]

$$V_{GG} \approx R_g C_{gs}\frac{dv_{gs}^B}{dt} + v_{gs}^B + L_s\frac{di_{ch}^B}{dt} \tag{20}$$

$$i_{ch}^B \approx \frac{K_p}{2}\left((v_{gs}^B - V_{th})^2 - \theta(v_{gs}^B - V_{th})^3\right) \tag{21}$$

$$\frac{di_{\rm dc}}{dt} \approx \frac{K_p(V_{GG} - v_{gs}^B)\left((v_{gs}^B - V_{th}) - (3\theta/2)(v_{gs}^B - V_{th})^2\right)}{R_g C_{gs} + K_p L_s\left((v_{gs}^B - V_{th}) - (3\theta/2)(v_{gs}^B - V_{th})^2\right)} \tag{22}$$

$$V_m = \frac{I_0\theta + \sqrt{(I_0\theta)^2 + 2I_0K_p}}{K_p} + V_{th}. \tag{23}$$

Value of L_s can be estimated such that the slope of i_{dc} at $i_{dc} = I_0$ [obtained by replacing $v_{gs}^B = V_m$ in (22)] matches with the experimentally obtained $(di_{\rm dc}/dt)$ value [see Fig. 11(a),(b)]. It is noteworthy that unlike internal device capacitances (for example, C_{gs}) the device parameters related to transfer and output characteristics are strong functions of temperature (for example, K_p and θ) [25]. So, the rate of change of i_{dc} reduces with the increase in temperature.

4) Test 4: This test is performed to measure the gate inductance $L_{g(e)}$ and $L_{g(i)}$. For measurement, the circuit given in Fig. 12(a) is used. Q_T is removed and Q_B is placed in the circuit.

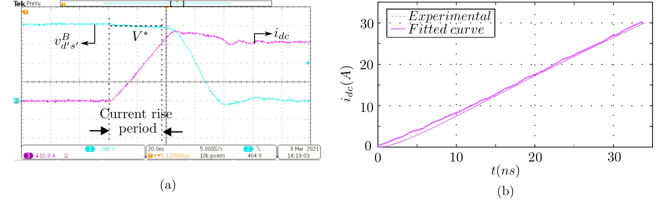

Fig. 11. Measured waveforms of Test 3 (SiC MOSFET C2M0080120D, $V_{dc} = 800$ V, $I_0 = 30$ A, $R_{g(e)} = 21\ \Omega$). (a) Experimental waveforms ($v_{d's'}^B$: 200 V/div, i_{dc}: 10 A/div). (b) Fitted curve.

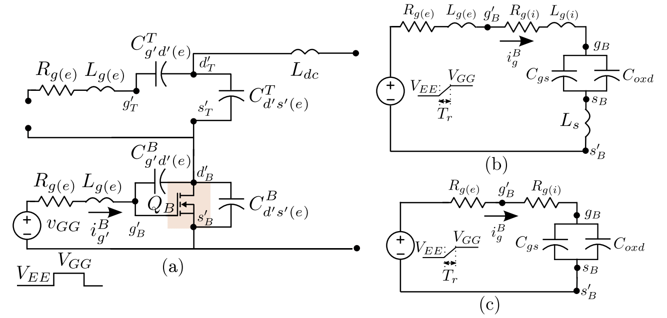

Fig. 12. (a) Circuit configuration of Test 5. (b) Approximate equivalent circuits for low $R_{g(e)}$. (c) Approximate equivalent circuit for high $R_{g(e)}$.

No C_{ext} is present across any of the devices and inductive load is also removed. Initially voltage v_{gs}^B is V_{EE} and v_{ds}^B is equal to zero.

Gate voltage v_{GG} of Q_B is switched from V_{EE} to V_{GG} and v_{gs}^B starts to rise from its initial value V_{EE}. For a significant portion of turn ON transient, $v_{gs}^B > V_{th}$ and the channel is ON with a small ON-state resistance resulting $v_{ds}^B \approx 0$. So, $v_{gs}^B \approx v_{gd}^B$ and $v_{gd}^B > 0$ (as $V_{th} > 0$) except for small initial portion. It implies $C_{gd} = C_{oxd}$ [see (3)]. Practically, the value of $C_{g's'(e)}$ is negligible compared to C_{gs} and, hence, the effect is neglected. Also, the effect of $C_{g'd'(e)}^B$ is not considered as the value of $C_{g'd'(e)}^B$ is small compared to C_{oxd}.

With these approximations, the gate loop of Q_B forms a series *RLC* circuit with $R_g = (R_{g(e)} + R_{g(i)})$, $L = (L_{g(i)} + L_{g(e)} + L_s)$, and $C = (C_{gs} + C_{oxd})$ [see Fig. 12(b)]. Along with $L_{g(e)}$ and $L_{g(i)}$, C is also unknown as the value of C_{oxd} is not directly available from device datasheet. Measurement of gate inductances $L_{g(i)}$ and $L_{g(e)}$ is divided into two parts, Test 4.1 and Test 4.2, respectively.

a) Test 4.1: This test is conducted to estimate the value of $C = (C_{gs} + C_{oxd})$. A moderately high value of $R_{g(e)}$ (in range of $10 - 100\ \Omega$) is used such that the damping factor of the *RLC* circuit $(R_g/2)\sqrt{C/L} \gg 1$ and it makes the circuit highly overdamped. Then, the response can be approximated by a series *RC* circuit. Fig. 12(c) represents the equivalent circuit of this mode. Gate voltage v_{GG} of Q_B is switched from V_{EE} to V_{GG} and $v_{g's'}^B(t)$ is measured. Note, v_{GG} changes from V_{EE} to V_{GG} with rise time T_r. T_r can be obtained from the gate driver datasheet and/or experiment. $R_{g(i)}$ is known from the device datasheet. The value of equivalent capacitance

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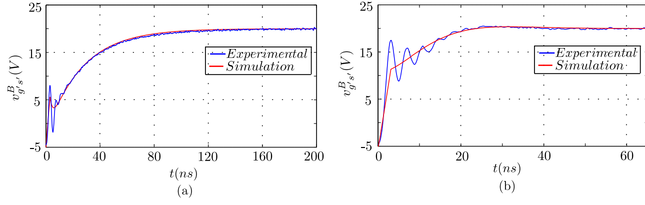

Fig. 13. Measured waveforms of Test 4 for SiC MOSFET C2M0160120D. (a) Fitted curve for $R_{g(e)} = 21\ \Omega$. (b) Fitted curve for $R_{g(e)} = 3.5\ \Omega$.

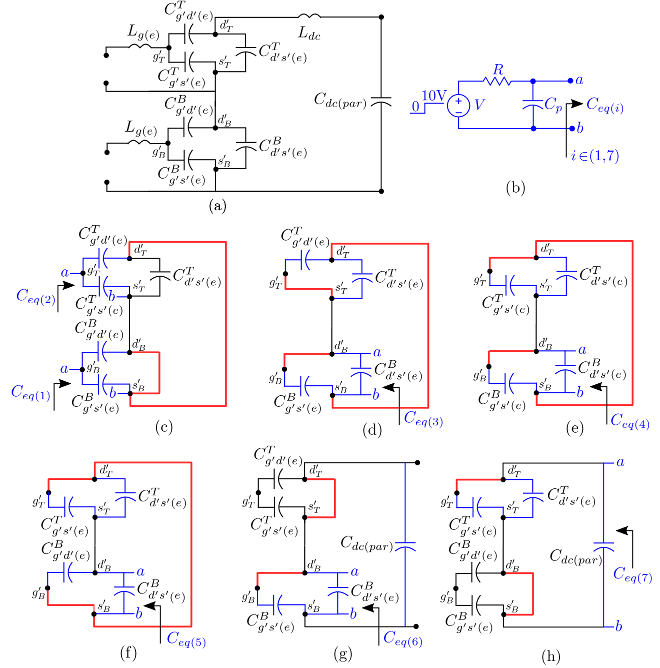

Fig. 14. Circuit configuration and equivalent circuits for parasitic capacitance measurement: (a) Circuit configuration, (b) Equivalent circuit of measurement set-up, (c) Circuit configuration for Test 5.1 and Test 5.2, (d) Test 5.3, (e) Test 5.4, (f) Test 5.5, (g) Test 5.6, (h) Test 5.7 (Red line indicates the nodes of the PCB shorted externally and blue colored capacitors are excited during measurement).

$C = (C_{gs} + C_{oxd})$ is adjusted such that the simulated $v^B_{g's'}$ from equivalent circuit given in Fig. 12(c) matches closely with the experimental result [see Fig. 13(a)].

a) Test 4.2: After obtaining the value of C, this test is conducted to estimate the values of $L_{g(e)}$ and $L_{g(i)}$. In this step, a small value of $R_{g(e)}$ is selected such that the damping factor of the *RLC* circuit $(R_g/2)\sqrt{C/L}$ is low and the effect of L_g is dominant. Fig. 12(b) represents the equivalent circuit for this test. Values of $R_{g(e)}$ and $R_{g(i)}$ are known and the estimated value of C from Test 4.1 is used. Rise time of v_{GG} (T_r) is also considered. Similar to Test 4.1, values of $L_{g(e)}$ and $L_{g(i)}$ are adjusted in simulation such that $v^B_{g's'}$ waveform obtained from the experiment matches with simulation result [see Fig. 13(b)]. Two different $R_{g(e)}$ are used to confirm the accuracy of the estimated $L_{g(e)}$ and $L_{g(i)}$. It is noteworthy that the values of $L_{g(e)}$ and $L_{g(i)}$ do not vary with temperature.

After Test 1 to Test 4, $L_{g(e)}$, $L_{g(i)}$, L_d, L_s, and L_{dc} are obtained in the following way: L_{eq} and L_{dc} are obtained from Test 1 and Test 2, respectively. The $(L_d + L_s) = (L_{eq} - L_{dc})/2$. L_s is directly estimated from Test 3 and then L_d can be separated. Gate loop inductances $L_{g(e)}$ and $L_{g(i)}$ are obtained from Test 4.

B. Layout Dependent Parasitic Capacitance Measurement

The objective of this section is to measure the layout dependent external parasitic capacitances important for switching transient study. These parasitic capacitances are contributed primarily by the PCB layout. Values of these capacitances are in the order of pico-farads and difficult to measure using a basic hand-held LCR meter. There are three parasitic capacitances associated with each of the SiC MOSFETs, namely $C_{g's'(e)}$, $C_{g'd'(e)}$, and $C_{d's'(e)}$ (superscript T and B are used for Q_T and Q_B, respectively). $C_{dc(par)}$ represents the parasitic capacitance of the dc bus [see Fig. 14(a)]. Please note, unlike internal device capacitances of SiC MOSFET, these PCB layout dependent parasitic capacitances are not functions of applied voltage.

Among the capacitance shown in Fig. 14(a), $C_{g's'(e)}$ has a negligible impact in switching dynamics of SiC MOSFET as internal MOSFET gate-source capacitance C_{gs} is large compared to $C_{g's'(e)}$. $C_{g'd'(e)}$ impacts both hard and soft switching dynamics of SiC MOSFET [8], [22]. On the other hand, $C_{d's'(e)}$ influences the hard switching dynamics [23]. However, it has less impact on soft switching dynamics as the practical values of $C_{d's'(e)}$ is small compared to the externally connected C_{ext} [22].

1) Test 5: For this measurement, a bare PCB is used. No components are placed in the PCB and the inductive load is disconnected. The circuit configuration is given in Fig. 14(a). The technique adopted to measure the capacitances of pico-farad range is described hereafter where the circuit configuration of Fig. 14(b) is used. The circuit consists of a step voltage source V in series with a resistor R. V is selected in the range of 5–10 V and the value of R is in the range of $R \approx 100k\ \Omega - 500k\ \Omega$. A voltage probe is connected across the nodes a and k. C_p represents the equivalent capacitance contributed by the input capacitance of the voltage probe and the parasitic capacitance of the resistor pad.

This circuit is connected externally in series with the accessible nodes in the PCB across which the capacitance has to be measured [i.e., g'_B and s'_B nodes of the PCB in Fig. 14(c)]. This forms a series *RLC* circuit with externally connected resistance, wire, and the lead inductance of the resistor (L) and equivalent capacitance $(C_p + C_{eq(i)})$. $C_{eq(i)}$ represents the equivalent parasitic capacitance to be measured where $i \in (1, 7)$ corresponds to test 5.1 to 5.7, respectively. A step voltage is applied to this *RLC* circuit and the voltage v_{ab} is measured. Now the external resistance is selected to be large such that the damping ratio $(R/2)\sqrt{C_{eq(i)}/L} \gg 1$ and the circuit response can be approximated by a first-order *RC* circuit with a time constant $\tau = (1/R(C_{eq(i)} + C_p))$. As the circuit is highly overdamped, the effect of parasitic inductances due to the PCB layout (e.g. L_{dc}) and the external connections can also be neglected.

Value of C_p is estimated from the RC response without connecting it to the PCB nodes. After estimating C_p, PCB nodes are connected across a and k and $C_{eq(i)}$ can be evaluated from the time constant (τ) of the *RC* circuit. Note the measured

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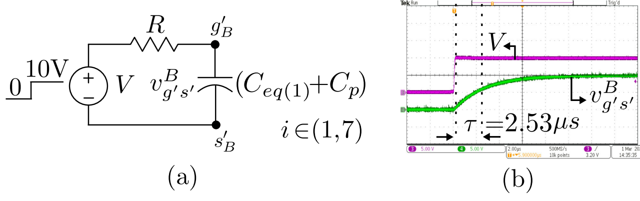

Fig. 15. Measurement of parasitic capacitance. (a) Equivalent circuit. (b) Experimental waveforms.

equivalent capacitance is $(C_{eq(i)}+C_p)$ and estimated C_p is subtracted from the obtained result to get the value of $C_{eq(i)}$. The following tests are conducted to estimate the values of the four capacitances, namely $C^T_{g'd'(e)}$, $C^B_{g'd'(e)}$, $C^T_{d's'(e)}$, and $C^B_{d's'(e)}$ from the set of seven different capacitances.

a) Test 5.1: For Test 5.1, nodes d'_T, s'_B and d'_B, s'_B of Fig. 14(a) are shorted externally and the equivalent parasitic capacitance across g'_B and s'_B is measured [see Fig. 14(c)]. The value of equivalent parasitic capacitance across g'_B and s'_B node is given as (24). To measure this capacitance, $R=100k\ \Omega$ is connected in series with the g'_B and s'_B pads accessible in the PCB [see Fig. 15(a)]. $C_{eq(1)}$ can be estimated from the time constant (τ) of the *RC* circuit [see Fig. 15(b)]. Note, the measured equivalent capacitance is $(C_{eq(1)}+C_p)$ and estimated C_p is subtracted from the obtained result to get the value of $C_{eq(1)}$.

b) Test 5.2: For this test, the same circuit configuration of Test 5.1 is used [see Fig. 14(c)]. The equivalent parasitic capacitance across g'_T and s'_T is measured using the same technique and it is equal to (24).

c) Test 5.3: For this test, Nodes d'_T, s'_B and g'_T, s'_T and g'_B, d'_B are shorted externally and the capacitance across d'_B and s'_B is measured [see Fig. 14(d)]. The equivalent capacitance across d'_B and s'_B is given by (26).

d) Test 5.4: For this test, Nodes d'_T, s'_B and g'_T, d'_T and g'_B, d'_B are shorted and the capacitance across d'_B and s'_B is measured [see Fig. 14(e)]. The equivalent capacitance across d'_B and s'_B is given by (27).

e) Test 5.5: For Test 5.5, Nodes d'_T, s'_B and g'_T, d'_T and g'_B, s'_B are shorted and the capacitance across d'_B and s'_B is measured [see Fig. 14(f)]. The equivalent capacitance across d'_B and s'_B is given by (28).

f) Test 5.6: For this test, circuit configuration given in Fig. 14(g) is used. Nodes d'_B, s'_B and d'_T, g'_T are shorted and The equivalent capacitance across d'_T and s'_B is measured. The equivalent capacitance is given by (29).

g) Test 5.7: For this test, circuit configuration given in Fig. 14(h) is used. Nodes d'_T, g'_T and d'_B, s'_B are shorted and The equivalent capacitance across d'_T and s'_B is measured. The equivalent capacitance is given by (30).

After completing Test 5.1 to Test 5.7, the algebraic equations are written in the form given in (31) and the individual values of the parasitic capacitances are obtained by solving (31). It is noteworthy that these layout dependent capacitance are weak functions of temperature

$$C_{eq(1)} = \left(C^B_{g'd'(e)} + C^B_{g's'(e)}\right) \tag{24}$$

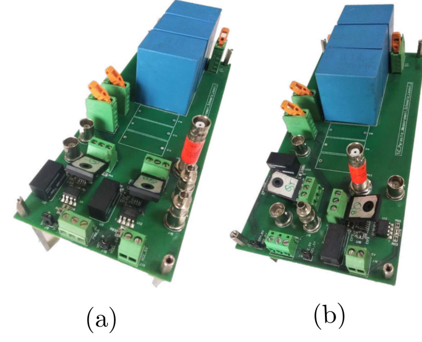

Fig. 16. Double pulse test setup: (a) L1, (b) L2.

$$C_{eq(2)} = \left(C^T_{g'd'(e)} + C^T_{g's'(e)}\right) \tag{25}$$

$$C_{eq(3)} = \left(C^B_{g's'(e)} + C^B_{d's'(e)} + C^T_{g'd'(e)} + C^T_{d's'(e)}\right) \tag{26}$$

$$C_{eq(4)} = \left(C^T_{g's'(e)} + C^T_{d's'(e)} + C^B_{g's'(e)} + C^B_{d's'(e)}\right) \tag{27}$$

$$C_{eq(5)} = \left(C^T_{g's'(e)} + C^T_{d's'(e)} + C^B_{g'd'(e)} + C^B_{d's'(e)}\right) \tag{28}$$

$$C_{eq(6)} = \left(C^B_{g's'(e)} + C^B_{d's'(e)} + C_{dc(par)}\right) \tag{29}$$

$$C_{eq(7)} = \left(C^T_{g's'(e)} + C^T_{d's'(e)} + C_{dc(par)}\right) \tag{30}$$

$$\begin{pmatrix} 0 & 0 & 0 & 1 & 1 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 0 & 1 & 0 \\ 1 & 0 & 1 & 1 & 0 & 1 & 0 \\ 1 & 0 & 1 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 1 & 0 & 1 & 1 \\ 1 & 0 & 1 & 0 & 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} C^T_{g's'(e)} \\ C^T_{g'd'(e)} \\ C^T_{d's'(e)} \\ C^B_{g's'(e)} \\ C^B_{g'd'(e)} \\ C^B_{d's'(e)} \\ C_{dc(par)} \end{pmatrix} = \begin{pmatrix} C_{eq(1)} \\ C_{eq(2)} \\ C_{eq(3)} \\ C_{eq(4)} \\ C_{eq(5)} \\ C_{eq(6)} \\ C_{eq(7)} \end{pmatrix}. \tag{31}$$

IV. Experimental Setup

To validate the circuit parasitic extraction procedures described in Section III through experiment, a half-bridge configuration with two different layouts are considered, as shown in Fig. 16(a) and (b), respectively. For each of these layouts, two different SiC MOSFETs are used, S1: C2M0160120D (19 A @25°) and S2: C2M0080120D (36 A @25°). Device related parameters are extracted from the datasheet @25° and given in Table I.

Double pulse test (DPT) setup is designed for 800 V dc bus voltage and 50 A load current. Air core inductor with 150 μH is used as the inductive load. The parasitic capacitance of the inductive load C_L is measured using PSM 3750 from Newtons4th Ltd and the value is 17.5 pF. Opto-isolator IX3180GS followed by a current booster IXDN609SI is used as gate driver. Parameters related to gate driver are given in Table II and it is common for both devices. $R_{dr(on)}$ and $R_{dr(off)}$ are the ON and

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TABLE I
DEVICE PARAMETERS EXTRACTED FROM DATASHEET (S1: C2M0160120D AND S2: C2M0080120D)

	V_{th} (V)	K_p (A/V^2)	K_f	θ (1/V)	P_{vf}	R_d (Ω)	$R_{g(i)}$ (Ω)	C_{gs} (nF)	k_1 (nF)	k_2 (V)	k_3	V_{td} (V)	k_4 (nF)	k_5 (V)	k_6 (nF)	k_7 (V)	k_8 (nF)	k_9 (V)
S1	4.6	1.3	1.54	0.03	0.33	0.03	6.5	0.53	0.8	0.2	1.24	12	0.06	0.02	0.43	5.5	0.75	2.21
S2	5.6	1.6	2.19	0.01	0.4	0.01	4.6	1.1	0.95	0.35	0.71	12	0.12	0.025	0.79	5.5	1.3	2.34

TABLE II
DRIVER PARAMETERS

V_{EE} (V)	V_{GG} (V)	$R_{dr(on)}$ (Ω)	$R_{dr(off)}$ (Ω)	T_r (ns)	T_f (ns)
-5	20	1	0.8	3	3

OFF state resistances of the gate driver. T_r and T_f are the rise and the fall times of the gate driver.

The accuracy of the estimated parasitics are strongly correlated with the accuracy of the measurement of high frequency waveforms (voltage and current). To measure these signals correctly, high bandwidth oscilloscope, voltage and current probes are required. Oscilloscope MDO3104 from Tektronix with 1 GHz bandwidth is used. Passive probe TPP1000 of 1 GHz bandwidth and high voltage single-ended probe P5100 A with 500 MHz bandwidth (both from Tektronix) are used for voltage measurement. To measure device current, coaxial current shunt SSDN-10 from T&M research is used. BNC connector is placed on the board to measure gate source ($v^B_{g's'}$) and drain source voltage ($v^B_{d's'}$) accurately. This reduces the ground loop inductance, EMI related issues and results in accurate measurement of the concerning signals. Also, the coaxial current shunt used for power loop current measurement is connected to the oscilloscope with a shielded BNC cable. Matching of propagation delay between voltage and current signals are done using a delay matching instrument available from Tektronix (067-1686-00, Power Measurement De-skew and Calibration Fixture). Amplitude and time scales of the oscilloscope are adjusted properly to measure the voltage and current waveforms with less quantization and sampling errors.

MATLAB/Simulink is used to simulate the behavioral model used for switching transient analysis. All the experiments are performed at room temperature (≈ 25 °C).

V. EXPERIMENTAL MEASUREMENT OF CIRCUIT PARASITICS

Experimental measurement of circuit parasitics are categorized into two parts: 1) parasitic inductance measurement, 2) parasitic capacitance measurement.

A. Parasitic Inductance Measurement

The parasitic inductances are L_d, L_s, $L_{g(e)}$, $L_{g(i)}$, and L_{dc}. Experiments are conducted on two different layouts L1 and L2. For each layout, two different devices S1 and S2 are considered. This totally means four different combinations: (L1,S1), (L1,S2), (L2,S1), and (L2,S2), respectively. Test 1 to Test 4 are conducted to estimate the values of parasitic inductances.

1) Test 1: Test 1 is conducted to estimate the values of L_{eq} and R_{eq} (see Test 1 of Section III). $V_{dc(test)}$ of 5 and 10 V are used alongwith $R_{g(e)} = 3.5\Omega$. The experiment is conducted for four different combinations (L1,S1), (L1,S2), (L2,S1), and (L2,S2). $T_{test} \approx 1\mu s$ is used for measurement. i_{dc} waveforms obtained through experiment are fitted using (6) to estimate L_{eq} and R_{eq} and the overlapped plots are given in Fig. 17 for (L1,S1) and (L2,S2). Also, the estimated values of L_{eq} and R_{eq} [using (6)] are tabulated in Table III for all four different combinations.

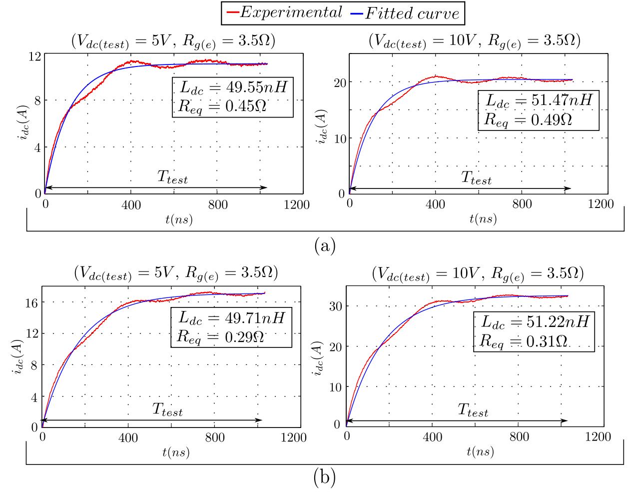

Fig. 17. Experimental results of Test 1.

TABLE III
L_{eq} AND R_{eq} ESTIMATION

	$V_{dc(test)} = 5$V		$V_{dc(test)} = 10$V	
	L_{eq}(nH)	R_{eq}(Ω)	L_{eq}(nH)	R_{eq}(Ω)
(L1,S1)	49.55	0.45	51.47	0.49
(L1,S2)	50.78	0.3	52.52	0.32
(L2,S1)	50.81	0.45	50.5	0.49
(L2,S2)	49.71	0.29	51.22	0.31

2) Test 2: Test 2 is conducted to estimate the values of L_{dc} separately (see Test 2 of Section III). For that, soft turn-OFF waveforms ($v^B_{d's'}$, i_{dc}) are captured for $V_{dc} = 800$ V, $R_{g(e)} = 3.3\ \Omega$, $C_{ext} = 470$ pF, $I_0 = 5$ A, 10 A for S1 and $I_0 = 10$ A, 20 A for S2. The time period of oscillation in i_{dc} (T_n) is measured from i_{dc} waveform during the voltage rise period. Fig. 18 provides result for two different combinations, (L1,S1) and (L2,S2). The experimentally obtained T_n values are tabulated in Table IV for (L1,S1), (L1,S2), (L2,S1), and (L2,S2). Also, the values of C_Q are calculated. Then, using the expression $L_{dc} = T_n^2/(4\pi^2 C_Q)$, L_{dc} is estimated (see Table IV). Note, 1% tolerance C_{ext} with NP0 dielectric is used to estimate the values of L_{dc} accurately.

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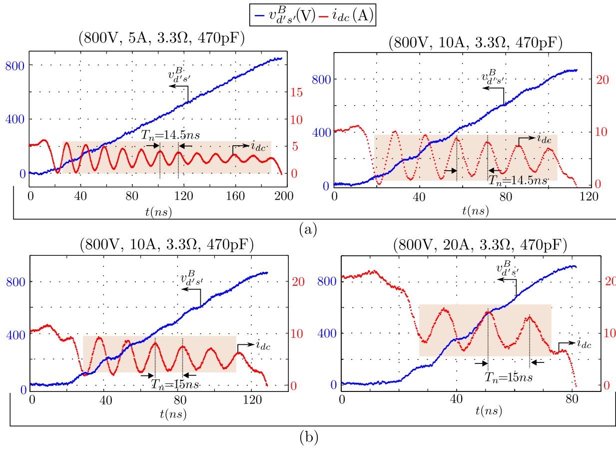

Fig. 18. Experimental results of Test 2.

TABLE IV
L_{dc} ESTIMATION

	I_0(A)	T_n(ns)	C_Q(nF)	L_{dc}(nH)
(L1,S1)	5,10	14.5	0.2881	18.50
(L1,S2)	10,20	14.6	0.3145	17.19
(L2,S1)	5,10	14.7	0.2898	18.91
(L2,S2)	10,20	15	0.3162	18.04

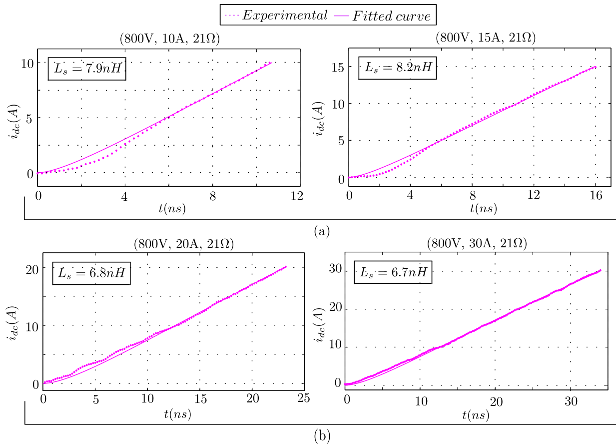

Fig. 19. Experimental results of Test 3.

3) Test 3: Test 3 is conducted to estimate the values of L_s (see Test 3 of Section III). $R_{g(e)} = 16\ \Omega$ and $21\ \Omega$ are used and the value of L_s is estimated from the slope of the current rise using (22). The experimental results are given in Fig. 19 for $R_{g(e)} = 21\ \Omega$ and (L1,S1), (L2,S2). Also, the estimated values of L_s are given in Table V for (L1,S1), (L1,S2), (L2,S1) and (L2,S2).

4) Test 4: Test 4 is conducted to estimate the values of $L_{g(e)}$ and $L_{g(i)}$ (see Test 4 of Section III). It is divided into two parts: Test 4.1 and Test 4.2. First, in Test 4.1, $R_{g(e)} = 21\,\Omega$ is used and the value of $C = (C_{gs} + C_{oxd})$ is estimated. C is only device dependent and the values are 1.04 nF and 2.2 nF for S1 and S2, respectively. Then from Test 4.2, the values of $L_{g(e)}$ and $L_{g(i)}$ are estimated using $R_{g(e)} = 1\,\Omega$ and 3.5 Ω. Fig. 20 provides the experimental results for (L1,S1) and (L2,S2) with $R_{g(e)} = 1\,\Omega$ and $R_{g(e)} = 3.5\,\Omega$. The estimated values of $L_{g(e)}$ and $L_{g(i)}$ are given in Table VI for (L1,S1), (L1,S2), (L2,S1), and (L2,S2).

TABLE V
L_s ESTIMATION

		$R_{g(e)} = 16\Omega$		$R_{g(e)} = 21\Omega$	
	I_0 (A)	$(di_{dc}/dt)_{exp}$ (A/ns)	L_s (nH)	$(di_{dc}/dt)_{exp}$ (A/ns)	L_s (nH)
(L1,S1)	10	1.07	7.8	1	7.9
	15	1	8	0.93	8.2
(L1,S2)	20	1	6.7	0.93	6.8
	30	0.92	6.7	0.86	6.7
(L2,S1)	10	1	8.5	0.92	8.9
	15	0.97	8.3	0.89	8.8
(L2,S2)	20	1	6.7	0.93	6.8
	30	0.93	6.6	0.86	6.7

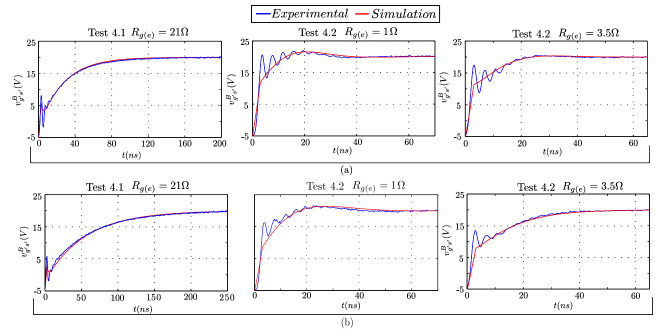

Fig. 20. Experimental results of Test 4.

TABLE VI
$L_{g(i)}$ AND $L_{g(e)}$ ESTIMATION

	$R_{g(e)} = 1\Omega$		$R_{g(e)} = 3.5\Omega$	
	$L_{g(e)}$(nH)	$L_{g(i)}$(Ω)	$L_{g(e)}$(nH)	$L_{g(i)}$(Ω)
(L1,S1)	17	19	17	21
(L1,S2)	18	10	18	10
(L2,S1)	21	19.5	19	19
(L2,S2)	21	10	18	10

TABLE VII
$L_{g(e)}$, $L_{g(i)}$, L_d, L_s, AND L_{dc} ESTIMATION (NH)

	$L_{g(e)}$	$L_{g(i)}$	L_d	L_s	L_{dc}
(L1,S1)	17	20	8.5	7.98	18.5
(L1,S2)	18	10	10.9	6.73	17.2
(L2,S1)	20	19.25	7.2	8.63	18.9
(L2,S2)	19.5	10	9.9	6.7	18.04

After conducting Test 1 to Test 4, $L_{g(e)}$, $L_{g(i)}$, L_d, L_s, and L_{dc} are estimated and the values are given in Table VII. It can be observed that $L_{g(i)}$, L_d, and L_s are mostly device dependent and has a small influence on PCB layout L1 and L2.

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TABLE VIII
EXPERIMENTAL MEASUREMENT OF C_1 TO C_7 (IN PF)

	C_1	C_2	C_3	C_4	C_5	C_6	C_7
L1	21.35	20.1	70.44	79.48	68.86	1720.2	1729.1
L2	19.42	20.5	76.76	85.96	75.92	1780.4	1791.2

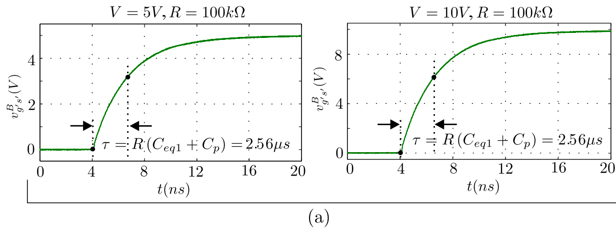

Fig. 21. Experimental results of Test 5.1.

TABLE IX
ESTIMATED PARASITIC CAPACITANCES (IN PF)

	$C^T_{g's'(e)}$	$C^T_{g'd'(e)}$	$C^T_{d's'(e)}$	$C^B_{g's'(e)}$	$C^B_{g'd'(e)}$	$C^B_{d's'(e)}$
L1	14.6	5.5	29.6	16	5.4	19.3
L2	14.8	5.7	33.5	14.7	4.7	22.9

B. Layout Dependent Parasitic Capacitance Measurement

The following tests are conducted to measure the parasitic capacitances (see Test 5.1 to Test 5.7 of Section III). These parasitic capacitances are solely dependent on PCB layout and different for L1 and L2. SMD resistor of $R = 100k\ \Omega$ is used. The use of SMD resistor will reduce the pad to ground parasitic capacitance. Passive voltage probe TPP1000 from Tektronix is used for voltage measurement. The estimated C_p of the measurement setup is ≈ 4 pF. Then using the given technique, values of C_1 to C_7 are estimated (given in Table VIII). Two different values of input step voltage (V) is used (see Fig. 15) and it is observed that the values of the estimated parasitic capacitances remain invariant with applied voltage. Fig. 21 shows one such example where the experimental result of Test 5.1 is given for Layout 1 (L1) for input voltage 5 V and 10 V, respectively. It can be observed that the estimated parasitic capacitance values remain unchanged with the variation in input step voltage.

After obtaining the values of C_1 to C_7, parasitic capacitances are estimated using (31) and the values are given in Table IX for both L1 and L2.

VI. VALIDATION OF PROPOSED PARASITIC ESTIMATION TECHNIQUE WITH DOUBLE PULSE TEST (DPT) AND BEHAVIORAL SIMULATION

After obtaining the circuit parasitics from the experimental measurement, these values are used to simulate the behavioral model. Similarly, double pulse test (DPT) is conducted to capture the hard and soft turn-OFF switching transients of SiC MOSFET in a half-bridge configuration. $v^B_{g's'}(t)$, $v^B_{d's'}(t)$, and $i_{dc}(t)$ waveforms obtained using behavioal simulation and experiment are overlapped over each other for different operating conditions (see Fig. 22). For example, four plots of Fig. 22(a) represent the turn-OFF waveforms for (L1,S1). The first two plots are for hard turn-OFF transient whereas the last two captures the switching dynamics of capacitor assisted soft turn-OFF conditions. The operating conditions are given at the top of each plot. For example, the triplet (800 V,10 A,3.3 Ω) in the first plot of Fig. 22(a) represents $V_{dc} = 800\,\text{V}$, $I_0 = 10\,\text{A}$ and $R_{g(e)} = 3.3\,\Omega$. Similarly, for the third plot of Fig. 22(a), the quadruple (800 V,10 A,3.3 Ω,470 pF) represents $V_{dc} = 800\,\text{V}$, $I_0 = 10\,\text{A}$, $R_{g(e)} = 3.3\,\Omega$ and $C_{ext} = 470\,\text{pF}$.

It can be observed that the experimentally obtained waveforms match closely with the simulated results for most of the operating conditions for both S1 and S2 and layout L1 and L2. The rise and fall slopes of $v^B_{d's'}(t)$ and $i_{dc}(t)$ are closely matched and the oscillations in $i_{dc}(t)$ are predicted with close magnitude and frequency. However, there are some mismatches observed between simulated and experimentally obtained waveforms; especially in $v^B_{g's'}$ and i_{dc} waveforms for some of the operating conditions (for example (800 V, 30 A, 3.3 Ω, 470 pF) for (L1,S2) and (800 V, 30 A, 3.3 Ω, 470 pF) for (L2,S2)). This may be because of the high-frequency resistance provided by the power loop and this effect is not considered in the behavioral model. State variables $v^B_{g's'}$ and i_{dc} are also directly coupled with each other through L_s. So, mismatch in i_{dc} will also reflect in $v^B_{g's'}$ waveform.

Despite slight mismatches between simulation and experimental results, behavioral simulation along with the extracted parasitics can replicate the switching transient fairly well for most of the operating conditions. To compare the accuracy of the behavioral model further, transition time (T_{off}), switching loss (E_{off}), (dv/dt), and transient over voltage (V_{ov}) obtained from experiment and behavioral simulation are compared for different operating conditions (see Table X). It can be observed that the values obtained from the simulation agree with the experimental results fairly well for the entire operating range. This verifies the correctness of the experimentally obtained circuit parasitics.

VII. VALIDATION OF PROPOSED PARASITIC ESTIMATION TECHNIQUE WITH FRA BASED MEASUREMENT

This section validates the circuit parasitic inductance and capacitance values obtained using the proposed technique with the existing FRA based one port measurement. Experimental measurement is adopted for validation purposes as the internal device geometry is unknown and hence, it is not possible to extract some of the parasitic values from theoretical estimation techniques like electromagnetic simulation [4], [5]. Using the impedance analyzer based one port measurement, the device dependent inductances ($L_{g(i)}$, L_d, L_s) and layout dependent parasitic capacitances are validated. Please note, unlike parasitic capacitances, parasitic inductance of small values need to be estimated at higher frequencies and hence, high-frequency measurements are necessary for parasitic inductance estimation. A special connecting fixture targeted for high-frequency measurement is used for the measurement of $L_{g(i)}$, L_d, L_s. On the other hand, L_{dc} and $L_{g(e)}$ are contributed by the PCB layout and circuit components and special connecting fixture cannot be used. Basic cable type connection between impedance analyzer/VNA and PCB may lead to erroneous results at this frequency range. So, it

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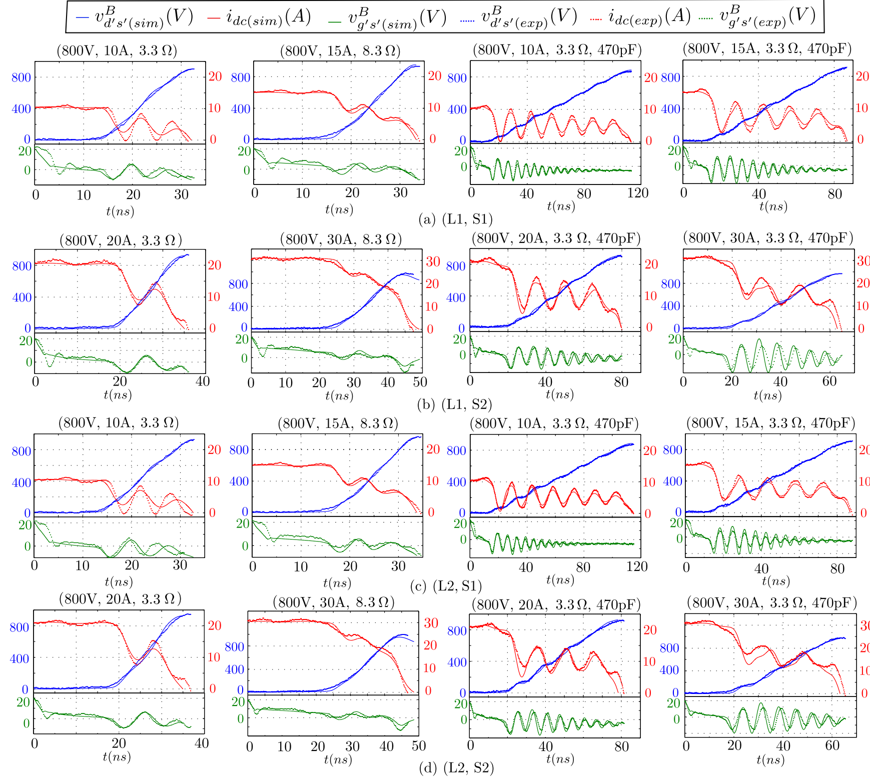

Fig. 22. Simulation versus experimental waveforms.

TABLE X
COMPARISON OF SWITCHING TRANSIENT RELATED QUANTITIES

		T_{off} (ns)		E_{off} (μJ)		(dv/dt) (V/ns)		(di/dt) (A/ns)		V_{ov} (V)	
		Exp	Sim	Exp	Sim	Exp	Sim	Exp	Sim	Exp	Sim
(L1,S1)	[800V,3.5Ω,10A]	31	31.9	32.49	32.56	53.94	52.1	2.21	1.98	896	904
	[800V,8.5Ω,10A]	37.2	35.93	37.24	34.1	49.71	53.23	1.10	1.03	920	900
	[800V,3.5Ω,10A,470pF]	113	113.1	209.28	217.23	9.37	9.30	0.56	0.53	868	884
(L1,S2)	[800V,3.5Ω,20A]	35.8	35.87	73.4	68	60	63	1.46	1.31	920	896
	[800V,8.5Ω,20A]	49.2	49.1	128.12	117	46.22	47.51	2.38	2.1	950	932
	[800V,3.5Ω,20A,470pF]	79.8	79.67	266.14	251.60	16.39	16.3	0.76	0.84	900	916.7
(L2,S1)	[800V,3.5Ω,10A]	31	31.85	32.99	33.93	51.71	53.77	2.25	2.02	900	909
	[800V,8.5Ω,10A]	37.4	36.77	35.64	34.68	48.92	50.92	0.68	0.72	940	910
	[800V,3.5Ω,10A,470pF]	114.8	113.9	218.58	218.83	9.28	9.39	0.62	0.6	872	885.4
(L2,S2)	[800V,3.5Ω,20A]	36.8	36.7	72.2	65.96	60	65.45	1.56	1.57	937	948
	[800V,8.5Ω,20A]	49.4	48.95	128.43	114.80	48.73	46.16	2.3	2.12	992	966
	[800V,3.5Ω,20A,470pF]	81	78.4	279.66	256.33	16.41	16.5	1.84	1.13	920	926.3

is difficult to measure L_{dc} and $L_{g(e)}$ accurately from FRA-based measurement.

The experimental procedure can be divided into two parts: parasitic inductance measurement and layout dependent parasitic capacitance measurement, respectively. Details are given below.

A. Parasitic Inductance Measurement

$$Z_{eq} = \left(\frac{(R_{on} + s(L_d + L_s))}{(L_d + L_s)C_{T(e)}s^2 + R_{on}C_{T(e)}s + 1} + \frac{(R_{on} + s(L_d + L_s))}{(L_d + L_s)C_{B(e)}s^2 + R_{on}C_{B(e)}s + 1} \right). \quad (32)$$

PSM3750 impedance analyzer from Newtons4th along with IAI Kelvin Fixture is used for measurement. To measure the device package related parasitic inductances L_d, L_s, $L_{g(i)}$, one port measurement technique given in [15] is used. Please note, here it is considered that the values of L_d, L_s, and $L_{g(i)}$ are mostly device package dependent and same for both layout 1 (L1) and layout 2 (L2). To describe the measurement process, let us consider a three terminal TO-247 packaged device with terminals g', d', and s' [see Fig. 23(a)]. $L_{g(i)}$, L_d, and L_s are the parasitic inductances of gate, drain, and source terminals, respectively and C_{gs}, C_{gd}, and C_{ds} are the internal parasitic capacitances of the device. C_{gs} is a constant capacitance, whereas C_{gd} and C_{ds} are functions of v_{dg} and v_{ds}, respectively. However, as the amplitude of the voltage excitation is small ($\approx$ 0.5 V peak), C_{gd} and C_{ds} have been approximated as a constant capacitance.

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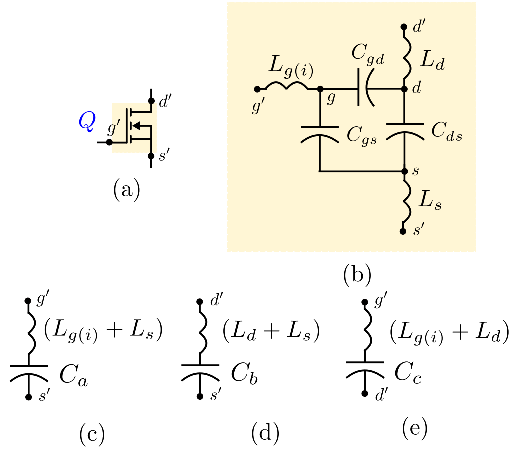

Fig. 23. $L_{g(i)}$, L_d and L_s measurement through FRA: (a) 3 terminal TO-247 packaged device Q, (b) high frequency model of Q, (c) equivalent circuit of Step 1, (d) equivalent circuit of Step 2 and (e) equivalent circuit of Step 3.

Also, $v_{gs} < V_{th}$ and channel of Q is OFF. Hence, it is not shown in Fig. 23(b). Necessary calibrations are performed before measurement. The following steps are followed to estimate the values of $L_{g(i)}$, L_d, and L_s.

- **Step 1** The impedance between g' and s' nodes are measured using an impedance analyzer keeping d' node floating. Then, the equivalent circuit can be a series LC circuit with equivalent inductance $L_a = (L_{g(i)} + L_s)$ and capacitance $C_a = C_{gs} + (C_{gd} \times C_{ds}/(C_{gd} + C_{ds}))$ [see Fig. 23(c)]. Now, experimentally obtained frequency response, values of L_a and C_a can be estimated.
- **Step 2** Similar to Step 1, impedance between g' and d' nodes are measured keeping s' node floating and values of $L_b = (L_{g(i)} + L_d)$ and capacitance $C_b = C_{gd} + (C_{gs} \times C_{ds}/(C_{gs} + C_{ds}))$ are estimated [see Fig. 23(d)].
- **Step 3** Similarly, the impedance between d' and s' nodes are measured keeping g' node floating and values of $L_c = (L_d + L_s)$ and capacitance $C_c = C_{ds} + (C_{gs} \times C_{gd}/(C_{gs} + C_{gd}))$ are estimated [see Fig. 23(e)].

The experiment is carried out for two TO-247 packaged SiC MOSFETs available from wolfspeed; C2M0160120D (S1) and C2M0080120D (S2), respectively. The impedance versus frequency plots for Step 1 to Step 3 are obtained using the equivalent circuits [see Fig. 23(c), (d) and (e)] and experiment are given in Fig. 24 [(a)–(c) for S1 and (d)–(f) for S2]. Small series resistance is considered for each of the equivalent circuits of Step 1 to Step 3 that limits the minimum impedance during resonance.

From the tests, L_a, L_b, and L_c can be estimated and the values can be used to obtain $L_{g(i)}$, L_d, and L_s. The estimated values are compared with the values obtained from the proposed measurement technique and a good match is observed (see Table XI).

B. Layout Dependent Parasitic Capacitance Measurement

Similar to parasitic inductance, layout dependent parasitic capacitances are also measured in LCR meter mode @ 1 MHz (see Table XII). It can be observed that most of the parasitic capacitances can be measured accurately using an impedance analyzer in LCR meter mode.

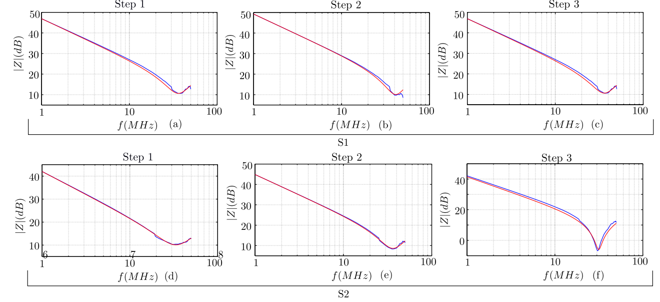

Fig. 24. Experimental results of $L_{g(i)}$, L_d and L_s measurement through FRA.

TABLE XI
COMPARISON OF DEVICE PARASITIC INDUCTANCES (IN NH)

		$L_{g(i)}$	L_d	L_s
(L1,S1)	Prop	20	8.5	7.98
	FRA	18.5	9.5	9.5
(L1,S2)	Prop	10	10.9	6.73
	FRA	10.05	10.95	7.95
(L2,S1)	Prop	19.25	7.2	8.63
	FRA	18.5	9.5	9.5
(L2,S2)	Prop	10	9.9	6.7
	FRA	10.05	10.95	7.95

TABLE XII
COMPARISON OF ESTIMATED PARASITIC CAPACITANCES (IN PF)

		$C^T_{g'd'(e)}$	$C^T_{d's'(e)}$	$C^B_{g'd'(e)}$	$C^B_{d's'(e)}$
L1	Prop	5.5	29.6	5.4	19.3
	FRA	4.9	29.3	6.3	25.9
L2	Prop	5.7	33.5	4.7	22.9
	FRA	6.1	36.9	5.7	16.3

From the above results, it can be concluded that the proposed parasitic measurement techniques accurately measure the values of parasitic inductance ($L_{g(i)}$, L_d and L_s) and layout dependent parasitic capacitances involved in the switching transient study of SiC MOSFET.

VIII. CONCLUSION

Accurate measurement of circuit parasitic is important for optimal design of a SiC MOSFET in a half-bridge pair. This article presents a set of experimental techniques to measure the parasitic inductance and capacitances involved in switching transient of SiC MOSFET in a half-bridge configuration. Values of circuit parasitic inductances (gate, drain, common-source, and power loop) and capacitances (gate-drain and drain-source) are measured. Two 1.2-kV SiC MOSFETs of different current ratings and two different PCB layouts are used to validate the proposed method. Measured circuit parasitic when used in switching transient model, correctly predicted both hard turn off and capacitor assisted soft turn-OFF switching dynamics over a wide range of operating conditions. Also, the proposed parasitic measurement technique is validated using FRA based one port

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measurement. It was observed that the values of gate, drain, and common-source inductances and parasitic capacitances obtained through two different techniques matched closely.

APPENDIX

A. Calculation of Z_{eq} for Test 1

The total impedance across d'_T and s'_B of the circuit [see Fig. 4(b)] is represented as Z_{eq} and given by (32) where $C_{T(e)} = (C^T_{g'd'(e)} + C^T_{d's'(e)})$ and $C_{B(e)} = (C^B_{g'd'(e)} + C^B_{d's'(e)})$. For all practical purposes, values of $\sqrt{1/((L_d + L_s)C_{T(e)})}$ and $\sqrt{1/((L_d + L_s)C_{B(e)})} \gg (R_{on}/(L_d + L_s))$. Also, $(R_{on}/2)\sqrt{C_{T(e)}/(L_d + L_s)}$ and $(R_{on}/2)\sqrt{C_{B(e)}/(L_d + L_s)} \ll 1$ results in complex conjugate poles located close to $\sqrt{1/((L_d + L_s)C_{T(e)})}$ and $\sqrt{1/((L_d + L_s)C_{B(e)})}$. So, to capture the average variation of i_{dc}, Z_{eq} can be approximated as (5).

As an example, SiC MOSFET C2M0080120D is considered along with the parameters of Layout 2 (L2). Parameters are $R_{on} = 0.08\ \Omega$, $L_d = 10.9$ nH, $L_s = 6.73$ nH, $C^T_{g'd'(e)} = 5.5$ pF, $C^T_{d's'(e)} = 29.6$ pF, $C^B_{g'd'(e)} = 5.4$ pF, $C^B_{d's'(e)} = 19.6$ pF. $\sqrt{1/((L_d + L_s)C_{T(e)})} = 35.5 \times 10^9$ rad/s, $\sqrt{1/((L_d + L_s)C_{B(e)})} = 47.92 \times 10^9$ rad/s and $(R_{on}/(L_d + L_s)) = 4.54 \times 10^6$ rad/s. Also, $(R_{on}/2)\sqrt{C_{T(e)}/(L_d + L_s)} = 6.4 \times 10^{-5}$, and $(R_{on}/2)\sqrt{C_{B(e)}/(L_d + L_s)} = 4.74 \times 10^{-5}$.

REFERENCES

[1] M. R. Ahmed, R. Todd, and A. J. Forsyth, "Predicting SiC mosfet behavior under hard-switching, soft-switching, and false turn-on conditions," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9001–9011, Nov. 2017.

[2] N. Oswald, P. Anthony, N. McNeill, and B. H. Stark, "An experimental investigation of the tradeoff between switching losses and EMI generation with hard-switched all-Si, Si-SiC, and all-SiC device combinations," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2393–2407, May 2014.

[3] S. K. Roy and K. Basu, "Analytical estimation of turn on switching loss of SiC mosfet and Schottky Diode pair from datasheet parameters," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 9118–9130, Sep. 2019.

[4] R. S. Krishna Moorthy *et al.*, "Estimation, minimization, and validation of commutation loop inductance for a 135-kW SiC EV traction inverter," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 286–297, Mar. 2020.

[5] Z. Liu, X. Huang, F. C. Lee, and Q. Li, "Package parasitic inductance extraction and simulation model development for the high-voltage cascode GaN HEMT," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1977–1985, Apr. 2014.

[6] W. Teulings, J. Schanen, and J. Roudet, "mosfet switching behaviour under influence of PCB stray inductance," in *Proc. Conf. Rec. IEEE Ind. Appl. Conf. 31st IAS Annu. Meeting*, vol. 3, 1996, pp. 1449–1453.

[7] M. Caponet, F. Profumo, R. De Doncker, and A. Tenconi, "Low stray inductance bus bar design and construction for good EMC performance in power electronic circuits," *IEEE Trans. Power Electron.*, vol. 17, no. 2, pp. 225–231, Mar. 2002.

[8] s.k. roy and K. Basu, "Analytical model to study hard turn off switching dynamics of SiC MOSFET and Schottky Diode pair," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 861–875, Jan. 2021.

[9] Y. Wu, S. Yin, H. Li, and W. Ma, "Impact of *RC* snubber on switching oscillation damping of SiC MOSFET with analytical model," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 163–178, Mar. 2020.

[10] S. K. Roy and K. Basu, "Measurement of important circuit parasitics for switching transient analysis of SiC MOSFET and Schottky Diode pair," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2019, pp. 1948–1952.

[11] "Probing techniques for accurate voltage measurements on power supplies with oscilloscopes," Jun. 2019. [Online]. Available: https://www.tek.com/en/documents/application-note/probing-techniques-accurate-voltage-measurements-power-converters-oscillos

[12] P. Nayak and K. Hatua, "Parasitic inductance and capacitance-assisted active gate driving technique to minimize switching loss of SiC MOSFET," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8288–8298, Oct. 2017.

[13] H. Zhu, A. R. Hefner, and J.-S. Lai, "Characterization of power electronics system interconnect parasitics using time domain reflectometry," *IEEE Trans. Power Electron.*, vol. 14, no. 4, pp. 622–628, Jul. 1999.

[14] T. Liu, T. T. Wong, and Z. J. Shen, "A new characterization technique for extracting parasitic inductances of SiC power MOSFETS in discrete and module packages based on two-port S-parameters measurement," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9819–9833, Nov. 2018.

[15] T. Liu, R. Ning, T. T. Y. Wong, and Z. J. Shen, "Equivalent circuit models and model validation of SiC MOSFET oscillation phenomenon," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–8.

[16] L. Yang and W. G. H. Odendaal, "Measurement-based method to characterize parasitic parameters of the integrated power electronics modules," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 54–62, Jan. 2007.

[17] A. N. Lemmon and R. C. Graves, "Comprehensive characterization of 10-kV silicon carbide half-bridge modules," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 4, pp. 1462–1473, Dec. 2016.

[18] K. Mitsui and K. Wada, "Design of a laminated bus bar optimizing the surge voltage, damped oscillation, and switching loss," *IEEE Trans. Ind. Appl.*, vol. 57, no. 3, pp. 2737–2745, May/Jun. 2021.

[19] K. Umetani, K. Aikawa, and E. Hiraki, "Straightforward measurement method of common source inductance for fast switching semiconductor devices mounted on board," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8258–8267, Oct. 2017.

[20] M. Trivedi and K. Shenai, "Parasitic extraction methodology for insulated gate bipolar transistors," *IEEE Trans. Power Electron.*, vol. 15, no. 4, pp. 799–804, Jul. 2000.

[21] S. Hu, M. Wang, Z. Liang, and X. He, "A frequency-based stray parameter extraction method based on oscillation in SiC MOSFET dynamics," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6153–6157, Jun. 2021.

[22] S. k. Roy and K. Basu, "Analytical model to study turn off soft switching dynamics of SiC MOSFET in a half-bridge configuration," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 13039–13056, Nov. 2021.

[23] D. N. Dalal *et al.*, "Impact of power module parasitic capacitances on medium-voltage SiC MOSFETS switching transients," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 298–310, Mar. 2020.

[24] M. Mudholkar, S. Ahmed, M. N. Ericson, S. S. Frank, C. L. Britton, and H. A. Mantooth, "Datasheet driven silicon carbide power MOSFET model," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2220–2228, May 2014.

[25] A. Marzoughi, J. Wang, R. Burgos, and D. Boroyevich, "Characterization and evaluation of the state-of-the-art 3.3-kV 400-A SiC MOSFETS," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8247–8257, Oct. 2017.

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