Analytical Model to Study Turn off Soft Switching Dynamics of SiC MOSFET in a Half-Bridge Configuration

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***Abstract*—Switching transients of SiC MOSFET is fast compared to its Si counterpart. Fast switching transient reduces switching loss but may induce prolonged oscillations, spurious turn on, high device stress and EMI related issues etc. In soft switched converters, use of external drain source capacitance can reduce these adverse effects along with the reduction in switching loss. However, the selection of external drain source capacitance is not straightforward. A large external capacitance reduces switching loss, (dv/dt), (di/dt) and transient over-voltage but may also result in higher dead-time loss and reduced switching frequency. This paper presents an analytical model that captures the soft turn off switching dynamics of SiC MOSFET using parameters obtained from device datasheet along with the values of external circuit parasitics. Unlike linear approximation, a non-linear channel current model is used along with a comprehensive model of transfer capacitance. The effect of external gate drain capacitance is also considered. This leads to a better estimation of switching transition time, actual loss, (dv/dt), (di/dt) and transient over-voltage. Also, a method to select an optimal value of external drain source capacitance is presented. The proposed model is validated through behavioural simulation and experiment for two 1.2kV discrete SiC MOSFETs.**

***Index Terms*—Soft switching, Turn off, dead-time, Double pulse test, Modelling, SiC MOSFET, ZVS, EMI**

NOMENCLATURE

V_{th}	Threshold voltage
K_p	Saturation region transconductance
K_f	Ohmic region transconductance factor
θ	Transverse electric field parameter
P_{vf}	Pinch-off voltage parameter
R_{gint}	Internal gate resistance of SiC MOSFET
R_{gext}	External gate resistance
$R_{g(driver)}$	Gate driver internal resistance
V_{GG},V_{EE}	Positive and negative gate supply voltage
T_f	Fall time of gate supply voltage
v_{gs},v_{ds},v_{dg}	Gate source, drain source and drain gate voltage of SiC MOSFET
C_{gs},C_{ds},C_{gd}	Gate source, drain source and gate drain capacitance of SiC MOSFET
C_{oxd}	Gate source part of oxide capacitance of SiC MOSFET

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I. INTRODUCTION

Superior switching, conduction and thermal performance of SiC MOSFET enable designers to increase the switching frequency of SiC MOSFET-based hard switched converters by 5-10 times compared to state of the art Si IGBTs based converters (5-10kHz $\rightarrow$ 50-100kHz) [1]. To further increase the switching frequency, zero voltage switching (ZVS) topologies are used [2]. Turn on switching loss is negligible in ZVS topologies and total switching loss is primarily contributed by the turn off loss [3], [4]. It is well established in the literature that the hard turn off switching loss of SiC MOSFET is small compared to the turn on loss [5]. However, for high values of load current and high switching frequency, hard turn off loss can be significant [6].

Small gate resistance will lead to fast switching transient and reduced turn off switching loss. However, the value of minimum gate resistance is limited by the internal gate resistance of the SiC MOSFET, the gate driver peak current rating and the damping of the gate circuit. Also, fast switching transient of SiC MOSFET excites circuit parasitics that can lead to sustained oscillation, high transient over-voltage, spurious turn on, EMI related issues etc. [7]–[9]. In order to achieve both the objectives of reduced switching transient and lower turn off switching loss, capacitor-assisted zero voltage turn off or soft switching turn off of SiC MOSFETs in a half-bridge pair is considered [10], [11].

Addition of external drain source capacitance results in reduced transition rates but prolongs the switching transition. This may lead to larger dead-time to avoid premature turn on of the complementary device and subsequent reduction in switching frequency. For DC-DC or DC-AC converters that experience variable load current, dead-time needs to be set for a lower load current value to avoid premature turn on. It is noteworthy that the body diode of the complementary device conducts for a fraction of dead-time and the forward drop of the body diode of SiC MOSFET is higher if compared to Si diode [12]. So for a fixed and relatively large dead-time, the conduction loss in the complementary device may be significant when the load current is high. This is called dead-time loss and it increases linearly with switching frequency. So the selection of an optimal value of external drain source capacitor is important.

Switching transient study is broadly classified into two categories: simulation and experiment. Experimental approaches like double pulse test (DPT) is inaccurate as it is not possible

to experimentally determine the switching loss through measurement due to the presence of device and circuit parasitics [13], [14]. Also, the measurement of device voltage and current is challenging as the probe introduces parasitic in the power and gate loops [15]. Calorimetric measurement is another experimental approach [3], [16]. However, it requires different circuit configuration alongwith a specially designed and calibrated thermal set-up [16]. Typically, these set-ups are not available in a regular converter development laboratory. In general, experimental measurements may be erroneous and the experimental set-ups are not available in the early stages of converter design.

Physics based model [17], [18] and behavioural model [19], [20] are both simulation based approaches. Physics based model is accurate but requires sophisticated software, longer simulation time and values of internal device parameters those can not be extracted easily from the device datasheet. The behavioural model is another simulation based approach and it can also capture the switching transients with sufficient accuracy [19], [20]. However, it is challenging to simulate the behavioural model in circuit simulators like MATLAB/Simulink® due to nonlinearity of the device characteristics, and it often suffers from the convergence problem [21]. The device manufacturers provide *Spice* based behavioural models. However, it is not possible to verify the soft switching criteria and obtain actual switching loss due to the inaccessibility of internal device variables (e.g. channel current). Also, the behavioural simulation does not provide insight into the switching process and applying it for a large number of operating points is time-consuming.

Analytical modelling approach is derived from the behavioural model through approximations. This approach provides insight into the switching process and overcomes most of the shortcoming of previously stated models. Analyical models are fast compared to behavioural model and provides results accurate enough for the early stages of power electronic converter design. Moreover, it can be coded in open-source software like C, Python etc. Analytical model for Si MOSFET [7] is not applicable for SiC MOSFET due to difference in device characteristics [22], [23]. Also, the impact of external circuit parasitic is significant for SiC MOSFET due to fast switching transient [24]. Analytical model for hard switching dynamics of SiC MOSFET has been proposed in [14], [24]–[26] but this study is not directly applicable for capacitor assisted soft turn off switching dynamics. Analytical modelling approach to study soft turn off switching dynamics of SiC MOSFET has been adopted in a number of earlier works [6], [8], [27].

Among these works, no external drain source capacitance is considered in [27]. The external drain source capacitance in soft switched converters can significantly reduce turn off switching loss, transition rates and transient over-voltage (case study is provided in Appendix). [6], [8] considers the external drain source capacitance in the analysis. However, these models are not accurate enough to study different aspects of soft turn-off switching transient and optimal external drain source capacitance design. Section II presents the limitations of the models given in [6], [8] on the mode by mode basis.

This paper presents an improved analytical model to study the soft turn off switching dynamics of SiC MOSFET in presence of an externally inserted capacitor. It is based on the behavioural model given in [24]. The proposed model overcomes most of the limitations of [6], [8] and results in an accurate estimation of transition time, actual loss, (dv/dt), (di/dt) and transient over-voltage for a given operating condition, device and external circuit parasitics along with the external drain source capacitance. It is also used to estimate the minimum external capacitance necessary to achieve soft switching at a given operating point. Also, a method to select an optimal external drain source capacitance is proposed that ensures soft switching over a given range of operating conditions and limits the maximum turn-off voltage slope. It also helps to estimate worst case switching loss and design dead-time. Simulation of behavioural model, along with experimental results verify the accuracy of the proposed model. A new mode termed as "Channel current collapse" is observed in addition to these three distinct modes (delay, voltage rise and current fall) seen in hard turn off of SiC MOSFET [24].

This paper is arranged in the following order. A mode by mode comparison of the proposed model with the existing models is given in Section II. In Section III, details of behavioural model to study turn off switching transient of SiC MOSFET is discussed. The proposed analytical model to study soft turn off switching dynamics of SiC MOSFET is given in Section IV. Details of the experimental set-up are provided in Section V and simulation and experimental results have been given in section VI. A method to select the optimal value of external drain source capacitance is discussed in Section VII. Finally, Section VIII draws the conclusion.

II. Prior Art

This section presents mode by mode details of the analytical approaches present in existing literature for the turn-off dynamics of SiC MOSFET along with their shortcomings and the improvements done by the present work.

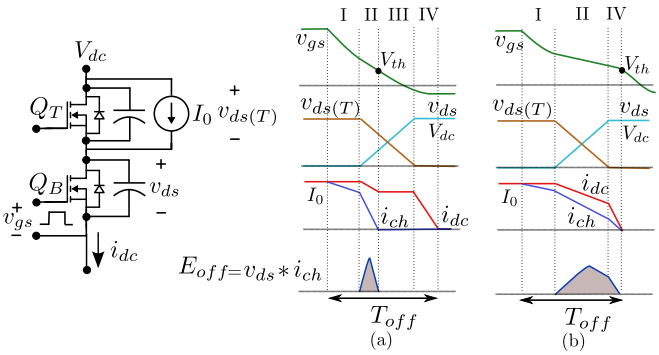

Fig. 1: Piecewise linear turn off transition waveforms: (a) Soft switched, (b) Hard switched

To understand the turn off transient, a half-bridge configuration is considered with devices Q_T and Q_B. Input is connected to a DC voltage source V_{dc} and output load is ideal current sink I_0 (Fig. 1). Illustrative waveforms of soft and hard turn off switching transients are shown in Fig. 1(a) and Fig. 1(b) respectively. During the turn off switching transition, Q_B is

TABLE I: Mode-wise discussion on existing literature

Mode	References	Assumptions	Limitations
Delay	[6], [8]	• Channel current is fixed to load current. • Drain-source voltage is clamped to a small on-state drop. • A constant gate-drain capacitance is considered corresponding to a small on-state drain source voltage. • A step change in gate supply voltage results in a exponential fall of gate-source voltage.	• Channel current may fall significantly below load current. • Consideration of drain-source voltage remaining constant leads to inconsistency at the boundary of ohmic-saturation region. • As the drain-gate voltage is negative for a significant portion of the delay period, the gate-drain capacitance is much higher than the value used in existing analysis and results in incorrect estimation of delay time.
Channel current collapse	[6]	• Dynamics of this mode has not been analyzed. • External drain source capacitance is directly connected across the drain source terminal of the SiC MOSFET (see Fig. 2(a)).	• Most of the switching loss occurs in this mode and it can not be estimated using this analytical model. • Results in inaccurate estimation of minimum external capacitance for soft switching and actual loss.
	[8]	• In this mode, SiC MOSFET is in saturation region and channel is modelled as a linear function of gate-source voltage. • Coupled dynamics of gate and power circuit is considered.	• Channel current of SiC MOSFET in saturation is highly non-linear function of gate-source voltage. Consideration of linear channel current approximation will underestimate the switching loss. • The external gate drain capacitance contributed by PCB layout, slows down the rate of fall of channel current.
Voltage rise	[6]	• Current through the output capacitance of the SiC MOSFET is assumed to be constant. • The voltage rise time is calculated by dividing the charge stored in output capacitance by average current flowing through it.	• Current through the output capacitance of SiC MOSFET is not constant during voltage rise period and results in inaccurate estimation of voltage rise time and (dv/dt).
	[8]	• Fully coupled dynamics of gate and power circuit is considered without any approximation.	• During this mode, the impact of gate circuit is minimal and simplified expression of voltage rise time and (dv/dt) can be obtained.
Drain current fall	[6]	• This mode has not been solved in this model.	• Time period of this mode, (di/dt) and transient over-voltage can not be estimated
	[8]	• Fully coupled dynamics of gate and power circuit is considered without any approximation.	• Similar to voltage rise, the impact of gate circuit is minimal and simplified expression of current fall time, (di/dt) and transient over-voltage can be obtained.

TABLE II: Mode wise improvements done by the proposed analytical model

Mode	Improvements
Delay	• Coupled dynamics of gate and power circuit is considered. • A comprehensive channel current model is used that captures a gradual transition from ohmic to saturation region and the transverse electric field effect in SiC MOSFETs [22], [23]. • A detailed model of the transfer capacitance, appropriate for SiC MOSFETs [28], is used.
Channel current collapse	• A better channel current model, modified square law [22], [23], is used. • The external drain source capacitance is connected after the lead inductance (see Fig. 2(b)). • The effect of external parasitic gate drain capacitance is considered here which has a significant impact in this mode [7]. • A reduced order model compared to [8] with better accuracy is presented.
Voltage rise	• A simple closed form expression of voltage rise time and (dv/dt) is provided.
Drain current fall	• Similar to voltage rise, simplified closed form expression of time duration, (di/dt) and transient over-voltage is provided.

turning off and load current I_0 is commuting from Q_B to the body diode of Q_T. v_{gs}, v_{ds} are gate-source and drain-source voltage of Q_B and i_{dc} and i_{ch} are the DC bus current and channel current of Q_B. $v_{ds(T)}$ represents the drain-source voltage of Q_T. In Fig. 1(a), $i_{ch}(t)$ collapses to zero before $v_{ds(T)}$ reaches zero value whereas in Fig. 1(b), $v_{ds(T)}$ reaches zero value before i_{ch}. The first scenario (see Fig. 1(a)) is defined as soft turn off and the later one (Fig. 1(b)) is defined as hard turn off. It can be observed that unlike hard turn off which has three different modes (delay, voltage rise and current fall), soft turn off has four different modes: Mode I to Mode IV respectively.

Mode I (Delay): After gate supply is turned off, v_{gs} reduces and MOSFET remains in ohmic region. This mode ends when the MOSFET enters into the saturation region.

Mode II (Channel current collapse): This mode starts when the MOSFET enters into the saturation region and ends when i_{ch} collapses to zero.

Mode III (Voltage rise): This mode starts when i_{ch} collapses to zero and ends when the free-wheeling diode of Q_T gets forward biased.

Mode IV (Drain current fall): Drain current fall period starts after the free-wheeling diode of Q_T gets forward biased and ends when i_{dc} reaches zero.

The assumptions made by [6], [8] and resulting limitations in mode by mode basis are summarised in Table I. The proposed analytical model aims to overcome the shortcomings of the existing models to provide a better estimate of turn off transition time, switching loss, (dv/dt), (di/dt) and transient over-voltage. The improvements done by the proposed analytical model is given in Table II on the mode by mode basis.

III. Behavioural Model

To analyse the soft turn off switching dynamics of SiC MOSFET, a half bridge configuration is considered (Fig. 3(a))

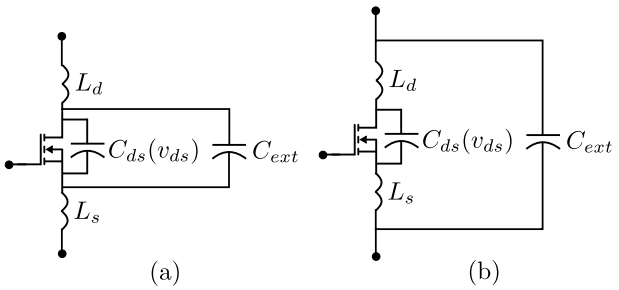

Fig. 2: Equivalent circuit model for behavioural model: (a) model given in the [6], (b) model used in this work

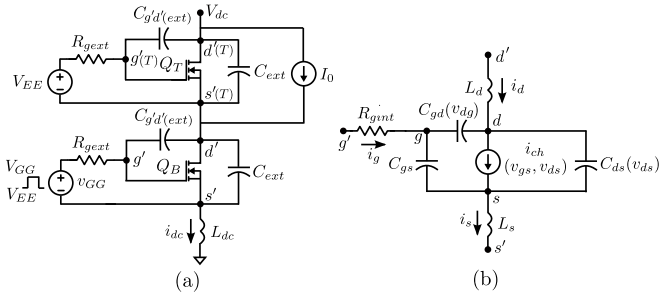

Fig. 3: Circuit configuration for soft turn off switching transient analysis: (a) Half bridge configuration, (b) Equivalent circuit model of SiC MOSFET

where Q_T and Q_B both are SiC MOSFET. Q_B is the active device and Q_T is used as synchronous MOSFET. Input is connected to an ideal DC voltage source V_{dc} and the output inductive load is modelled as a current sink I_0. SiC MOSFET is modelled as a three terminal device with external terminals gate (g'), drain (d') and source (s'). C_{ext} is the external capacitance connected directly across the d' and s' nodes of both the MOSFETs. v_{GG} is the applied gate driver voltage, which has two levels, V_{GG} and V_{EE} respectively. When the gate signal is removed, v_{GG} changes from V_{GG} to V_{EE} with a fall time T_f. R_{gext} is the total external gate resistance, which is the summation of the gate driver's internal resistance and external gate resistance.

The equivalent circuit model or behavioural model of the SiC power MOSFET is shown in Fig. 3(b). R_{gint} is the internal gate resistance of the MOSFET. Channel current $i_{ch} = 0$ for $v_{gs} < V_{th}$ (Cut-off). For $v_{ds} < (v_{gs} - V_{th})/P_{vf}$ and $v_{gs} > V_{th}$ (ohmic), i_{ch} is modelled as (1). For $v_{ds} > (v_{gs} - V_{th})/P_{vf}$ and $v_{gs} > V_{th}$ (saturation), i_{ch} is modelled as (2). Note, the resistive drop of the drift region needs to be subtracted from the drain source voltage of the output characteristics given in the datasheet before curve fitting. All the parameters are temperature dependent and have been extracted for the data given at 25^oC.

$$i_{ch}(v_{gs}, v_{ds}) \approx \frac{K_p K_f \left((v_{gs} - V_{th})\, v_{ds} - \left(\frac{P_{vf}^{y-1}}{y} \right) (v_{gs} - V_{th})^{2-y}\, v_{ds}^{y} \right)}{(1 + \theta(v_{gs} - V_{th}))} \quad (1)$$

$$i_{ch}(v_{gs}) \approx \frac{K_p\, (v_{gs} - V_{th})^2}{2(1 + \theta(v_{gs} - V_{th}))} \quad (2)$$

C_{gs} is modelled as a constant capacitance whereas C_{gd} and C_{ds} both are non-linear functions of v_{dg} (3) and v_{ds} (4) respectively.

$$C_{gd}(v_{dg}) = \begin{cases} C_{oxd} = \dfrac{k_1}{k_3}, & -\infty < v_{dg} < 0 \\ \dfrac{k_1}{\left(1 + \dfrac{v_{dg}}{k_2}\right)^{1/2} + k_3}, & 0 \le v_{dg} < V_{td} \\ \dfrac{k_4}{\left(1 + \dfrac{v_{dg} - V_{td}}{k_5}\right)^{1/4}}, & V_{td} \le v_{dg} < \infty \end{cases} \quad (3)$$

$$C_{ds}(v_{ds}) = \frac{k_6}{\left(1 + \dfrac{v_{ds}}{k_7}\right)^{1/2}} \quad (4)$$

The top MOSFET is modelled as a non linear voltage dependant capacitor C_{oss} in the reverse biased condition and it is a function of drain source voltage $v_{ds(T)}$ of Q_T (5). When the body diode of the top MOSFET gets forward biased, it is modelled as an ideal diode with zero voltage drop ($v_{ds(T)} \approx 0$) across it. k_8 and k_9 can be obtained using (5) through curve fitting. Details of device modelling is provided in [24].

$$C_{oss}(v_{ds(T)}) = \frac{k_8}{\left(1 + \dfrac{v_{ds(T)}}{k_9}\right)^{1/2}} \quad (5)$$

Due to the fast switching transition, external circuit parasitics play a significant role in switching dynamics. External circuit parasitics are L_d, L_s, L_{dc} and $C_{g'd'(ext)}$ (see Table III). L_d and L_s are mainly contributed by the wire-bond and lead inductance of drain and source terminals of the MOSFET respectively and considered to be same for both Q_T and Q_B. This model will be still valid if the inductances for Q_T and Q_B are different. L_{dc} is the summation of the DC bus inductance and the connection inductance between the MOSFETs. L_s is the parasitic inductance common to both gate and power circuit loop whereas L_d and L_{dc} are part of only power circuit loop. $C_{g'd'(ext)}$ is the external parasitic capacitance between g', d' nodes. Circuit parasitic values get impacted due to both device package as well as PCB layout.

TABLE III: External circuit Parasitics

L_{dc}	Power loop inductance
L_d	Drain inductance of SiC MOSFET
L_s	Common source inductance of SiC MOSFET
$C_{g'd'(ext)}$	Gate- drain parasitic capacitance

Simulated waveforms using behavioural model are plotted for SiC MOSFET C2M0080120D from Wolfspeed in Fig. 4(a) and 4(b) for parameters $(V_{dc}, I_0, R_{gext}, C_{ext})$ equal to $(800V, 20A, 2.5\Omega, 470pF)$ and $(800V, 20A, 8.5\Omega, 100pF)$ respectively. Device and the external circuit related parameters used for simulation are listed in the experimental set-up section. Extracted waveforms from the simulation are v_{gs}, v_{ds}, $v_{ds(T)}$, i_d, i_{dc} and i_{ch}. Time evolution of gate source $v_{gs}(t)$ and internal drain source voltage $v_{ds}(t)$ along with

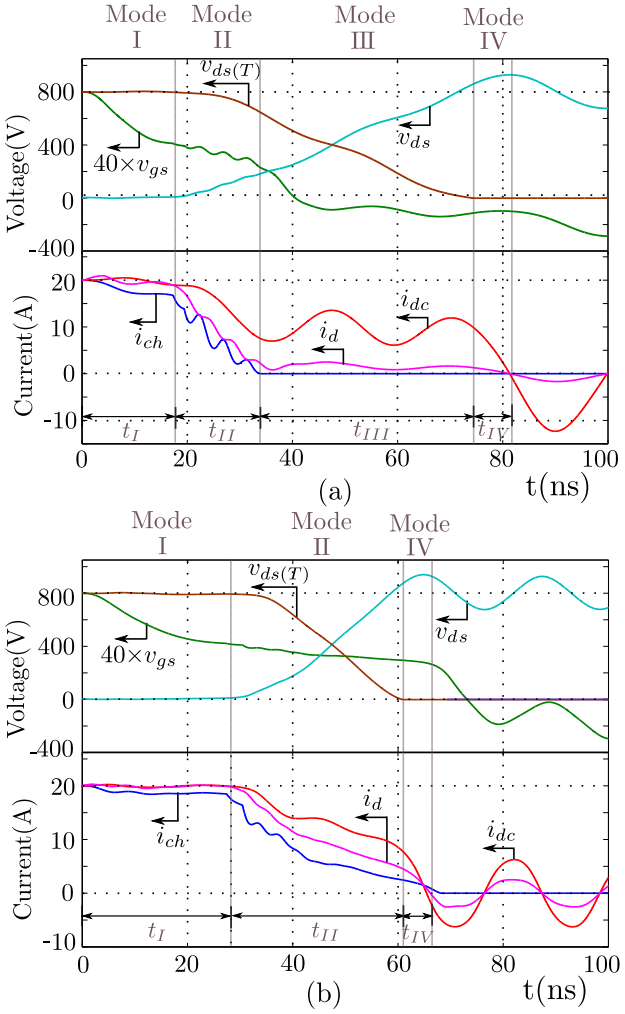

Fig. 4: Simulation waveforms of C2M0080120D: (a) Soft switched, (b) Hard switched

the channel current $i_{ch}(t)$ during switching transitions are important for the study of switching dynamics and switching loss estimation. Due to the presence of L_d, L_s, R_{gint}, C_{ext} and device parasitic capacitances, it is not possible to measure these waveforms experimentally. The measurable waveforms are $v_{g's'}(t)$, $v_{d's'}(t)$ and $i_{dc}(t)$ (Fig. 3). Actual switching loss in the MOSFET is given by (6) and the measured loss is given by (7), where T_{off} is the turn off switching transition time. It can be observed from Fig. 4(a) that i_{ch} collapses to zero before $v_{ds(T)}$ whereas $v_{ds(T)}$ reaches zero before i_{ch} in Fig. 4(b). It is self evident that the actual switching loss for the first case is small compared to the second case. *In this paper, the turn off switching transition is considered to be soft switched when i_{ch} collapses to zero before $v_{ds(T)}$*. Using this definition, turn off switching transient of Fig. 4(a) is soft switched whereas switching transient of Fig. 4(b) is hard switched.

$$E_{off} = \int_0^{T_{off}} v_{ds}(\tau) i_{ch}(\tau)\, d\tau \tag{6}$$

$$E'_{off} = \int_0^{T_{off}} v_{d's'}(\tau) i_{dc}(\tau)\, d\tau \tag{7}$$

IV. Analytical Model and Estimation of Minimum External Capacitor for Soft Switching

At first, an analytical model to study the soft turn off switching dynamics of SiC MOSFET is proposed. Then this analytical model is used to estimate the minimum external drain source capacitance ($C_{ext(min)}$) required to meet the soft switching condition for a given operating condition.

A. Analytical model

The objective of this section is to analyse the turn off soft switching dynamics of SiC MOSFET and accurately estimate transition time (T_{off}), actual switching loss (E_{off}), $(dv/dt)_{off}$ and $(di/dt)_{off}$ rates and transient over-voltage ($V_{ds(max)}$) for a given operating condition (V_{dc}, I_0), gate driver parameters (V_{EE}, V_{GG}, R_{gext}), datasheet related parameters of the devices (V_{th}, K_p, K_f, θ, R_{gint}, C_{gs}, $C_{gd}(v_{dg})$, $C_{ds}(v_{ds})$, $C_{oss}(v_{ds(T)})$) and the value of external capacitor C_{ext}. High value of C_{ext} helps in reducing $(dv/dt)_{off}$, $(di/dt)_{off}$ rates and E_{off} but T_{off} increases. This may lead to the larger dead-time selection, higher dead-time loss and a compromise on switching frequency. So the selection of optimum C_{ext} is important that keep a balance between the achievable $(dv/dt)_{off}$, $(di/dt)_{off}$ rate, T_{off} and E_{off}. The external circuit parasitics (L_{dc}, L_d, L_s and $C_{g'd'(ext)}$) can be approximately estimated from package information and electromagnetic simulation [20] or experimental measurements [29]. T_f is neglected to reduce the complexity of the analysis and a step voltage change of v_{GG} is considered.

Soft switching turn off transient of SiC MOSFET can be broadly divided into four modes: 1) Mode I (Delay period), 2) Mode II (Current collapse period), 3) Mode III (Voltage rise period) and 4) Mode IV (Ringing period) (Fig. 4). t_I, t_{II}, t_{III} and t_{IV} are the time period of Mode I to Mode IV respectively.

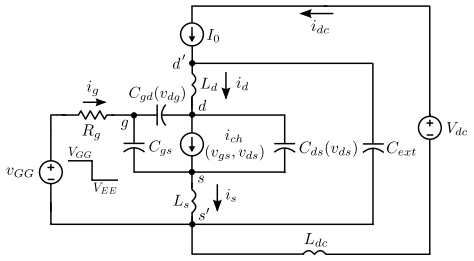

Fig. 5: Equivalent circuits of Mode I

1) Mode I (delay period): At the start of Mode I (delay period), v_{gs} is equal to V_{GG} and the full load current I_0 is flowing through the SiC MOSFET, so $i_{dc} = i_d = i_s = I_0$ (Fig. 3). Q_B is in ohmic region and $v_{ds} = V_{ds(on)} \approx I_0 R_{on}$, where R_{on} is the on-state resistance of the SiC MOSFET. Q_T is in cut off region and it is blocking voltage $v_{ds(T)} \approx (V_{dc} - I_0 R_{on})$. When the gate is turned off, the gate driver voltage v_{GG} will change from V_{GG} to V_{EE} (see Fig. 5).

The primary assumption of this mode is $i_{dc} \approx I_0$. This approximation holds good because of the change in $v_{d's'}$ during Mode I is small and the presence of comparatively large inductance in power loop (L_{dc}) restricts the change in

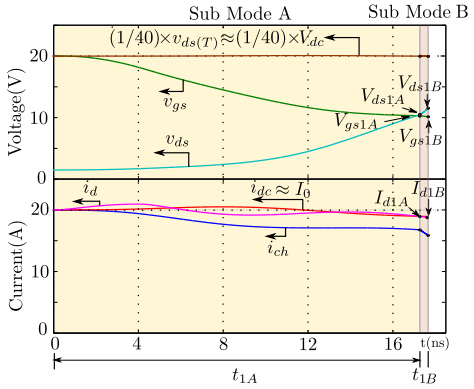

Fig. 6: Simulation waveforms of Mode I

power circuit state variables (i_{dc} and $v_{d's'(T)}$). So i_{dc} and $v_{d's'(T)}$ remain almost constant to their initial values (see Fig. 6). For the entire Mode I, Q_B is in ohmic region, so i_{ch} is a function of both v_{gs} and v_{ds}, (1). As v_{dg} is small during this mode, $C_{gd}(v_{gd})$ is large compared to the external parasitic capacitances $C_{g'd'(ext)}$ and its effect can be neglected. Fig. 5 represents the equivalent circuit of this mode where $R_g = (R_{gext} + R_{gint})$. Mode I is divided into two sub modes, a) Sub Mode A and b) Sub Mode B respectively (see Fig. 6).

a) ***Sub Mode A****:* During Sub Mode A, v_{GG} changes from V_{GG} to V_{EE} instantaneously. KCL at g, d and d' node of Fig. 5 gives (8) (9), (10) respectively. Applying KVL in the gate loop, we get (11). KVL in the loop formed by node g, d, s and d', d, s, s' gives (12) and (13) respectively. During this sub mode $v_{dg} < 0$, so $C_{gd}(v_{dg}) = C_{oxd}$, (3). Applying KCL at node s' and using (10), we get (14). As $(di_g/dt) \ll (di_d/dt)$ except for the small initial period, so $(di_s/dt) \approx (di_d/dt)$.

$$i_g = C_{gs}\frac{dv_{gs}}{dt} + C_{gd}(v_{gd})\frac{dv_{gd}}{dt} \tag{8}$$

$$(i_d - i_{ch}) = C_{gd}(v_{dg})\frac{dv_{dg}}{dt} + C_{ds}(v_{ds})\frac{dv_{ds}}{dt} \tag{9}$$

$$I_0 = i_d + C_{ext}\frac{dv_{d's'}}{dt} \tag{10}$$

$$V_{EE} = R_g i_g + v_{gs} + L_s\frac{di_s}{dt} \tag{11}$$

$$v_{gs} = v_{gd} + v_{ds} \tag{12}$$

$$v_{d's'} = v_{ds} + L_d\frac{di_d}{dt} + L_s\frac{di_s}{dt} \tag{13}$$

$$i_s = i_d + i_g \tag{14}$$

From (13) with approximation $(di_s/dt) \approx (di_d/dt)$, we get (15). Using (8), (9), (11), (12) and (15) with $C_{gd}(v_{dg}) = C_{oxd}$, we get (16) and (17) where the expression for $i_{ch}(v_{gs}, v_{ds})$ and $C_{ds}(v_{ds})$ are given in (1) and (4) respectively. (dv_{gs}/dt) and (dv_{ds}/dt) are of comparable magnitude and the gate and the power circuits are fully coupled through L_s and $C_{gd}(v_{dg})$. Time evolution of the four state variables of this sub-mode (v_{gs}, v_{ds}, $v_{d's'}$ and i_d) is obtained by solving (10), (15), (16) and (17). This forms a set of coupled non-linear differential equation and finite difference technique is employed for solution. The initial conditions are $v_{gs} = V_{GG}$, $v_{ds} = v_{d's'} \approx I_0 R_{on}$ and $i_d = I_0$.

$$\frac{di_d}{dt} \approx \left(\frac{v_{d's'} - v_{ds}}{L_d + L_s}\right) \tag{15}$$

$$\frac{dv_{gs}}{dt} \approx \frac{V_{EE} + R_g C_{oxd}\left(\frac{i_d - i_{ch}}{C_{oxd} + C_{ds}(v_{ds})}\right) - v_{gs} - \frac{L_s(v_{d's'} - v_{ds})}{L_d + L_s}}{\left(R_g\left(C_{gs} + C_{oxd}\right) - \frac{R_g C_{oxd}^2}{C_{oxd} + C_{ds}(v_{ds})}\right)} \tag{16}$$

$$\frac{dv_{ds}}{dt} \approx \frac{(i_d - i_{ch}) + \left(\frac{C_{oxd}}{R_g\left(C_{gs} + C_{oxd}\right)}\right)\left(V_{EE} - v_{gs} - \frac{L_s(v_{d's'} - v_{ds})}{L_d + L_s}\right)}{\left((C_{oxd} + C_{ds}(v_{ds})) - \frac{C_{oxd}^2}{C_{gs} + C_{oxd}}\right)} \tag{17}$$

Sub Mode A ends when $v_{gs} = v_{ds}$ or $v_{dg} = 0$ and t_{1A} is the time duration of this sub-mode. At the end of this sub mode $v_{gs} = V_{gs1A}$, $v_{ds} = V_{ds1A}$, $v_{d's'} = V_{d's'1A}$ and $i_d = I_{d1A}$.

b) ***Sub Mode B****:* $v_{dg} > 0$ dictates the start of Sub Mode B. Same approximations of Sub Mode A holds good for this sub mode. So the governing equations of Sub Mode A will prevail in this sub mode. As $v_{dg} \in [0, V_{td})$ during this sub mode, $C_{gd}(v_{dg})$ is no longer a constant capacitance C_{oxd} and has a non-linear functional dependence on v_{dg} (second expression of (3)). Reduction in $C_{gd}(v_{dg})$ as v_{dg} increases brings down the coupling between gate and power loop through $C_{gd}(v_{dg})$. This results in a faster fall of i_{ch} compared to Sub Mode A (see Fig. 6). Expressions for $i_{ch}(v_{gs}, v_{ds})$ and $C_{ds}(v_{ds})$ are given in (1) and (4) respectively. Finite difference method is used to find out the time evolution of $v_{gs}(t)$, $v_{ds}(t)$, $v_{d's'}(t)$ and $i_d(t)$.

This sub mode ends when $v_{ds}P_{vf} = (v_{gs} - V_{th})$. t_{1B} is the time duration of this sub-mode. At the end of this sub mode $v_{gs} = V_{gs1B}$, $v_{ds} = V_{ds1B}$, $v_{d's'} = V_{d's'1B}$ and $i_d = I_{d1B}$. E_1 quantifies the actual switching loss during Mode I and can be represented as (18) where $t_I = (t_{1A} + t_{1B})$.

$$E_I = \int_0^{t_I} v_{ds}(\tau) i_{ch}(\tau)\, d\tau \tag{18}$$

Special Case: For low values of I_0 and/or low R_{gext}, $v_{ds}P_{vf} = (v_{gs} - V_{th})$ condition is satisfied prior to the point where $v_{gs} = v_{ds}$ condition is met. In that scenario, end of Sub Mode A is defined as the point where $v_{ds}P_{vf} = (v_{gs} - V_{th})$. During Sub Mode B, $C_{gd}(v_{dg}) = C_{oxd}$ and $i_{ch}(v_{gs}, v_{ds})$ is given by (2). This sub mode ends when $v_{gs} = v_{ds}$. Also, for very low I_0 and/or low R_{gext}, i_{ch} may collapse during Mode I and no Mode II will be present.

2) Mode II (Current collapse period): This mode starts when $v_{ds}P_{vf} > (v_{gs} - V_{th})$ and the SiC MOSFET enters into saturation region. i_{ch} solely depends on v_{gs} (see (2)). All the state variables of the gate and the power circuit changes noticeably during this mode. Effect of $C_{g'd'(ext)}$ is considered because of its comparable magnitude with the internal depletion capacitance $C_{gd}(v_{dg})$. Fig. 7 represents the equivalent circuit of this mode. Gate circuit of Q_T is not participating in the dynamics and Q_T can be modelled as $C_{oss}(v_{ds(T)})$.

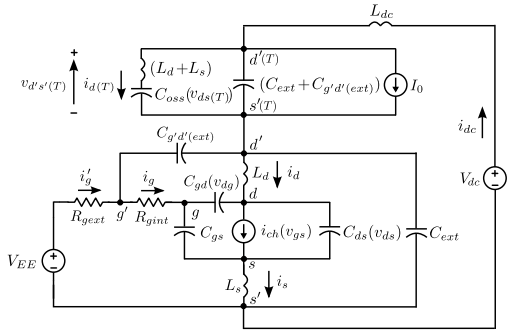

Fig. 7: Equivalent circuit model of Mode II

$(L_d + L_s)$ is the total lead and wire-bond inductance of Q_T. $\left(C_{ext} + C_{g'd'(ext)}\right)$ is the total capacitance connected across $d'(T)$ and $s'(T)$ terminals of Q_T (see Fig. 7). Equivalent impedance across $d'(T)$ and $s'(T)$ nodes is denoted as Z_T and approximately given by (19) as $v_{ds(T)} \approx v_{d's'(T)}$ and $v_{d's'(T)}$ is close to V_{dc}, $C_{oss}(v_{ds(T)}) \ll (C_{ext} + C_{g'd'(ext)})$.

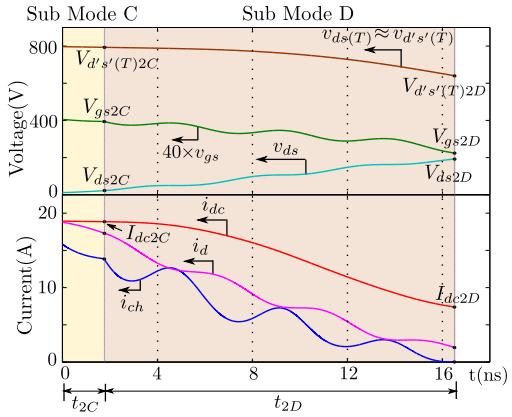

Fig. 8: Simulation waveforms of Mode II

$$Z_T \approx \frac{1}{s\left(C_{oss}(v_{ds(T)}) + C_{ext} + C_{g'd'(ext)}\right)} = \frac{1}{sC_{T(eq)}} \tag{19}$$

Mode II is divided into two sub modes, a) Sub Mode C, and b) Sub Mode D respectively (see Fig. 8).

*a) **Sub Mode C**:* In Sub Mode C, SiC MOSFET is in saturation region and v_{gs} starts decreasing from its initial value V_{gs1B}. This results in a fast change in i_{ch} as in saturation region, i_{ch} solely depends on v_{gs} which is approximately quadratic in nature (2). i_d will follow i_{ch} as the total inductance $(L_d + L_s)$ of the inner loop (loop formed by nodes d', d, s and s') is small. There is a high frequency oscillation observed both in i_d and i_{ch} with the frequency of oscillation in the order the resonant frequency of the LC circuit formed by the L and C values of $(L_d + L_s)$ and $\left(C_{oss}(v_{ds}) \parallel (C_{ext} + C_{g'd'(ext)})\right)$ respectively. This high frequency oscillation present in i_d and i_{ch} is of higher order compared to their low frequency variations and can be neglected. The objective of the analytical model to capture the slow variation of these quantities which results in moderately accurate estimation of time period and actual loss of this mode. So $(di_d/dt) \approx (di_{ch}/dt)$. Power loop current i_{dc} cannot change fast due to the presence of inductance L_{dc}. v_{ds} increases from its initial value V_{ds1A2} and other state variables i_{dc} and $v_{d's'(T)}$ starts changing from their initial values I_0 and $(V_{dc} - R_{on}I_0)$ respectively. Functional form of internal MOSFET capacitances $C_{gd}(v_{dg})$ and $C_{ds}(v_{ds})$ are defined in second expression of (3) (as $v_{dg} \in [0, V_{td})$) and (4) respectively. $C_{oss}(v_{ds(T)})$ is defined in (5) and can be approximated as $C_{oss}(v_{ds(T)}) \approx C_{oss}(v_{d's'(T)})$.

KVL in the power loop of Fig. 7 gives (20). Applying KCL at $d'(T)$ and d' nodes, we get (21) and (22). KCL at d node gives (23). Applying KCL at node g and KVL in the gate loop, we get (24) and (25) respectively.

$$v_{d's'} = V_{dc} - v_{d's'(T)} - L_{dc}\frac{di_{dc}}{dt} \tag{20}$$

$$i_{dc} = I_0 + C_{T(eq)}(v_{d's'(T)})\frac{dv_{d's'(T)}}{dt} \tag{21}$$

$$i_{dc} = i_d + C_{g'd'(ext)}\frac{dv_{d'g'}}{dt} + C_{ext}\frac{dv_{d's'}}{dt} \tag{22}$$

$$i_d = i_{ch} + C_{gd}(v_{dg})\frac{dv_{dg}}{dt} + C_{ds}(v_{ds})\frac{dv_{ds}}{dt} \tag{23}$$

$$i_g = C_{gs}\frac{dv_{gs}}{dt} + C_{gd}(v_{dg})\frac{dv_{gd}}{dt} \tag{24}$$

$$V_{EE} = i_g R_g + R_{gext}C_{g'd'(ext)}\frac{dv_{g'd'}}{dt} + v_{gs} + L_s\frac{di_s}{dt} \tag{25}$$

As the drop across L_d and L_s is small compared to v_{ds} and $v_{d's'}$ during this sub-mode, $v_{ds} \approx v_{d's'}$ and (20) can be approximated to (26). During this sub-mode $(di_s/dt) \approx (di_d/dt)$ and $(di_d/dt) \approx (di_{ch}/dt)$ [1]. Also applying KVL in the loop formed by g', g, d, d', we get (27). $(dv_{g'g}/dt), (dv_{dd'}/dt) \ll (dv_{gd}/dt)$, so $(dv_{g'd'}/dt) \approx (dv_{gd}/dt)$. Using (24) and (25) with all the previously mentioned approximations, we get (29). From the power loop, rate of change of voltage at node g is small compared to d, so $(dv_{dg}/dt) \approx (dv_{ds}/dt)$ and $(dv_{d'g'}/dt) \approx (dv_{dg}/dt) \approx (dv_{ds}/dt)$. Adding (22) and (23) with the previously mentioned approximation and $v_{ds} \approx v_{d's'}$, we get (28).

$$v_{ds} \approx V_{dc} - v_{d's'(T)} - L_{dc}\frac{di_{dc}}{dt} \tag{26}$$

$$v_{g'd'} = (v_{g'g} + v_{gd} + v_{dd'}) \tag{27}$$

$$(i_{dc} - i_{ch}) \approx \underbrace{\left(C_{gd}(v_{dg}) + C_{ds}(v_{ds}) + C_{g'd'(ext)} + C_{ext}\right)}_{C_{B(eq)}(v_{gs}, v_{ds})}\frac{dv_{ds}}{dt} \tag{28}$$

These set of equations (21), (26), (28) and (29) along with (2) form a set of coupled non-linear differential equations. The state variables are $v_{gs}(t)$, $v_{ds}(t)$, $v_{d's'(T)}(t)$ and $i_{dc}(t)$ with initial values $v_{gs} = V_{gs1B}$, $v_{ds} = V_{ds1B}$, $v_{d's'(T)} = (V_{dc} - I_0R_{on})$ and $i_{dc} = I_0$. Sub Mode C ends when $v_{dg} = V_{td}$. At the end of this sub mode $v_{gs} = V_{gs2C}$, $v_{ds} = V_{ds2C}$, $v_{d's'(T)} = V_{d's'(T)2C}$ and $i_{dc} = I_{dc2C}$.

*b) **Sub Mode D**:* Sub Mode D starts when $v_{dg} > V_{td}$. Approximations of Sub Mode C hold good for this sub mode also. (21), (26), (28) and (29) along with (2) dictates the time evolution of the state variables. Functional form of internal MOSFET capacitances $C_{gd}(v_{dg})$ and $C_{ds}(v_{ds})$ are defined in

[1] $(di_{ch}/dt) \approx K_p\left((v_{gs} - V_{th}) - (3\theta/2)(v_{gs} - V_{th})^2\right)$

$$V_{EE} \approx \underbrace{\left(R_g \left(C_{gs} + C_{gd}(v_{dg}) \right) + R_{gext} C_{g'd'(ext)} + K_p L_s \left((v_{gs} - V_{th}) - \frac{3\theta \left(v_{gs} - V_{th} \right)^2}{2} \right) \right)}_{\tau_1(v_{gs}, v_{ds})} \frac{dv_{gs}}{dt} + v_{gs} - \underbrace{\left(R_g C_{gd}(v_{dg}) + R_{gext} C_{g'd'(ext)} \right)}_{\tau_2(v_{gs}, v_{ds})} \frac{dv_{ds}}{dt} \tag{29}$$

third expression of (3) (as $v_{dg} \in [V_{td}, \infty)$) and (4) respectively. $C_{oss}(v_{ds(T)})$ is defined in (5) and can be approximated as $C_{oss}(v_{ds(T)}) \approx C_{oss}(v_{d's'(T)})$.

This sub mode ends when i_{ch} becomes zero. At the end of this sub mode $v_{ds} = V_{ds2D}$, $v_{d's'} = V_{d's'2D} \approx V_{ds2D}$, $(dv_{d's'}/dt) \approx (dv_{ds}/dt) = V'_{d's'2D}$ and $i_{dc} = I_{dc2D}$. $t_{II} = (t_{2C} + t_{2D})$ is the total time period of Mode II. E_{II} quantifies the actual switching loss of this mode and can be evaluated using (18), where the integration limit will be zero to t_{II}.

Special Case: For low values of I_0 and/or low R_{gext}, i_{ch} collapses to zero in Sub Mode C. In that scenario, there is no Sub Mode D present.

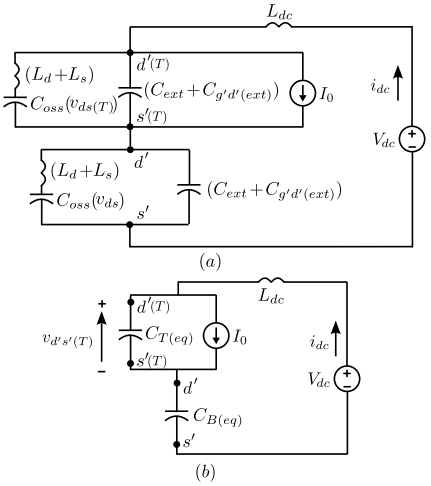

Fig. 9: Approximate equivalent circuit model of Mode III

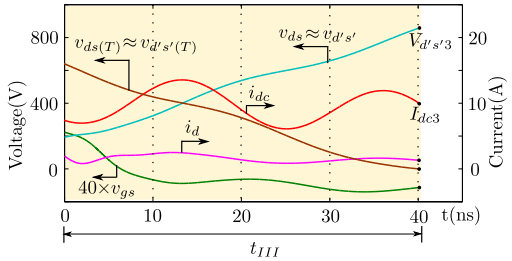

Fig. 10: Simulation waveforms of Mode III

3) Mode III (voltage rise period): This mode starts after i_{ch} collapses to zero. Gate circuit of Q_B looses its control over the state variables of power circuit. Switching dynamics of this mode is solely dictated by the power circuit (see Fig. 10). Fig. 9(a) represents the approximate equivalent circuit of Mode III. Using similar argument given in Mode II (see (19)), Fig. 9(a) can be reduced to Fig. 9(b), where $C_{T(eq)}$ and $C_{B(eq)}$ are given below [2]. Note, this approximation for Q_T will be valid for most of this mode except towards the end where $v_{d's'(T)} \approx 0$ and $C_{oss}(v_{d's'(T)})$ and C_{ext} are of comparable magnitude. But this is a small portion of the total voltage rise period and it has been ignored for the simplicity of the analysis. Fig. 9(b) is considered as the approximate equivalent circuit throughout Mode III.

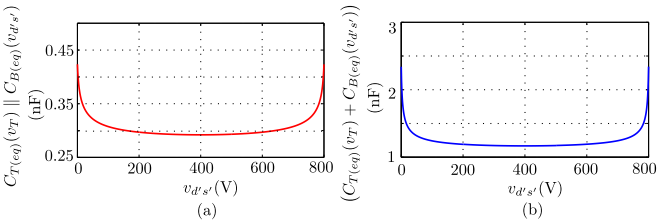

Fig. 11: (a) $\left(C_{T(eq)}(v_{d's'(T)}) \parallel C_{B(eq)}(v_{d's'})\right)$ vs $v_{d's'}$ and (b) $\left(C_{T(eq)} + C_{B(eq)}\right)$ vs $v_{d's'}$ plot of C2M0080120D with $C_{ext} = 470pF$

Applying KVL in the power loop of Fig. 9(b), we get (30). KCL at node $d'(T)$ and d' gives (31) and (32) respectively. Using (30), (31), (32) and substituting $v_{d's'(T)}$ and i_{dc}, we get a differential equation of $v_{d's'}$ (33). Here first and second time derivative of $C_{B(eq)}(v_{d's'})$ is neglected as $v_{d's'}$ is high and $C_{B(eq)}(v_{d's'})$ remains almost constant with the change in $v_{d's'}$. During this mode drop across L_{dc} is small compared to $v_{d's'}$ and $v_{d's'(T)}$, so $v_{d's'(T)} \approx (V_{dc} - v_{d's'})$. $\left(C_{T(eq)} \parallel C_{B(eq)}\right)$ and $\left(C_{T(eq)} + C_{B(eq)}\right)$ are plotted as a function of $v_{d's'}$ in Fig. 11(a) and Fig. 11(b) respectively. Both $\left(C_{T(eq)} \parallel C_{B(eq)}\right)$ and $\left(C_{T(eq)} + C_{B(eq)}\right)$ remains almost constant with $v_{d's'}$ and can be replaced with charge related capacitances given by C_{Q1} and C_{Q2} respectively in the voltage range $v_{d's'} \in (0, V_{dc})$. Charge related capacitance C_Q for a non-linear capacitance $C(v)$ in the voltage interval $v \in (V_1, V_2)$ given by (34).

$$v_{d's'} = V_{dc} - v_{d's'(T)} - L_{dc} \frac{di_{dc}}{dt} \tag{30}$$

$$i_{dc} = I_0 + C_{T(eq)}(v_{d's'(T)}) \frac{dv_{d's'(T)}}{dt} \tag{31}$$

$$i_{dc} = C_{B(eq)}(v_{d's'}) \frac{dv_{d's'}}{dt} \tag{32}$$

$$L_{dc} \left(C_{T(eq)} || C_{B(eq)} \right) \frac{dv^3_{d's'}}{dt^3} + \frac{dv_{d's'}}{dt} = \left(\frac{I_0}{C_{T(eq)} + C_{B(eq)}} \right) \tag{33}$$

$$C_Q = \frac{1}{V_2 - V_1} \int_{V_1}^{V_2} C(v)\, dv \tag{34}$$

Solving (33) with approximations $C_{Q1} \approx \left(C_{T(eq)} \parallel C_{B(eq)}\right)$ and $C_{Q2} \approx \left(C_{T(eq)} + C_{B(eq)}\right)$, we get the time evolution of $v_{d's'}$ (35) [3]. $\left(d^2 v_{d's'}/dt^2\right)\big|_{t=0} = 0$ is considered as it can not

[2] $C_{T(eq)} \approx \left(C_{oss}(v_{d's'(T)}) + C_{ext} + C_{g'd'(ext)}\right)$, $C_{B(eq)} \approx \left(C_{oss}(v_{d's'}) + C_{ext} + C_{g'd'(ext)}\right)$

[3] $\omega_0 = \frac{1}{\sqrt{L_{dc} C_{Q1}}}$, $A_0 = V_{d's'2D}$, $A_1 = \left(\frac{I_0}{C_{Q2}}\right)$, $A_2 = \left(\frac{V'_{d's'2D} - (I_0/C_{Q2})}{\omega_0}\right)$

be estimated accurately from the end of the Mode II (current collapse period) and in all practical purposes, it has negligible impact on the switching trajectories of voltage rise period. *This mode ends when* $v_{d's'(T)} = 0$ *and the anti-parallel diode of* Q_T *gets forward biased.* But it is difficult to solve for $i_{dc}(t)$ and $v_{d's'(T)}(t)$ as $C_{T(eq)}$ and $C_{B(eq)}$ are functions of $v_{d's'(T)}$ and $v_{d's'}$ respectively. At the end of this Mode, $v_{d's'}$ is close to V_{dc} making $C_{B(eq)}$ is approximately constant to $C^*_{B(eq)}$ [4]. Then $i_{dc}(t)$ is solved using (32) and given by (36). $v_{d's'(T)}(t)$ is solved from (30) using $v_{d's'}(t)$ and $i_{dc}(t)$ and given by (37) [5].

$$v_{d's'}(t) \approx A_0 + A_1 t + A_2 \sin(\omega_0 t) \tag{35}$$

$$i_{dc}(t) \approx C^*_{B(eq)} \left(A_1 + A_2 \omega_0 \cos(\omega_0 t)\right) \tag{36}$$

$$v_{d's'(T)}(t) \approx (V_{dc} - A_0) - A_1 t + A_2 A_3 \sin(\omega_0 t) \tag{37}$$

Mode III ends when $v_{d's'(T)} = 0$ and time duration of this mode t_{III} is estimated by equating (37) to zero. At the end of this mode $v_{d's'} = V_{d's'3}$ and $i_{dc} = I_{dc3}$. Also $(dv/dt)_{off}$ is approximately given by $\left(V_{d's'3} - V_{d's'2D}\right)/t_{III}$.

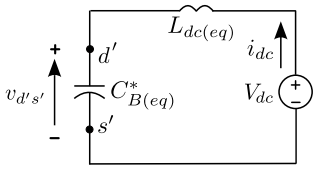

Fig. 12: Approximate equivalent circuit model of Mode IV

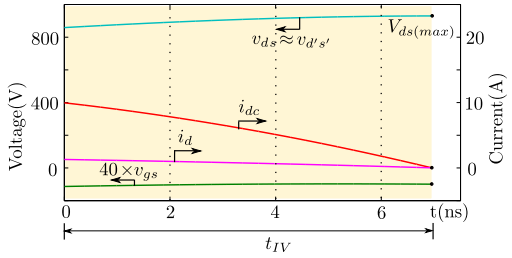

Fig. 13: Simulation waveforms of Mode IV

4) Mode IV (drain current fall): This Mode starts when the anti-parallel diode of Q_T gets forward biased and $v_{d's'(T)} \approx 0$. Fig. 12 represents the approximate equivalent circuit of this mode and the important waveforms of this mode are given in Fig. 13. L_d and L_s of Q_T will be part of power loop inductance and total equivalent power loop inductance will be $L_{dc(eq)}$ [6]. As $v_{ds} \approx v_{d's'}$ is in the range of V_{dc}, so $C_{B(eq)}$ is almost constant to $C^*_{B(eq)}$ [7]. Applying KVL in power loop and KCL at node d' gives (38) and (39) respectively.

$$v_{d's'} \approx V_{dc} - L_{dc(eq)} \frac{di_{dc}}{dt} \tag{38}$$

$$i_{dc} \approx C^*_{B(eq)} \frac{dv_{d's'}}{dt} \tag{39}$$

Time evolution of $v_{d's'}$ is given in (40) [8]. This sub mode ends when $v_{d's'}$ reaches its maximum value. Duration of this sub mode is denoted by t_{3A} and given in (41). Maximum $v_{ds} \approx v_{d's'}$ overshoot puts a constraint on the maximum allowable $L_{dc(eq)}$ as it can lead to device failure due to transient over-voltage. Maximum value of $v_{d's'} = V_{ds(max)}$ is given in (42).

$$v_{d's'} = V_{dc} + A_4 \sin(\omega_1 t + \phi) \tag{40}$$

$$t_{3A} = \left(\frac{\frac{\pi}{2} - \phi}{\omega_1}\right) \tag{41}$$

$$V_{ds(max)} = V_{dc} + A_4 \tag{42}$$

At the end of this sub mode $v_{d's'} = V_{ds(max)}$ and $i_{dc} = 0$. t_{IV} is the total time period of this mode. $(di/dt)_{off}$ is approximately given by (I_{dc3}/t_{IV}).

Total turn off switching transition time $T_{off} = (t_I + t_{II} + t_{III} + t_{IV})$. Total soft switching loss is given by $E_{off} = (E_I + E_{II})$. $(dv/dt)_{off}$ and $(di/dt)_{off}$ are given as $(V_{d's'3} - V_{d's'2D})/t_{III}$ and (I_{dc3}/t_{IV}) respectively. $V_{ds(max)}$ represent the turn off transient over-voltage. The flowchart of the proposed analytical model is given in Fig. 14.

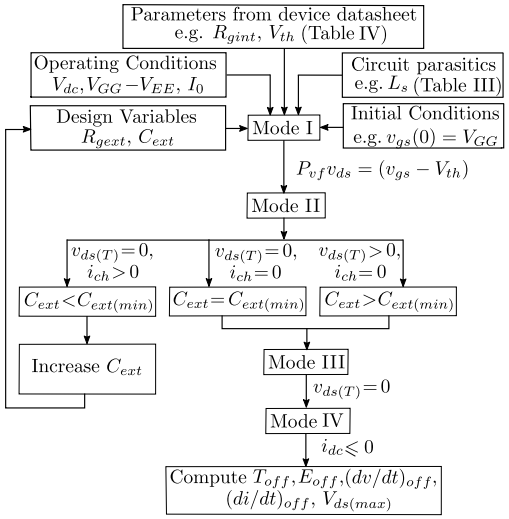

Fig. 14: Flowchart of analytical model and $C_{ext(min)}$ estimation

B. Estimation of minimum external capacitor for soft switching ($C_{ext(min)}$)

Soft switching condition is satisfied when $v_{ds(T)} = 0$ and $i_{ch} \geq 0$ at the end of Mode II. At the boundary of hard and soft switching, both the equalities $v_{ds(T)} = 0$ and $i_{ch} = 0$ will be satisfied simultaneously at the end of Mode II. So to find out the minimum value of the external capacitor required to achieve soft switching ($C_{ext(min)}$) for a given V_{dc}, R_{gext} and I_0, an iterative process is followed where C_{ext} is increased from small value and first two modes (Mode I and Mode II) of the analytical model are solved till the conditions $v_{ds(T)} = 0$

[4] $C^*_{B(eq)} = \left(C_{oss}(v_{d's'} = V_{dc}) + C_{ext} + C_{g'd'(ext)}\right)$
[5] $A_3 = \left(L_{dc} C^*_{B(eq)} \omega_0^2 - 1\right)$
[6] $L_{dc(eq)} = (L_{dc} + L_d + L_s)$
[7] $C^*_{B(eq)} = \left(C_{oss}(v_{d's'} = V_{dc}) + C_{ext} + C_{g'd'(ext)}\right)$
[8] $\omega_1 = \frac{1}{\sqrt{L_{dc(eq)} C^*_{B(eq)}}}$, $A_4 = \sqrt{\left(V_{d's'3} - V_{dc}\right)^2 + \left(\frac{L_{dc(eq)}}{C^*_{B(eq)}}\right)(I_{dc3})^2}$, $\phi = \tan^{-1}\left(\frac{\left(V_{d's'3} - V_{dc}\right)}{I_{dc3}} \sqrt{\frac{C^*_{B(eq)}}{L_{dc(eq)}}}\right)$

and $i_{ch} = 0$ are satisfied simultaneously. The corresponding value of C_{ext} is given as $C_{ext(min)}$ (see Fig. 14). Note, the analytical model is valid only for values of $C_{ext} \geq C_{ext(min)}$.

V. Experimental Set-up

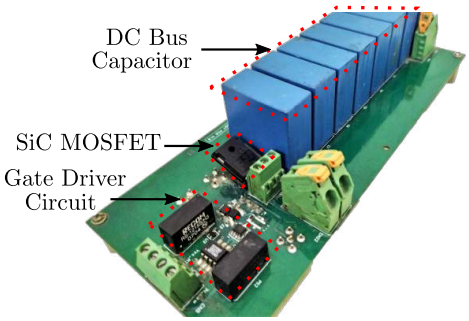

Fig. 15: Double pulse test setup

The behavioural model is validated experimentally through double pulse test (DPT). Two different SiC MOSFETs of 1.2kV are used, S1: C2M0160120D (19A @25^o) and S2: C2M0080120D (36A @25^o). Device related parameters extracted from the datasheet are given in TABLE IV.

DPT is designed for V_{dc}=800V and I_0=30A. Air core inductor with L =150 μH is used as the output inductive load. The values of external circuit related parameters used for behavioural simulation and the proposed analytical model are obtained through experiment [29] and given in TABLE V. Values of external circuit parameters depend on the package type as well as layout. For each diode switch pair (S1, S2), experiments are conducted for two values of V_{dc}, five values of I_0, three values of R_{gext} and three values of C_{ext} for each device. This implies a total 180 different operating conditions. Details of C_{ext} used for experiment is given in Table VI. All the capacitors are 1kV rated.

Opto-isolator IX3180GS followed by a current booster IXDN609SI is used to drive the gate of the SiC MOSFET. Gate driver parameters are given in TABLE VII and it is common for both the devices. Negate gate voltage $V_{EE} = -5V$ is used as it is standard for SiC MOSFET. It also helps to reduce T_{off} and E_{off} for soft turn off transition when compared with soft turn off transition with $V_{EE} = 0V$.

Experimentally measured signals are $v_{g's'}(t)$, $v_{d's'}(t)$ and $i_{dc}(t)$. Oscilloscope MDO3104 from Tektronix with 1 GHz bandwidth is used for measurement. $v_{g's'}(t)$ measurement is done using a passive probe from Tektronix with 1 GHz bandwidth (TPP1000). A high voltage single ended probe from Tektronix (P5100A) with 500 MHz bandwidth is used for $v_{d's'}(t)$ measurement. Current $i_{dc}(t)$ is measured using a AC/DC current probe from Tektronix (TCP0030A) with 120 MHz bandwidth and 50A peak current measurement capability. Matching of propagation delay between voltage and current signals are done using a delay matching instrument available from Tektronix (067-1686-00, Power Measurement De-skew and Calibration Fixture).

MATLAB/Simulink® is used to simulate the behavioural model. All the experiments are performed at room temperature ($\approx 25^o$C).

VI. Simulation and Experimental Results

The objective of this section is to validate the soft turn off switching dynamics analysis presented in this paper through behavioural simulation and experiment.

A. Validation of the behavioural model (simulation) through experiment and comparison of actual loss and measured loss

$v_{d's'}(t)$ and $i_{dc}(t)$ are measured experimentally. Results obtained from behavioural simulation and experiment are plotted on top of each other in Fig. 16 for both S1 and S2 (4 different operating conditions for each device). Experimental waveforms match closely with behavioural simulation over the switching transition period. This observation is seen to hold good for other 172 operating conditions also. It is noteworthy that there is a damping effect present in $i_{dc(exp)}$ during voltage rise period mostly due to the losses present in high frequency resistance of power loop, device parasitic capacitances and C_{ext}. This could not be captured by $i_{dc(sim)}$ as the behavioural model does not incorporate the effect of high frequency resistance and the losses in the device capacitances [30] and C_{ext}. But this effect is only visible for low I_0 and high C_{ext} and it has minimal impact on the final parameters estimated using this behavioural model (T_{off}, E_{off}, $(dv/dt)_{off}$, $(di/dt)_{off}$ and $V_{ds(max)}$) and hence neglected to reduce the complexity of the behavioural model. It is noteworthy that the loss in ESR of C_{ext} is negligible compared to the loss in channel of the SiC MOSFET for most of the operating conditions except for small values of I_0. Also, ESL of C_{ext} can be neglected the maximum frequency content of i_{dc} is much smaller that the resonant frequency of C_{ext}. Hence the parasitics of C_{ext} has a negligible impact in switching transient.

Channel current i_{ch} can not be measured directly from the experimental measurement. Experimentally measured i_{dc} is different from i_{ch}. From experimental result, it is difficult to verify the soft switching condition. Also, it is not possible to obtain the actual switching loss directly from experiment. On the other hand, behavioural model has access to the internal state variables. So to verify the soft switching condition and estimate the actual switching loss, behavioural model is required. Actual loss obtained using behavioural model ($E_{off(sim)}$) is compared with the measured loss from experiment ($E'_{off(exp)}$) for S1 and S2 in Fig. 17(a) and Fig. 17(b) respectively. The values of (V_{dc}, R_{gext}, C_{ext}) are (800V, 2.5Ω, 200pF) for S1 and (800V, 2.5Ω, 470pF) for S2. It can be observed that the $E_{off(sim)}$ values are small compared to $E'_{off(exp)}$ for all operating conditions. So it is established here that the actual loss for turn off soft switching can not be obtained from experimental measurement and behavioural model is important to estimate the actual loss.

B. Verification of the proposed analytical model through behavioural model

To verify the correctness of the proposed analytical model, important intermediate quantities obtained from behavioural model for each mode are compared with the values obtained using the analytical model. Behavioural model is used for comparison as it is not possible to get the values of most

TABLE IV: Device parameters extracted from data-sheet (S1: C2M0160120D and S2: C2M0080120D)

	V_{th} (V)	K_p (A/V^2)	K_f	θ (1/V)	P_{vf}	R_{gint} (Ω)	C_{gs} (nF)	k_1 (nF)	k_2 (V)	k_3	V_{td} (V)	k_4 (nF)	k_5 (V)	k_6 (nF)	k_7 (V)	k_8 (nF)	k_9 (V)
S1	4.6	1.3	1.54	0.03	0.33	6.5	0.53	0.6	0.2	1.24	12	0.06	0.02	0.43	5.5	0.75	2.21
S2	5.6	1.6	2.19	0.01	0.4	4.6	0.95	0.95	0.35	0.71	12	0.12	0.025	0.79	5.5	1.3	2.34

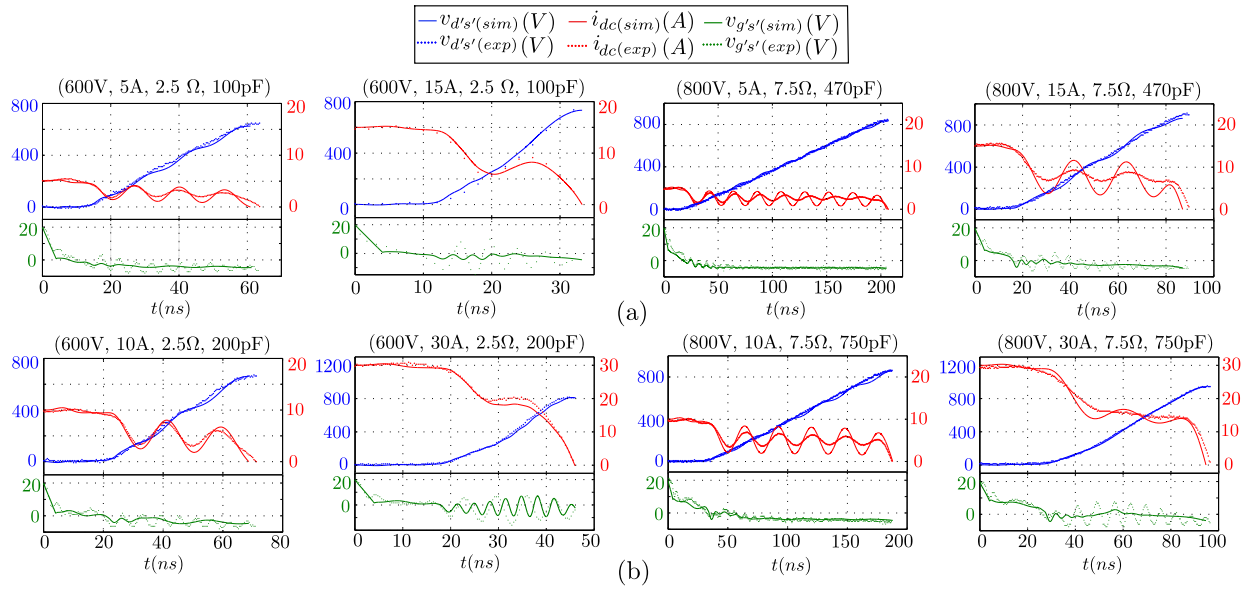

Fig. 16: Simulation vs experimental waveforms: (a) S1, (b) S2

TABLE V: External circuit parameters

	L_{dc} (nH)	L_d (nH)	L_s (nH)	$C_{g'd'(ext)}$ (pF)	C_{ext} (pF)
S1	45	6	6	15	100, 200, 470
S2	45	6	9	15	200, 470, 750

TABLE VI: Information of C_{ext}

C_{ext}(pF)	Manufacturer	Part No.	Dielectric
100	KEMET	C1206C101KDGAC	C0G
200		C1206C201KDGAC	
470		C1206C471KDGAC	
750		C1206C751KDGAC	

TABLE VII: Driver parameters

V_{EE} (V)	V_{GG} (V)	$R_{g(driver)}$ (Ω)	R_{gext} (Ω)	T_f (ns)
-5	20	0.5	3, 4.5, 8	4

of the intermediate quantities from the experimental result. Single operating condition is considered for each device and it is ensured that the soft switching condition is satisfied for these operating conditions (Table VIII). These numbers match closely. Also to verify the correctness of the assumptions in each mode, the time evolution of important state variables obtained from the proposed model in each mode is plotted over simulated results for S1 (Fig. 18). A close match is observed between simulated waveforms and waveforms obtained using the proposed analytical model. Only in Mode I, $t_{I(anly)}$ is

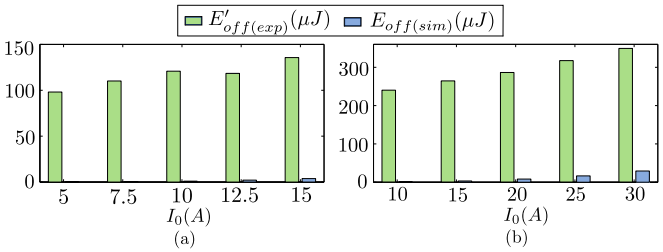

Fig. 17: Comparison of loss obtained through simulation and experiment: (a) S1, (b) S2

found to be a bit smaller compared to $t_{I(sim)}$ as the ramp fall of gate supply voltage is approximated as step fall in the proposed analytical model. A similar study is carried out for other operating conditions and close agreements are observed. This validates the proposed analytical model in each mode of switching transition (Section III).

C. Minimum C_{ext} required for soft switching

Minimum C_{ext} values required to achieve soft switching are obtained using proposed analytical model and behavioural simulation and plotted with respect to I_0 for two different $R_{gext} = 2.5, 7.5\Omega$ and $V_{dc} = 600, 800V$ for S1 and S2 in Fig. 19(a) and Fig. 19(b) respectively. Close agreement is observed for S2 whereas analytical model slightly underestimates the minimum C_{ext} value for S1. Also, it can be observed from these figures that the minimum amount of C_{ext} required for a given V_{dc} and R_{gext} increases with I_0. For low values of I_0, soft switching happens without any C_{ext}. As R_{gext} increases

TABLE VIII: Comparison of important intermediate quantities (Simulation and Analytical)

		Mode I				Mode II				Mode III		Mode IV		
		V_{ds1B} (V)	I_{ch1B} (A)	t_I (ns)	E_I (μJ)	V_{ds2D} (V)	$V_{d's'2D}$ (V)	t_{II} (ns)	E_{II} (μJ)	t_{III} (ns)	$\left(\frac{dv}{dt}\right)_{off}$ (V/ns)	t_{IV} (ns)	$V_{ds(max)}$ (V)	$\left(\frac{di}{dt}\right)_{off}$ (A/ns)
S1	Sim	10.22	7.03	11.17	0.31	123.1	116.6	7.51	0.67	39.33	16.42	7.32	875.05	0.57
(800V, 10A, 2.5Ω, 200pF)	Anly	10.34	6.87	8.87	0.25	93	93	6.32	0.61	41	17.26	5.94	867	0.75
S2	Sim	11.27	16.01	17.63	1.24	193.95	183.07	16.6	6.94	40	16.6	7.04	929.7	1.41
(800V, 20A, 2.5Ω, 470pF)	Anly	11.4	15.9	14.8	1.11	169.14	169.14	16.02	5.8	39.56	16.45	7.91	900.85	1.2

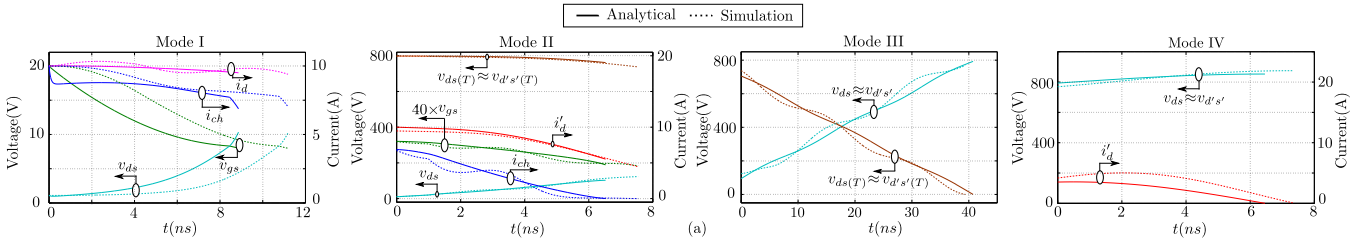

Fig. 18: Mode-wise overlapped waveform of S1, Operating conditions: [800V, 10A, 2.5Ω, 200pF]

for a fixed value of V_{dc} and I_0, the minimum amount of C_{ext} required for soft switching increases. So it is beneficial to use a small value of R_{gext}. The minimum value of R_{gext} is limited by the peak current capability of the gate driver used. For a fixed value of I_0 and R_{gext}, as V_{dc} reduces, the minimum amount of C_{ext} required to achieve soft switching increases.

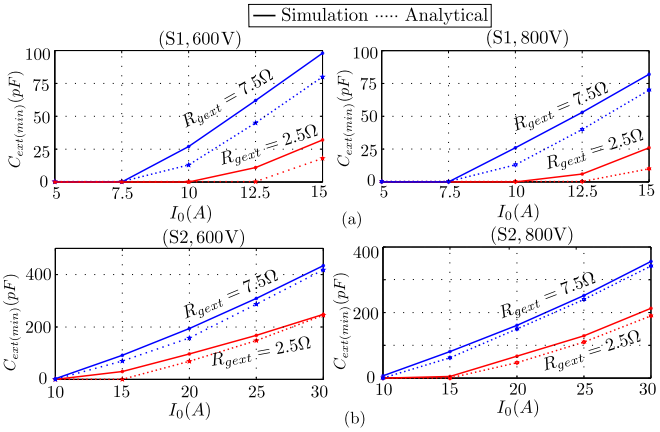

Fig. 19: Minimum C_{ext} for soft switching using behavioural simulation and analytical model: (a) S1, (b) S2

D. Estimation of important quantities related to soft turn off switching dynamics

In this subsection, the estimated quantities obtained using proposed analytical model (T_{off}, E_{off}, $(dv/dt)_{off}$, $(di/dt)_{off}$ and $V_{ds(max)}$) are compared with the behavioural simulation and/or experimental results.

1) T_{off} comparison: In the first part, total turn off time (T_{off}) obtained from the proposed analytical model ($T_{off(anly)}$), behavioural simulation ($T_{off(sim)}$) and experiment ($T_{off(exp)}$) are compared for S1 with operating conditions $V_{dc} = 800V$, $I_0 \in (5, 15)A$, $C_{ext} = 200, 470pF$ and $R_{gext} = 2.5\Omega$ in Fig. 20(a) and for $R_{gext} = 7.5\Omega$ in Fig. 20(b). It can be observed that there a close match between $T_{off(anly)}$, $T_{off(sim)}$ and $T_{off(exp)}$ for the entire operating conditions. For a fixed V_{dc}, C_{ext} and R_{gext} with the increase of I_0, T_{off} reduces and it remains almost constant for high values of I_0. The reduction in T_{off} is primarily contributed by the reduction in voltage rise time as I_0 increases. Also with fixed V_{dc}, I_0 and R_{ext}, T_{off} has a strong positive correlation with C_{ext} and it increases significantly with C_{ext}. This is mainly because of the increase in voltage rise time with the increase in C_{ext}. On the contrary, for constant V_{dc}, I_0 and C_{ext}, T_{off} has a weak dependence on R_{gext} as a major fraction of T_{off} is contributed by voltage rise period and gate circuit does not impact the switching transition in voltage rise. Similar plots are given for S2 with operating conditions $V_{dc} = 800V$, $I_0 \in (10, 30)A$, $C_{ext} = 470, 750pF$ and $R_{gext} = 2.5\Omega$ in Fig. 20(c) and for $R_{gext} = 7.5\Omega$ in Fig. 20(d). Estimation of T_{off} is important as it helps to optimize the dead-time between two complementary devices of a voltage source converter.

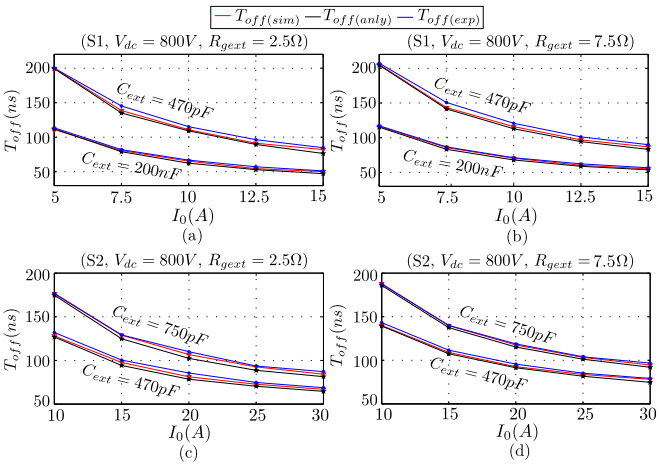

Fig. 20: T_{off} estimation

2) E_{off} comparison: Actual turn off loss (E_{off}) estimated using proposed analytical model ($E_{off(anly)}$) is compared with the actual switching loss obtained using behavioural

simulation ($E_{off(sim)}$) for S1 with operating conditions $V_{dc} = 800V$, $I_0 \in (5, 15)A$, $C_{ext} = 200, 470pF$ and $R_{gext} = 2.5\Omega$ in Fig. 21(a) and for $R_{gext} = 7.5\Omega$ in Fig. 21(b). Close agreement is observed for S2 whereas analytical model slightly underestimates the minimum C_{ext} value for S1. It can be observed that $E_{off(anly)}$ increases with I_0 for a fixed value of V_{dc}, R_{gext} and C_{ext}. Also for a fixed value of V_{dc}, I_0 and R_{gext}, $E_{off(anly)}$ reduces with C_{ext}. $E_{off(anly)}$ is a monotonically decreasing function of C_{ext} when other parameters remain fixed.

It has already been established that the experimentally measured loss ($E'_{off(exp)}$) is much higher compared to the actual loss estimated using behavioural simulation ($E_{off(sim)}$) (see Fig. 17) and the proposed analytical model estimates the actual loss which is close to $E_{off(sim)}$.

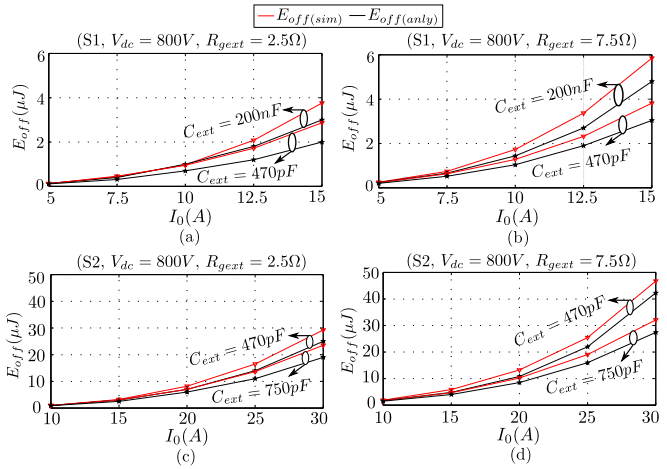

Fig. 21: E_{off} estimation

3) $(dv/dt)_{off}$ comparison: $(dv/dt)_{off}$ represents the (dv/dt) rate during turn off condition and it is plotted for S1 with operating conditions $V_{dc} = 800V$, $I_0 \in (5, 15)A$, $C_{ext} = 200, 470pF$ and $R_{gext} = 2.5\Omega$ in Fig. 22(a) and $R_{gext} = 7.5\Omega$ in Fig. 22(b). Note, for calculating $(dv/dt)_{off(exp)}$, 10% to 90% change in V_{dc} is considered. With V_{dc}, R_{gext} and C_{ext} remain fixed, $(dv/dt)_{off}$ is a monotonically increasing function of I_0. This is due to the fast charge-discharge of the output capacitance (C_{ext} included) with the increase in I_0. Also for a fixed V_{dc}, R_{gext} and I_0, $(dv/dt)_{off}$ reduces with the increase in C_{ext}. As i_{ch} is zero during voltage rise period, gate looses its control over power circuit and R_{gext} has very weak control over $(dv/dt)_{off}$ as can be seen from Fig. 22(a) and Fig. 22(b). Similar trends have been observed for S2 as given in Fig. 22(c) and Fig. 22(d).

4) $(di/dt)_{off}$ comparison: $(di/dt)_{off}$ obtained from proposed analytical model, behavioural simulation and experiment are compared for S2 and $V_{dc} = 800V$ in Table IX and a close agreement is found. It can be observed that $(di/dt)_{off}$ is weakly correlated with both C_{ext} and R_{gext}. A similar observation holds true for S1 also.

5) $V_{ds(max)}$ comparison: $V_{ds(max)}$ obtained from proposed analytical model, behavioural simulation and experiment are compared for S2 and $V_{dc} = 800V$ in Table X and a close agreement is observed. Similar to $(di/dt)_{off}$, $V_{ds(max)}$ is also

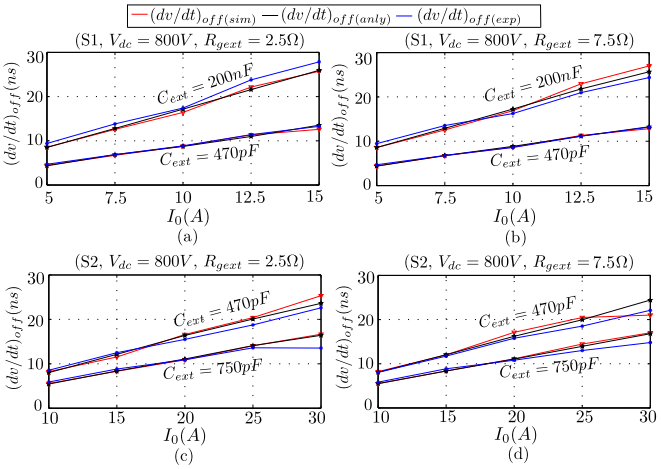

Fig. 22: $(dv/dt)_{off}$ estimation

TABLE IX: Comparison of $(di/dt)_{off}$ (A/ns)

		(30A,2.5Ω)			(30A,7.5Ω)		
	C_{ext} (pF)	Sim	Anly	Exp	Sim	Anly	Exp
S2	470	1.44	1.39	1.12	1.41	1.49	1.11
	750	1.13	1.07	1.05	1.28	1.35	1.03

weakly corrected with C_{ext} and R_{gext}. A similar observation is found to be true for S1 also.

TABLE X: Comparison of $V_{ds(max)}$ (V)

		(30A,2.5Ω)			(30A,7.5Ω)		
	C_{ext} (pF)	Sim	Anly	Exp	Sim	Anly	Exp
S2	470	961.7	942.04	968	962.60	939.82	976
	750	937.73	914	952	946	926	952

VII. Selection of C_{ext} for a given operating range

The objective of this section is to find out the optimal value of C_{ext} that ensures soft switching for a given V_{dc}, R_{gext} and load current range $I_{0(min)} \leq I_0 \leq I_{0(max)}$ while maintaining the $(dv/dt)_{off}$ below a specified limit ($(dv/dt)_{off(spec)}$). The value of $(dv/dt)_{off(spec)}$ is decided from the EMI filter design requirements. Moreover, it facilitates to select an optimal dead-time and estimate the worst case switching power loss for a given switching frequency. From the results presented in previous section, it can be observed that C_{ext} is strongly correlated with T_{off}, E_{off} and $(dv/dt)_{off}$ whereas it has a weak correlation with $(di/dt)_{off}$ and $V_{ds(max)}$. So, $(di/dt)_{off}$ and $V_{ds(max)}$ are not considered for C_{ext} selection. The following steps are followed to obtain the optimal value of C_{ext}.

- **Step 1** In the first step, value of R_{gext} needs to be selected. Use of low R_{gext} helps to achieve soft turn off and the minimum value is limited by the peak current rating of the gate driver used (see Fig. 19 and Fig. 21).
- **Step 2** Use the flowchart given in Fig. 14 with $I_0 = I_{0(max)}$ to obtain the value of the minimum external drain source capacitance required for soft turn off ($C_{ext(min)}$). This ensures that for any $C_{ext} \geq C_{ext(min)}$, the soft

switching condition is satisfied for all operating conditions ($I_{0(min)} \leq I_0 \leq I_{0(max)}$) (see Fig. 19).

- **Step 3** For a given V_{dc}, R_{gext} and C_{ext}, $(dv/dt)_{off}$ is maximum at $I_0 = I_{0(max)}$ and $(dv/dt)_{off}$ reduces with increase in C_{ext} when other parameters remain fixed (see Fig. 22). So the value of C_{ext} is increased starting from $C_{ext(min)}$ such that the value of $(dv/dt)_{off}$ at $I_0 = I_{0(max)}$ is smaller than $(dv/dt)_{off(spec)}$ (see Fig. 23). The corresponding value of C_{ext} is $C_{ext(opt)}$.

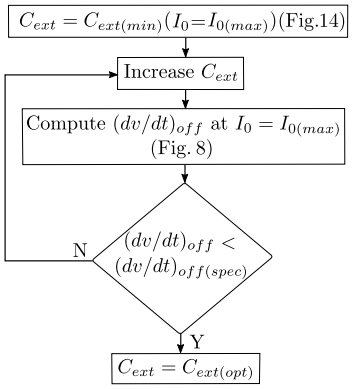

Fig. 23: Flowchart for optimal C_{ext} selection

- **Step 4** Similar to $(dv/dt)_{off}$, E_{off} is maximum at $I_0 = I_{0(max)}$ for a given V_{dc}, R_{gext} and C_{ext}, (see Fig. 21). In this step, C_{ext} is kept fixed at $C_{ext(opt)}$ and the value of E_{off} is estimated using Fig. 14 at $I_0 = I_{0(max)}$. The corresponding value $E_{off(max)}$ represents the worst case turn off switching loss.
- **Step 5** For a given V_{dc}, R_{gext} and C_{ext}, T_{off} is maximum at $I_0 = I_{0(min)}$ (see Fig. 20). Similar to step 4, C_{ext} is kept fixed at $C_{ext(opt)}$ and the value of T_{off} is estimated using Fig. 14 at $I_0 = I_{0(min)}$. The corresponding value $T_{off(max)}$ represents the maximum turn off transition time. The value of dead-time has to be higher than $T_{off(max)}$.

To illustrate the design process of selecting optimal C_{ext}, an example is considered for S2 is with $V_{dc} = 800V$ and I_0 varies in the range 10-30A. Following Step 1, $R_{gext} = 2.5\Omega$ is used as it satisfies the peak gate current limit. $C_{ext(min)}$ is obtained for $I_0 = 30A$ and it is equal to 190pF (Step 2). $(dv/dt)_{off(spec)} = 10V/ns$ is specified for this problem. Using the flowchart given in Step 3, $C_{ext(opt)}$ is obtained as 1390pF which satisfies the constrain $(dv/dt)_{off} < 10V/ns$ at $I_0 = 30A$. For the selected value of $C_{ext(opt)} = 1390pF$, $E_{off(max)} = 17\mu J$ at $I_0 = 30A$ (Step 4). $T_{off(max)}$ is obtained at $I_0 = 10A$ and it is equal to 285ns and the dead-time is selected as 300ns (Step 5). Similarly, for S1 with $V_{dc} = 800V$, $R_{gext} = 2.5\Omega$ and I_0 varies in the range 10-15A, $C_{ext(opt)} = 645pF$ is obtained following the above design procedure. Using this value of C_{ext}, $(dv/dt)_{off} < 10V/ns$, $E_{off(max)} = 2.2\mu J$ at $I_0 = 15A$ and $T_{off(max)} = 253$ns. The dead-time is selected as 280ns.

VIII. Conclusion

An analytical model to study the turn off soft switching dynamics of SiC MOSFET using datasheet parameters and external circuit parasitic is presented in this paper. In this work, the turn off switching transition is considered to be soft switched, if the channel current collapses before the voltage across the drain-source terminal of the complementary MOSFET falls to zero. This model is derived using behavioural model of the SiC MOSFET through approximations. The behavioural model is taken from a previous work related to the study of hard switching dynamics of SiC MOSFET. Firstly, the behavioural model is validated through experiment for two 1200V SiC MOSFETs and a wide range of operating conditions. Then the proposed analytical model is validated using the behavioural model.

The proposed analytical model is used to calculate turn off transition time, actual loss, $(dv/dt)_{off}$, $(di/dt)_{off}$ and transient over-voltage when the MOSFET is soft-switched. Proposed model estimates these quantities accurately and the numbers are close to behavioural simulation and/or experimental approaches. The important conclusions of this work are: a) for soft turn off transient, gate circuit dynamics do not impact the voltage rise and drain current fall modes, b) small external gate resistance is beneficial to achieve soft switching, c) common source inductance opposes channel current to collapse and small value is preferable to minimize turn off switching loss. The analytical model is also used to compute the minimum external capacitance necessary to achieve soft switching at a given operating point. A step by step design procedure is provided to select an optimal external drain-source capacitance that ensures soft switching over a given range of operating conditions and limits the maximum turn-off voltage slope. It also helps in selecting dead-time that guarantees ZVS turn-on of the complementary device. Also, the design provides the worst case switching loss and the maximum value of the transient over voltage as performance measures. The problem is solved for a given range of operating conditions (one DC bus voltage, external gate resistance and a range of load currents), typical in DC-DC, DC-AC applications. It is found that the turn off time, actual loss, $(dv/dt)_{off}$ are strongly correlated with external capacitance while $(di/dt)_{off}$ and transient over-voltage weakly depend on its value. Also, it is noteworthy that the proposed analytical model estimates the actual switching loss which is significantly smaller compared to the experimentally measured loss.

In brief, the proposed analytical model provides a fast, inexpensive method to accurately estimate the turn off soft switching transient related quantities of SiC MOSFET using datasheet parameters and external circuit parasitic and subsequent selection of an optimal value of the external drain source capacitance.

IX. Appendix

A. Comparison of proposed analytical model with existing models

The performance of the proposed analytical model is compared with the existing analytical models for soft turn off transient study. Minimum external drain source capacitance ($C_{ext(min)}$) to achieve soft switching, turn off transition time (T_{off}), switching loss (E_{off}) are the indices selected for

comparison. Among the existing analytical models [6], [8], [8] is used for comparison as this analytical model is more accurate when compared with [6]. Note, [6] considers soft turn off loss to be zero. Also, two different modes namely channel current collapse and drain current fall are not been analysed.

First the $C_{ext(min)}$ required to achieve soft switching is compared in Fig. 24 for two different SiC MOSFETs, S1 (C2M0160120D) and S2 (C2M0080120D) respectively. Operating conditions are $V_{dc} = 800V$, $R_{gext} = 7.5\Omega$ and $I_0 = 5-15A$ for S1 and $I_0 = 10-30A$ for S2. Values obtained from behavioural simulation is used as reference. It can be observed that the existing model grossly underestimates the value of $C_{ext(min)}$. On the contrary, the proposed analytical model can estimate $C_{ext(min)}$ with sufficient accuracy.

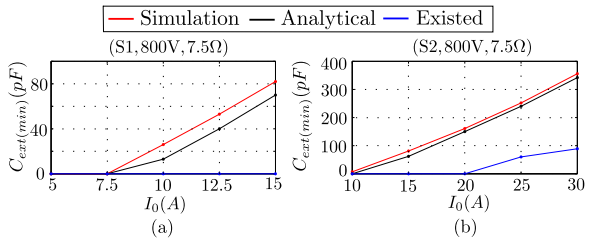

Fig. 24: Comparison of minimum C_{ext} required for soft switching using behavioural simulation, analytical model and existed model given in [8]: (a) S1, (b) S2

In the second part, T_{off} and E_{off} values obtained from behavioural simulation, proposed analytical model and existing model are compared for $V_{dc} = 800V$, $R_{gext} = 7.5\Omega$. $C_{ext} = 200pF$, $I_0 = 5-15A$ for S1 and $C_{ext} = 470pF$, $I_0 = 10-30A$ for S2 (see Fig. 25 and Fig. 26 respectively). Existing model grossly underestimate both T_{off} and E_{off} whereas numbers estimated using proposed analytical model are close to behavioural simulation.

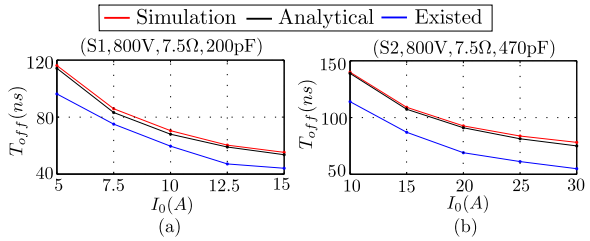

Fig. 25: Comparison of T_{off} estimated using behavioural simulation, analytical model and existed model given in [8]: (a) S1, (b) S2

From the above discussion it can be concluded that the proposed analytical model estimates $C_{ext(min)}$, T_{off} and E_{off} of SiC MOSFET accurately whereas the existing analytical model [8] lacks accuracy.

B. Turn off switching dynamics comparison with minimum R_{gext} and with/without C_{ext}

Here in the following discussion, two different cases are considered: a) permissible minimum R_{gext} and no C_{ext}, b)

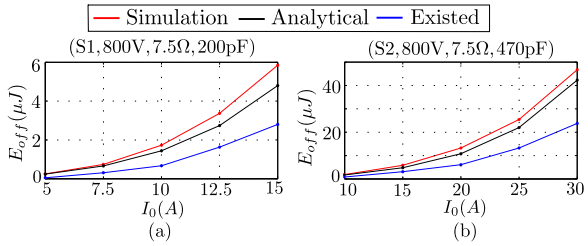

Fig. 26: Comparison of E_{off} estimated using behavioural simulation, analytical model and existed model given in [8]: (a) S1, (b) S2

permissible minimum R_{gext} along-with C_{ext}. C2M0080120D SiC MOSFET is considered with $V_{dc} = 800V$, $I_0 = 10-30A$ in steps of 5A and $R_{gext} = 2.5\Omega$ and $C_{ext} = 750pF$. Minimum permissible R_{gext} is selected such that the transient over-voltage is in permissible limit for $I_0 = 30A$ and C_{ext} is not present.

E_{off}, (dv/dt), (di/dt), $V_{ds((max)}$ with and without C_{ext} are compared in Fig. 27. E_{off} is estimated from behavioural model as it is not possible to obtain E_{off} directly from experiment. (dv/dt), (di/dt) and $V_{ds((max)}$ are estimated from experimental waveforms. It can be observed from both the results that with the external drain source capacitance $C_{ext} = 750pF$, E_{off}, (dv/dt), (di/dt) and $V_{ds(max)}$ has been significantly reduced. The charge and energy equivalent capacitances of C_{ds} in the voltage range (0,V_{dc}) are $130pF$ and $93.3pF$ respectively and it is small compared to $C_{ext} = 750pF$.

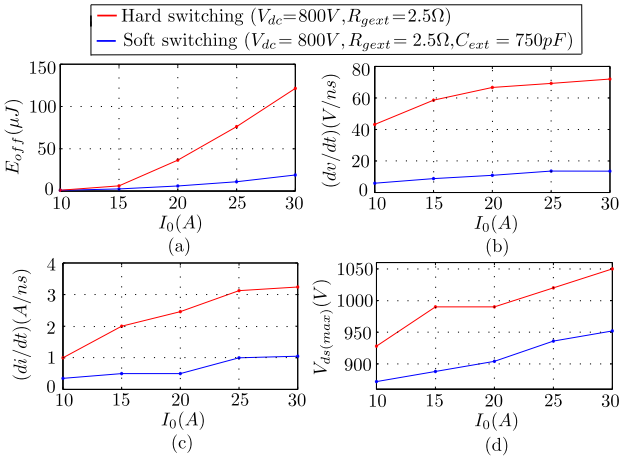

Fig. 27: Hard and soft switching performance comparison: (a) E_{off}, (b) (dv/dt), (c) (di/dt) and (d) $V_{ds(max)}$

The charge and energy equivalent capacitances of C_{ds} ($C_{ds(Q)}$ and $C_{ds(Er)}$) in the voltage range (0,$V_{dc} = 800V$) are compared with the value of the optimal external capacitor ($C_{ext(opt)}$) obtained in Section VII for both S1 and S2 in Table XI. It can be observed that $C_{ds(Q)}$ and $C_{ds(Er)}$ values are small compared to $C_{ext(opt)}$ for both S1 and S2.

TABLE XI: Comparison of $C_{ds(Q)}$ and $C_{ds(Er)}$ with $C_{ext(opt)}$

Device	$C_{ds(Q)}$ (pF) $(0, V_{dc})$	$C_{ds(Er)}$ (pF) $(0, V_{dc})$	$C_{ext(opt)}$ (pF)
S1	75	52.4	645
S2	130	93.3	1390

C. Comparison of behavioural models where C_{ext} is connected directly across C_{ds} and C_{ext} is connected across d' and s' nodes

In Table XII, E_{off} obtained from two different behavioural models ($E_{off(sim(a))}$ and $E_{off(sim(b))}$ for circuit configurations shown in Fig. 2(a) and Fig. 2(b) respectively) are compared for SiC MOSFET C2M0080120D (S2) with operating condition $V_{dc} = 800V$, $R_{gext} = 7.5\Omega$, $I_0 = 10, 20, 30A$ and $C_{ext} = 470, 750pF$. Also the percentage of error is calculated where $E_{off(sim(b))}$ is considered as standard. It can be observed that the approximate equivalent circuit of Fig.2(a) grossly underestimates E_{off}.

TABLE XII: E_{off} comparison

Device	C_{ext} (pF)	I_0 (A)	$E_{off(sim(b))}$ (μJ) (for Fig. 2(b))	$E_{off(sim(a))}$ (μJ) (for Fig. 2(a))	$Error$ (%)
S2	470	10	1.88	1	80.8
		20	13.25	11.5	14.7
		30	46.74	34.53	35.4
	750	10	1.66	0.95	74.6
		20	11.12	7.5	36.31
		30	32.1	28.4	12.97

Next, $V_{ds(max)}$ obtained using two different behavioural models and experiment ($V_{ds(max)(sim(a))}$, $V_{ds(max)(sim(b))}$ and $V_{ds(max)(exp)}$ respectively) are compared in Table XIII for the same device. The operating conditions are $V_{dc} = 800V$, $R_{gext} = 7.5\Omega$, $I_0 = 25, 30A$ and $C_{ext} = 470, 750pF$. It can be observed that the approximate equivalent circuit given in Fig. 2(a) underestimates $V_{ds(max)}$ for most of the operating conditions. On the contrary, $V_{ds(max)}$ values estimated using equivalent circuit model given in Fig. 2(b) are close to $V_{ds(max)(exp)}$.

TABLE XIII: $V_{ds(max)}$ comparison

Device	C_{ext} (pF)	I_0 (A)	$V_{ds(max)(exp)}$(V)	$V_{ds(max)(sim(b))}$ (V) (for Fig. 2(b))	$V_{ds(max)(sim(a))}$ (V) (for Fig. 2(a))
S2	470	25	952	946	908
		30	976	963	948
	750	25	944	932	878
		30	952	946	906

So from the above discussion it can be concluded that the behavioural model where the external drain source capacitance is directly connected across the drain-source depletion capacitance grossly underestimates E_{off} and $V_{ds(max)}$.

D. Difficulty in soft switching prediction using experimental measurement

$v_{g's'}(t)$ can be measured from experiment (Fig. 3) which is different from v_{gs} during switching transient as the drops $R_{gint}i_g$ and $L_s(di_s/dt)$ are significant (see (43)).

$$v_{g's'}(t) = v_{gs}(t) + R_{gint}i_g + L_s\frac{di_s}{dt} \tag{43}$$

$v_{g's'}(t)$, $v_{d's'}(t)$ and $i_{dc}(t)$ obtained from experiment ($v_{g's'(exp)}(t)$, $v_{d's'(exp)}(t)$ and $i_{dc(exp)}(t)$) and behavioural simulation ($v_{g's'(sim)}(t)$, $v_{d's'(sim)}(t)$ and $i_{dc(sim)}(t)$) are overlapped over each other in Fig. 28(a) for SiC MOSFET C2M0080120D. A close agreement is observed between behavioural simulation and experimental measurement. In Fig. 28(b), $v_{gs(sim)}(t)$, $v_{g's'(sim)}(t)$, $v_{d's'(sim)}(t)$, $i_{dc(sim)}(t)$ and $i_{ch(sim)}(t)$ obtained from behavioural simulation are plotted. It can be observed that $v_{g's'(sim)}(t)$ is smaller than $v_{gs(sim)}(t)$ for the entire switching transient period (see (43)).

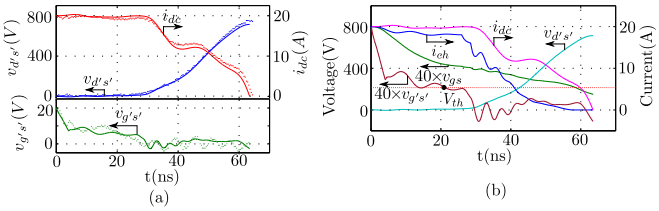

Fig. 28: Result for S2 (600V,20A,7.5Ω,200pF): (a) simulation and experimental result overlapped, (b) simulation result

In summery, $v_{g's'(exp)}(t)$ can be obtained from experimental measurement which is equivalent to $v_{g's'(sim)}(t)$ and both are significantly different from $v_{gs(sim)}(t)$. $i_{ch}(t)$ is a algebraic function of $v_{gs}(t)$ and it can not be estimated from experimentally measured $v_{g's'(exp)}(t)$.

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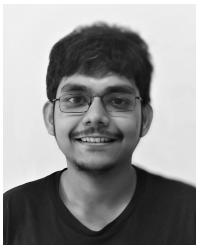

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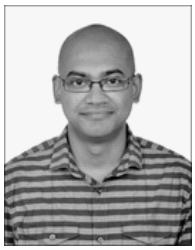

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