An Uni-directional Single Stage Single Phase Soft-Switched Resonant High Frequency Link Inverter

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***Abstract*—In this paper, a single stage High Frequency Link (HFL) uni-directional single phase inverter topology is reported for the application of grid integration of solar and fuel cells. The inverter supports only unity power factor operation. The converter is realized using a parallel resonant structure followed by a full bridge unfolder. This avoids undesirable voltage stress caused by parasitic ringing in PWM based approach. A hybrid modulation strategy - Variable Frequency Modulation (VFM) in most part of the line cycle, fixed frequency Pulse Width Modulation (PWM) near the zero crossing of line cycle is adopted here. The proposed modulation strategy provides the conditions for Zero Voltage Switching (ZVS) over most part of the line cycle and ensures that the variation of the switching frequency of the converter is within an acceptable range. A state plane based exact analysis is used for modulator implementation and design of the converter. Also, a design procedure is given that ensures minimization of the component stresses over the line cycle. The operation of converter is experimentally verified using a 3 kW hardware prototype.**

***Index Terms*—single stage, resonant converter, pulse width modulation, variable frequency modulation, parallel resonant, state plane analysis, fundamental harmonic approximation, phase shift modulation, zero voltage switching**

I. Introduction

High frequency link (HFL) single-phase inverter topologies are becoming popular in applications such as grid integration of rooftop solar and fuel cell based energy sources [1], [2]. A high frequency transformer (HFT) is employed here to provide galvanic isolation which helps to limit the ground leakage current [3], [4] and ensures safety. These HFL inverters employ either a multi-stage or a single-stage power conversion technique. A multi-stage HFL inverter [5] uses an isolated DC-DC stage followed by a DC-AC inverter where the interstage DC link is voltage stiff. Often an electrolytic capacitor is used in the interstage DC link leading to reliability issues. Additionally, the active switches in the grid side inverter are typically hard-switched resulting in higher losses. In single-stage power conversion, the interstage filtering is normally avoided. In literature the single-stage topologies are broadly classified in two categories- cyclo-converter based HFL (CHFL) and Rectifier type HFL (RHFL). In a CHFL topology [6]–[8], the output of the HFT is fed to a cyclo-converter for direct conversion of high frequency to line frequency AC . In a RHFL topology [9]–[11], the cyclo-converter is replaced by a rectifier and an inverter stage where the intermediate DC link is pulsating. In applications like grid integration of rooftop PV, power flow is uni-directional (DC to AC grid) and converter operates at unity power factor (UPF) [12], [13]. Here, it is possible to use uncontrolled diodes in the rectifier stage of RHFL topologies [14]. Fig. 1(a) shows schematic of a HFL inverter supporting UPF operation. Operation of the converter in $P_g - Q_g$ plane is shown in Fig. 1(b). The operation of this converter is similar to a boost converter based power factor correction circuit which can only accept active power at UPF. Predominantly pulse width modulation (PWM) is used for the generation of the sinusoidal line frequency AC voltage. In literature, dual active bridge (DAB) based single-stage HFL solutions are proposed for bi-directional power flow but require higher number of active devices [15]. The PWM based RHFL topologies suffer from over voltage

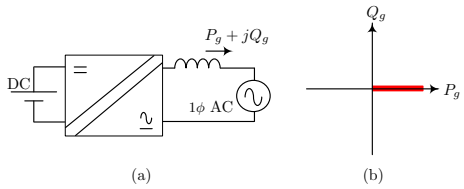

Fig. 1: (a) Isolated DC-AC converter (b) UPF operation shown in $P_g - Q_g$ plane

stress due to resonant oscillation caused by the interaction of the transformer leakage inductance and the device parasitic capacitances during the switching state transitions [16]. Hence additional snubber circuits are needed to protect the devices. Moreover these converters are either hard-switched or soft switched in a limited range of operation. Auxiliary circuits are essential to achieve soft switching over a wider range [17]. Both of these problems can be addressed using resonant power conversion [18] technique. Here, the parasitic elements participate in the power conversion process obviating need of snubbers. The wider range of soft switching enables increase in switching frequency which further increases the converter power density [19], [20].

Several resonant based HFL topologies are reported in literature, [21]. A single-stage, series resonance (SR) based

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CHFL topology is discussed in [22] which uses **V**ariable **F**requency **M**odulation (VFM). Similar SR based CHFL topology using fixed frequency **P**hase **S**hift **M**odulation (PSM) is presented in [23]. A Dual SR converter with a modified RHFL based line frequency unfolding topology using fixed frequency PSM is explored in [24]. It is well known that with the SR topology the wide range of gain variation is difficult to achieve [25]. Additionally, the SR converter suffers from poor light load regulation. A higher order (LCL) resonant based CHFL topology using PSM is investigated in [26]. A parallel resonance (PR) based CHFL topology using VFM is discussed in [27]. All these converters used the Fundamental Harmonic Approximation (FHA) based analysis as introduced in [25]. But the FHA based analysis is erroneous when the switching frequency varies widely which is essential to achieve wide variation of voltage gain [28], [29].

In this context, this paper has following contributions.

- A parallel resonance based unidirectional single-stage RHFL inverter topology is presented (Fig. 2).
- A novel hybrid modulation strategy is proposed here. It employs VFM for most part of the line cycle and uses PWM towards the zero crossing to limit the switching frequency variation in an acceptable range.
- The proposed modulation strategy ensures zero voltage switching (ZVS) of the DC side bridge over most of the line cycle and line frequency switching of the grid side converter.
- Unlike previous work, instead of FHA, a state-plane based exact analysis is used for modulator implementation and design of the converter. FHA uses only fundamental harmonic component of the applied square wave voltage to the resonant tank and neglects all other harmonics. Since, no such approximations are involved in state-plane analysis, it results in more accurate result.
- A design procedure based on exact analysis is provided which ensures overall minimization of RMS circulating current and component stresses.

A 3 kW prototype is built and tested. Part of this work was presented in [30]. The organization of this paper is as follows. Section II presents the operation of the converter and the modulation strategy along-with the detailed circuit analysis. The details of the converter design is given in section III. Key experimental results are presented to validate the design and modulation strategy in Section IV.

II. Modulation Strategy

In this section, the modulation of the converter to generate adjustable magnitude 1ϕ AC voltage at the output from input DC is discussed in detail.

The architecture of the converter is shown in Fig. 2. The **H**igh **F**requency DC-AC (HF DC-AC) converter is switched to generate a variable frequency quasi-square wave input to the L_r, C_r resonant tank. The high frequency transformer provides the galvanic isolation of the DC side from the grid. The tank voltage is rectified by the **D**iode **B**ridge **R**ectifier (DBR) and further inverted by the **L**ow **F**requency DC-AC (LF DC-AC) converter. Let the grid voltage be, v_g at a fundamental frequency, ω_g. The output voltage, v_o shown in Fig. 2 shall contain components at high frequency and the frequency, ω_g due to the synchronized nature of switching between the HF DC-AC and LF DC-AC converters. The objective of modulation is to ensure that the average value of v_o, denoted as $\overline{v_o}$ shall track a reference voltage, v_{ref} as given by the expression below

$$v_{ref} = V_{pk}\sin(\omega_g t) \tag{1}$$

The current through the filter inductor, i_o is assumed to be ripple free due to the presence of the inductor, L_f and shall be in phase with $\overline{v_o}$ due to the presence of the diode bridge. The expression for the current into the grid is given below

$$i_o \approx I_{pk}\sin(\omega_g t) \tag{2}$$

If P_g is the desired active power to be transferred to the grid, the grid with the filter inductor appears as a resistance, R_e as given in (3) and shown in Fig. 2.

$$R_e = \frac{V_{pk}}{I_{pk}} = \frac{V_{pk}^2}{2P_g} \tag{3}$$

The modulation strategy for the switches, S_5 to S_8 on the LF DC-AC bridge is to switch them in synchronization with the zero crossing of v_{ref} as shown in Fig. 3. The switching as per this modulation by the controller ensures that the average value of the voltage on the pulsating DC link, $\overline{v}$ is the rectified value of v_{ref}. Similarly, current i shall be rectified version of the output current, i_o as shown in Fig. 3. Let, V and I represent the value of the average link voltage $\overline{v}$ and link current i at a specific instant in time. The entire ciruit can be reflected on the secondary side of the converter as shown in Fig. 4(a). The LF DC-AC converter is represented by a current sink of magnitude, I and the average output voltage, $\overline{v}$ at this point in time is V. The quasi-square wave source, nv_{ab} is produced by the HF DC-AC bridge. Let the switching frequency of the HF DC-AC converter be f_s and the switching time, $T_s = \dfrac{1}{f_s}$. Let d represent the duty cycle in the operation of the converter.

The objective of the HF DC-AC modulation at this instant is to find f_s and d so that the average output voltage $\overline{v} = V$ is synthesized for a given $R_e = \dfrac{V}{I}$.

Before going ahead with the analysis to arrive at the required f_s and d for a particular operating point, the converter is per-unitized with respect to base parameters given in Table I. Based on this per-unitization, the converter parameters of interest are converted into their **P**er **U**nit (PU) values as given in Table II. The emulated resistance, R_e, in PU is the load quality factor, Q defined as given below

$$Q = \frac{R_e}{R_b} = \frac{R_e}{n\sqrt{\dfrac{L_r}{C_r}}} = \frac{M}{J} \tag{4}$$

where, M and J are as defined in Table II. The equivalent circuit of the converter as described in Fig. 4(a) can now be further reduced and shown in Fig. 4(b).

In Fig. 4(b), m_{ab} represents the PU voltage applied to the resonant tank and j_s represent the PU current input to the diode bridge, i_s, as shown in Fig. 4(a). The values of inductance

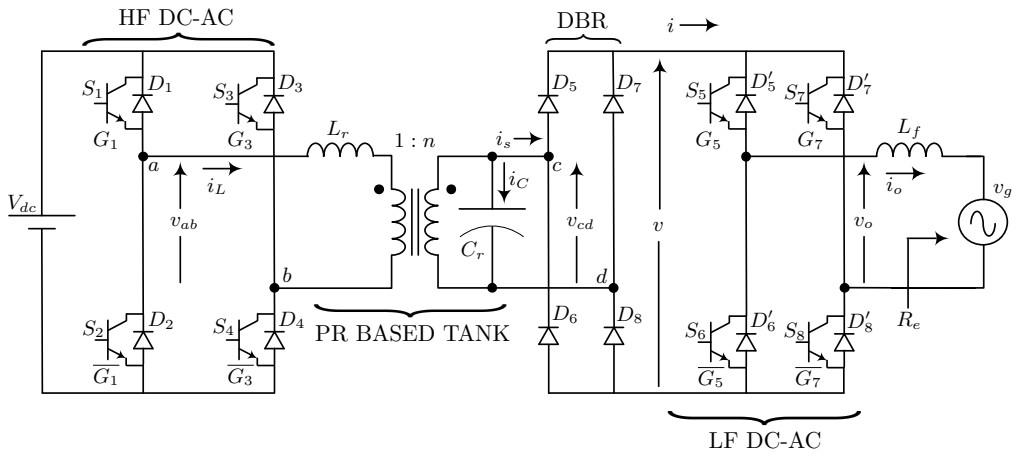


Fig. 2: Proposed **P**arallel **R**esonant (PR) based single stage unidirectional isolated DC-AC converter

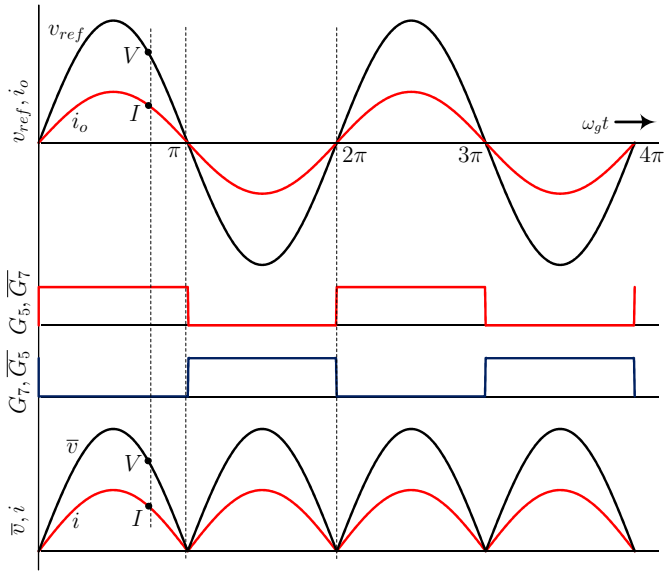


Fig. 3: Modulation of LF DC-AC Bridge

and capacitance is effectively reduced to unity by the per-unitization process. Different circuit operating modes shall be observed in this equivalent circuit based on the values of $m_{ab} = (0, \pm 1)$ and $j_S = (\pm J)$.

In Fig. 2, due to LF DC-AC, the absolute average output voltage $|\overline{v_o}|$ is same as the average rectifier output voltage, $\overline{v}$ as shown in Fig. 3. Due to the action of the diode bridge, this is also the absolute average value of the capacitor voltage, $|\overline{v_{cd}}|$. From Table II, voltage gain, $M = \frac{V}{V_b}$. Since V represents the output voltage at a specific instant in time as shown in

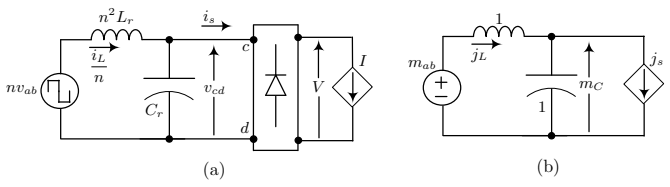


Fig. 4: Parallel Resonant structure of the HFL converter (a) Reduced circuit of the converter reflected onto the secondary side of transformer and LF DC-AC modeled as a current sink (b) Per-unitized equivalent circuit

TABLE I: Per-unitisation Base parameters

Description	**Formula**
Base Voltage, V_b	nV_{dc}
Base Impedance, R_b	$n\sqrt{L_r/C_r}$
Base Current, I_b	V_b/R_b
Base Frequency, f_b	$1/2\pi n\sqrt{L_r C_r}$

TABLE II: PU quantities

Description	**Formula**
Resonant capacitor voltage, m_C	v_{cd}/V_b
Resonant inductor current, j_L	i_L/I_b
Switching frequency, F	f_s/f_b
Angular half-period, γ	π/F
Output current, J	I/I_b
Voltage gain, M	V/V_b
Angle variable, θ	$2\pi f_b t$

Fig. 3, it can be seen that $M = \frac{|\overline{v_o}|}{V_b} = \frac{|\overline{v_{cd}}|}{V_b}$ and $m_C = \frac{v_{cd}}{V_b}$. Hence M at a particular switching frequency, F and $d = 1$ can be found by integrating m_C over the angular half-period, $M = \frac{1}{\gamma}\int_0^{\gamma} |m_C(\theta)| d\theta$. In **C**ontinuous **C**onduction **M**ode (CCM - when capacitor C_r is never clamped to zero voltage), the gain M, Quality factor, Q and PU switching frequency, F are related by (5) and (6), for $1 < F < 2$ [31].

$$M = \left(\frac{2F}{\pi}\right)\left(\delta - \frac{\sin\delta}{\cos\frac{\pi}{2F}}\right) \tag{5}$$

$$\delta = -\cos^{-1}\left(\cos\frac{\pi}{2F} + \frac{M}{Q}\sin\frac{\pi}{2F}\right) \tag{6}$$

Operation above resonant frequency ensures that ZVS conditions of the HF DC-AC bridge is met as far as the direction of the current is concerned. So, for a given R_e or Q in PU, one can find a PU frequency, F, so that average output voltage of $V = nV_{dc}M$ can be achieved. Based on (5), (6) it is possible to find a function, G as given below.

$$F = G_Q(M) \tag{7}$$

For a given Q, F increases as M reduces. For most part of the line cycle, v_{ref}, for a given active power to be transferred (P_g or Q), PU switching frequency, F is adjusted with $d = 1$ to achieve the required voltage gain. Hence, this is called VFM.

In comparison with known literature where VFM is applied for the entire period of a line cycle, the proposed strategy applies PWM instead of VFM towards the zero crossing. This limits the variation of frequency to a maximum value. It was found that the voltage gain (M) is inversely related with frequency (F) in VFM mode. So near zero crossings of $v_{ref}(t)$, when M becomes close to zero and the required frequency becomes twice the resonant frequency ($F = 2$), the proposed technique switches from VFM to PWM. Thus the maximum switching frequency of the converter is limited to twice the resonant frequency. To see this, for simplicity of analysis, let us assume no load ($Q \to \infty$) condition. From equation (5) and (6) we can write M as a function of F, (8) and then we can find dM/dF as a function of F, (9), as shown in Fig. 5. As expected the function is negative and after $F = 2$, small change in M requires very large change in F.

$$M|_{Q^{-1}\to 0} = \left(\frac{2F}{\pi}\right)\left(\tan\frac{\pi}{2F}\right) - 1 \tag{8}$$

$$\left.\frac{dM}{dF}\right|_{Q^{-1}\to 0} = \frac{2}{\pi}\tan\frac{\pi}{2F} - \frac{1}{F\cos^2\frac{\pi}{2F}} \tag{9}$$

Hence, towards the zero crossing of v_{ref} when gain is small, the switching frequency, F is kept constant at 2 and the duty cycle, d is modulated to achieve the required voltage gain. The technique is termed as PWM. Fundamental harmonic based analysis shows for a given Q and $F = 2$, the gain M_Q is given by (10).

$$M_Q = G_Q^{-1}(F = 2) \approx \frac{8}{\pi^2}\left(\frac{1}{\sqrt{9 + \frac{256}{\pi^4 Q^2}}}\right) \tag{10}$$

To achieve a gain below M_Q, based on FHA, duty cycle, d can be modulated as per (11). This is the PWM mode.

$$d = \frac{2}{\pi}\sin^{-1}\left[\frac{M}{M_Q}\right] \tag{11}$$

As the exact analysis of **P**arallel **R**esonant **C**onverter (PRC) for duty cycle modulated operation is not present in literature,

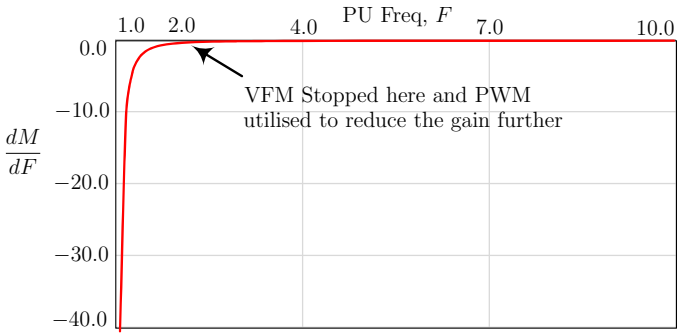


Fig. 5: Sensitivity, $\frac{dM}{dF}$ as a function of F

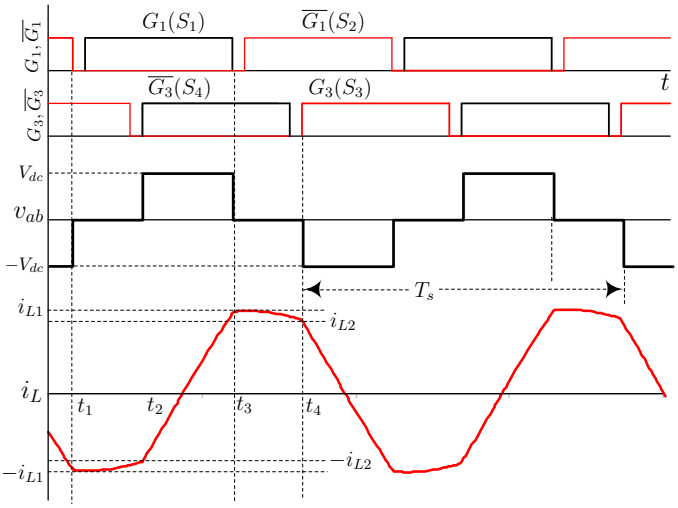


Fig. 6: LTSpice simulation of switching waveforms of the converter in PWM

FHA is employed in this mode. Numerical calculations show that the error introduced by this approximation is small. Also, note that M_Q is small compared with M_{pk} (V_{pk} in PU)) so that the PWM mode is much shorter than VFM mode over a line cycle. For the PWM mode of operation, it is not known theoretically if ZVS condition can be met. From extensive simulation using LTSpice it was found that for the most part, the inductor current in the resonant tank is in correct direction leading to ZVS. One such simulation result is plotted in Fig. 6 for $F = 2$, $Q = 1.2$ and $M = 0.18$. In this figure, G_1 is the drive signal for device, S_1. G_3 is the drive signal for S_3. Devices S_2 and S_4 switch in a complimentary fashion with regards to S_1 and S_3 respectively with a finite dead time as shown here. The pole voltage, v_{ab} is generated based on the phase relationship between S_1 and S_3. Over a switching cycle there are four switching transitions - two per each leg. The transitions of a leg are symmetrical. At every switching instant the pole current direction is such that after the turn OFF of an outgoing switch, the anti-parallel diode of the incoming switch conducts. Hence applying the turn ON gating pulse after a pre-fixed dead time ensures ZVS turn ON of all switches. For example when S_2 is turned OFF and after a time delay S_1 is turned ON, inductor current, i_L is negative ($i_L = -i_{L1} < 0$)

A. Modulation over a line cycle

The objective of the proposed modulation strategy is to generate desired adjustable amplitude and grid frequency voltage, $v_{ref}(t)$ at converter output through proper adjustment of frequency and duty cycle (F and d). The desired voltage is such that a specified active power, P_g, can be transferred to the grid approximately at unity power factor. This is assuming that the grid frequency component of the voltage drop across filter inductance L_f is negligible. Given grid voltage, $v_g(t)$ and P_g the desired grid current, i_{ref}, must be $\frac{2v_g(t)P_g}{V_{rms}^2}$. V_{rms} is the RMS value of the grid voltage $v_g(t)$. A current controller is fed the error between the sensed and desired grid current, in turn the controller generates the required voltage reference, $v_{ref}(t)$, which is shown in Fig. 7.

Fig. 7 also shows the flow-chart of how switching frequency, $F(t)$ and duty ratio, $d(t)$ are arrived at based on the required gain, $M(t)$ and M_Q. Given v_{ref}, one can arrive at the required PU gain, $M(t)$. Similarly, based on the power output, P_g, the quality factor, Q and in turn, M_Q can be deduced from (10). The choice of the particular operating mode is based on the value of $M(t)$ with respect to M_Q.

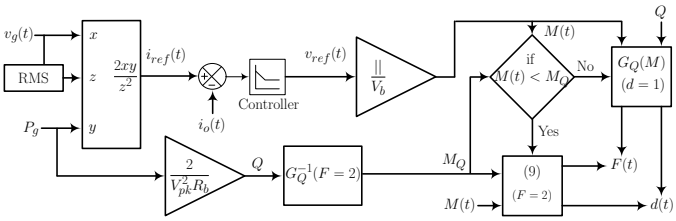


Fig. 7: Current control scheme of the proposed converter

As explained in Fig. 7, the gain of the converter, $M(t)$ shall vary over a line-cycle as given by the expression below

$$M(t) = M_{pk}|\sin(2\pi f_g t)| \tag{12}$$

As $M(t)$ varies from 0 to M_{pk} over a line cycle, appropriate modulation strategy as per Fig. 7 needs to be adopted. Fig. 8(a) shows the plot of (7) for two different values of Q. As gain, M increases from M_Q towards M_{pk}, the switching frequency of the converter, F is reduced to meet the required gain that satisfies (7) in VFM shown in Fig. 8(a). As M decreases from M_Q and moves towards 0, the switching frequency is held constant at $F = 2.0$ and the duty ratio of the converter, d is reduced from maximum value of 1 to 0 as per (11) in PWM. This variation in d with respect to M is plotted in Fig. 8(b) for two different values of Q. This modulation strategy shall now be applied for operation of the converter.

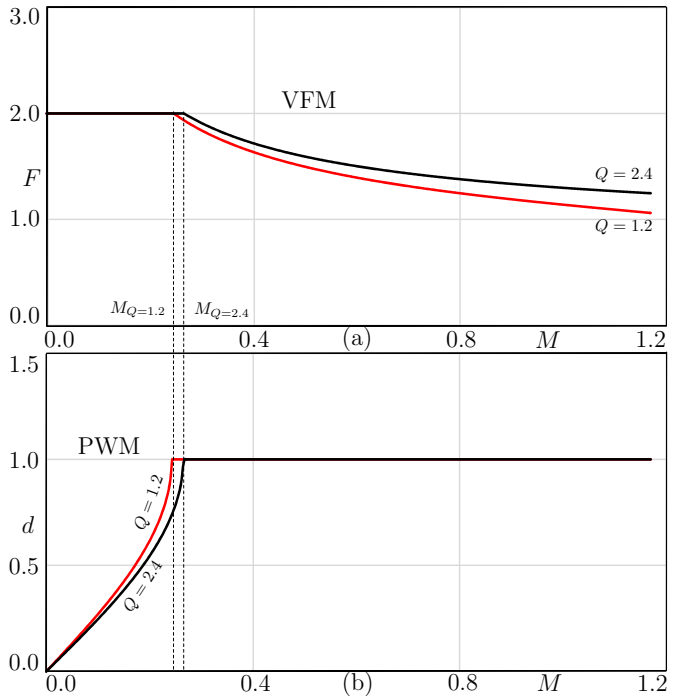


Fig. 8: Switching frequency, F and duty ratio, d as function of the converter gain, M for different value of Q

The variation of $M(t)$ over the line cycle is plotted in Fig. 9(a) where, M_Q is as defined in (10). The time variation of F and d over the line cycle is plotted in Fig. 9(b) and Fig. 9(c) respectively. It can be observed that close to the zero crossing of M, PWM is employed to achieve the required gain which is low. As seen from Table IV, PWM is employed less than 15% of a line cycle, near the zero crossings. In the rest of the line cycle, VFM is employed. Application of VFM and PWM as shown in $F(t)$ and $d(t)$ respectively results in the quasi-square wave modulation on the resonant tank input voltage, v_{ab} in Fig. 9(d). The response of the resonant tank is the sine frequency-amplitude modulated waveform shown as $v_{cd}(t)$ in Fig. 9(e). This is rectified by the DBR to generate the pulsating DC link voltage, $v(t)$ in Fig. 9(f). The switching on the LF DC-AC bridge inverts the pulsating DC link voltage to generate the inverter output voltage, $v_o(t)$ in Fig. 9(h) which has the desired line frequency component, $v_{ref}(t)$.

B. Switching function realization

After $F(t)$ and $d(t)$ are determined as shown in Fig. 7, generation of gating signals G_1 and G_3 for driving the switches is needed. Let v_1 and v_2 be two high frequency carriers as defined in (13) and (14) respectively where, $\omega_b = 2\pi f_b$ is base angular frequency. The carriers used by the modulator are

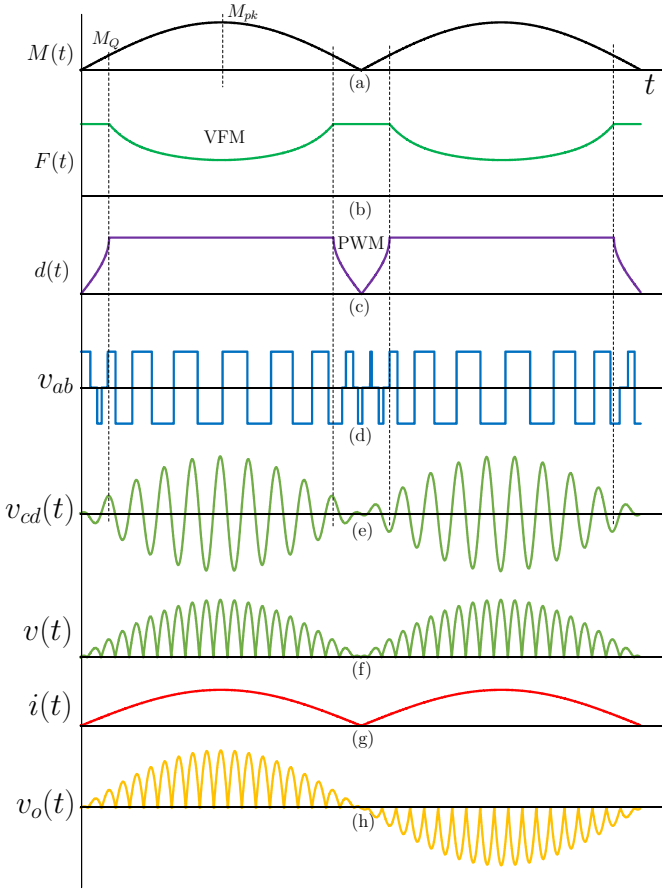
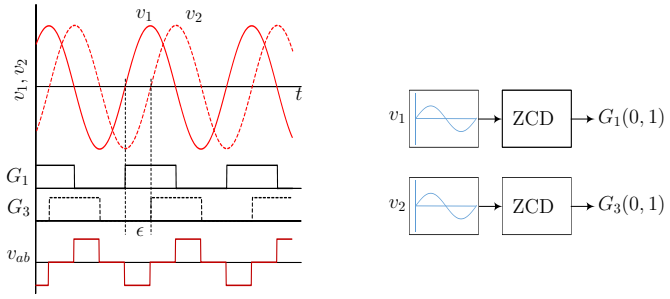


Fig. 9: Modulation of the converter and intermediate waveforms

TABLE IV: Angular range of PWM modulation over half of a line cycle for different value of Q

Q Value	PWM range in half line cycle(%)
1.2	13.5
1.6	14.0
2.4	14.4
4.8	14.8

shown in Fig. 10. ϵ shown in Fig. 10(a) is the phase difference between the carriers and here $\epsilon = \pi d(t)$. Frequency variation in VFM mode is achieved by varying F.



(a) PWM Waveform generation (b) Carrier based ZCD Circuit

Fig. 10: Carrier based modulation of the HF DC-AC converter

$$v_1 = \sin\left(\omega_b t F + \frac{\pi d}{2}\right) \tag{13}$$

$$v_2 = \sin\left(\omega_b t F - \frac{\pi d}{2}\right) \tag{14}$$

Switching functions, G_1 and G_3 shall be generated by passing these carriers through a **Z**ero **C**rossing **D**etection (ZCD) circuit as shown in Fig. 10(b). The output of the ZCD circuit will be a square wave of levels 0 and 1 with 50% duty cycle as shown in Fig. 10(a).

III. Design and Implementation

The previous section described the modulation of the converter. The design of the converter to achieve the desired operation is described here in detail. The specification given in Table V is considered for designing the components of the converter. The design of the converter entails arriving at values of the resonant tank components, L_r and C_r, transformer turns ratio, n. As VFM is applied most part of the line cycle to meet ZVS condition, operation above resonant frequency is considered. Fig. 12 shows the output (M, J) plane of parallel resonant converter of Fig. 4(b) for $F > 1$. To keep the operation in CCM, the region of operation must be to the right of the blue line in Fig. 12. The minimum value of

TABLE V: Converter Design specifications

Description	**Value**
Input Voltage V_{dc}	$390V$
Grid Voltage Peak $V_{g,pk}$	$325V$
Grid Frequency $f_g = 1/T_g$	$50Hz$
Power Output P_g	$3kW$
Max Switching Freq $f_{s,max}$	$120kHz$

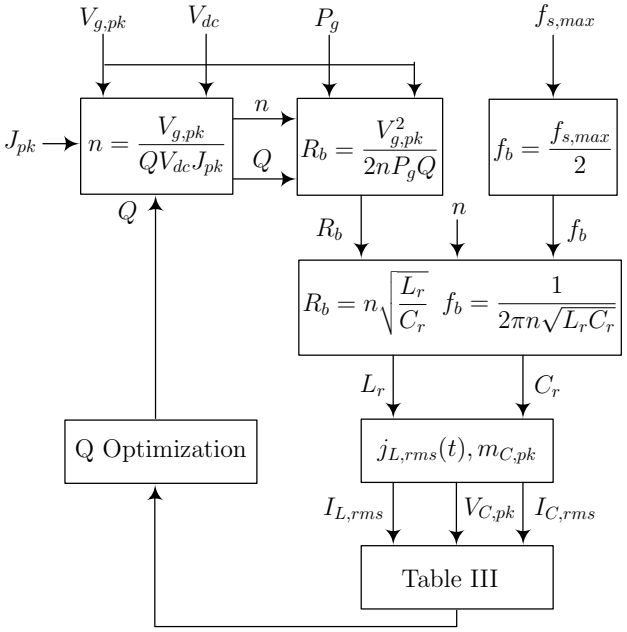


Fig. 11: Flow chart showing the converter design procedure

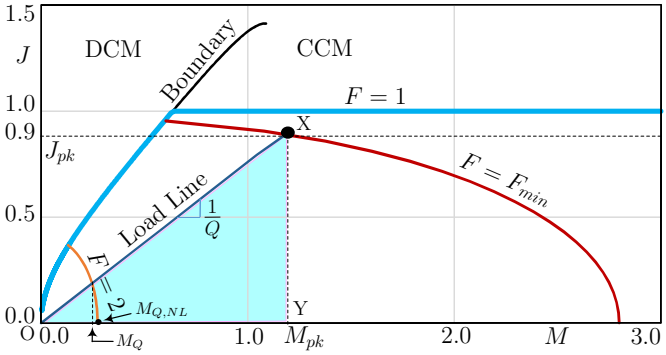


Fig. 12: Output plane of the PR converter for design

TABLE III: Design Optimization using Q as parameter

Q value	Xfmr ratio n	$L_r(\mu H)$	$C_r(nF)$	$I_{L,rms}(A)$	$V_{C,pk}(V)$	$I_{C,rms}(A)$
0.6	1.544	32.68	215.3	28.37	628.8	12.97
0.8	1.158	43.57	161.5	23.42	589.1	13.02
1.0	0.927	54.47	129.2	20.70	567.5	16.10
1.2	0.772	65.36	107.6	19.02	554.3	19.16
1.4	0.662	76.25	92.3	17.91	545.7	22.19
1.6	0.579	87.15	80.8	17.13	539.7	25.21
1.8	0.515	98.04	71.8	16.56	535.3	28.21

frequency, F_{min} happens at the maximum value of voltage, M_{pk}.The other boundary that fixes the region of operation in VFM is $F_{max} = 2$. As the switching frequency, F is varied in this region between $F = F_{min}$ and $F_{max} = 2$, the converter gain changes from M_{pk} to M_Q as shown in Fig. 12. From these two bounds and the maximum switching frequency specification it's possible to arrive at the desired base frequency, $f_b = \frac{f_{s,max}}{F_{max}} = \frac{1}{2\pi n\sqrt{L_r C_r}} = 60kHz$.

From (4), as $M = QJ$, over a line cycle the operating point will follow a line with slope $\frac{1}{Q}$, passing through the origin. This is depicted as "Load Line" in Fig. 12. The tip of this line represents (M_{pk}, J_{pk}) at the operating frequency, F_{min}. The intersection of the "Load Line" with the $F = 2$ curve represents the boundary between the PWM and VFM operation.

Once M_{pk} and J_{pk} are chosen the design can be completed as the component parameters are linked to this choice. For $F = 1$, in CCM, $J = 1$ as seen in Fig. 12. The choice of J_{pk} is made as a value less than $J = 1$ to remain in CCM but large enough to utilize the entire design plane for reducing the control sensitivity. So, J_{pk} is chosen as 0.9 to have operational margin. Following the flow chart in Fig. 11, for a choice of Q and J_{pk}, L_r, C_r and n can be estimated. Q is optimally designed to minimize the following

- **R**oot **M**ean **S**quare (RMS) Inductor current, $I_{L,rms}$ ($j_{L,rms}$ in PU)
- Peak capacitor voltage, $V_{C,pk}$ ($m_{C,pk}$ in PU)
- RMS capacitor ripple current, $I_{C,rms}$ ($j_{C,rms}$ in PU)

The conduction loss is related to the RMS inductor current. The RMS capacitor ripple current is an important parameter as the tank capacitor needs to provide this current and there's a limitation on it's maximum value. Given a particular value of Q, each of these parameters are arrived at by using analytical closed form expressions at a particular instant in time [31].

$$j^2_{L,rms}(t) = 0.5\left[3\frac{M^2(t)}{Q^2} + 1 + \frac{\sin^2\delta}{\cos^2\frac{\pi}{2F(t)}}\right] - \frac{2F(t)}{\pi}[a(t) + b(t)\delta(t)] \quad (15)$$

$$m_{C,pk}(t) = \begin{cases} \sqrt{(b(t)+1)^2 + (J(t)-a(t))^2} - 1, & a(t) > J(t) \\ \sqrt{1 + (J(t)-a(t))^2} + 1, & a(t) < J(t) \end{cases} \quad (16)$$

$$j^2_{C,rms}(t) = j^2_{L,rms}(t) - J^2(t) \quad (17)$$

where,

$$a(t) = -(J^2(t) - 1)\tan\frac{\pi}{2F(t)}$$

$$b(t) = -\frac{J(t)\sin\delta(t)}{\cos\frac{\pi}{2F(t)}}$$

In order to arrive at RMS value of the inductor and capacitor current, the expressions in (15) and (17) are integrated over the fundamental half line cycle as given below.

$$I^2_{rms} = \left[\frac{1}{0.5T_g}\int_0^{0.5T_g} j^2_{rms}(t)dt\right] I_b^2 \quad (18)$$

The choice of Q for which these values are evaluated is in the range $0.6 - 1.8$. Operation of the converter in DCM under both VFM and PWM modes must be avoided through design. To meet this requirement, values of Q below 0.6 are not considered for design as this shall result in "Load line" falling in DCM region as seen in Fig. 12. For values of Q above 1.8, the ripple current requirement in the capacitors goes up significantly and there are no commercially available parts that can supply that current.

The RMS inductor and capacitor current values are arrived at numerically. The peak capacitor voltage from (16) can be found by considering $F = F_{min}$. The value of Q that results in the least stress on the components is chosen as shown in Table III. The calculated stress values are plotted Fig. 13. It can be seen that the choice of $Q = 1.2$ provides the optimal value in the parameters of interest. The values of L_r, C_r and n corresponding to $Q = 1.2$ are chosen for the resonant tank and are tabulated in Table VI.

Capacitor peak voltage, it's ripple current and RMS inductor current values for optimization are tabulated in Table III. The values tabulated here are important for the design of the inductor and for selecting the capacitor.

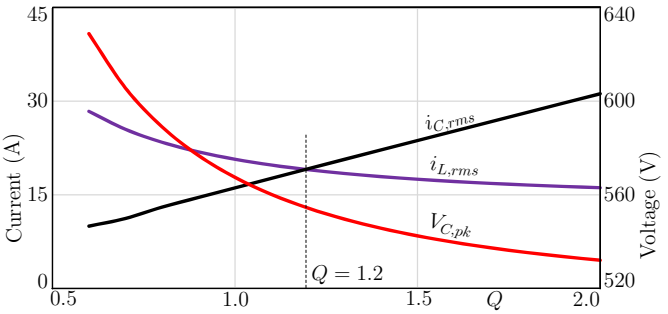


Fig. 13: Design optimization using Q parameter

TABLE VI: Component Design Values

Description	Value
Resonant Inductance, L_r	$65.36\mu H$
Resonant Capacitance, C_r	$107.6nF$
Transformer turns ratio, n	0.772

Note as load changes from full load, P_g to no load, the peak point of the "Load line" will move from X to Y in Fig. 12. The gain at transition, M_Q for full load $Q = 1.2$ is 0.249. At no-load, this value is $M_{Q,NL} = 0.273$. Note $M_{pk} = 1.2$, which remains independent of load variation. So, this implies that over the entire load range VFM is applied for most part of the line cycle. For the given specification of V_{dc}, $V_{g,pk}$, P_g and $f_{s,max}$, the design steps to estimate the tank parameters and the transformer turns ratio are presented as a flowchart in Fig. 11.

IV. Experimental Validation

The modulation strategy and it's implementation discussed in the previous sections is simulated using LTSpice and validated with an experimental prototype as shown in Fig. 14. Table VII provides the details of the various components

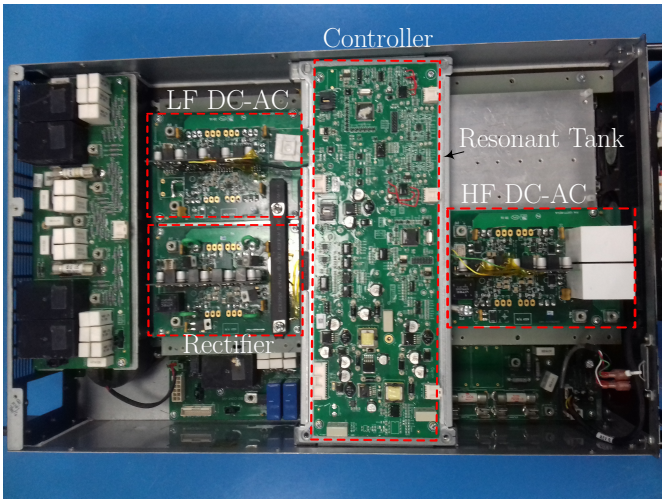


Fig. 14: Hardware Prototype

TABLE VII: Prototype Component details

Description	Value
Active Switches	IRGP50B60PD
Diodes	IDW30S120
Resonant Inductor	31 Turns, Ferrite Core - EE80-38-20
Transformer	Turns ratio ($N_1 : N_2$) - 20:14
Resonant Capacitor	WIMA FKP1 series, 2X4 bank of 100 nF
Filter Inductance	31 Turns, AMCC40 Core

used in the hardware prototype. The switching frequency of HF DC-AC is varied between $60kHz$ and $120kHz$. The resonant frequency of the converter is $60kHz$. The required PWM signals for both HF DC-AC and LF DC-AC converters is generated from a controller based on the TMS320F2808 μController. An effective dead time of $750ns$ is provided between the switching of devices on the same leg.

The converter is now operated under open loop as per the conditions given in Table V. As shown in Fig. 7, $v_{ref}(t)$ comes from the output of the current controller. Following analysis shows how in open-loop operation, the $v_{ref}(t)$ is generated from the specifications of grid peak $V_{g,pk}$, reference power P_g and inductive line impedance, X_f. This converter can support only instantaneous unidirectional power flow. The equivalent circuit and the phasor diagram of the grid interface is shown in Fig. 15. $V_{g,pk}$ is the peak of the grid voltage

$$V_{pk}\angle 0^\circ = V_{g,pk}\angle -\phi + jX_f I_{pk}\angle 0^\circ \tag{19}$$

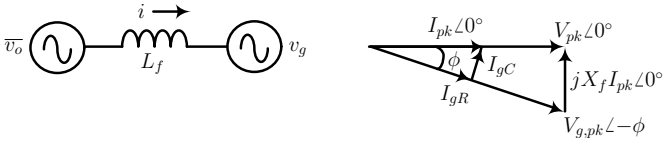


Fig. 15: Equivalent circuit and phasor diagram of the converter

(19) can now be solved based on the output power, $P_g = \frac{V_{pk}I_{pk}}{2}$ to arrive at the magnitude of the output voltage, V_{pk}.

$$V_{pk} = \left(\frac{V_{g,pk}^2}{2} + \sqrt{\frac{V_{g,pk}^4}{4} - 4X_f^2 P_g^2}\right)^{(1/2)} \tag{20}$$

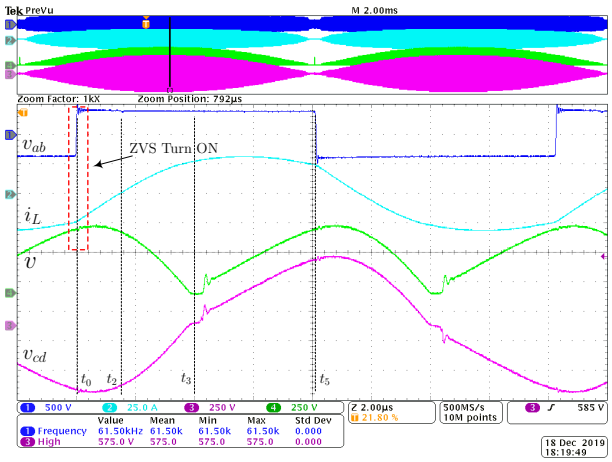
where, X_f is the inductive reactance at the fundamental frequency, f_g and V_{pk}, I_{pk} correspond to the peak values of the inverter output voltage v_o and i respectively (Fig. 15). The line current i leads the grid voltage, v_g by $\phi = \cos^{-1}\left(\frac{V_{pk}}{V_{g,pk}}\right)$. Once V_{pk} is estimated the reference voltage v_{ref} is given by (1). In case of an open loop implementation $\omega_g t$ in (1) is given by a free running counter.

Following analysis shows how grid can emulated with a parallel RC network for the intended operation. As seen from the phasor diagram in Fig. 15, the line current has a component in phase with the grid voltage, $I_{gR} = I_{pk}\cos\phi$ and another component in quadrature, $I_{gC} = I_{pk}\sin\phi$. Hence the grid can be emulated with a parallel RC network where $R = \frac{V_{g,pk}}{I_{gR}}$ and $C = \frac{I_{gC}}{\omega_g V_{g,pk}}$.

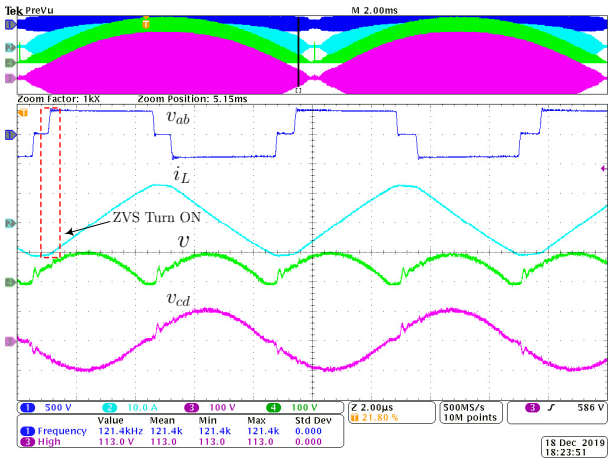
A. Experimental Validation of converter operation

This section presents the key results from the experimental data. The converter is operated under the conditions given in Table V. The peak of output voltage generated by the converter given is $325V$. The expected peak output current under this condition is $I_{pk} = \frac{2P_g}{V_{pk}} = 18.44A$. Fig. 17 shows the actual grid voltage, v_g in [CH1] and current, i_o in [CH2] from the experiment. These waveforms match the expected voltage and current as shown in Fig 3 in section II. [CH3] in Fig. 17 shows the envelope of the output voltage, v_o and [CH4] shows the pulsating DC link voltage, v. These waveforms match the prediction in Fig 9(f) and Fig 9(h) respectively in section III. Near the zero crossing of the line current i_o, voltage spikes are observed in v_o waveform. The sudden change in filter inductor current (i_o) for the switching action of H-bridge ($S_5 - S_8$) near the current zero crossing causes these voltage spikes. These spikes can be avoided either by a using overlap between the gating signals of switches of the H-bridge legs or using a snubber circuit across the intermediate pulsating DC link.

The operation of the converter in the VFM mode is shown in Fig. 16(a). The individual waveforms shown here are zoomed into to highlight the switching cycle variation over the fundamental half line cycle. [CH1] is the applied tank input voltage, v_{ab}. Since the zoom is close to the peak of the AC waveform, the measured switching frequency, $61.5kHz$ is close to the resonant frequency, $60kHz$. The switching frequency is above the resonant frequency to ensure ZVS as indicated in dotted lines. It's also clear that the duty ratio of the applied waveform is unity. The inductor current waveform, i_L in shown in [CH2] and the capacitor voltage, v_{cd} in [CH3]. Different operating modes based on the switching instants and the circuit changeover due to the secondary diode conduction reversal can be observed in these waveforms. [CH4] shows the



(a) VFM - [CH1] 500 V/div,[CH2] 25 A/div,[CH3] 500 V/div,[CH4] 250 V/div



(b) PWM - [CH1] 500 V/div,[CH2] 10 A/div,[CH3] 100 V/div,[CH4] 100 V/div

Fig. 16: Waveforms that indicate the Variable Frequency Modulation (VFM) and Pulse Width Modulation (PWM) of the converter - [CH1] Tank voltage - v_{ab}, [CH2] Inductor current - i_L, [CH3] Capacitor voltage - v_{cd}, [CH4] DC Link voltage - v

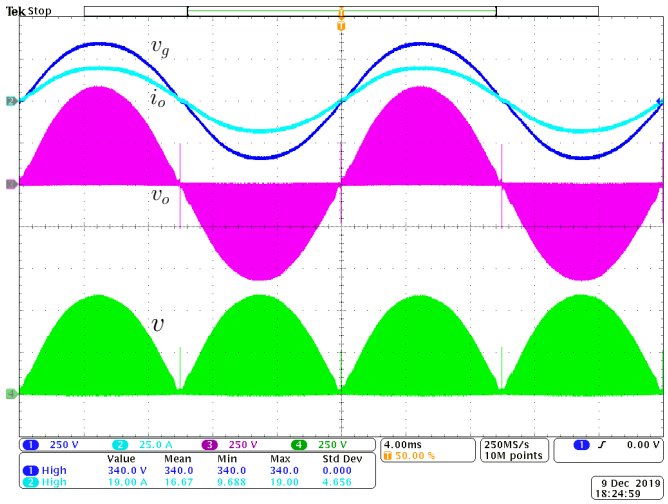


Fig. 17: Waveforms of converter operation - [CH1] Grid Voltage, v_g (250 V/div), [CH2] Output Current, i_o (25 A/div), [CH3] Output Voltage, v_o (250 V/div), [CH4] DC Link Voltage, v (250 V/div)

high frequency component in the pulsating DC link voltage. This verifies the operation of the diode bridge rectifier.

The operation of the converter in the PWM mode is shown in Fig. 16(b). [CH1] to [CH4] in this plot is the same as in Fig. 16(a). The portion of zoom in this plot is close to the zero crossing in the fundamental half line cycle where PWM is applied. The measured switching frequency is $121kHz$ close to the maximum switching frequency of $120kHz$. The applied duty ratio is less than 1 and based on the required voltage close to the zero crossing. The variation in the switching frequency, f_s and duty ratio, d over the line cycle can now be understood. The switching frequency, f_s is minimum close to the peak of the line voltage as shown in Fig. 16(a) and maximum close to the zero crossing as shown in Fig. 16(b). The duty cycle is unity close to the peak of the voltage and moves towards 0 close to the zero crossing as shown in 16(b). This validates the proposed modulation strategy.

The pole voltage waveform, v_{ab} indicating the changeover from PWM to VFM and vice versa is described in Fig. 9(d). Fig. 18(a) and Fig. 18(b) shows the experimental waveform that validates the transition between the modes. Tank input voltage, v_{ab} is shown in [CH1] and the inductor current, i_L is shown in [CH2]. The grid voltage, v_g is shown in [CH3] and the DC link voltage, v is shown in [CH4]. The transition from VFM to PWM happens when the switching frequency in the VFM mode is close to the maximum switching frequency, $120kHz$ as seen in Fig. 18(b). Similarly, the transition from PWM to VFM mode happens when the duty cycle of the tank input voltage, v_{ab} approaches 1. This can be observed in [CH1] of Fig. 18(a).

B. Experimental validation of soft-switching

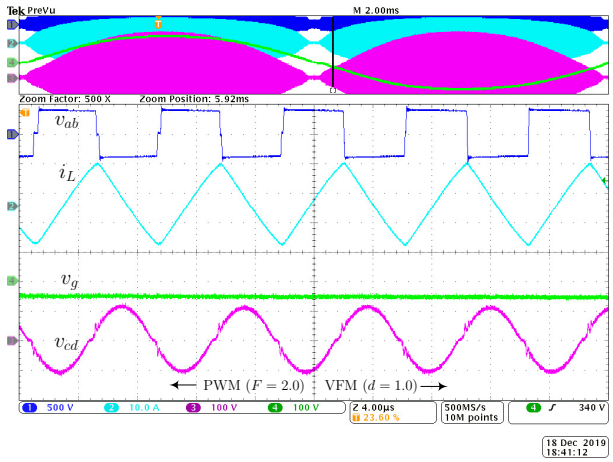
Fig. 19 presents ZVS turn ON of S_1. Before $t = t_0$, S_2 is conducting the pole current i_L. At t_0, S_2 is turned OFF (as the gating signal G_2 becomes low). The presence of device capacitance ensures ZVS turn OFF of S_2. As seen from Fig. 19, after t_0 i_L remains negative. i_L charges and discharges the device capacitances across S_2 and S_1 respectively. At t_1, when the voltage across S_1, v_{ea} becomes zero, the anti-parallel diode of S_1 is forward biased and starts conducting. At t_2, the gating pulse of S_1, G_1 is applied (when the body diode is in conduction) to ensure ZVS turn ON. At t_3, i_L changes its direction and S_1 starts conducting. A dead time of $.75\mu$s between $G_1 - G_2$ ensures these ZVS transitions.

C. Effect of variation of load and tank parameters

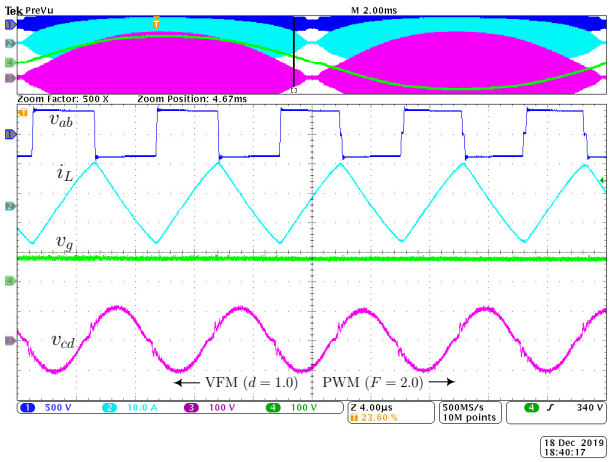
TABLE VIII: Effect of load variation on operational parameters

Q Value	M_Q	F_{min}	Load (%)
4.80	0.269	1.289	25
2.40	0.265	1.246	50
1.60	0.258	1.169	75
1.20	0.249	1.059	100

Fig 20 shows the experimentally obtained output voltage and grid current waveforms for four different values of loading (25% to 100%) with input 300V DC. The effect of load



(a) Transition from PWM to VFM



(b) Transition from VFM to PWM

Fig. 18: Waveforms that indicate transition between the operating modes, VFM and PWM - [CH1] Tank voltage, v_{ab} (500 V/div), [CH2] Inductor current, i_L (10 A/div), [CH3] Capacitor voltage, v_{cd} (100 V/div), [CH4] Grid voltage, v_g, (100 V/div)

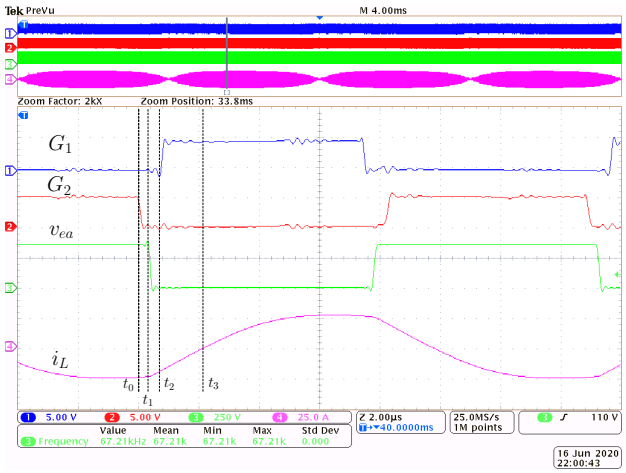


Fig. 19: ZVS turn ON of the device S_1- [CH1] Gate Signal, G_1 (5 V/div), Gate Signal, G_2 (5 V/div), [CH3] S_1 Drain source voltage, v_{ea} (250 V/div), [CH4] Inductor current, i_L (25 A/div)

TABLE IX: Effect of tank component variation on the gain

L_r Value (μH)	C_r Value (nF)	Grid Current Peak (A)
65.4	107.6	18.5
63.4 (-3%)	104.4 (-3%)	19.6 ($+6\%$)
63.4 (-3%)	110.8 ($+3\%$)	19.1 ($+3\%$)
67.3 ($+3\%$)	110.8 ($+3\%$)	17.4 (-6%)
67.3 ($+3\%$)	104.4 (-3%)	18.0 (-3%)

variation on F_{min} and M_Q is shown in Table VIII. With the decrease in load, Q increases. Hence the slope of the load line in Fig. 12 is changed, leading to a change in F_{min}. From (10), it is seen that with the increase in Q, M_Q increases. Table IX presents the effect of variation (upto $\pm 3\%$) of L_r and C_r on the output power. It is observed that, the grid current peak changes $\pm 6\%$ due to the change in the nominal tank gain. This table shows simulated results.

D. Converter soft-start up

To avoid initial inrush current a gradual soft-start process is followed here and is shown in Fig. 21. At t_0, the converter is started in PWM mode with low voltage gain. After some time

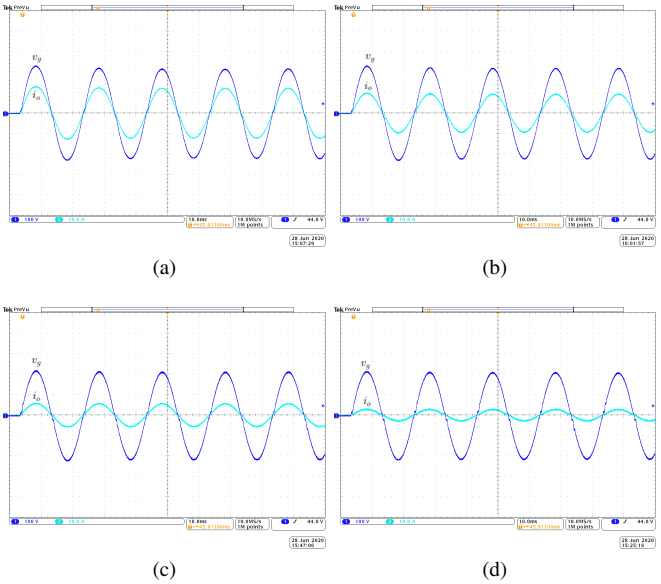


Fig. 20: Output waveforms showing load variations, [CH1] Grid voltage, v_g (100 V/ div), [CH2] Output Current, i_o (10 A/ div) (a) 100% Load (b) 75% Load (c) 50% Load (d) 25% Load

at t_1, mode changeover happens and the converter is switched to the VFM mode of operation.

E. Closed loop control

The closed loop scheme shown in Fig. 7 is simulated in LTspice at rated power. A PI controller is designed with the parameters $K_p = 100$, $K_i = 40000$. Fig. 22(a) shows the simulated grid voltage and output current. As seen from the result in Fig. 22(b) the output current is perfectly tracking the reference current signal.

F. Measured power quality

Table X presents the grid current THD at different output power. Fig. 23 shows the harmonic spectrum of the grid current at rated power. It is seen that the THDs at all power are less

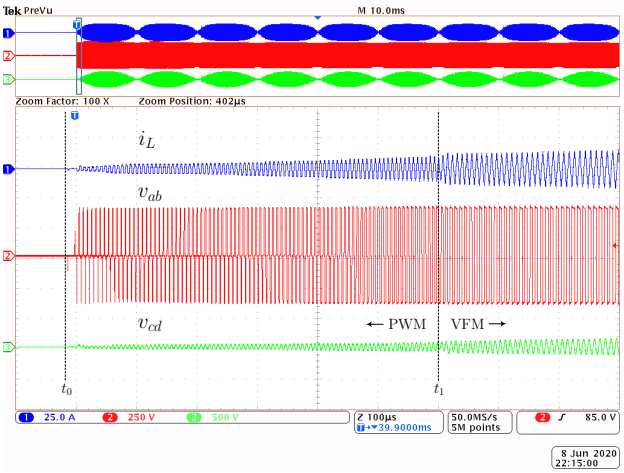


Fig. 21: Waveform indicating the startup strategy as converter starts in PWM mode and transitions to VFM mode [CH1] Inductor current, i_L (25 A/div), Tank Voltage, v_{ab} (250 V/div), [CH3] Capacitor voltage, v_{cd} (500 V/div)

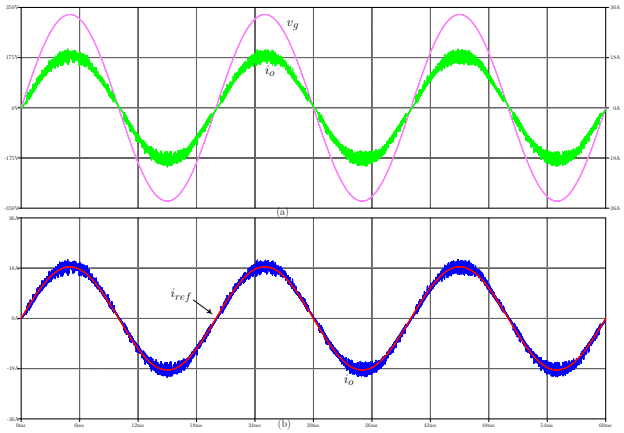


Fig. 22: Closed loop control. Grid voltage (v_g), grid current i_o and current reference (i_{ref}).

than 5% which confirms good power quality at the grid port.

TABLE X: Measured current THD at different power

AC Power (W)	THD (%)
760.0	3.68
1508.8	2.33
2111.4	1.93
2950.0	1.55

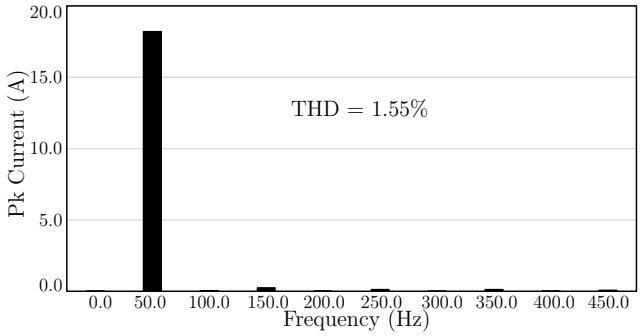


Fig. 23: Frequency Spectrum of the output current at rated power

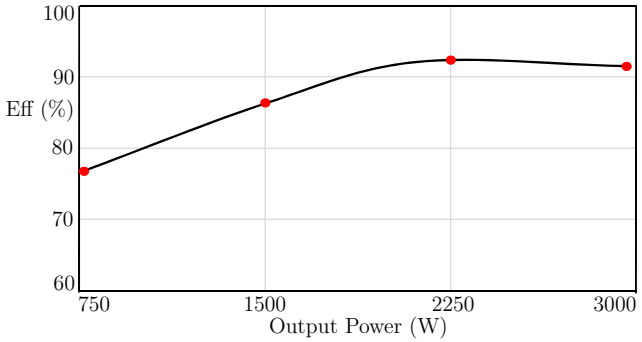


Fig. 24: Variation of the converter efficiency with the output power

G. Power loss and efficiency

Fig. 24 shows the measured efficiency of the converter. The efficiency is measured for a variation of output power between 0.75kW to 3kW. The converter has a peak efficiency 92% at 2.25kW output power. The converter power loss is also analytically estimated. As the converter is soft-switched, only the conduction losses of the power devices are considered here. The device parameters like on state resistance, voltage drop are obtained from corresponding device datasheet. The average and RMS currents through the devices are estimated using simulation. At the rated power of $3kW$, the analytically estimated power loss is $274W$, whereas the experimentally measured value is $269W$. Thus the analytical estimation method is experimentally validated. The loss distribution, obtained analytically at the rated power in different components of the converter, is shown in Fig. 25. As the prototype is not optimally designed at the rated power, the converter has relatively low efficiency.

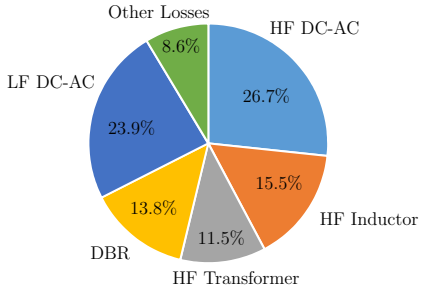


Fig. 25: Loss distribution in the proposed single stage converter

H. Performance comparison with existing topology

The proposed topology is compared with an existing single-stage parallel resonant based CHFL topology [27] and a conventional multi-stage topology (a parallel resonant converter followed by a single phase inverter with interstage DC bus filter capacitor). Both the proposed topology and [27] employ same number of active devices. But [27] uses four-quadrant active switches which results in implementation complexities. From the topology perspective [27] has issues like, DC bus capacitor voltage unbalance, more number of resonant tank components, lower transformer utilization, voltage stress and non-ideal operation due to transformer leakage. These issues are completely avoided in the proposed topology. The total

number of active devices and diodes of the proposed topology is same as the multi-stage topology. The device RMS currents of the proposed topology are either comparable or slightly higher than the multi-stage topology. Hence the proposed topology has comparable conduction loss with the multi-stage topology. The DC side converters of both the topologies are zero voltage switched. The grid interfaced converter of the proposed topology is line frequency switched incurring negligible switching loss whereas it is high frequency hard-switched in multi-stage topology. Hence the proposed topology has better efficiency compared to the multi-stage. Additionally, unlike the multi-stage topology, the interstage electrolytic filter capacitor is avoided in the proposed configuration which reduces filtering requirement and improves reliability and power density.

V. Conclusions

In this paper, a parallel resonant based high frequency link inverter is presented which supports only UPF operation. It was found that through proposed hybrid modulation and design it is possible to limit the variation in frequency within a factor of two to achieve the required gain variation. The soft-switching conditions, as far as the direction of current is concerned is met for most part of the line cycle by operating above resonant frequency. Through simulation and experiment it was found that the condition is also met for the small part of the line cycle for which fixed frequency duty cycle modulation is employed. Part of the converter is line frequency switched incurring minimal switching loss. State-plane based exact analysis is used to determine frequency necessary to achieve a particular gain. A design procedure to determine resonant tank component values and turns ratio of the high frequency transformer is presented. In the exact analysis based design a degree of freedom is used to minimize the RMS circulating current and component stresses over the line cycle. This work presents a way using zero crossing detectors to generate gating pulses to synthesize a variable frequency variable pulse width output voltage using a H bridge inverter. A closed loop scheme is presented here, which is also verified in simulation. Experimental validation of this scheme and stability analysis is considered as future work. With inherent advantages of resonant approach: utilization of transformer parasitic to power transfer and wider ZVS range, this isolated single stage solution provides a safe, compact, reliable and efficient solution for grid integration of alternative energy sources like solar and fuel cell.

Appendix

A. Converter design with 48V input DC

A 1kW design with 48V input DC (rooftop solar output) is presented here. Other design parameters are same as in Table V. Following the design procedure presented in section III, the resonant tank parameters and transformer turns ratio are estimated and presented in Table XI.

TABLE XI: Component Design Values

Description	Value
Resonant Inductance, L_r	$3.0\mu H$
Resonant Capacitance, C_r	$2.35\mu F$
Transformer turns ratio, n	6.0

B. State-plane Analysis of PRC

The analysis of the **P**arallel **R**esonant (PR) converter gain is given below. The analysis of the PR converter is done at a DC operating point. The per-unitization base parameters and the PU quantities to be used in the analysis is given in Table I and Table II respectively. The equivalent circuit of converter at this operating point and the per-unitized model is given in Fig. 4(a) and Fig. 4(b) respectively. The operation of the converter in steady state can now be explained as follows

- In the equivalent circuit of Fig. 4(b), the input voltage, m_{ab} is ± 1 and the load current, j_s is $\pm J$ based on the sign of the capacitor voltage, m_C. This results in 4 modes of operation as seen in Fig. 26.
- The two state variables, j_L and m_C, evolve sinusoidally with resonant frequency in each of these modes..
- Fig. 26 shows the m_{ab}, j_s, j_L and m_C waveforms for $F > 1$ in a switching cycle. Here, $\gamma = \frac{\pi}{F}$
- In the state-plane j_L and m_C are plotted together as a point. The curve traced by this point is a circle in each mode with centre at (m_{ab},j_s). As there are four modes in a switching cycle, in steady state the point in state-plane traces a closed trajectory with four circular arcs. This is shown in Fig. 27.
- The Output voltage is obtained through rectification of capacitor voltage waveform, m_C
- Through trigonometric analysis of Fig. 27, it's possible to arrive at the expression for the converter gain as given in (5). Please refer to [31] for details of the derivation.

C. Comparison of FHA and State Plane analysis

For a given load $Q = 1.2$, to synthesis the desired voltage gain M, the computation of frequency F is done using both state-plane and FHA based analysis. Here the peak of v_{ref} is 325V. As seen from Table XII, the state plane based method synthesizes better output voltage waveform with desired peak and low THD.

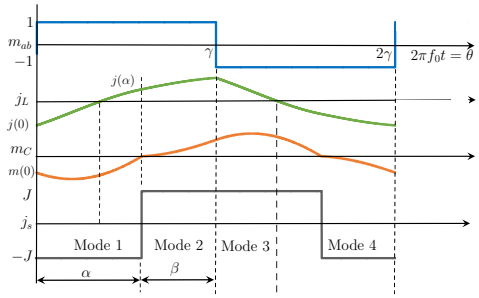


Fig. 26: Different circuit modes of operation within one switching cycle of the PR converter

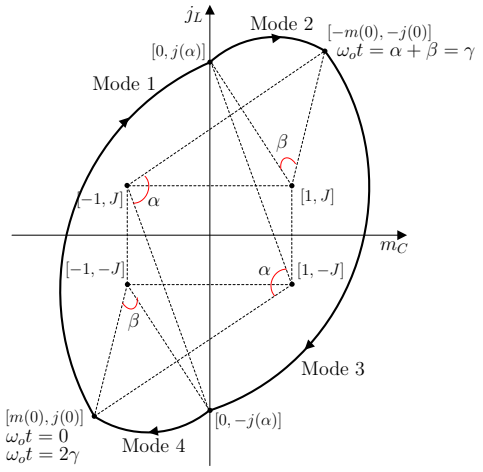


Fig. 27: State plane portrait of the Parallel Resonant converter

TABLE XII: Comparison of State plane analysis and FHA

Method	THD(%)	Peak (V)
FHA	4.1	320
State Plane	0.7	325

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