Hardware Emulation of Energization of a Long Transmission Line by High Frequency Power Electronic Converter

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***Abstract*—Hardware emulators, simulating a test environment in real-time, are an essential tool in testing power system equipments. This paper presents a hardware emulator of a programmable transmission line capable of simulating high frequency transients. Emulation of, energization of long transmission line, requires the observer to solve transmission line or telegraphers equations in real-time. The paper identifies a continuous time model that captures the wave nature and suitable for real-time implementation. Paper derives the discrete time model to be solved in the observer of the hardware emulator. A step by step procedure is given to determine two key emulator parameters: observer sampling frequency and switching frequency of the power amplifier considering different hardware, event and software related constraints. For high bandwidth requirement, a high switching frequency, 100 kHz, 12 kVA SiC based voltage source converter is designed to operate under a current controller with a gain cross over frequency of 5 kHz. A SoC that combines an ARM processor along with a FPGA, is used to implement the observer. Experimental results verify accuracy of the designed emulator in the event of energization of a long transmission line. Though proposed TLE can only be used to study the energization of a long line with one end terminated with shunt reactor, the solution can be extended for emulation of a long line that links two sections of power grid.**

***Index Terms*—Hardware emulator, power hardware in loop, transmission line energization, SiC based power amplifier**

I. Introduction

IT is difficult to perform direct on-field-tests of power generation and transmission equipments. So, it is necessary to simulate the test environment in real-time. This is usually done through real-time digital simulators. A control hardware under test can be interfaced with a real-time digital simularor through Analog to Digital (A/D) and Digital to Analog (D/A) converters. The signals received from the ontrol hardware under test are processed in real-time by real-time digital simulator in accordance to a mathematical model representing the emulated test environment. This is called hardware in loop testing [1]–[4]. A power apparatus can also be tested in real-time by inserting a Power Amplifier (PA) between the real-time digital simulator and the power hardware under test. The PA is usually realized with a power electronic converter and such a test setup is known as Power-Hardware-In-The-Loop (PHIL). PHIL to emulate test environments such as photo-voltaic system [5], variable speed wind turbine with doubly fed induction generator and permanent magnet synchronous machine emulation [6] has been done. Various kind of faults in a grid has also been emulated [7]. Testing of microgrids by PHIL technology is reported in [8], [9]. The most expensive component of PHIL is the real-time digital simulator like OPAL-RT, Typhoon-HIL, RTDS, dSPACE or RT-Box etc. Usually this type of real-time digital simulator is capable of real-time simulation of a complex test environments like large power system network. In general the real-time digital simulator, in PHIL test set-up, finds the current reference to be tracked by the power amplifier from the sensed voltage signal, by solving the electrical characteristics of the emulated environment, or plays the role of the observer. To emulate a specific test environment a real-time controller (DSP or FPGA) can be programmed to perform as an observer. This type of emulated test environment, as shown in Fig. 1, is known as hardware emulator. Hardware emulator of synchronous generator and electrical load has been reported in [10], [11] and [12]–[14] respectively. Hardware in loop of an induction machine is attempted in [15].

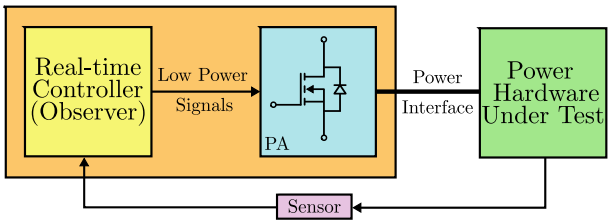

Fig. 1. Schematic of a hardware emulator

Being the fundamental element of the power system, hardware emulator for transmission line is required to bridge the gap between the source (synchronous generator) and load emulators. Hence a programmable Transmission Line Emulator (TLE) needs to be developed which will have the flexibility of emulating transmission line with varying line parameters. The general architecture of a TLE is shown in Fig. 2 [16]–[18]. The two major components of this setup are the observer and the PA. With the line end voltages ($v_{se(J)}$ and $v_{re(J)}$) as the input, the observer solves the transmission line model in

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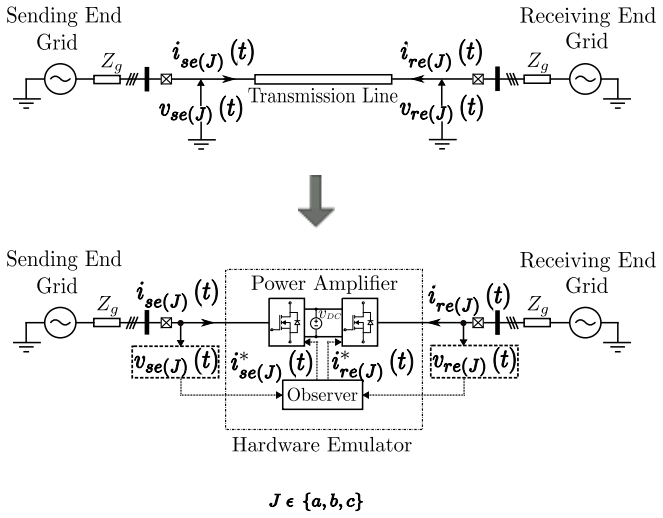


Fig. 2. General architecture of a transmission line emulator

real-time and estimates the line end currents. These currents ($i^*_{se(J)}$ and $i^*_{re(J)}$) are then tracked by the PA by controlling its output currents.

The PA is comprised of two back-to-back connected 3ϕ Voltage Source Converters (VSCs) operating under closed loop current control. Based on similar architecture, emulation of short lossless transmission line during steady state has been reported in [16], [17]. The transmission line is modeled as a lumped inductor and is emulated by the VSCs using two approaches, namely, phasor domain model and time domain model. In [18], a TLE for symmetrical 3ϕ fault emulation of short lines has been reported. In [19] a TLE is developed for emulation of three-phase symmetrical fault at an arbitrary point of a long transmission line. To capture the distributed nature of a long line, a model based on method of characteristics is used in [19], which is taken from [20]. As voltages and currents are computed at intermediate points of the transmission line and this helps in determining the initial conditions required for post fault emulation in [19].

This paper focuses on the design of TLE for emulation of transients in a long line with a shunt reactor connected at the open end. In this PHIL test set-up, the sending grid which is switched on to the transmission line is the device under test (DUT). As we are moving towards converter-based generation [21], DUT could be one or a group of voltage source inverters interfacing wind or solar based sources to the grid. The transient currents during energization need to be supplied by the DUT, while the voltage at the point of common coupling will also be distorted. It is important that these group of converters (DUT) does smoothly ride-through this transient. The proposed TLE will serve as a test setup. The paper makes following contributions.

- Unlike previously studied phenomena like power-flow or fault, this paper attempts at the emulation of the energization of a long transmission line.
- As a first step through simulation, the paper identifies a transmission line model that is suitable for real-time implementation on an embedded platform. It also ensures faithful reproduction of the transient phenomenon under study.
- The derivation of the discrete time version of the identified model to be solved in the observer of the hardware emulator is then presented in the paper.
- A step by step method has been developed for the determination of two key parameters a) Sampling frequency of the observer and b) Switching frequency of the power amplifier, considering hardware and software related constraints.
- Due to high bandwidth requirement a SiC based power converter along with a resonant based closed loop controller are designed for the implementation of the power amplifier. Both the observer and controller are implemented on Zynq 7000 a System on Chip (SoC) platform from Xilinx.
- A test setup and a suitable test procedure for the emulation of energization has been developed.

The organization of the paper is as follows : Section II provides the modelling of a distributed parameter lossy transmission line suitable for emulation of high frequency transients. Section III describes the details of implementation of the real-time observer on an embedded platform. Simulation of the developed observer in MATLAB/Simulink is shown in Section IV. Section V deals with scaling of the actual transmission line to laboratory level emulator. Details of the controller design for the PA has been discussed in Section VI. The proposed test bench setup for the TLE is given in Section VII. Finally the relevant simulation and experimental results are provided in Section VIII followed by conclusion in Section IX. Though the proposed TLE is meant for emulation of energization of a long transmission line only, appendix A gives a brief outline how the presented design can be extended to a general TLE of Fig. 2.

TABLE I
PARAMETERS OF THE ACTUAL TRANSMISSION LINE UNDER STUDY

Parameter	Value
3ϕ Line-Line (RMS) voltage of sending end grid, $V_{LL(RMS)}$	400 kV
Nominal grid frequency, F_{line}	50 Hz
Apparent power rating of the system, $S_{3\phi}$	500 MVA
Line inductance per unit length, L	1 mH/km
Line capacitance per unit length, C	12.96 nF/km
Line resistance per unit length, R	0.03 Ω/km
Line length, l	400 km
Shunt reactor inductance, L_{sh}	10.2 H
Grid impedance (Inductive), Z_g	80 Ω
Grid inductance, $L_g = \frac{Z_g}{2*\pi*F_{line}}$	0.25 H
Switching instant	Positive peak of a phase voltage

II. MODEL SELECTION

In PHIL emulator design, one of the most important tasks is to identify a model of the emulated system (here transmission line). A more complex model ensures accurate results but at the cost higher computation burden. We need to identify a

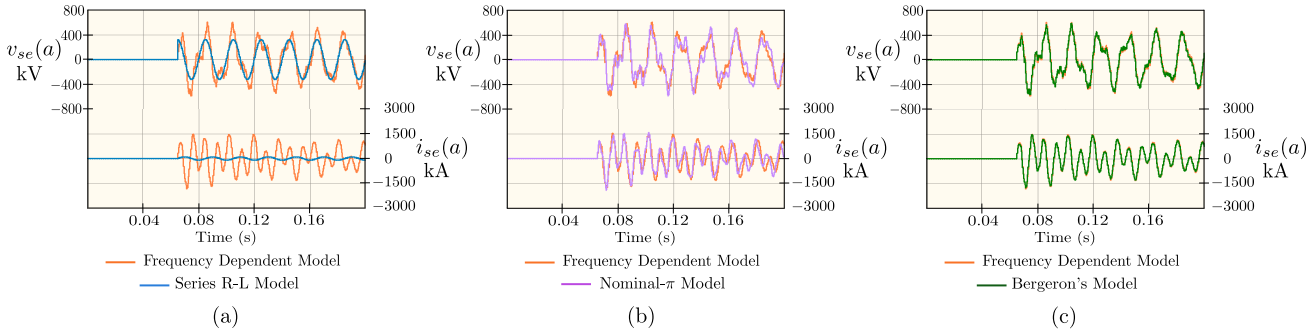


Fig. 3. Waveforms for the switching of the circuit shown in Fig. 4 at the positive peak of the a phase voltage with the parameters given in Table-I using (a) FDM and R-L Model, (b) FDM and Nominal-π Model and (c) FDM and Bergeron's model in PSCAD software

$$i_{se(J)}(t) = C_1 v_{se(J)}(t) \underbrace{-C_2 v_{se(J)}(t-\tau) - C_3 i_{se(J)}(t-\tau) - C_4 v_{re(J)}(t-\tau) - C_5 i_{re(J)}(t-\tau)}_{I_{s(J)}(t-\tau)} \quad (1)$$

$$i_{re(J)}(t) = C_1 v_{re(J)}(t) \underbrace{-C_2 v_{re(J)}(t-\tau) - C_3 i_{re(J)}(t-\tau) - C_4 v_{se(J)}(t-\tau) - C_5 i_{se(J)}(t-\tau)}_{I_{r(J)}(t-\tau)} \quad (2)$$

model that is computationally least challenging but results in faithful reproduction of the event under consideration.

A simple series connected resistance and inductance (R-L) model is fairly accurate for the short lines (length (l) $<$ 80 km), but not sufficient for the medium or long lines. For medium lines (80 km $< l <$ 250 km), the nominal-π lumped parameter model can be used for steady state analysis but it fails to generate appropriate results during transients. For long lines ($l >$ 250 km), both R-L and the nominal-π model are inadequate for producing the correct result during the transients as well as in the steady state conditions. The circuit diagram for energization of a transmission line with a shunt reactor connected at the other end is shown in Fig. 4. The breaker B is closed at the positive peak of the a phase of the grid voltage. The simulation is done in PSCAD software using the Frequency Dependent Model (FDM) [22] with a set of parameters given in Table-I. The subscripts se and re denotes the sending and receiving end of the transmission line respectively.

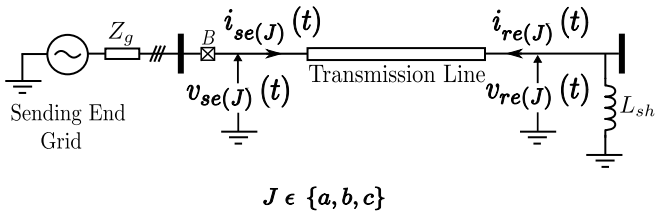


Fig. 4. Circuit schematic of voltage switching of an unenergized transmission line with shunt reactor connected at the receiving end

The FDM of the PSCAD has been taken as the benchmark model and compared with R-L and nominal-π models for the same parameters provided in Table-I. The mismatch in the sending end voltage and current of the 'a' phase are shown in Figs. 3(a) and 3(b). Therefore for lines above 250 km, one must consider the fact that the parameters are not lumped but rather distributed.

Among the numerical schemes that capture distributed nature of the line, the model in [19] and Bergeron's model are considered. Both are derived using method of characteristics in solving telegrapher's equations. Compared to the method used in [19], in Bergeron's model, series resistance is considered only in lumped form and shunt conductance is neglected. It is shown in appendix D, in emulation of energization of a long transmission line with one end terminated with shunt reactor, Bergeron's model is more computationally efficient compared to the scheme used in [19]. In this work Bergeron's model is selected as the numerical scheme to solve the transmission line in real-time and emulate by a VSC. In Bergeron's model, the terminal currents $\left(i_{se(J)}(t) \text{ and } i_{re(J)}(t) \text{ where } J\epsilon\ \{a,b,c\}\right)$ at time t can be computed using (1) and (2) from the knowledge of the the terminal voltages $\left(v_{se(J)}(t) \text{ and } v_{re(J)}(t)\right)$ and the values of these quantities at retarded time instant $(t-\tau)$, where $\tau = \frac{l}{c}$ is the wave travel time, l is the length of the line and $c = \frac{1}{\sqrt{LC}}$ is the velocity of the wave. R, L and C are the line resistance, inductance and capacitance per unit length respectively. The coefficients C_{1-5} can be computed using the line parameters as shown in Table-VI, in the appendix C, where $Z_c = \sqrt{\frac{L}{C}}$ is the characteristic impedance of the line and $R_T = lR$ is the total line resistance. $v_{seg(J)}(t)$ is the grid voltage.

Model to be Implemented in Embedded Platform

(3) and (4) can be written by considering the circuit configuration of Fig. 4 at the sending and receiving end of the line respectively.

$$v_{se(J)}(t) = v_{seg(J)}(t) - L_g \frac{\mathrm{d}i_{se(J)}(t)}{\mathrm{d}t} \quad (3)$$

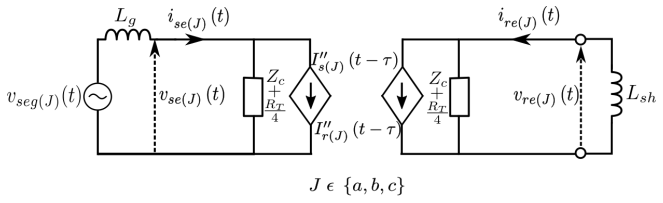


Fig. 5. Equivalent Network of the Transmission Line

$$v_{re(J)}(t) = -L_{sh}\frac{\mathrm{d}i_{re(J)}(t)}{\mathrm{d}t} \tag{4}$$

The equivalent circuit based on (1), (2), (3) and (4) is shown in the Fig. 5, where $v_{seg(t)}$ is the grid voltage, L_g is the grid inductance and L_{sh} is the inductance of the shunt reactor connected at the receiving end.

III. Implementation of Observer on Embedded Platform

The observer computes the current reference ($i_{se(J)}(t)$) to be tracked by the power amplifier by sensing $v_{seg(J)}(t)$. The observer is implemented on an embedded platform to digitally compute the current reference in discrete time. In this section we first determine the set of difference equations to implement the circuit shown in Fig. 5. We also will outline a step-by-step procedure for determination of two key parameters namely a) sampling time period of the observer (T_{ob}) and b) the switching period (T_{sw}) of the VSC.

A. Discretized Equation of Bergeron's Model

For digital implementation, τ must be an integral multiple of T_{ob} in order to avoid the complex interpolation schemes, [23]. Hence substituting $\tau = NT_{ob}$, $t = kT_{ob}$ (where k is the discrete time index) and defining $i_{se(J)}[k] = i_{se(J)}(t = kT_{ob})$, (1) and (2) can be written as,

$$\begin{aligned} i_{se(J)}[k] &= C_1 v_{se(J)}[k] - C_2 v_{se(J)}[k-N] - \\ & C_3 i_{se(J)}[k-N] - C_4 v_{re(J)}[k-N] - C_5 i_{re(J)}[k-N] \end{aligned} \tag{5}$$

and,

$$\begin{aligned} i_{re(J)}[k] &= C_1 v_{re(J)}[k] - C_2 v_{re(J)}[k-N] - \\ & C_3 i_{re(J)}[k-N] - C_4 v_{se(J)}[k-N] - C_5 i_{se(J)}[k-N] \end{aligned} \tag{6}$$

(5) and (6) demands the use of three memory buffers for each phase of the transmission line to store the past values of the sending end voltages, currents and receiving end currents. Therefore the size of the First In First Out (FIFO) buffers should be atleast N. Using Backward Euler on (4) and (3) we can write,

$$v_{re(J)}[k] = -\frac{L_{sh}}{T_{ob}}\left(i_{re(J)}[k] - i_{re(J)}[k-1]\right) \tag{7}$$

and

$$v_{se(J)}[k] = v_{seg(J)}[k] - \frac{L_g}{T_{ob}}\left(i_{se(J)}[k] - i_{se(J)}[k-1]\right) \tag{8}$$

Substituting $v_{re(J)}[k]$ and $v_{se(J)}[k]$ using (7) and (8) respectively into (5) and (6), we derive (9) and (10). The constants are defined in Table-VII in the appendix C.

$$\begin{aligned} i_{se(J)}[k] &= C_6 v_{seg(J)}[k] + C_7 i_{se(J)}[k-1] + C_8 v_{seg(J)}[k-N] \\ &+ C_9 i_{se(J)}[k-N] + C_{10} i_{se(J)}[k-N-1] \\ &+ C_{11} i_{re(J)}[k-N] + C_{12} i_{re(J)}[k-N-1] \end{aligned} \tag{9}$$

$$\begin{aligned} i_{re(J)}[k] &= C_{13} i_{re(J)}[k-1] + C_{14} i_{re(J)}[k-N] \\ &+ C_{15} i_{re(J)}[k-N-1] + C_{16} v_{seg(J)}[k-N] \\ &+ C_{17} i_{se(J)}[k-N] + C_{18} i_{se(J)}[k-N-1] \end{aligned} \tag{10}$$

Equation (8) - (10) *are solved in real-time to implement the observer.* $v_{seg(J)}[k]$ *is the input,* $i_{se(J)}[k]$ *and* $i_{re(J)}[k]$ *are the state variables and* $v_{se(J)}[k]$ *and* $i_{se(J)}[k]$ *are the outputs.*

TABLE II
Instruction Cycle Requirements by the Zynq SoC

Instructions	Number of cycles
Load and Store, n_{ls}	3
Multiplication, n_{mul}	5
Subtraction, n_{sub}	4
Addition, n_{add}	4
Move, n_{mov}	2
Compare, n_{cmp}	3

B. Determination of Observer Computation Time

Xilinx make Zynq System-on-Chip (SoC) has been selected as the embedded platform which has an ARM Cortex-A9 based Processing System (PS). The required number of instruction cycles for execution of different operations or instructions has been listed in the Table-II, [24]. We assume that the 3ϕ transmission line is balanced and transposed throughout its length. So we calculate the line end currents for two phases and the third one is taken as the negative sum of the other two phases. This reduces the computational burden for real-time implementation. The number of instructions to be executed in every observer computational cycle can be found considering the following steps :

- Feed the latest sending end grid voltage of the a and b phase of the transmission line. $[2 \times n_{ls}]$
- Referring (9), seven multiplication and six addition are involved for calculating the sending end current for each a and b phase. $[14 \times n_{mul}\ ,\ 12 \times n_{add}]$
- Referring (10), six multiplication and five addition are involved for calculating the receiving end current for each a and b phase. $[12 \times n_{mul}\ ,\ 10 \times n_{add}]$
- Referring (8), one multiplication and two subtraction are involved for calculating the sending end line voltage for each a and b phase. $[2 \times n_{mul}\ ,\ 4 \times n_{sub}]$
- $N + 1$ number of shifting operations in the memory buffers of the sending end grid voltage and current of a and b phase, so that it can be recycled and used. $\left[4 \times (N+1) \times n_{mov}\right]$

- $N+1$ number of shifting operations in the memory buffers of the receiving end current of a and b phase, so that it can be recycled and used. $\left[2\times(N+1)\times n_{mov}\right]$
- Sending end current calculation for the c phase. $\left[2\times n_{sub}\right]$

The shifting operation in the memory buffers is done by a counter, which needs to be incremented and compared with the reference value. Denoting the instruction clock period of the PS as $T_{clk(PS)}$ (which is 6 ns for the selected processor), the total computational time required by the observer (T_{obc}) can be written as,

$$T_{obc}=T_{clk(PS)}\left[277+19N\right]\approx\left(1.66+\frac{114}{1000}\frac{\tau}{T_{ob}}\right)\mu s \tag{11}$$

C. Determination of Frequency Content of the Sending End Line Currents during the Switching Instant

The FFT analysis of the sending end current waveforms generated from the Bergeron's model of PSCAD for the case discussed earlier has been done at the switching instant of the line, choosing the time window till the transients die down completely. The result of the FFT analysis is shown in Fig. 6. The maximum frequency content ($F_{i(max)}$) in the sending end line currents is found to be nearly 500 Hz.

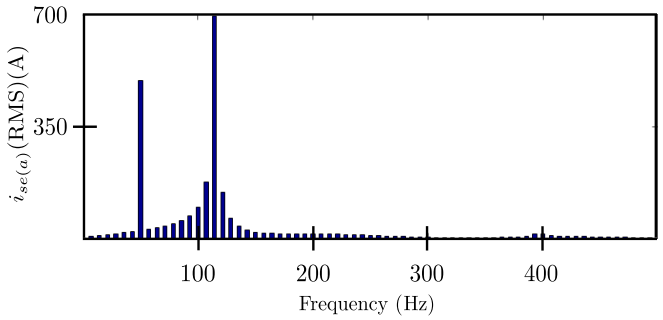


Fig. 6. Harmonic analysis of the a phase sending end current of Bergeron's model of PSCAD

D. Determination of T_{ob} and T_{sw}

1) Constraints on Switching Period of the Voltage Source Converter: The switching frequency of the converter (F_{sw}) is kept atleast 10 times higher than the current control loop bandwidth to minimize the phase-loss of the current control loop gain, which is again kept at 10 times the maximum frequency of the current signal to be tracked. So we can say that the minimum value of the switching frequency,

$$F_{sw(min)}=100\times F_{i(max)}=50\text{ kHz}$$
$$\Rightarrow T_{sw(max)}=20\ \mu s\ \geq T_{sw} \tag{12}$$

Silicon Carbide (SiC) based converter is designed to operate at a maximum switching frequency of 100 kHz. So

$$\therefore T_{sw(min)}=10\ \mu s\ \leq T_{sw} \tag{13}$$

2) Determination of Wave Travel Time: The length of the transmission line is considered to vary from 300 km to 500 km. The wave velocity for the chosen line with the parameters shown in Table-I is 2.78×10^5 km/s. Considering a standard set of line parameters [25], the range of wave velocity is found to vary from 2.5×10^5 km/s to 3×10^5 km/s. So the minimum wave travel time,

$$\tau_{min}=\frac{300}{3\times10^5}=1000\ \mu s \tag{14}$$

Similarly the maximum wave travel time,

$$\tau_{max}=\frac{500}{2.5\times10^5}=2000\ \mu s \tag{15}$$

3) Constraints on Observer Sampling Period: Observer digitally simulates the transmission line in real-time, by sampling the sending end voltage, $v_{seg(J)}[k]$, and computing the current reference, $i^*_{se(J)}[k]$. According to sampling theorem, the sampling frequency must be at least twice that of the largest frequency component present in the input signal, here $v_{seg(J)}$, in order to avoid aliasing. This implies the input signal must be band-limited. If this is not the case, we need to pass it through a low pass filter, also known as anti-aliasing filter. In present case during energization when the breaker (B in Fig. 4) is closed there is a step change in the input signal, which theoretically contains all frequency components. In the current waveform, which is the output here, we have seen that there is no component beyond 500 Hz. Since the system (Bergeron's model) is a linear system, therefore we can say that it acts as a low pass filter with a cut-off frequency of 500 Hz. So, we will come up with the same current waveform even if we remove the components beyond 500 Hz from the input step voltage and apply it to the system (Bergeron's model). The cut-off frequency of the anti-aliasing filter ($F_{c(aa)}$) is kept at 5 kHz, so that there is negligible amount of phase-loss to the components up to 500 Hz. Now, following sampling theorem, sufficient guard band width, the minimum sampling frequency of the observer is set at 5 times higher than the cut-off frequency of the anti-aliasing filter. So, the minimum sampling frequency is set at 25 kHz. Therefore the maximum possible value of the observer sampling period ,

$$T_{ob}\leq T_{ob(max)}=\frac{1}{5\times F_{c(aa)}}=\frac{1}{5\times(5\times10^3)}=40\ \mu s \tag{16}$$

In digital control of power converters, generally the controller output is updated at every switching period, T_{sw}. Therefore, it is not necessary to update the control loop reference signal coming from the observer faster than this rate. Hence we can write,

$$T_{ob}\geq T_{sw} \tag{17}$$

There are approximately T_{ob}/T_{sw} number of switching cycles in one observer sampling cycle. So the amount of observer computation that needs to be done in each switching cycle is $\frac{T_{obc}}{T_{ob}/T_{sw}}$. Hence we should ensure that

$$T_{sw}\geq\Delta t+\frac{T_{obc}}{T_{ob}/T_{sw}} \tag{18}$$

where, Δt is the time required to perform (i) sensing and signal filtering, (ii) closed-loop control and duty cycle updation and (iii) protection. Δt is nearly 5 μs for the selected Zynq PS. Substituting (11) in (18), we get

$$T_{sw} \geq \frac{5T_{ob}^2}{T_{ob}^2 - 1.66T_{ob} - 0.114\tau} \tag{19}$$

4) Steps to determine N, T_{ob} and T_{sw}: In summary for a given τ, T_{ob} and T_{sw} needs to satisfy (12), (13), (16), (17) and (19). Graphically this results in the shaded feasible region in the $T_{sw} - T_{ob}$ plane as shown in Fig. 7. Note here that the transmission line parameter τ affects determination of T_{ob} and T_{sw} through (19). Substituting the extreme values of τ from (14) and (15) in (19), we come up with,

$$T_{sw} \geq \frac{5T_{ob}^2}{T_{ob}^2 - 1.66T_{ob} - 114} \tag{20}$$

and

$$T_{sw} \geq \frac{5T_{ob}^2}{T_{ob}^2 - 1.66T_{ob} - 228} \tag{21}$$

Fig. 7 also shows how (19) changes for two extreme values of τ. Based on this, a step by step procedure for selecting N, T_{ob} and T_{sw} is developed.

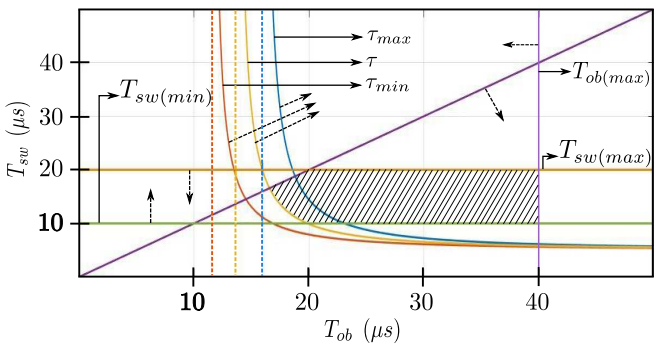


Fig. 7. Feasible region of T_{ob} and T_{sw} for all possible values of τ

Step 1 - Determination of N: It is clear from Fig. 7, that for any value of τ it is possible to achieve T_{ob} close to $T_{ob(max)}$ and T_{sw} close to $T_{sw(max)}$. From (11), it can be seen that T_{obc} reduces on maximizing the value of T_{ob} for a given value of τ. Hence the buffer size, N is chosen as,

$$N = \left[\frac{\tau}{T_{ob(max)}}\right]_{ceil} \tag{22}$$

where the ceiling function $[x]_{ceil}$ rounds off x to nearest higher integer.

Step 2 - Determination of T_{ob}:

$$T_{ob} = \frac{\tau}{N} \tag{23}$$

Hence it is ensured that the chosen T_{ob} is always less than $T_{ob(max)}$.

Step 3 - Determination of T_{sw}: In order to reduce the switching loss in the voltage source converter, T_{sw} is selected on the higher side of its range, i.e. close to $T_{sw(max)}$. At the same time, for ease of implementation in the digital platform, T_{sw} is chosen such that, T_{ob} becomes an integral multiple of T_{sw}. Hence T_{sw} is chosen as,

$$T_{sw} = \frac{T_{ob}}{\left[\frac{T_{ob}}{T_{sw(max)}}\right]_{ceil}} \tag{24}$$

IV. Simulation in MATLAB/Simulink

As shown in Fig. 8, a block has been developed in MATLAB/Simulink which acts as an observer to solve the distributed parameter transmission line. The development of the block is based on (8), (9) and (10). Using the line parameters given in Table-I, τ is obtained as 1440 μs. Hence applying (16), (22) and (23), the buffer size as well as the the sampling time period of the observer has been chosen as shown below.

$$N = \left[\frac{1440}{40}\right]_{ceil} = 36$$

and

$$T_{ob} = \frac{1440}{36} = 40\ \mu s$$

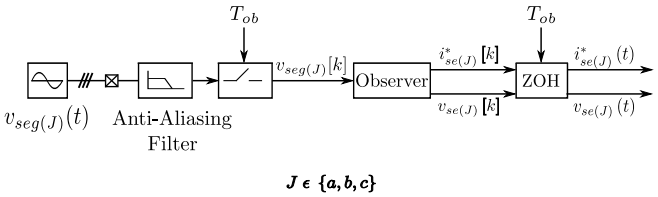


Fig. 8. Block Diagram of observer Simulation in MATLAB/Simulink software

Voltage switching action of the transmission line, as shown in Fig. 4 is then simulated with the parameters provided in Table-I. From Fig. 9, we can see that the result of the developed observer in the MATLAB/Simulink matches well with the Bergeron's model of PSCAD. Hence this justifies the modeling ((8) - (10)) and developed procedure to determine observer sampling period and the buffer size for digital implementation.

V. Scaling Down of the Actual System to Laboratory Level Hardware

For emulating the transmission line using laboratory level power electronic hardware, we need to scale down the system to the power and voltage level which can be safely handled in the lab. But while scaling we should ensure that the system dynamics remains unaltered. Hence the wave velocity in both the actual and the scaled down transmission line should be same. From Fig. 3(c) it is seen that the maximum value of current (I_m) in a phase, is nearly 1800 Amp. Now with reference to the ratings of the device used in the power amplifier, the maximum possible value of current in the scaled down system (I'_m) is set at 28 Amp. Similarly mapping the

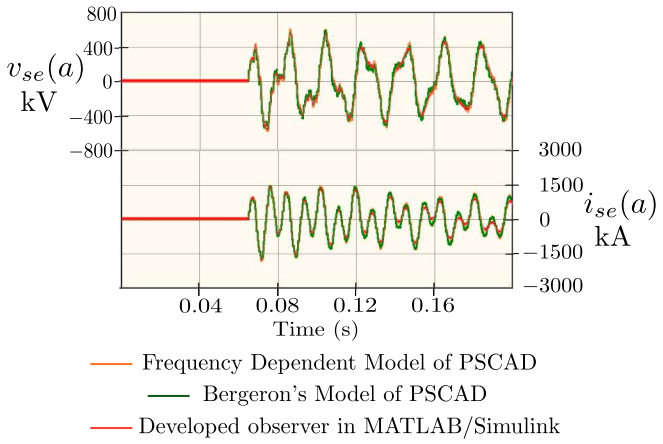


Fig. 9. Sending end voltage and current waveforms for the simulation of the circuit shown in Fig. 4 with the parameters given in Table-I using frequency dependent and Bergeron's model of PSCAD and the developed observer (Fig. 8) in MATLAB/Simulink

400 kV level of the original system to 220 V level of the scaled down system, the scaling factor S_z can be written as,

$$S_z = \frac{\frac{V'_{LL(RMS)}}{I'_m}}{\frac{V_{LL(RMS)}}{I_m}} = \frac{\frac{220}{28}}{\frac{400000}{1800}} = 0.03536 \tag{25}$$

Since the per unit values are same both in the original and the scaled down system for the conservation of the system dynamics, hence denoting R', L' and C' as the line resistance, inductance and capacitance per unit length of the scaled down transmission line system, we can write

$$R' = R \times S_z$$
$$L' = L \times S_z$$

and

$$C' = \frac{C}{S_z}$$

Therefore the travel time of the wave in the scaled down transmission line,

$$\tau' = l \times \sqrt{L'C'} = l \times \sqrt{LC} = \tau$$

Similarly the values of the grid inductance and the line end reactor for the scaled down system can be obtained as,

$$L'_g = L_g \times S_z$$

and

$$L'_{sh} = L_{sh} \times S_z$$

The parameters of the scaled down system are given in Table-III.

TABLE III
PARAMETERS OF THE SCALED DOWN TRANSMISSION LINE SYSTEM

R' (mΩ/km)	L' (μH/km)	C' (μF/km)	L'_g (mH)	L'_{sh} (H)
1.063	35.437	0.365	9.03	0.361

VI. Controller Design for Power Amplifier

In this section a closed loop current controller for the power amplifier is designed for tracking the sending end current following the current reference generated by the observer.

A. Plant Model

The voltage source inverter in the sending side of the power amplifier is needed to operate under current control with current reference, $i^*_{se(J)}$ coming from the observer, Fig. 12 of paper. This inverter is connected to the sending end grid, $v_{seg(J)}$, through a filter inductor L_f which has a parasitic series resistance R_f. After sensing the inductor current and grid side voltage, the control is similar to the control of a grid tied inverter under current control. With grid and DC bus voltage feed forward cancellation and as switching frequency is sufficiently higher than the control loop gain cross over frequency 5 kHz, it is possible to model the plant for each phase, $i_{se(J)}(s)/d(s) = 1/(R_f + sL_f)$.

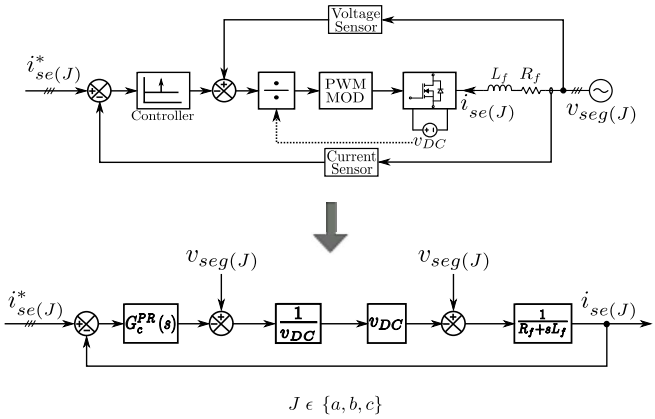


Fig. 10. Block diagram representation of the controller for PA

B. Design Objectives

1) The dominant component of the line current during energization is 50 Hz, Fig. 6. Also, the current in the post energization steady state is essentially a sinusoid at frequency 50 Hz. So the controller must provide large gain at 50 Hz as the controller is designed in natural abc frame.

2) During energization the current has frequency components up to 500 Hz. The controller must ensure sufficiently large loop gain (at least greater than 10 or 20 dB) for all frequencies below 500 Hz.

C. Controller Design

A PR controller, given in (26), is chosen. It has three parameters, resonant frequency $\omega_\circ$, proportional gain K_{pr} and integral gain K_{ir}.

$$G_c^{PR}(s) = K_{pr} + \frac{sK_{ir}}{s^2 + \omega_\circ^2} = K_{pr}\frac{s^2 + s\frac{K_{ir}}{K_{pr}} + \omega_\circ^2}{s^2 + \omega_\circ^2} \tag{26}$$

With this the open loop gain becomes, (27).

$$G_{oltf}^{TLE}(s) = K_{pr}\frac{s^2 + s\frac{K_{ir}}{K_{pr}} + \omega_\circ^2}{s^2 + \omega_\circ^2} \times \frac{\frac{1}{R_f}}{1 + \frac{L_f}{R_f}s} \tag{27}$$

The first objective is met by choosing $\omega_\circ = 100\pi$ rad/sec. The second objective is met through the following procedure.

a) By setting the gain cross over frequency at 5 kHz which is ten times of 500 Hz. This is done by choosing K_{pr} using the following procedure. With $R_f = 0.2\Omega$ and $L_f = 0.5$ mH for the selected filter and equating the gain cross-over frequency (ω_{gc}) for the above transfer function to 5 kHz, we can write,

$$\left|G_{oltf}^{TLE}(j\omega)\right|_{\omega=\omega_{gc}} \approx \frac{K_{pr}}{L_f \times \omega_{gc}} = 1 \tag{28}$$

$$\Rightarrow K_{pr} = L_f \times \omega_{gc} = 0.5 \times 10^{-3} \times 2\pi \times 5000 \approx 15.71$$

b) The gain of open loop transfer function at 500 Hz is set to 20 dB by selecting the parameter K_{ir}. K_{ir} is evaluated by equating the gain of $G_{oltf}^{TLE}(s)$ to 20 dB at a frequency of 500 Hz, i.e.

$$\left|G_{oltf}^{TLE}(j\omega)\right|_{\omega=2\pi\times500} \approx \frac{5\sqrt{K_{pr}^2 + \left(\frac{K_{ir}}{2\pi\times500}\right)^2}}{\sqrt{1+\left(\frac{2\pi\times500\times0.5\times10^{-3}}{0.2}\right)^2}} = 10 \tag{29}$$

$$\Rightarrow K_{ir} = 2\pi \times 500 \times 1.945 \approx 6110$$

The loop gain is plotted in Fig. 11. It shows that loop gain is more than 20 dB for all frequencies below 500 Hz and gain is quite high at 50 Hz. Closed loop transfer function shows almost unity gain and zero phase upto 500 Hz.

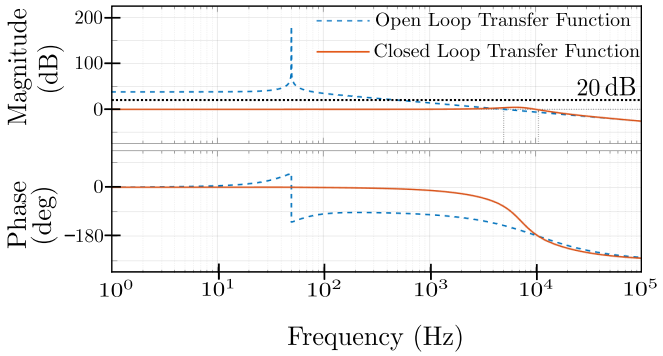


Fig. 11. Bode diagram of the current control loop of Fig. 10

TABLE IV
PARAMETERS OF THE CONTROLLER USED FOR THE PA OF THE TLE

Parameter	Value
Converter switching frequency, F_{sw}	50 kHz
Nominal grid frequency, F_{line}	50 Hz
Filter inductance, L_f	0.5 mH
Filter resistance, R_f	0.2 Ω
Gain cross-over frequency, ω_{gc}	5 kHz
K_{pr}	15.71
K_{ir}	6110
Phase margin	39.6°

VII. PROPOSED SCHEME OF IMPLEMENTATION OF THE TLE TEST SETUP

A proposed test bench setup for the hardware emulation of the energization of a transmission line with a shunt reactor connected on the other side (Fig. 4) is shown in Fig. 12. The test procedure has been elaborately discussed below.

- 3ϕ VSC is used to track the sending end currents of the transmission line during the instant of switching.
- An Active Front End Converter (AFEC) is used to provide a stable dc bus, v_{DC}, and also supply for the losses in the VSC along with supporting the emulated resistive loss in the transmission line.
- To have the flexibility of implementing a programmable grid impedance in the experimental setup, a strong grid (sinusoidal voltage source) is used and the inductive grid impedance is emulated inside the embedded platform.
- Since the switching phenomenon of the transmission line will be emulated by VSC, it should be synchronized to the grid before the emulation is being done. The steps are as follows :
  - The VSC is run in standalone mode generating the output voltage of same magnitude, frequency and phase as that of the grid.
  - Once the grid synchronization is being done the contactor C_1 is closed and the VSC is operated in current control mode with current reference, $i^*_{se(J)} = 0$.
- Again to have the flexibility to emulate the switching of the transmission line at different values of the phase voltage, we need to extract the voltage information of the grid before switching. Then depending on the desired instant of switching, the contactor C_2 will be energized and a step voltage will get applied at the input of the observer. This will start the emulation process and the VSC will start tracking the current generated by the observer.

VIII. EXPERIMENTAL VERIFICATION

As shown in Fig. 13, a SiC based 3ϕ Voltage Source Converter (VSC) rated for 415 V/ 50 Hz ac, 10 kW, 800 V dc and 100 kHz switching frequency has been designed and fabricated in the laboratory. Single leg modules of half bridge topology with plug and play type gate driver card has been developed and then connected to achieve the required topology. The modularity in the design not only allows the flexibility to adopt different converter topology but also facilitates easy repair and replacement. Discrete SiC devices from Rohm (SCH2080KE) of TO-247 package has been used to build the VSC. The gate drive IC (ADuM4135BR) from Analog Devices has been used to build the gate driver card. A prototype of the TLE, as shown in Fig. 12, has been fabricated in the laboratory to verify the proposed emulation scheme. The corresponding hardware setup of the developed TLE test bench is shown in Fig. 14. The observer is implemented on a Zynq SoC XC7Z010-1CLG400C from Xilinx.

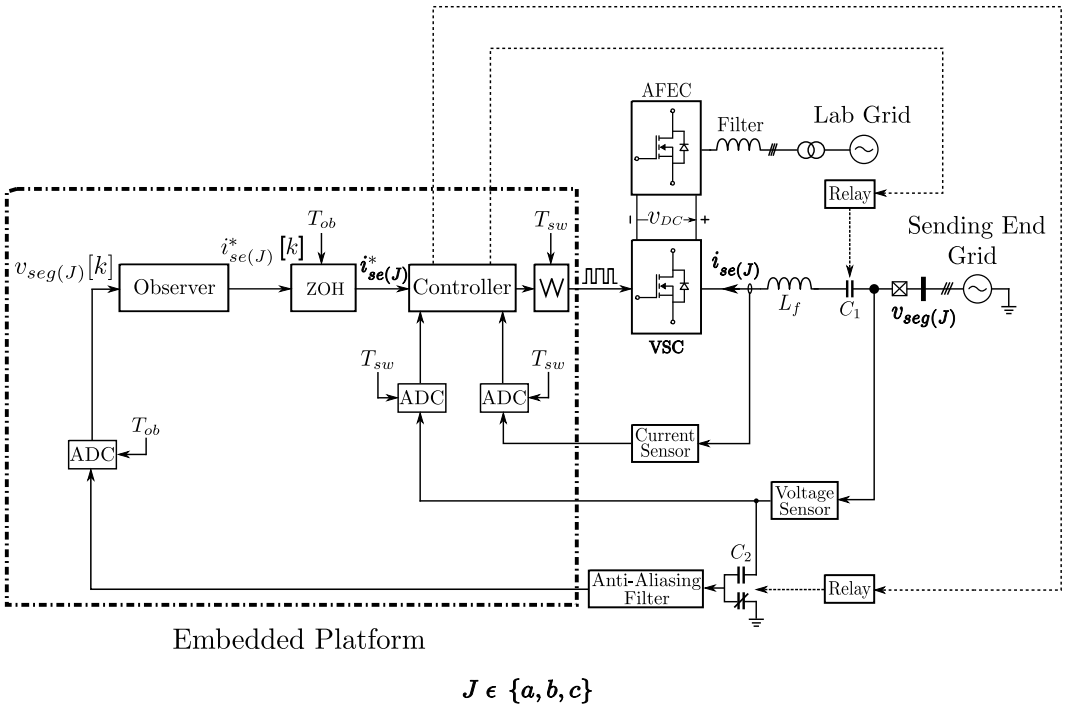


Fig. 12. Proposed scheme for the hardware implementation of the TLE

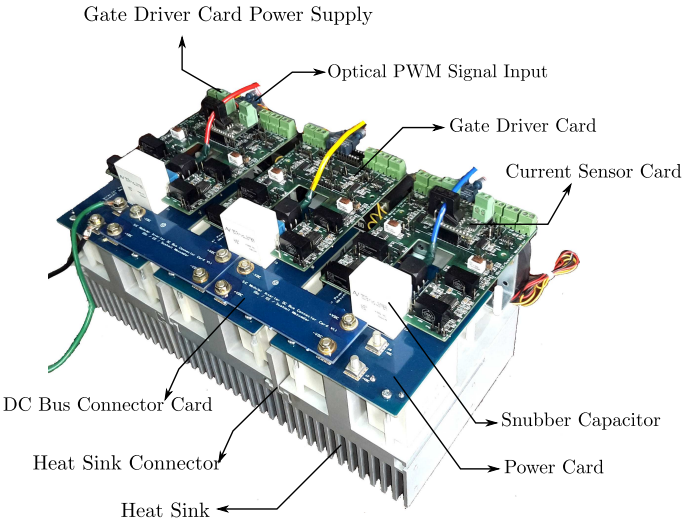


Fig. 13. Developed SiC based Voltage Source Converter

TABLE V
EXPERIMENTAL PARAMETERS FOR THE OBSERVER AND POWER AMPLIFIER

l (km)	τ (μs)	N	T_{ob} (μs)	T_{sw} (μs)
300	1080	27	40	20
400	1440	36	40	20
500	1800	45	40	20

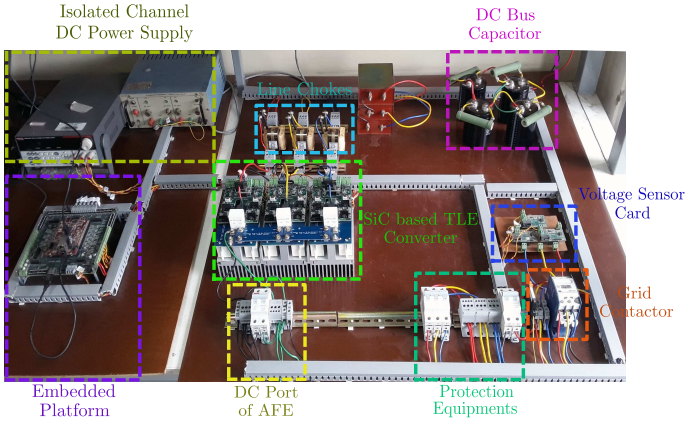
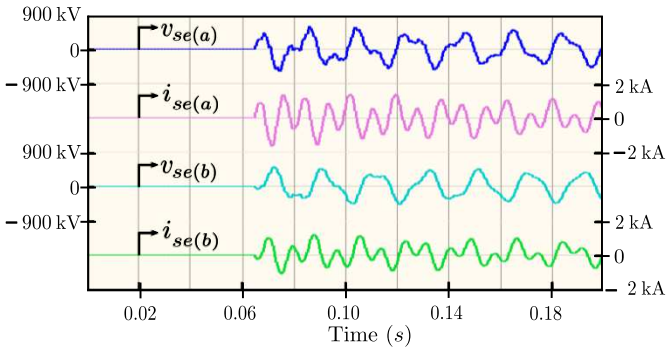


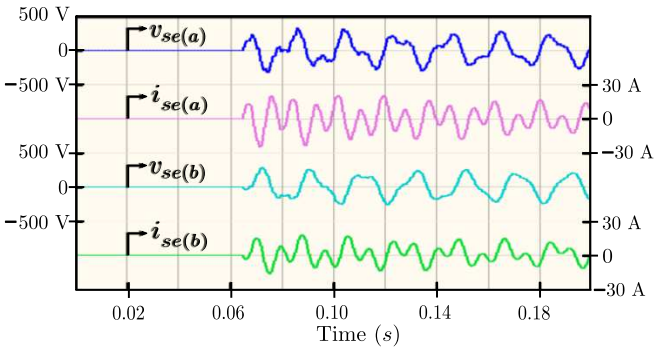
Fig. 14. Hardware setup of the TLE test setup

A. Parameters and Test Conditions

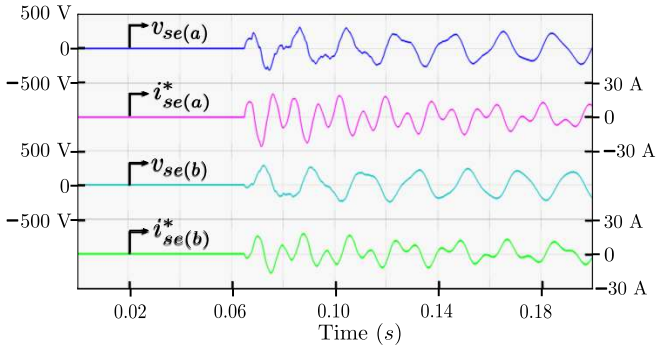
For a set of line parameters, grid impedance and shunt reactor, the transients in the line currents are studied for three different values of line length. The parameters of the original and scaled down system are provided in Table-I and III respectively. Considering the values of l to be 300 km, 400 km and 500 km, we obtain three different values of wave travel time. As given in Table-V, the values of the size of FIFO Buffer (N), observer sampling period (T_{ob}) and the switching period of the VSC (T_{sw}) are chosen based on the calculations proposed in Section III. Also to verify the functionality of the observer under different test conditions, the lines are switched at the zero crossing ($\Phi = 0°$) and the positive peak ($\Phi = 90°$) of 'a' phase of the sending end grid voltage.



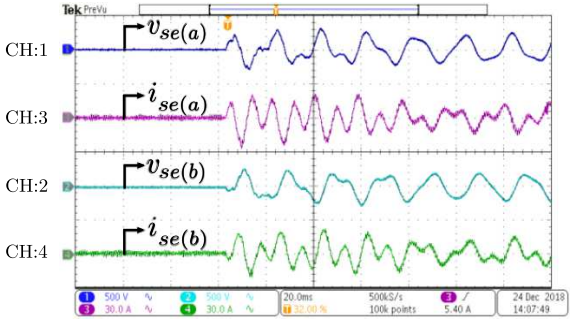
(a) Simulation of circuit schematic shown in Fig. 4 using parameters of original system given in Table-I by FDM in PSCAD



(b) Simulation of circuit schematic shown in Fig. 4 using parameters of scaled system given in Table-III by FDM in PSCAD



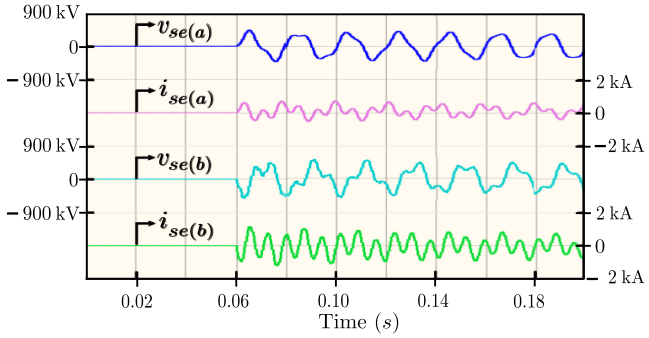
(c) Simulation of block diagram schematic shown in Fig. 8 using parameters of scaled system given in Table-III by MATLAB/Simulink



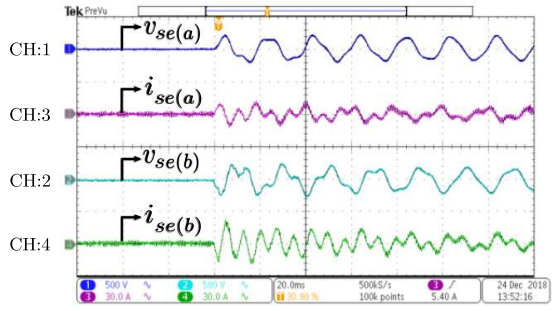
[CH:1,CH:2-500V/div], [CH:3,CH:4-30A/div], [Time Scale-20ms/div]

(d) Hardware emulation using parameters of scaled system given in Table-III by the proposed emulation scheme shown in Fig. 12

Fig. 15. Waveforms for the switching of the circuit shown in Fig. 4 at the positive peak of the a phase voltage and line length of 400 km



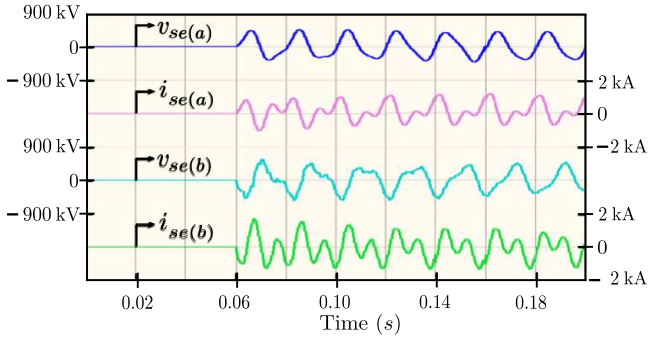
(a) Simulation of circuit schematic shown in Fig. 4 using parameters of original system given in Table-I by FDM in PSCAD



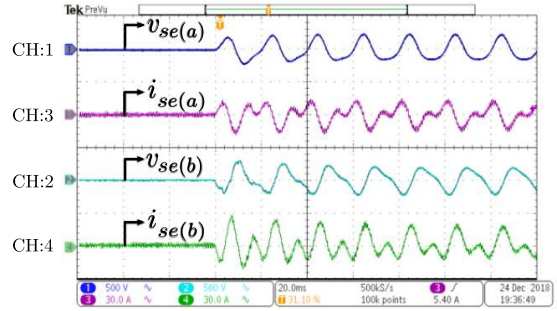
[CH:1,CH:2-500V/div], [CH:3,CH:4-30A/div], [Time Scale-20ms/div]

(b) Hardware emulation using parameters of scaled system given in Table-III by the proposed emulation scheme shown in Fig. 12

Fig. 16. Waveforms for the switching of the circuit shown in Fig. 4 at the positive zero crossing of the a phase voltage and line length of 300 km



(a) Simulation of circuit schematic shown in Fig. 4 using parameters of original system given in Table-I by FDM in PSCAD



[CH:1,CH:2-500V/div], [CH:3,CH:4-30A/div], [Time Scale-20ms/div]

(b) Hardware emulation using parameters of scaled system given in Table-III by the proposed emulation scheme shown in Fig. 12

Fig. 17. Waveforms for the switching of the circuit shown in Fig. 4 at the positive zero crossing of the a phase voltage and line length of 500 km

B. Results

The sending end voltage and current of the transmission line for the 'a' and 'b' phase are captured for each of the test cases. The results of the conducted test corresponding to a particular value of line length and switching instant are shown in Figs.15, 16 and 17, where each of the figure again contains sub-figures as described.

Fig. 15(a) shows the simulation of the circuit schematic shown in Fig. 4 with the parameters of the original system given in Table-I using FDM in PSCAD for the mentioned value of the line length and switching instant. Fig. 15(b) shows the simulation of the circuit schematic shown in Fig. 4 with the parameters of the scaled system given in Table-III using FDM in PSCAD for the mentioned value of the line length and switching instant. Fig. 15(c) shows the simulation of the block diagram schematic shown in Fig. 8 with the parameters of the scaled system given in Table-III by the observer in MATLAB/Simulink for the mentioned value of the line length and switching instant. Fig. 15(d) shows the hardware emulation of the scaled system with the parameters given in Table-III, as per the proposed emulation scheme shown in Fig. 12 for the mentioned value of the line length and switching instant. To investigate the performance of the developed transmission line emulator, the sending end voltage and current of a phase, of Fig. 15 (b) and (d) are plotted together as shown in Fig. 18. The corresponding FFT analysis of the current waveforms generated from the simulation as well as the experiment is also shown in the Fig. 19.

Figs.16(a) and 17(a) shows the simulation of the circuit schematic shown in Fig. 4 with the parameters of the original system given in Table-I using FDM in PSCAD for the mentioned value of the line length and switching instant. Figs.16(b) and 17(b) shows the hardware emulation of the scaled system with the parameters given in Table-III, as per the proposed emulation scheme shown in Fig. 12 for the mentioned value of the line length and switching instant.

C. Observation

It is observed that, on switching the transmission line of different lengths at the zero crossing of a particular phase voltage, the transient in the line currents for that phase is minimum compared to the other phases. Moreover, as the length of the line is increased the transients get damped out faster due to the increase in the effective line resistance which is also observed from the waveforms. It is also noted that the peak value of the current transient increases with increase in line length. This is due to the addition of more shunt capacitance associated with the transmission line. It can be seen that in all cases the emulation performed by the developed TLE closely matches with the PSCAD results.

IX. Conclusion

The problem of hardware emulation of energization of a long unenergized transmission line has been successfully addressed in this paper. After studying various line models, a traveling wave based numerical solution (Bergeron's model) was selected to solve the distributed parameter lossy transmission line in real-time by the observer. The wave travel time, computed from transmission line parameters directly impacts, the determination of the observer sampling frequency, the key discretisation parameter of the transmission line emulation. This paper shows how to derive the switching frequency of the VSC. For the power amplifier of the TLE setup, a SiC based Voltage Source Converter (VSC) rated for 415 V/ 50 Hz ac, 10 kW, 800 V dc and capable of operating at a switching frequency greater than 50 kHz has been designed and fabri-

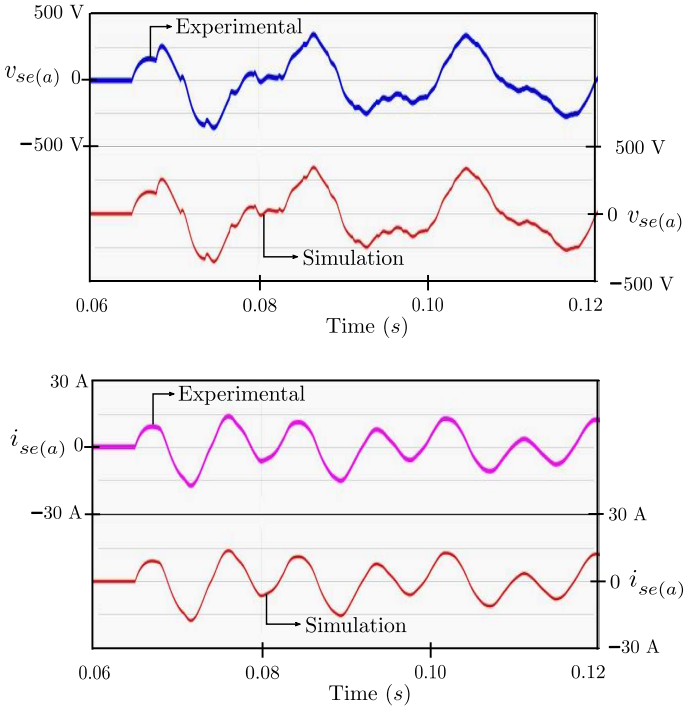


Fig. 18. Exaggerated view for the sending end voltage and current of a phase, of Fig. 15 (b) and (d)

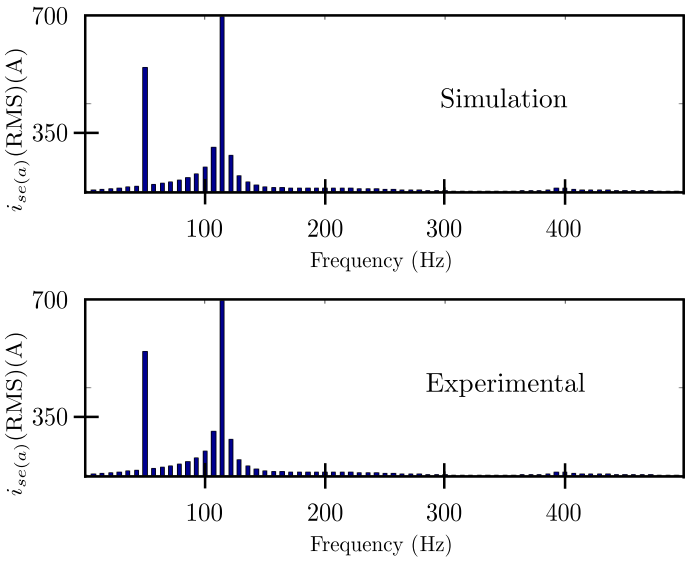


Fig. 19. FFT analysis of the current waveforms generated from the simulation as well as experiment shown in Fig. 18

cated in the laboratory. Further, the hardware topology for the implementation of the TLE as well as scaling of the actual transmission line to laboratory level emulator is presented. The design of the proportional resonant controller is also given in the paper which is used by the power amplifier to track the currents provided by the observer. Finally from the results it can be concluded that the developed Transmission Line Emulator (TLE) exhibits a high level of similarity with the actual transmission line system results obtained from the Frequency Dependent Model (FDM) of PSCAD. One limitation of the presented TLE is its applicability only in the energization but it can be extended to a general TLE of Fig. 2 as shown in appendix A.

APPENDIX A

A brief outline of implementation of the general scheme of Fig. 2 with Bergerons model is given in this appendix. Equations (5) and (6) are solved by the observer. The observer computation time in this case following the procedure of III B is given by $\left(T_{obc} = \left(1.1 + \frac{138}{1000}\frac{\tau}{T_{ob}}\right)\ \mu s\right)$. As now instead of one VSI we need to control two VSIs, effectively controller computation time (Δt) in (18) will become double. Equations, (19), (20) and (21) will be modified as follows.

$$T_{sw} \geq \frac{10T_{ob}^2}{T_{ob}^2 - 1.66T_{ob} - 0.114\tau} \tag{30}$$

$$T_{sw} \geq \frac{10T_{ob}^2}{T_{ob}^2 - 1.66T_{ob} - 114} \tag{31}$$

and

$$T_{sw} \geq \frac{10T_{ob}^2}{T_{ob}^2 - 1.66T_{ob} - 228} \tag{32}$$

Rest of the procedure as in section III remains same.

APPENDIX B

For the ease of digital implementation and to reduce the cost of the emulator system, both the observer and the controller for the power amplifier has been implemented on a single embedded platform. In equation (18), the parameter Δt is used to account for the time taken for(i) sensing and signal filtering, (ii) closed-loop control and duty cycle updation and (iii) protection in the selected Zynq processing system. The digitization of the PR controller is given below. To eliminate the necessity of online calculation of trigonometric functions or maintaining a look up table, Two Integrator with Forward and Backward (TIFB) Euler is used to implement the PR controller in the digital platform. The block diagram structure of the PR controller in continuous time domain is shown in Fig. 20. After discretization by TIFB, the difference equations of the Resonant Integrator (RI) can be expressed as,

$$x_{1(J)}[k] = x_{1(J)}[k-1] + \left\{K_{ir} \times \left(i^*_{se(J)}[k] - i_{se(J)}[k]\right) \times T_{sw}\right\} - \left\{x_{2(J)}[k-1] \times \omega_\circ \times T_{sw}\right\} \tag{33}$$

and

$$x_{2(J)}[k] = x_{2(J)}[k-1] + \left(x_{1(J)}[k] \times \omega_\circ \times T_{sw}\right) \tag{34}$$

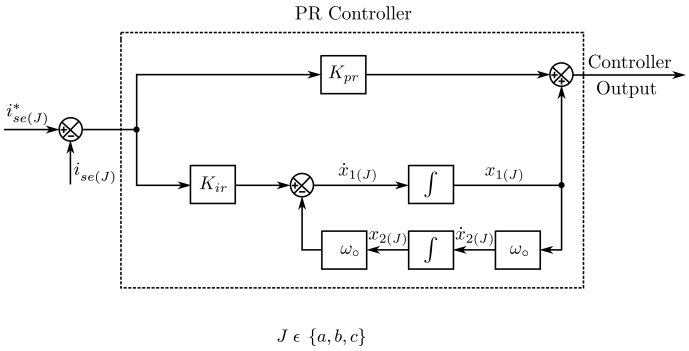


Fig. 20. Block Diagram structure of PR Controller in Continuous Time Domain

Considering $(\omega_\circ \times T_{sw})$ and $(K_{ir} \times T_{sw})$ being the predetermined quantities, from equations 33, 34 and Fig. 20, we can say that the computations involved per phase with the controller are : (i) 4 multiplication, (ii) 3 addition, (iii) 2 subtraction and (iv) 2 move operation. Hence referring Table-II, the total computation time taken by the PR controller is nearly $0.8\ \mu s$ for the selected Zynq processor.

APPENDIX C

TABLE VI
CONSTANTS OF BERGERON'S MODEL

C_1	C_2	C_3	C_4	C_5
$\frac{1}{Z_c + \frac{R_T}{4}}$	$\frac{R_T}{4}C_1^2$	$\frac{\frac{R_T}{4}\left(Z_c - \frac{R_T}{4}\right)}{\left(Z_c + \frac{R_T}{4}\right)^2}$	$Z_c C_1^2$	$\frac{Z_c\left(Z_c - \frac{R_T}{4}\right)}{\left(Z_c + \frac{R_T}{4}\right)^2}$

TABLE VII
ADDITIONAL OBSERVER CONSTANTS

$K_1 = 1 + C_1\frac{L_g}{T_{ob}}$	$C_9 = \frac{-C_3 + C_2\frac{L_g}{T_{ob}}}{K_1}$	$C_{14} = \frac{-C_3 + C_2\frac{L_{sh}}{T_{ob}}}{K_2}$
$K_2 = 1 + C_1\frac{L_{sh}}{T_{ob}}$	$C_{10} = \frac{-C_2\frac{L_g}{T_{ob}}}{K_1}$	$C_{15} = \frac{-C_2\frac{L_{sh}}{T_{ob}}}{K_2}$
$C_6 = \frac{C_1}{K_1}$	$C_{11} = \frac{-C_5 + C_4\frac{L_{sh}}{T_{ob}}}{K_1}$	$C_{16} = \frac{-C_4}{K_2}$
$C_7 = \frac{C_1\frac{L_g}{T_{ob}}}{K_1}$	$C_{12} = \frac{-C_4\frac{L_{sh}}{T_{ob}}}{K_1}$	$C_{17} = \frac{-C_5 + C_4\frac{L_g}{T_{ob}}}{K_2}$
$C_8 = \frac{-C_2}{K_1}$	$C_{13} = \frac{C_1\frac{L_{sh}}{T_{ob}}}{K_2}$	$C_{18} = \frac{-C_4\frac{L_g}{T_{ob}}}{K_2}$

APPENDIX D

We have compared the computational burden of the numerical scheme used in [19] with Bergeron's model when applied to the emulation of energization of a long transmission with one end terminated with a shunt reactor in this appendix. The Telegrapher's equation of a long transmission line are given by (35) and (36).

$$Ri_{(J)} + L\frac{\partial i_{(J)}}{\partial t} + \frac{\partial v_{(J)}}{\partial x} = 0 \tag{35}$$

$$Gv_{(J)} + C\frac{\partial v_{(J)}}{\partial t} + \frac{\partial i_{(J)}}{\partial x} = 0 \tag{36}$$

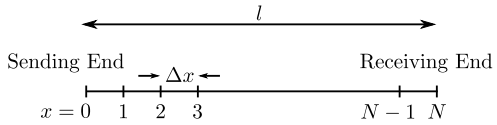


Fig. 21. Space discretization by the numerical scheme using Method of Characteristics used in [19]

As shown in Fig. 21, we can write $\Delta x = \frac{l}{N}$. Choosing Δt as $\frac{\Delta x}{c}$ we can write,

$$\Delta t = \frac{l}{Nc} = \frac{\tau}{N} = T_{ob} \tag{37}$$

We discretize the continuous quantity $w \,\epsilon\, \{v, i\}$ in space and time of (3), (4), (35) and (36) as,

$$w\,(x,t) = w\,(p\Delta x, k\Delta t) = W_p[k] \tag{38}$$

and obtain (39), (40), (41) and (42). The constants C_{23-36} are given in Table-VIII. In this particular case, $J \,\epsilon\, \{a, b\}$, $\Delta t = T_{ob}$, $\Delta x = cT_{ob}$ and $p = 0, 1, 2, ...N$. At every k^{th} time step, to solve $W_p[k]$ at any internal point on the line, the observer solves (39) and (40) using the previous step information at two adjacent points $W_{p-1}[k-1]$ and $W_{p+1}[k-1]$.

$$\text{For } 1 \leq p \leq N-1,$$

$$v_{p(J)}[k] = C_{23}\left(v_{p-1(J)}[k-1] + v_{p+1(J)}[k-1]\right) + C_{24}\left(i_{p-1(J)}[k-1] - i_{p+1(J)}[k-1]\right) \tag{39}$$

$$i_{p(J)}[k] = C_{25}\left(v_{(p-1(J)}[k-1] - v_{p+1(J)}[k-1]\right) + C_{26}\left(i_{p-1(J)}[k-1] + i_{p+1(J)}[k-1]\right) \tag{40}$$

(41) and (42) are solved using previous step data at one adjacent point and sampled value of the grid voltages. The solved k^{th} step data are stored and used to solve the $(k+1)^{\text{th}}$ step in the next computation cycle and in this way the numerical scheme advances in real-time.

$$i_{se(J)}[k] = C_{30}v_{seg(J)}[k] + C_{31}i_{se(J)}[k-1] + C_{32}v_{1(J)}[k-1] + C_{33}i_{1(J)}[k-1] \tag{41}$$

and

$$i_{re(J)}[k] = C_{34}i_{re(J)}[k-1] + C_{35}v_{N-1(J)}[k-1] + C_{36}i_{N-1(J)}[k-1] \tag{42}$$

Following the procedure of III B, the observer computation time in this case is given by $\left(T_{obc} = T_{clk(PS)}\,[95 + 103N]\right)$. From (11), $T_{obc[19]} > T_{obc(Bergeron)}$ for $N > 2$. Note, typically N is relatively large (minimum value of which is 27 in the example used in this paper).

TABLE VIII
CONSTANTS FOR OBSERVER BASED ON ALGORITHM USED IN [19]

$C_{19} = \sqrt{LC} + \frac{G}{2}\sqrt{\frac{L}{C}}$	$C_{26} = \frac{C_{22}}{2C_{20}}$	$C_{31} = \frac{C_{27}\frac{L_g}{T_{ob}}}{K_3}$
$C_{20} = L + \frac{R\Delta t}{2}$	$C_{27} = \frac{C_{19}}{C_{20}}$	$C_{32} = -\frac{C_{28}}{K_3}$
$C_{21} = \sqrt{LC} - \frac{G}{2}\sqrt{\frac{L}{C}}$	$C_{28} = \frac{C_{21}}{C_{20}}$	$C_{33} = \frac{C_{29}}{K_3}$
$C_{22} = L - \frac{R\Delta t}{2}$	$C_{29} = \frac{C_{22}}{C_{20}}$	$C_{34} = \frac{C_{27}\frac{L_{sh}}{T_{ob}}}{K_4}$
$C_{23} = \frac{C_{21}}{2C_{19}}$	$K_3 = 1 + C_{27}\frac{L_g}{T_{ob}}$	$C_{35} = -\frac{C_{28}}{K_4}$
$C_{24} = \frac{C_{22}}{2C_{19}}$	$K_4 = 1 + C_{27}\frac{L_{sh}}{T_{ob}}$	$C_{36} = -\frac{C_{29}}{K_4}$
$C_{25} = \frac{C_{21}}{2C_{20}}$	$C_{30} = \frac{C_{27}}{K_3}$	

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