Analytical Model to Study Hard Turn off Switching Dynamics of SiC MOSFET and Schottky Diode Pair

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***Abstract*—Fast switching transient of SiC MOSFET may lead to prolonged oscillations, spurious turn on, large device stress and high amount of EMI generation. For an optimal layout and gate driver design, study of switching dynamics is important. This paper presents an analytical model that captures the turn off switching dynamics of SiC MOSFET and SiC Schottky barrier diode (SBD) pair using parameters obtained from device and gate driver datasheets and the values of external circuit parasitics. Unlike linear approximation, a detailed model of channel current is considered that captures the gradual transition from ohmic to saturation region and the transverse electric field effect. A comprehensive model of the transfer capacitance is used and the effect of external gate-drain capacitance is considered. This results in a better estimation of switching transition time, actual loss incurred, (dv/dt), (di/dt) and transient over-voltage. The behavioural simulation and experimental results confirm the accuracy of the presented analytical model over a range of operating conditions for two 1.2kV discrete SiC MOSFET and SBD pairs of different current ratings.**

***Index Terms*—Hard switching, Turn off, dead-time, Double pulse test, Modelling, SiC MOSFET**

I. Nomenclature

Term	Description
V_{th}	Threshold voltage
K_p	Saturation region transconductance
K_f	Ohmic region transconductance factor
θ	Transverse electric field parameter
P_{vf}	Pinch-off voltage parameter
R_d	Drift region resistance of SiC MOSFET
R_{gint}	Internal gate resistance of SiC MOSFET
R_{gext}	External gate resistance
$R_{g(driver)}$	Gate driver internal resistance
V_{GG}, V_{CC}	Positive and negative gate supply voltage
T_f	Fall time of gate supply voltage
L_d	Power loop inductance
L_s	Common source inductance
$C_{g'd'(ext)}$	External gate drain capacitance
$C_{ak(ext)}$	External anode cathode capacitance

II. Introduction

SiC MOSFET is a wide bandgap (WBG) power device and commercially available predominantly in the voltage range of 900-1700V. With superior switching, conduction and thermal performance, it is in close competition with state of the art Si IGBTs in this voltage range [1]–[3]. Device characteristics of SiC MOSFET are highly nonlinear [4]–[7]. So the Si MOSFET based switching transient study [8]–[12] will not be applicable for SiC MOSFET. Hard turn on switching dynamics considering nonlinear characteristics of the devices and the effect of external circuit parasitics has already been studied in [13]. This paper concerns with the study of the hard turn off switching dynamics of SiC MOSFET and Schottky diode pair.

It has been well established in the literature that the turn off switching loss of SiC MOSFET is small compared to turn on loss [14]. But for high load currents, turn off switching loss can be significant [15]. Switching transient of SiC MOSFET is approximately 5-10 times faster than a similarly rated Si IGBT. It reduces the switching loss but excites parasitics which can lead to sustained oscillation, high device stress, spurious turn on, EMI related issues etc. [12], [16], [17]. So the estimation of turn off switching transition time, actual loss, (dv/dt), (di/dt), transient over-voltage and optimal choice of external gate resistance is important for power electronic converter design.

Experimental approach to capture switching dynamics is expensive and requires sophisticated high frequency measurement setup [13]. Moreover, the measurement may be erroneous and it is not possible to obtain the actual switching loss directly from experimental waveforms due to the parasitics present in the circuit [12], [13], [18]. In [19], an energy related estimation technique is discussed using which actual switching loss can be estimated indirectly from experimental waveforms. Calorimetric measurement technique is another experimental approach that can be used to measure actual switching loss [20] but it also requires a sophisticated measurement setup. Physics based model [21], [22] and behavioural model [23], [24] are both simulation based approaches. Though accurate, physics based model requires sophisticated software, longer simulation time and values of internal device parameters that are not generally available in the device datasheet. Behavioural model based approach does not provide insight into the switching process and applying it for a large number of operating points is time consuming. Also, it often suffers from convergence problem [25]. Analytical modelling approach is based on the simplified approximate solution of a set of coupled nonlinear differential equations obtained from the behavioural model. This approach is suitable to gain insight into the switching process and overcomes most of the limitations of

Manuscript received January 06, 2020; revised February 12, 2020; accepted May 15, 2020. This work was supported by the Department of Science and Technology, Government of India under the project titled “Development of an advanced System on Chip (SoC) based embedded controller for power electronic converter”. (*Corresponding author : Shamibrota Kishore Roy*).
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TABLE I: Mode-wise discussion on existing literature

Mode	References	Assumptions	Limitations
Delay	[15], [16]	Drain-source voltage is clamped to small on-state drop and channel current is fixed to load current. A constant value of gate-drain capacitance is considered corresponding to small drain-source voltage. A step change in gate supply voltage results in exponential fall of the gate-source voltage.	Channel current may fall way below the load current and the assumption that drain-source voltage remaining constant leads to inconsistency in meeting the condition for transitioning from ohmic to saturation region. As drain-gate voltage is negative for a significant portion of the delay period, the gate-drain capacitance value is much higher compared to the value used in existing analysis and results in incorrect estimation of delay time. The actual ramp fall time (a gate driver property) is small but could be a significant part of the total delay time for low current SiC MOSFETs.
	[19], [26]	A sub mode is added where drain-source voltage is raised from on state drop to a value which is consistent with the assumption that channel current is load current at the boundary of ohmic-saturation region.	
Voltage rise	[15], [27]	Gate-source voltage and channel current are assumed to be constant and drain-source voltage changes due to the charging of device parasitic capacitances primarily through the gate current.	In reality, channel current changes quite a bit. Neglecting parasitic external gate-drain capacitance and linear channel current model results in significant inaccuracies in estimation in loss, (dv/dt) etc.
	[16], [19], [26]	The above assumptions are relaxed but a linear channel current model is considered.	
Current fall	[15], [19], [26], [27]	Drain-source voltage is assumed to be constant and using linear channel current dependence, gate-source voltage falls exponentially with an enlarged time constant due to feedback effect of common source inductance.	Channel current of SiC MOSFET in saturation is a nonlinear function of gate-source voltage, so linear approximation will lead to error in estimating current fall time, transient over-voltage and loss incurred.
	[16]	Combined dynamics of both gate and power loop is considered with a linear channel current model.	

the previously stated approaches. It provides result accurate enough for the early stages of power electronic converter design. This approach to study the switching dynamics of SiC MOSFET was adopted in several earlier works [15], [16], [19], [26], [27]. In this paper, an analytical modelling approach is proposed to study the turn off switching transient.

Turn off switching transient can be divided into three modes: delay, voltage rise and current fall period. All of the previous work [15], [16], [19], [26] assume channel current to be constant during the delay period but in reality, the channel current may fall well below the load current. MOSFET is in saturation region during voltage rise and current fall period and channel current is a nonlinear function of gate-source voltage. In all of the previous work [15], [16], [19], [26], [27], a linear model of channel current is assumed leading to inaccurate estimations. The device parasitic capacitances are a nonlinear function of voltages. Except [16], in all other work, constant capacitances are used. Variable capacitances are replaced either with charge related equivalent capacitances [15], [26] or simply updated with large changes in drain-source voltage [19]. Only power loop dynamics in voltage rise period [15], [27] and gate loop dynamics during current fall [15], [19], [26], [27] are considered in the majority of the previous work. In [16], a more realistic combined gate and power loop dynamics are considered for both of these two modes. In this context, the paper makes the following contributions.

- During delay period the MOSFET is in ohmic region. A channel current model is considered in this region that captures the gradual transition from ohmic to saturation region and the transverse electric field effect in SiC MOSFETS [4], [7]. It can be noted that no channel current modelling was needed in the existing approach.
- A detailed model of the transfer capacitance, appropriate for SiC MOSFETs [5], is used.
- Instead of step, a ramped fall in gate supply voltage is considered as the fall time (a gate driver property) is small but could be a significant part of the total delay time for low current SiC MOSFETs.
- A better channel current model in saturation region called modified square law [4], [7], is used.
- The effect of external parasitic gate-drain capacitance is considered which has a significant impact in voltage rise period [12].
- Between voltage rise and current fall period, a transition mode is identified where the difference between the channel and drain currents present at the end of voltage rise period, comes to zero. This mode also predicts the voltage overshoot.

This paper is arranged in the following order. A mode by mode discussion on existing models is given in Section III. In section IV, behavioural model for switching transient study and calculation of hard turn off switching loss are discussed. The proposed analytical model to study hard switching turn off dynamics of SiC MOSFET and Schottky diode pair is given in section V. Details of the experimental set-up are provided in section VI and simulation and experimental results have been given in section VII. A comparative study between the proposed analytical model and the state-of-the-art model is provided in section VIII. Finally, Section IX draws the conclusion.

III. Prior Art

This section presents mode by mode details of the behavioural model based analytical approaches present in existing literature for the turn-off dynamics of SiC MOSFET along with their shortcomings which provides motivation for the present work. The turn-off process can be divided into three distinct modes: Delay, Voltage rise and Current fall. The definitions of these modes are given below. Table I shows, the key assumptions made in the previous literature and resulting limitations in predicting the actual switching dynamics for each of these modes.

Delay: After gate supply is turned off, gate-source voltage reduces and MOSFET remains in ohmic region. This mode ends when MOSFET enters into the saturation region.

Voltage rise: This mode starts when the MOSFET enters into the saturation region and ends when the free-wheeling diode gets forward biased.

Current fall: Current fall period starts after the free-wheeling diode gets forward biased and ends when the gate-source voltage reaches the threshold voltage.

IV. Behavioural Model for hard turn off switching dynamics study

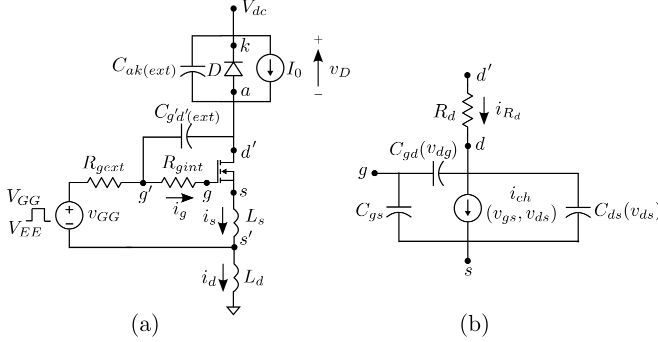


Fig. 1: Circuit configuration for switching transient analysis

To analyse the hard turn off dynamics of SiC MOSFET and Schottky diode pair, a buck-chopper configuration is considered as shown in Fig. 1(a). V_{dc} is an ideal voltage source and the output inductive load is modelled as a current sink I_0. A SiC MOSFET is used as the active device with three terminals gate (g), drain (d') and source (s). A SiC based Schottky barrier diode (SBD) is used as the free-wheeling diode and it is modelled as a two terminal device with terminals anode (a) and the cathode (k). SiC SBD is selected due to its minimal reverse recovery and low on-state drop compared to the intrinsic body diode of the SiC MOSFET [2]. Few commercially available SiC MOSFETs are being offered with an anti-parallel SiC SBD inside the package [28]. So the study will be relevant when applied to a common bidirectional chopper configuration consisting of two such series-connected SiC MOSFETs.

v_{GG} is the applied gate driver voltage, which has two levels, V_{GG} and V_{EE} respectively. When the gate signal is removed, first v_{GG} falls from V_{GG} to V_{EE} linearly with a fall time of T_f and then settles to V_{EE}. R_{gext} is the total external gate resistance which is the summation of internal resistance of the driver and external gate resistance. R_{gint} is the internal gate resistance of the MOSFET.

The equivalent circuit model or behavioural model of the SiC power MOSFET is shown in Fig. 1(b). R_d represents the drift region resistance. Channel current (i_{ch}) is modelled the same as described in [4], [7]. Single channel approximation has been considered to reduce complexity. MOSFET is in cut-off region for $v_{gs} < V_{th}$ and i_{ch} is equal to zero. Here V_{th} is the threshold voltage of the MOSFET. For $v_{ds} < (v_{gs} - V_{th})/P_{vf}$ and $v_{gs} > V_{th}$, MOSFET is in ohmic region and the channel current i_{ch} can be modelled by (1). Similarly in saturation region $v_{ds} > (v_{gs} - V_{th})/P_{vf}$ and $v_{gs} > V_{th}$, i_{ch} is given by (2). K_p, K_f, θ and P_{vf} are defined in Section I. P_{vf} defines how sharp the transition from ohmic region to saturation region happens. Considering long channel approximation, the channel length modulation index $\lambda \approx 0$. y is defined as $\left(\dfrac{K_f}{K_f - P_{vf}/2}\right)$. This model does not incorporate the effect of parameter variation with temperature. Parameters R_d, K_p, K_f, V_{th}, θ and P_{vf} are obtained from the transfer characteristics (in saturation region) and output characteristics (in ohmic region) of the SiC MOSFET for a given temperature (provided in the datasheet) Fig. 2 and Fig. 3 respectively). Note, in static condition $i_d = i_{ch}$ as negligible current flows through device parasitic capacitances. As seen from Fig. 2(a) and Fig. 3(a), there is a mismatch between datasheet curve and fitted curve for low values of i_d/i_{ch} due to the use of single channel approximation of i_{ch}. But this has a negligible impact in switching dynamics as for moderate to high value of load current, the switching transient encounters low channel current region (where there is a mismatch between fitted curve and datasheet value) at the very end of the current fall period which is negligible compared to the total turn off switching period. On the other hand, for low value of load current (I_0), i_{ch} collapses to zero at the beginning of switching transient and switching trajectories are no longer dependent on the channel current dependence on gate source voltage. All the parameters are temperature dependent and has been extracted for 25^oC.

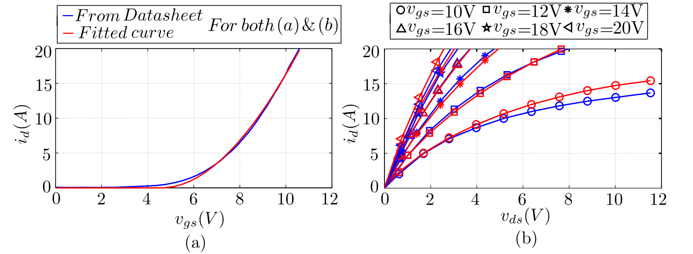


Fig. 2: (a) i_d vs. v_{gs} curve (b) i_d vs. v_{ds} curve for C2M0160120D from Wolfspeed

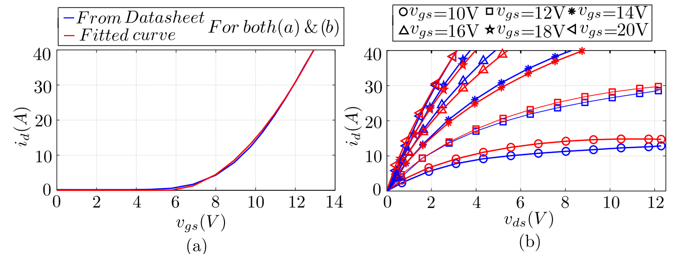


Fig. 3: (a) i_d vs. v_{gs} curve (b) i_d vs. v_{ds} curve for C2M0080120D from Wolfspeed

C_{gs}, C_{gd} and C_{ds} are the gate to source, gate to drain and the drain to source device parasitic capacitances respectively. Input capacitance C_{iss} is the summation of C_{gs} and C_{gd}. Transfer capacitance C_{rss} is C_{gd} itself. And the output capacitance C_{oss} is the summation of C_{ds} and C_{gd}. In datasheet, C_{iss}, C_{rss} and C_{oss} are plotted as a function of drain-source voltage (v_{ds}). C_{gs} is modelled as a constant capacitance. For high value of v_{ds}, C_{gd} is negligible with respect to C_{gs}. So

$$i_{ch}(v_{gs},v_{ds}) \approx \frac{K_pK_f\left((v_{gs}-V_{th})\,v_{ds}-\left(P_{vf}^{y-1}/y\right)(v_{gs}-V_{th})^{2-y}\,v_{ds}^{y}\right)}{(1+\theta(v_{gs}-V_{th}))} \quad (1) \qquad i_{ch}(v_{gs}) \approx \frac{K_p\,(v_{gs}-V_{th})^2}{2(1+\theta(v_{gs}-V_{th}))} \quad (2)$$

C_{gs} will be approximately equal to C_{iss} for high v_{ds}. C_{gd} is a nonlinear capacitance, depends on v_{dg}. For $v_{dg} < 0$, $C_{gd} \approx C_{oxd}$. When $v_{dg} > 0$, C_{oxd} will be in series with the gate-drain depletion capacitance. As v_{dg} increases, there are two distinct decay rate of C_{gd} can be observed in SiC MOSFET [5]. At $v_{dg} = V_{td}$, the depletion region expands from JFET to drift region and the decay rate of C_{gd} with respect to v_{dg} changes. Also for high v_{dg}, the effect of C_{oxd} is negligible and C_{gd} solely depends on the gate to drain depletion capacitance. So C_{gd} can be represented by the set of equations given in (3). Note, C_{gd} vs v_{dg} curve available in the datasheet is measured in the off-state condition. In [29], it is stated that the C_{gd} value during transient condition may differ from it's off state value. This may reduce the accuracy of the model. But it can be observed from the results given in Section VII that the C_{gd} model used here can capture the turn off switching transient accurately for a wide operating range. Similarly, C_{ds} is also a depletion capacitance depends upon v_{ds} and can be modelled as (4).

$$C_{gd}(v_{dg}) = \begin{cases} C_{oxd} = \dfrac{k_1}{k_3}, & v_{dg} \in (-\infty, 0) \\ \dfrac{k_1}{\left(1+\dfrac{v_{dg}}{k_2}\right)^{1/2}+k_3}, & v_{dg} \in [0, V_{td}) \\ \dfrac{k_4}{\left(1+\dfrac{v_{dg}-V_{td}}{k_5}\right)^{1/4}}, & v_{dg} \in [V_{td}, \infty) \end{cases} \tag{3}$$

$$C_{ds}(v_{ds}) = \frac{k_6}{\left(1+\dfrac{v_{ds}}{k_7}\right)^{1/2}} \tag{4}$$

The Schottky diode is considered as ideal with zero voltage drop across it during the forward bias condition ($v_D \approx 0$). In reverse bias, the diode is modelled as a capacitance C_D, which is also a nonlinear function of voltage (v_D) across the diode, (5).

$$C_D(v_D) = \frac{k_8}{\left(1+\dfrac{v_D}{k_9}\right)^{1/2}} \tag{5}$$

C_{gs} is taken the same as the C_{iss} value given in the datasheet for high values of v_{ds}. Extraction of parameters k_1 to k_9 and V_{td} are done by fitting the equations (3), (4) and (5) to the plots given in the datasheet. C_{gd} vs v_{dg} plot is not directly given in the datasheet. But during C_{gd} vs v_{ds} measurement, $v_{gs} \approx 0$ [30]. Then C_{gd} vs v_{ds} plot given in the datasheet can be directly converted to C_{gd} vs v_{dg} plot. Similarly, C_{ds} vs. v_{ds} plot has been obtained by subtracting C_{rss} vs v_{ds} plot from C_{oss} vs v_{ds} plot. Fig. 4(a) and (b) shows one such example of fitting equation (3) and (4) to the C_{gd} vs v_{dg} and C_{ds} vs v_{ds} curve taken from the datasheet. Similarly, k_8 and k_9 can be obtained using (5).

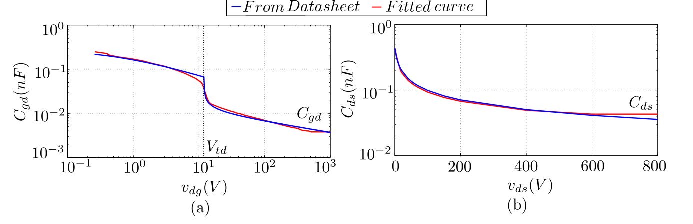


Fig. 4: C_{gd} vs v_{dg} and C_{ds} vs v_{ds} plot for C2M0160120D from Wolfspeed

Due to fast switching transition, external circuit parasitics that play a significant role in switching dynamics are the common source inductance (L_s), power loop inductance (L_d) and external gate to drain capacitance ($C_{g'd'(ext)}$). L_s is the parasitic inductance that is common to both gate and power circuit loop whereas L_d is only part of the power circuit loop. L_d is the summation of the DC bus inductance, the lead inductances of the MOSFET and the diode and connection inductance between the MOSFET and the diode. $C_{g'd'(ext)}$ and $C_{ak(ext)}$ are the external parasitic capacitance between g', d' nodes and a, k nodes respectively. $C_{g'd'(ext)}$ depends on the geometry of gate and drain planes routed in the PCB and the dielectric material used (FR4 for our case). On the other hand, $C_{ak(ext)}$ is the parallel combination of the parasitic capacitance due to the PCB layout of the anode and cathode plane along-with the FR4 material and the parasitic capacitance of the inductive load. These capacitances are in picofarad range. There is also an external parasitic capacitance across node d' and s'. But in all practical purposes, the value of this parasitic capacitance is small compared to the depletion capacitance $C_{ds}(v_{ds})$ and its effect is neglected. The maximum value of $C_{g'd'(ext)}$ and $C_{ak(ext)}$ are much smaller compared to the maximum value of internal depletion capacitances $C_{gd}(v_{dg})$ and $C_D(v_D)$ respectively.

The time evolution of gate-source ($v_{gs}(t)$) and drain-source ($v_{d's}(t)$) voltage along with the channel current ($i_{ch}(t)$) during switching transitions are important for the study of switching dynamics and switching loss estimation. Due to the presence of L_s, R_{gint} and device parasitic capacitances, it is not possible to measure these waveforms experimentally. The measurable waveforms are $v_{g's'}(t)$, $v_{d's'}(t)$ and $i_d(t)$ (Fig. 1), where T_{off} is the turn off switching transition time. The actual switching loss in the MOSFET is given by (6) and the measured loss is given by (7).

$$E_{off} = \int_0^{T_{off}} \left(v_{ds}(\tau)i_{ch}(\tau) + i_{R_d}^2 R_d\right)\, d\tau \tag{6}$$

$$E'_{off} = \int_0^{T_{off}} v_{d's'}(\tau)i_d(\tau)\, d\tau \tag{7}$$

V. Analytical model for hard turn off switching dynamics study

The objective of this section is to analyse the turn off switching dynamics of SiC MOSFET and Schottky barrier diode pair

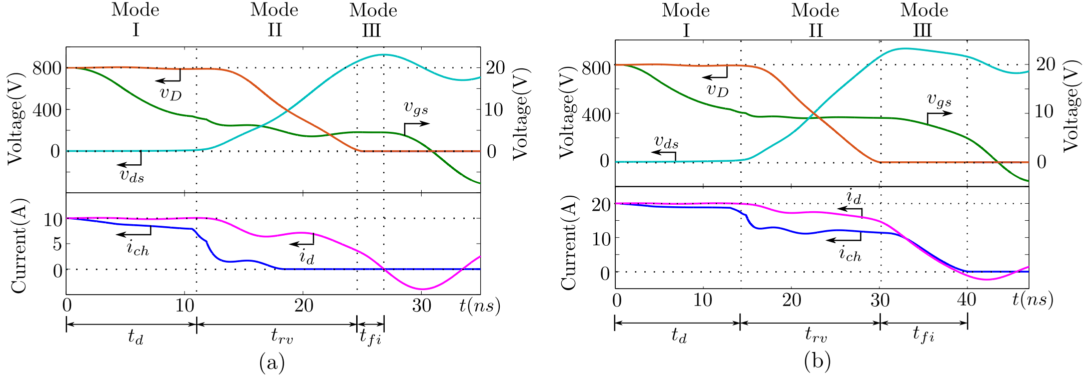


Fig. 5: Simulation waveform for C2M0160120D SiC MOSFET and C4D05120A SiC schottky diode pair: a) Low I_0 and/or R_{gext}: $I_0 = 10A$, $R_{gext} = 2.5\Omega$, b) High I_0 and/or R_{gext}: $I_0 = 20A$, $R_{gext} = 8.5\Omega$

and accurately estimate transition time (T_{off}), actual switching loss, (dv/dt) and (di/dt) rates and transient over-voltage ($V_{ds(max)}$) for a given operating condition (V_{dc}, I_0), gate driver parameters (V_{EE}, V_{GG}, R_{gext}, T_f) and datasheet related parameters of the devices (C_{gs}, $C_{gd}(v_{dg})$, $C_{ds}(v_{ds})$, $C_D(v_D)$, V_{th}, K_p, K_f, θ, R_{gint}). The external circuit parasitics (L_s, L_d, $C_{g'd'(ext)}$ and $C_{ak(ext)}$) can be approximately estimated from package information and/or electromagnetic simulation [24] or experimental measurements [31]. Effect of R_d is neglected as it has a negligible impact in switching dynamics. So d and d' are concentrated at a single node d for the analysis.

Hard switching turn off transient of SiC MOSFET can be broadly divided into three modes 1) Mode I (delay period), 2) Mode II (voltage rise period) and 3) Mode III (current fall period) (Fig. 5).

A. *Mode I (delay period)*

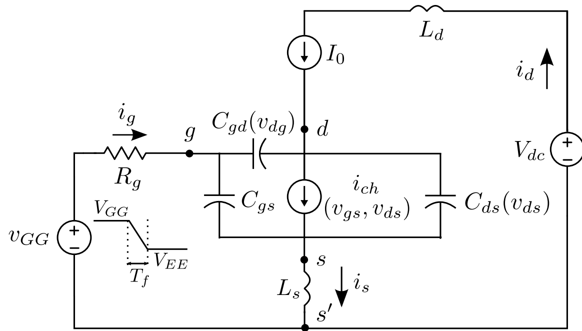


Fig. 6: Equivalent circuits of Mode I

At the start of delay period, v_{gs} is equal to V_{GG} and the full load current I_0 is flowing through the SiC MOSFET, so $i_d = i_s = I_0$. The MOSFET is in ohmic region and the drop across the MOSFET $V_{ds(on)} = I_0 (R_{on} - R_d)$, where R_{on} is the on state resistance of the SiC MOSFET. SiC SBD is reverse biased and drop across it $v_D = (V_{dc} - I_0 R_{on})$. When the negative gate signal is applied, first the gate driver voltage v_{GG} will ramp down from V_{GG} to V_{EE} with a fall time of T_f and then clamp to V_{EE} (see Fig. 6).

Main assumption of this mode is $i_d \approx I_0$. This approximation holds good because of the change in v_{ds} during Mode I is small, so other state variables of the power circuit (i_d and v_D) remains almost constant (see Mode I of Fig. 5). For the entire Mode I, SiC MOSFET is in ohmic region, so i_{ch} is a function of both v_{gs} and v_{ds} (1). As v_{dg} is small during this mode, $C_{gd}(v_{gd})$ is large compared to the external parasitic capacitances $C_{g'd'(ext)}$ and its effect can be neglected. Fig. 6 represents the equivalent circuit of this mode where $R_g = (R_{gext} + R_{gint})$. Mode I is divided into three sub modes, a) Sub Mode A, b) Sub Mode B1 and c) Sub Mode B2 respectively (Fig. 7).

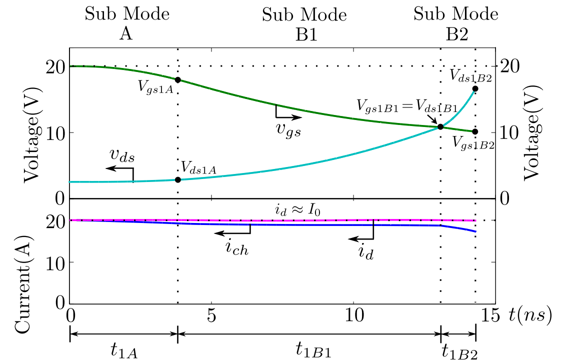


Fig. 7: Simulation waveforms of Mode I

*1) **Sub Mode A**:* During Sub Mode A, v_{GG} changes from V_{GG} to V_{EE} within a time duration of T_f, so v_{GG} is written as (8). Consideration of ramp fall instead of step fall of v_{GG} is important as ramp fall time is a significant portion of total delay time in case of SiC MOSFETs (low current discrete devices). Ramp fall time T_f can be obtained from gate driver datasheet [32].

KCL at g node of Fig. 6 gives (9). During this sub mode ($v_{dg} < 0$), so $C_{gd}(v_{dg}) = C_{oxd}$ (3). Also $(dv_{gs}/dt) \gg (dv_{ds}/dt)$ during this sub mode. Then $C_{oxd}(dv_{ds}/dt) \approx 0$ and (9) can be approximated as (10). Gate loop forms a series RLC circuit excited by a ramp input and can be solved independently. Poles of the circuit are P_1 and P_2 [1]. In practical scenario, damping ratio $\zeta = (R_g/2)\sqrt{(C_{gs} + C_{oxd})/L_s} \gg 1$ makes it over damped and the poles P_1 and P_2 are real. Also it can be shown that if $\zeta \gg 1$, then poles P_1 and P_2 are far apart and can be represented approximately by

[1] $P_1, P_2 = -\dfrac{R_g}{2L_s} \pm \sqrt{\left(\dfrac{R_g}{2L_s}\right)^2 - \left(\dfrac{1}{L_s(C_{gs} + C_{oxd})}\right)}$

$P_1 \approx -(1/(R_g(C_{gs}+C_{oxd})))$ and $P_2 \approx -(R_g/L_s)$ and $v_{gs}(t)$ is given as (11).

$$v_{GG} = V_{GG} + \left(\frac{V_{EE}-V_{GG}}{T_f}\right) t \tag{8}$$

$$i_g = C_{gs}\frac{dv_{gs}}{dt} + C_{gd}(v_{gd})\frac{dv_{gd}}{dt} \tag{9}$$
$$= C_{gs}\frac{dv_{gs}}{dt} + C_{oxd}\frac{dv_{gs}}{dt} - C_{oxd}\frac{dv_{ds}}{dt}$$
$$\approx (C_{gs}+C_{oxd})\frac{dv_{gs}}{dt} \tag{10}$$

$$v_{gs}(t) = V_{GG} + \frac{(V_{EE}-V_{GG})}{T_f}\left(t - \frac{P_1P_2}{P_2-P_1}\left(\frac{e^{P_1 t}}{P_1^2} - \frac{e^{P_2 t}}{P_2^2}\right) + \frac{P_1+P_2}{P_1P_2}\right) \tag{11}$$

After solving $v_{gs}(t)$, we need to find out $v_{ds}(t)$ and $i_{ch}(t)$ to quantify the actual loss (6). Applying KCL at d node of Fig. 6, we get (13). As stated before $C_{gd}(v_{dg}) = C_{oxd}$ during this sub mode. Also the effect of $C_{oxd}\,(dv_{gs}/dt)$ is significant as $(dv_{gs}/dt) \gg (dv_{ds}/dt)$ and value of C_{oxd} is comparable with $C_{ds}(v_{ds})$ during this sub mode. So $v_{ds}(t)$ strongly depends on the change in $v_{gs}(t)$. Time evolution of v_{ds} is evaluated from (13) using finite difference method where functional form of $i_{ch}(v_{gs}, v_{ds})$ and $C_{ds}(v_{ds})$ are given in (1) and (4) respectively.

$$(I_0 - i_{ch}(v_{gs}, v_{ds})) = C_{gd}(v_{dg})\frac{dv_{dg}}{dt} + C_{ds}(v_{ds})\frac{dv_{ds}}{dt} \tag{12}$$
$$= (C_{oxd} + C_{ds}(v_{ds}))\frac{dv_{ds}}{dt} - C_{oxd}\frac{dv_{gs}}{dt}$$

$$\frac{dv_{ds}}{dt} = \frac{(I_0 - i_{ch}(v_{gs}, v_{ds})) + C_{oxd}\frac{dv_{gs}}{dt}}{C_{oxd} + C_{ds}(v_{ds})} \tag{13}$$

Sub Mode A ends when $t = T_f = t_{1A}$. At the end of this sub mode $v_{gs} = V_{gs1A}$ and $v_{ds} = V_{ds1A}$ (Fig. 7).

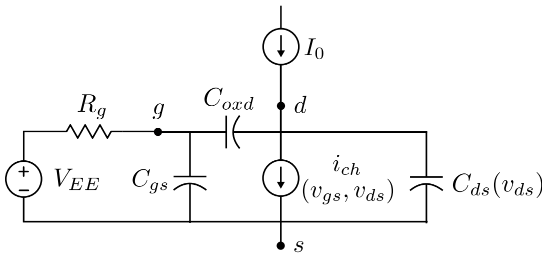


Fig. 8: Approximate equivalent circuit of Sub Mode B1 of Mode I

*2) **Sub Mode B1**:* In Sub Mode B1, v_{gg} is clamped to V_{EE}. $v_{dg} < 0$ during this sub mode, so $C_{gd}(v_{dg}) = C_{oxd}$. It can be shown that for a series RLC circuit with step excitation and $\zeta \gg 1$, the response is dominated by $P_1 \approx -(1/(R_g(C_{gs}+C_{oxd})))$ and the effect of L_s can be neglected. v_{gs} starts falling from initial value V_{gs1A}. Difference in the current $(I_0 - i_{ch})$ starts charging the output capacitance. As the increase in v_{ds} reduces the output capacitance (see Fig. 4), it leads to a comparatively fast rise in v_{ds}. Rise in voltage v_{ds} acts as negative feedback through $C_{gd}(v_{dg})$ and slows down the v_{gs} fall and eventually fall in i_{ch} also gets slowed down (see (1)). (dv_{gs}/dt) and (dv_{ds}/dt) are of comparable magnitude and gate and power circuit are fully coupled through $C_{gd}(v_{dg}) = C_{oxd}$. Fig. 8 represents the approximate equivalent circuit of Sub Mode B1. Solving this equivalent circuit and rearranging, we get (14) and (15) respectively, where the expression for $i_{ch}(v_{gs}, v_{ds})$ and $C_{ds}(v_{ds})$ are given in (1) and (4) respectively. (14) and (15) form a set of first order coupled nonlinear differential equations. Finite difference approach is employed for solution.

$$\frac{dv_{gs}}{dt} = \frac{V_{EE} + R_g\left(\frac{C_{oxd}}{C_{oxd}+C_{ds}(v_{ds})}\right)(I_0 - i_{ch}) - v_{gs}}{\left(R_g\,(C_{gs}+C_{oxd}) - \frac{R_g C_{oxd}^2}{C_{oxd}+C_{ds}(v_{ds})}\right)} \tag{14}$$

$$\frac{dv_{ds}}{dt} = \frac{(I_0 - i_{ch}) + \left(\frac{C_{oxd}}{C_{gs}+C_{oxd}}\right)\left(\frac{V_{EE}-v_{gs}}{R_g}\right)}{\left((C_{oxd}+C_{ds}(v_{ds})) - \frac{C_{oxd}^2}{C_{gs}+C_{oxd}}\right)} \tag{15}$$

This sub mode ends when $v_{gs} = v_{ds}$ and at the end of Sub Mode B1 $V_{gs} = V_{gs1B1}$ and $v_{ds} = V_{ds1B1}$ (Fig. 7).

*3) **Sub Mode B2**:* $v_{dg} > 0$ dictates the start of Sub Mode B2. Same approximations of Sub Mode B1 holds good for this sub mode. So Fig. 8 represents the approximate equivalent circuit of Sub Mode B2 also. Same set of governing equations of Sub Mode B1 will prevail in this sub mode. As $v_{dg} \in [0, V_{td})$ during this sub mode, so $C_{gd}(v_{dg})$ is no longer a constant capacitance C_{oxd} and has a nonlinear functional dependence on v_{dg} (second expression of (3)). Reduction in $C_{gd}(v_{dg})$ as v_{dg} increases reduces the coupling between gate and power loop results in a comparatively faster fall in i_{ch} during this sub mode compared to Sub Mode B1. $i_{ch}(v_{gs}, v_{ds})$ and $C_{ds}(v_{ds})$ are given in (1) and (4). Finite difference method is used to find out the time evolution of $v_{gs}(t)$ and $v_{ds}(t)$.

This sub mode ends when $v_{ds}P_{vf} = (v_{gs} - V_{th})$. At the end of this sub mode $v_{gs} = V_{gs1B2}$ and $v_{ds} = V_{ds1B2}$ (Fig. 7). E_1 quantifies the actual switching loss during Mode I and can be represented as (16) where $t_1 = (t_{1A} + t_{1B1} + t_{1B2})$.

$$E_1 = \int_0^{t_1} v_{ds}(\tau) i_{ch}(\tau)\ d\tau \tag{16}$$

Special Case: For low value of I_0 and/or low R_{gext}, $v_{ds}P_{vf} = (v_{gs} - V_{th})$ condition is satisfied prior to the point where $v_{gs} = v_{ds}$ condition is met. In that scenario, end of Sub Mode B1 is defined as the point where $v_{ds}P_{vf} = (v_{gs} - V_{th})$. During Sub Mode B2, $C_{gd}(v_{dg}) = C_{oxd}$ and $i_{ch}(v_{gs}, v_{ds})$ is given by (2). This sub mode ends when $v_{gs} = v_{ds}$.

B. Mode II (voltage rise period)

This mode starts when $v_{ds}P_{vf} > (v_{gs} - V_{th})$ and the SiC MOSFET enters into saturation region. i_{ch} solely depends on v_{gs} (see (2)). All the state variables of the power circuit (v_{ds}, v_D and i_d) changes noticeably during Mode II. Effect of $C_{g'd'(ext)}$ and $C_{ak(ext)}$ are considered because of their

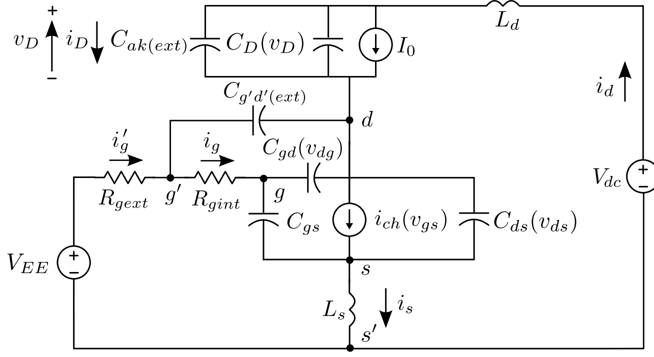


Fig. 9: Equivalent circuit model of Mode II

comparable magnitude with the respective internal depletion capacitances $C_{gd}(v_{dg})$ and $C_D(v_D)$. Also the effect of external parasitic inductances L_d and L_s are significant and has been considered in Mode II. Fig. 9 represents the equivalent circuit of this mode. It is divided into two sub modes, a) Sub Mode A1, and b) Sub Mode A2 respectively (Fig. 10).

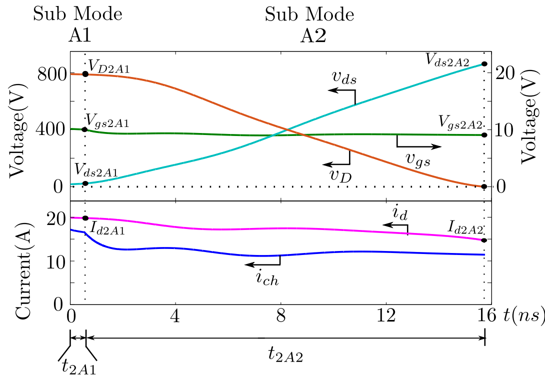


Fig. 10: Simulation waveforms of Mode II

*1) **Sub Mode A1**:* In Sub Mode A1, SiC MOSFET is in saturation region and v_{gs} starts decreasing from its initial value V_{gs1B2}. This results in a fast change in i_{ch}, as in saturation region i_{ch} is approximately a quadratic function of v_{gs}. Power loop current i_d cannot change fast due to the presence of inductance L_d and L_s and the difference in current $(i_d - i_{ch})$ starts charging the output capacitance (see Fig. 5). So v_{ds} increases from it's initial value V_{ds1B2} and other state variables i_d and v_D starts changing from their initial values I_0 and $(V_{dc} - R_{on}I_0)$ respectively. The functional form of internal MOSFET capacitances $C_{gd}(v_{dg})$ and $C_{ds}(v_{ds})$ are defined in second expression of (3) (as $v_{dg} \in [0, V_{td})$) and (4) respectively. $C_D(v_D)$ is defined in (5) and can be approximated as $C_D(v_D) \approx \left(\alpha_3/\sqrt{v_D}\right)$ because $(v_D/k_9) \gg 1$ during this sub mode, where $\alpha_3 = \left(k_8\sqrt{k_9}\right)$.

KVL in the power loop (Fig. 9) gives (17). As $i_s = \left(i_d + i_g'\right)$ and $i_g' \ll i_d$, (17) can be approximated as (18). Applying KCL at d node, we get (19) and (20). Change in d node voltage is much higher compared to both g and g' node resulting $(dv_{dg'}/dt) \approx (dv_{dg}/dt)$. Also $v_{ds} = (v_{dg} - v_{gs})$ and $(dv_{gs}/dt) \ll (dv_{ds}/dt)$ gives $(dv_{dg}/dt) \approx (dv_{ds}/dt)$. Then (20) reduces to (21). Applying KCL at node g and KVL in gate loop, we get (22) and (23) respectively. Using (22), $i_g' \ll i_d$ and $(v_{dg'}/dt) \approx (dv_{dg}/dt)$, (23) gets reduced to (24) [2].

$$v_{ds} = V_{dc} - v_D - L_d\frac{di_d}{dt} - L_s\frac{di_s}{dt} \tag{17}$$

$$\approx V_{dc} - v_D - (L_d + L_s)\frac{di_d}{dt} \tag{18}$$

$$i_d = I_0 + \underbrace{\left(C_D(v_D) + C_{ak(ext)}\right)}_{C_{D(eq)}(v_D)}\frac{dv_D}{dt} \tag{19}$$

$$(i_d - i_{ch}) = C_{ds}(v_{ds})\frac{dv_{ds}}{dt} + C_{gd}(v_{dg})\frac{dv_{dg}}{dt} + C_{g'd'(ext)}\frac{dv_{dg'}}{dt} \tag{20}$$

$$\approx \underbrace{\left(C_{ds}(v_{ds}) + C_{gd}(v_{dg}) + C_{g'd'(ext)}\right)}_{C_{oss(eq)}(v_{dg},v_{ds})}\frac{dv_{ds}}{dt} \tag{21}$$

$$i_g = C_{gs}\frac{dv_{gs}}{dt} + C_{gd}(v_{dg})\frac{dv_{gd}}{dt} \tag{22}$$

$$V_{EE} = i_g\left(R_{gext} + R_{gint}\right) + R_{gext}C_{g'd'(ext)}\frac{dv_{g'd}}{dt} + v_{gs} + L_s\frac{di_s}{dt} \tag{23}$$

$$\approx \tau_1\frac{dv_{gs}}{dt} + v_{gs} + L_s\frac{di_d}{dt} - \tau_2\frac{dv_{ds}}{dt} \tag{24}$$

These set of equations (18), (19), (21) and (24) along with (2) form a set of coupled nonlinear differential equations and has been written in a compact form in the Appendix (35). Finite difference technique is employed to solve this set of coupled nonlinear differential equation.

Sub Mode A1 ends when $v_{dg} = V_{td}$. At the end of this sub mode $v_{ds} = V_{ds2A1}$, $v_{gs} = V_{gs2A1}$, $v_D = V_{D2A1}$ and $i_d = I_{d2A1}$.

*2) **Sub Mode A2**:* Sub Mode A2 starts when $v_{dg} > V_{td}$. Approximations of Sub Mode A1 hold good for this sub mode also. (35) dictates the time evolution of the state variables. As $v_{dg} = (v_{ds} - v_{gs})$ and $v_{ds} \gg v_{gs}$ during this sub mode, then $v_{dg} \approx v_{ds}$ and $C_{gd}(v_{dg} \approx v_{ds}) \approx k_4 \Big/ \left(1 + \dfrac{v_{ds} - V_{td}}{k_5}\right)^{1/4}$. Also $\left(\dfrac{v_{ds} - V_{td}}{k_5}\right) \gg 1$ for most of the part of this sub mode makes $C_{gd}(v_{ds}) \approx \left(\alpha_1/\sqrt[4]{v_{ds} - V_{td}}\right)$ where $\alpha_1 = \left(k_4\sqrt[4]{k_5}\right)$. Using similar argument $C_{ds}(v_{ds}) \approx \left(\alpha_2/\sqrt{v_{ds}}\right)$ and $C_D(v_D) \approx \left(\alpha_3/\sqrt{v_D}\right)$ where $\alpha_2 = \left(k_6\sqrt{k_7}\right)$ and $\alpha_3 = \left(k_8\sqrt{k_9}\right)$.

This sub mode ends when $v_D = 0$. At the end of this sub mode $v_{ds} = V_{ds2A2}$, $v_{gs} = V_m$, $i_d = I_{d2A2}$ and $\dfrac{di_d}{dt} = \left(\dfrac{V_{dc} - V_{ds2A2}}{L_d + L_s}\right)$.

Special case: For low values of I_0 and/or R_{gext}, channel current i_{ch} collapses to zero before $v_D = 0$ (see Fig. 5).

[2] $\tau_1 = \left(R_g\left(C_{gs} + C_{gd}(v_{dg})\right) + R_{gext}C_{g'd'(ext)}\right)$, $\tau_2 = \left(R_gC_{gd}(v_{dg}) + R_{gext}C_{g'd'(ext)}\right)$

$t_2 = (t_{2A1} + t_{2A2})$ is the total time period of Mode II. E_2 quantifies the actual switching loss of this mode and can be evaluated using (16), where integration limit will be zero to t_2.

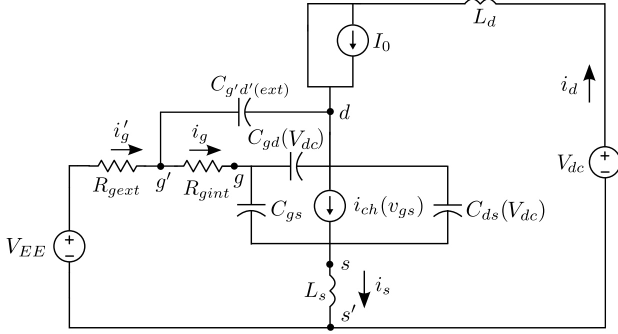


Fig. 11: Approximate equivalent circuit model of Mode III

C. Mode III (Voltage overshoot and current fall period)

This mode starts when the diode gets forward biased and voltage across the diode $v_D \approx 0$. Fig. 11 represents the equivalent circuit of Mode III. Similar as Mode II, the effect of external circuit related parasitic capacitance $C_{g'd'(ext)}$ is considered. As $v_{ds} \geq V_{dc}$ throughout this mode and $C_{ds}(v_{ds})$ and $C_{gd}(v_{dg} \approx v_{ds})$ almost remains constant in this voltage range, so $C_{gd}(v_{dg}) = C_{gd}(v_{dg} \approx V_{dc})$, $C_{ds}(v_{ds}) = C_{ds}(v_{ds} = V_{dc})$ (Fig. 11). Mode III is divided into two sub modes, a) Sub Mode A, and b) Sub Mode B respectively (Fig. 12).

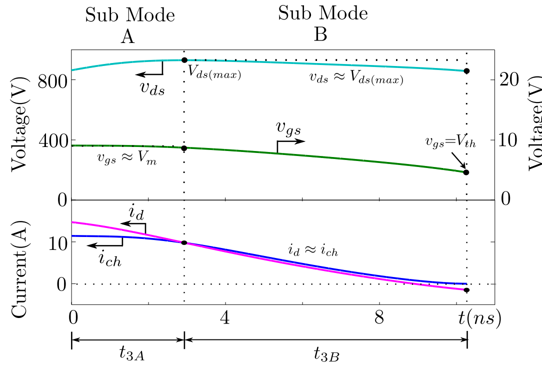


Fig. 12: Simulation waveforms of Mode III

1) ***Sub Mode A****:* At the start of this sub mode, there is a substantial difference between i_d and i_{ch}. $v_{gs} \approx V_m$ and i_{ch} remains almost constant to I_{ch} throughout this sub mode and i_d reduces from its initial value. This will lead to the rise in v_{ds} from V_{ds2A2} and reaches it's peak value when $i_d = i_{ch}$. This dictates the end of Sub Mode A. Applying KVL in the power loop of Fig. 11 and considering $i'_g \ll i_d$, we get (25). KCL at node d with the approximation $(dv_{dg'}/dt) \approx (dv_{dg}/dt) \approx (dv_{ds}/dt)$ gives (26) [3].

$$v_{ds} \approx V_{dc} - (L_d + L_s)\frac{di_d}{dt} \tag{25}$$

$$(i_d - I_{ch}) \approx C_{oss(eq3)}\frac{dv_{ds}}{dt} \tag{26}$$

Time evolution of v_{ds} is given in (27), where constants are defined below [4]. This sub mode ends when v_{ds} reaches it's maximum value and duration of this sub mode is given in (28). Maximum v_{ds} overshoot puts a constraint on the maximum allowable $(L_d + L_s)$ as it can lead to device failure due to transient over-voltage. Maximum value of $v_{ds} = V_{ds(max)}$ is given in (29).

$$v_{ds} = V_{dc} + A_4 \sin(\omega_3 t + \phi) \tag{27}$$

$$t_{3A} = \left(\frac{\frac{\pi}{2} - \phi}{\omega_3}\right) \tag{28}$$

$$V_{ds(max)} = V_{dc} + A_4 \tag{29}$$

It is possible to get a closed form expression of the actual switching loss of Sub Mode A. Switching loss during sub mode is calculated using (30). At the end of this sub mode $v_{ds} = V_{ds(max)}$, $v_{gs} = V_m$ and $i_d = I_{ch}$.

$$\begin{aligned} E_{3A} &= I_{ch}\int_0^{t_{3A}} v_{ds}(\tau)\, d\tau \\ &= V_{dc} I_{ch} t_{3A} + (L_d + L_s)(I_{d2B} - I_{ch}) I_{ch} \end{aligned} \tag{30}$$

2) ***Sub Mode B****:* This sub mode starts after v_{ds} reaches it's maximum value $V_{ds(max)}$. At the end of the previous sub mode, $i_d = i_{ch}$. During this sub mode i_d and i_{ch} both reduces from it's initial value and $i_d \approx i_{ch}$. The rate of change of v_{ds} is small, so $v_{ds} \approx V_{ds(max)}$. Applying KVL in the gate circuit and considering $(dv_{g'd}/dt) \approx (dv_{gd}/dt) \approx (dv_{gs}/dt)$, we get (31). i_{ch} can be approximately represented as $i_{ch} \approx \left(\frac{K_p}{2}\right)(v_{gs} - V_{th})^2$ as $(v_{gs} - V_{th})$ is small during this sub mode and $\theta \ll 1$. Then using (26) and (31) and above approximations, we get (32).

$$V_{EE} \approx \tau_1 \frac{dv_{gs}}{dt} + v_{gs} + L_s \frac{di_{ch}}{dt} \tag{31}$$

$$\approx \tau_1 \frac{dv_{gs}}{dt} + v_{gs} + \left(\frac{K_p L_s}{2}\right)\frac{d}{dt}(v_{gs} - V_{th})^2 \tag{32}$$

Though nonlinear, (32) can be solved with initial condition $v_{gs} = V_m$ and v_{gs} can be written implicitly as a function of time (33). Sub Mode B ends when i_{ch} reaches zero or $v_{gs} = V_{th}$. t_{3B} is the time period of Sub Mode B or the channel current fall time and can be estimated using (33) with $v_{gs} = V_{th}$.

E_{3B} quantifies the actual loss of energy during Sub Mode B. Using change of variable technique and integrating, we have arrived at a closed form expression of E_{3B} (34) [5].

$t_3 = (t_{3A} + t_{3B})$ is the total time period of this mode and total switching loss is given by $E_3 = (E_{3A} + E_{3B})$.

---

[3] $C_{oss(eq3)} = (C_{gd}(V_{dc}) + C_{g'd'(ext)} + C_{ds}(V_{dc}))$

[4] $\omega_3 = \frac{1}{\sqrt{(L_d + L_s)C_{oss(eq3)}}}$,

$A_4 = \sqrt{(V_{ds2A2} - V_{dc})^2 + \left(\frac{L_d + L_s}{C_{oss(eq3)}}\right)(I_{d2A2} - I_{ch})^2}$,

$\phi = \tan^{-1}\left(\frac{(V_{ds2A2} - V_{dc})}{(I_{d2A2} - I_{ch})}\sqrt{\frac{C_{oss(eq3)}}{L_d + L_s}}\right)$

[5] $d_1 = (\tau_1 + K_p L_s (V_{EE} - V_{th}))$, $d_2 = K_p L_s (V_{EE} - V_{th})$, $d_3 = \left(\frac{V_m - v_{th}}{V_{EE} - V_{th}}\right)$

$$t = \varphi(v_{gs}) = -\left(\tau_1 + K_p L_s \left(V_{EE} - V_{th}\right)\right) \ln\left(1 - \frac{v_{gs} - V_m}{V_{EE} - V_m}\right) - K_p L_s (v_{gs} - V_m) \tag{33}$$

$$E_{3B} = \int_0^{t_{3B}} v_{ds}(\tau) i_{ch}(\tau)\ d\tau \approx \frac{K_p V_{ds(max)}}{2} \int_0^{t_{3B}} \left(v_{gs} - V_{th}\right)^2\ d\tau = \frac{K_p V_{ds(max)}}{2} \int_{v_{gs}=V_m^*}^{V_{th}} \left(v_{gs} - V_{th}\right)^2 \left(\frac{d\varphi(v_{gs})}{dv_{gs}}\right) dv_{gs}$$
$$= \frac{K_p V_{ds(max)}}{2} \left(V_{EE} - V_{th}\right)^2 \left(d_1 \left(d_3 + \frac{d_3^2}{2} + \ln\left(1 - d_3\right)\right) + \frac{d_2 d_3^3}{3}\right) \tag{34}$$

Total turn off switching transition time $T_{off} = (t_1 + t_2 + t_3)$. Actual turn off switching loss is given by $E_{off} = (E_1 + E_2 + E_3)$. (dv/dt) and (di/dt) are given as $\left(\frac{V_{ds2A2} - V_{ds1B2}}{t_2}\right)$ and $\left(\frac{I_{d2A2}}{t_3}\right)$ respectively. $V_{ds(max)}$ represent the turn off transient over-voltage. Flowchart of the proposed analytical model is given in Fig. 13. Input to this model are operating conditions, device and circuit related parameters and gate driver parameters. The outputs of this proposed analytical model are calculated at the end of the flowchart.

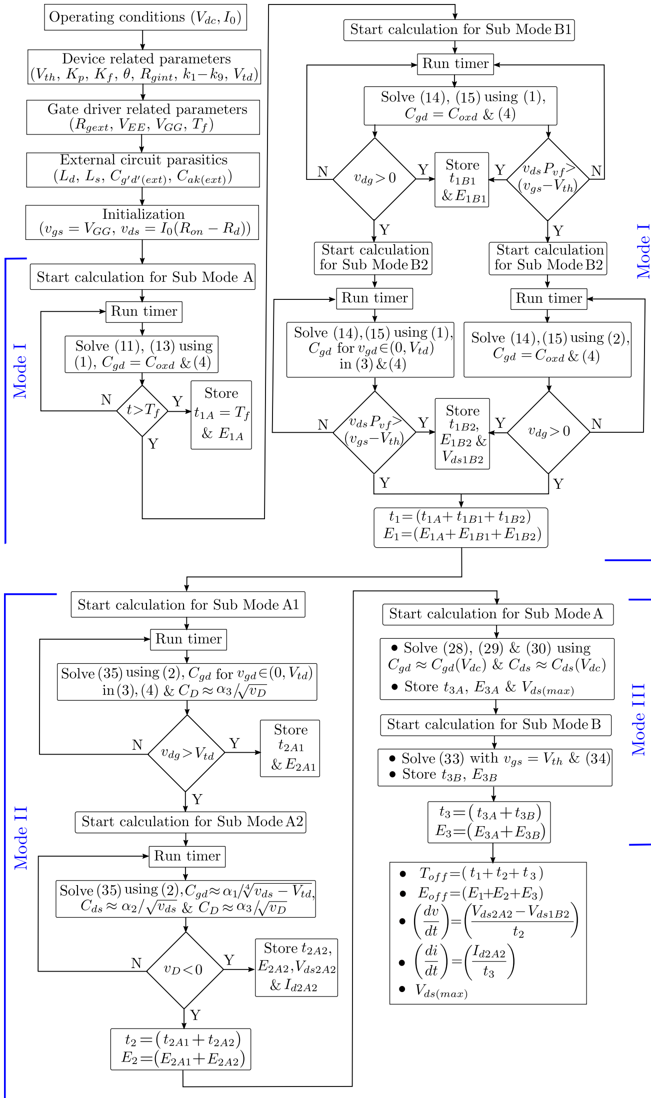
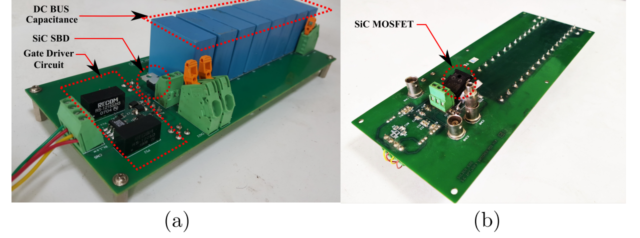


Fig. 13: Flowchart for turn-OFF analysis of SiC MOSFETs

VI. EXPERIMENTAL SET-UP



(a) (b)

Fig. 14: Double pulse test setup: (a) Top side, (b) Bottom side

The behavioural model is validated experimentally through double pulse test (DPT). Two sets of SiC MOSFET and SiC SBD diode pairs (TABLE II) are used. Device related parameters extracted from the datasheet are given in TABLE III and TABLE IV. Note, the V_{th} number obtained using (1) and (2) (see TABLE III) is higher compared to the value given in datasheet. As mentioned in Section IV, a single channel approximation of i_{ch} is used as modelling of low channel current region is not important from switching transition point of view and this results in a comparatively higher V_{th}.

TABLE II: Device list (1200V)

	SiC MOSFET (TO-247)	Current (A) @25°C	SiC SBD (TO-220)	Current (A) @25°C
SET1	C2M0160120D	19	C4D05120A	19
SET2	C2M0080120D	36	C4D10120A	33

DPT is designed for V_{dc}=800V and I_0=30A. Total DC bus capacitor of 64 μF is used. Eight flim capacitors from EPCOS (B32776G1805+000) with 8μF capacitance and 1300V DC blocking capability are connected in parallel to get the equivalent capacitance. It also minimizes the equivalent DC bus inductance. Air core inductor with L =210 μH (@200kHz) is used as the output inductive load. The values of circuit related parameters used for simulation and the proposed method are obtained through experiment [31] and given in TABLE V. Values of external circuit parameters depend on the package type as well as layout. Both $C_{g'd'(ext)}$ and $C_{ak(ext)}$ are of picofarad range and difficult to measure using typical capacitance measurement equipment. For $C_{g'd'(ext)}$ measurement, the MOSFET is disconnected and a large resistance is connected in series. Finally, the step response of the resultant circuit is observed and it is approximately $15pF$. The same technique is used for the first part of $C_{ak(ext)}$ measurement ($\approx 9pF$). The parasitic capacitance of the inductive load is estimated from the frequency response of the inductive load

TABLE III: Device parameters (From static characteristics)

	V_{th} (V)	K_p (A/V^2)	K_f	θ (1/V)	P_{vf}	R_d (Ω)	R_{gint} (Ω)
SET1	4.6	1.3	1.54	0.03	0.33	0.04	6.5
SET2	5.6	1.6	2.1875	0.01	0.4	0.01	4.6

TABLE IV: Device parameters (From dynamic characteristics)

	C_{gs} (nF)	k_1 (nF)	k_2 (V)	k_3	V_{td} (V)	k_4 (nF)	k_5 (V)	k_6 (nF)	k_7 (V)	k_8 (nF)	k_9 (V)
SET1	0.525	0.6	0.2	1.24	12	0.055	0.02	0.4323	5.5	0.39	2
SET2	0.95	0.95	0.35	0.7050	12	0.12	0.025	0.785	5.5	0.754	1.7

TABLE V: External circuit parameters

	L_d (nH)	L_s (nH)	$C_{g'd'(ext)}$ (nF)	$C_{ak(ext)}$ (nF)
SET1	60	6	0.015	0.015
SET2	65	4	0.015	0.015

TABLE VI: Driver parameters

V_{CC} (V)	V_{GG} (V)	$R_{g(driver)}$ (Ω)	R_{gext} (Ω)	T_f (ns)
-5	20	0.5	2.5, 4.5, 8.5	4

and it is approximately $\approx 6pF$. PSM3750 from N4L Ltd. is used for this purpose. Then the equivalent $C_{ak(ext)} = (9+6)pF = 15pF$. For each diode switch pair (SET1,2), experiments are conducted for two values of V_{dc}, five values of I_0 and three values of $R_{g(ext)}$. This implies a total of 60 different operating conditions.

Opto-isolator IX3180GS followed by a current booster IXDN609SI is used to drive the gate of the SiC MOSFET. Gate driver parameters are given in TABLE VI and it is common for both the sets.

Signals need to be measured are $v_{g's'}(t)$, $v_{d's'}(t)$ and $i_d(t)$. 1 GHz oscilloscope (MDO3104) from Tektronix is used for measurement. Passive probe from Tektronix with 1 GHz bandwidth (TPP1000) is used for $v_{g's'}(t)$ measurement. $v_{d's'}(t)$ is measured using a high voltage single ended probe from Tektronix (P5100A) with 500 MHz bandwidth and Current $i_d(t)$ is measured using a AC/DC current probe from Tektronix (TCP0030A) with 120 MHz bandwidth and 50A peak current measurement capability. Matching of propagation delay between voltage and current signals are done using a delay matching instrument available from Tektronix (067-1686-00, Power Measurement Deskew and Calibration Fixture).

Circuit simulator called SimPowerSystems from MATLAB/Simulink® is used to simulate the behavioural model. To implement the behavioural model of the MOSFET (Fig. 1) and also the SBD, we used voltage dependent current sources and variable capacitances available in SimPowerSystems library. Backward Euler solver with a fixed time step of 1 pico-second is used for simulation. All the experiments are performed at 25°C.

VII. Simulation and Experimental Results

The objective of this section is to validate the turn off switching dynamics analysis presented in Section V through simulation of the behavioural model and experiment.

A. Validation of the behavioural model

$v_{d's'}(t)$ and $i_d(t)$ are the important experimentally obtained waveforms related to turn off transition. In Fig. 15, behavioural simulation and experimental results are plotted in the same plot for $V_{dc} = 800V$, $R_{gext} = 2.5\Omega$ and $R_{gext} = 8.5\Omega$ and two different current levels (I_0) for SET1 and SET2 respectively. Experimental waveforms match closely with simulation over the switching transition period. This observation is seen to hold good for other 52 operating conditions also.

From the above observations, we can conclude that the behavioural model is accurate enough to predict the turn off switching dynamics and the device, gate driver and external circuit parameters are correctly estimated and used in the simulation.

B. Verification of proposed analytical model

To verify the correctness of the proposed analytical model, important intermediate quantities obtained from the behavioural model for each mode is compared with the values obtained using the analytical model. The behavioural model is used for comparison as it is not possible to get the correct values of most of the intermediate quantities from the experimental result. The operating conditions are $V_{dc} = 800V$, $R_{gext} = 8.5\Omega$ and $I_0 = 15A$ for SET1 and $I_0 = 25A$ for SET2 (Table VII). These numbers match closely. Also to verify the correctness of the assumptions in each mode, the time evolution of important state variables obtained from the proposed model in each mode is plotted over a simulated result for ($V_{dc} = 800V$, $R_{gext} = 2.5\Omega$, $I_0 = 10A$) and ($V_{dc} = 800V$, $R_{gext} = 8.5\Omega$, $I_0 = 15A$) for SET1 (Fig. 16(a) and Fig. 16(b) respectively). A close match is observed between simulated waveforms and waveforms obtained using the proposed model for both the operating conditions. A similar study is carried out for other 59 operating conditions and close agreements are observed. This validates the proposed analytical model in each mode of switching transition (Section V).

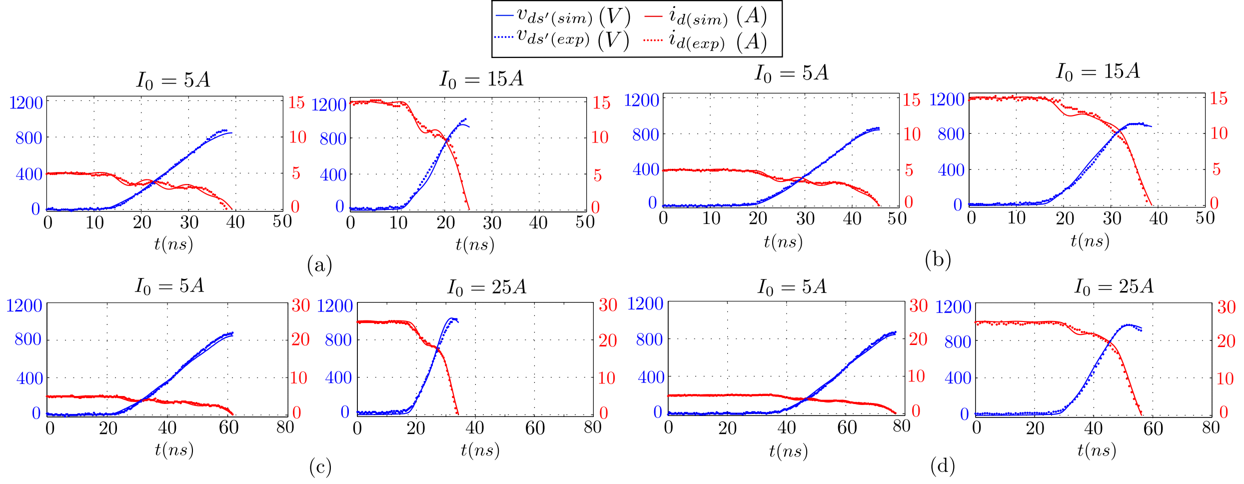


Fig. 15: Simulation vs experimental waveforms, Operating condition: (a) [800V, 2.5 Ω, SET1], (b) [800V, 8.5 Ω, SET1], (c) [800V, 2.5 Ω, SET2] and (d) [800V, 8.5 Ω, SET2]

TABLE VII: Comparison of important intermediate quantities (Simulation and Analytical)

		Mode I					Mode II				Mode III			
		V_{gs1B2} (V)	V_{ds1B2} (V)	I_{ch1B2} (A)	t_1 (ns)	E_1 (μJ)	I_{ch2A2} (A)	t_2 (ns)	E_2 (μJ)	$\left(\frac{dv_{ds}}{dt}\right)$ (V/ns)	$V_{ds(max)}$ (V)	t_3 (ns)	E_3 (μJ)	$\left(\frac{di_d}{dt}\right)$ (A/ns)
SET1	Sim	9.27	14.74	12.48	15.31	1.072	6.99	17	48.79	49.66	919	7.85	27.98	1.48
	Anly	9.22	13.94	12.17	14.8	0.889	7.27	17.2	50.29	49.53	902.36	8.53	31.35	1.16
SET2	Sim	11.03	13.82	22.42	26.65	3.27	13.81	20.93	118.2	41.3	961.75	10.38	70.82	2.07
	Anly	10.95	13.38	21.75	26.06	2.98	13.88	20.77	121.65	42.11	927	10.94	72.18	1.6

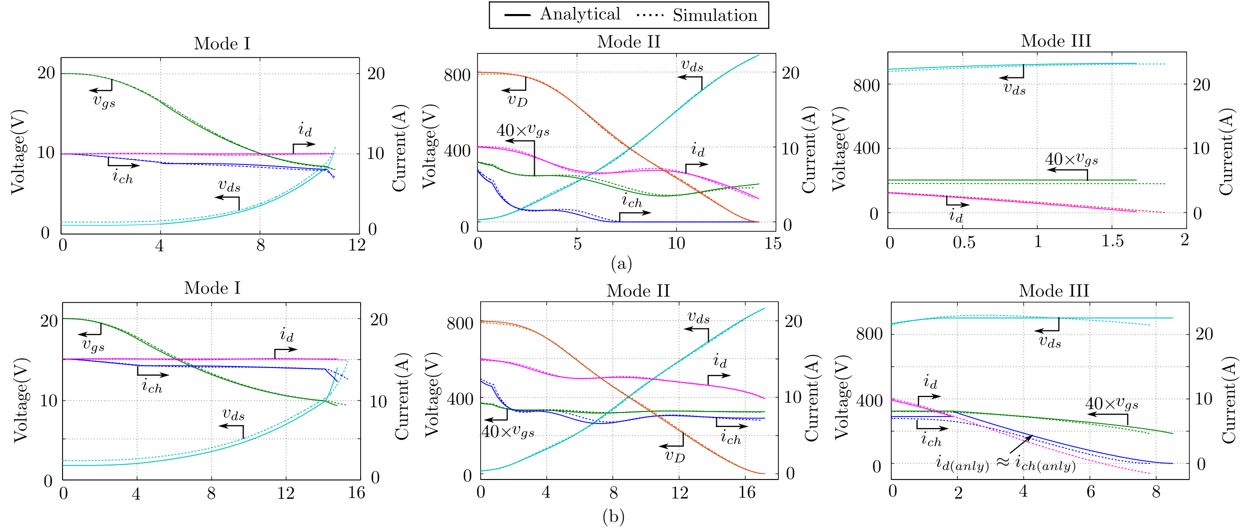


Fig. 16: SET1: Operating conditions: (a) [800V, 2.5Ω, 10A], (b) [800V, 8.5Ω, 15A]

C. Effect of V_{dc}, I_0 and R_{gext} on turn off switching dynamics

In this subsection, the effect of variation in V_{dc}, I_0 and R_{gext} on turn off switching transient has been studied. Turn off switching transition time T_{off} is plotted as a function of I_0 and R_{gext} for SET1 and SET2 in Fig. 17(a) and Fig. 17(b) respectively. A close match can be seen in between behavioural simulation, analytical and experimental results. Only for SET1, $T_{off(sim)}$ and $T_{off(anly)}$ deviate slightly from $T_{off(exp)}$ for high values of I_0. It can be observed that for a given R_{gext} as I_0 increases, T_{off} reduces sharply first and then almost saturates at high values of I_0. Also for a given I_0, increase in R_{gext} leads to an increase in T_{off}. This increase is more prominent for high I_0. For low I_0, channel current i_{ch} collapses to zero at the beginning of the voltage rise period and parameters of the gate circuit have a negligible impact on switching transition. For $V_{dc} = 600V$, the switching transition time is smaller compared to $V_{dc} = 800V$ due to the reduction in voltage rise time. The proposed analytical model is also valid for a half bridge configuration where two SiC MOSFET are series connected. In that case, diode capacitance will be

replaced by the equivalent output capacitance (C_{oss}) of the complementary device. Proper estimation of delay and voltage rise time is required to select optimum dead-time, otherwise, it may lead to premature turn on if dead-time is not sufficient or higher dead-time loss (because of diode conduction) when the dead-time is long. Delay time is of comparable magnitude with voltage rise time for SiC MOSFET and accurate estimation of delay time is important. Accurate estimation of T_{off} for a wide operating range helps in optimum dead-time selection.

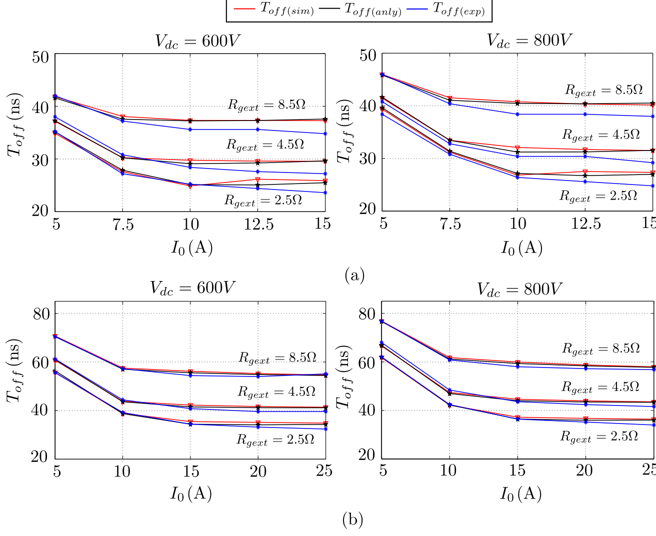


Fig. 17: Turn off transition time (T_{off}): (a) SET1, (b) SET2

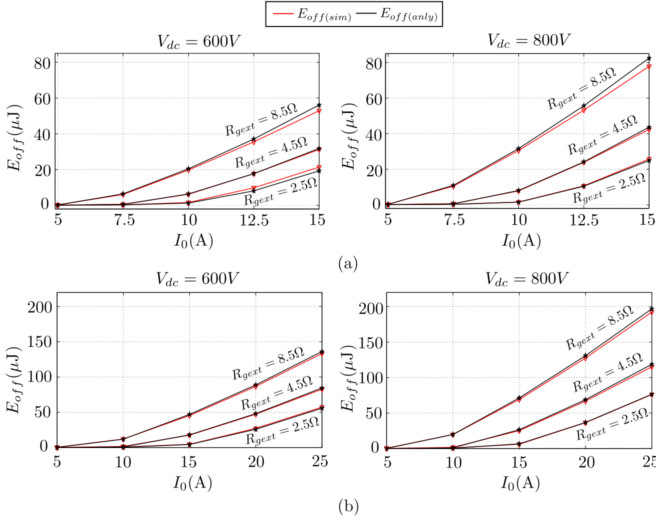


Fig. 18: Turn off actual loss (E_{off}): (a) SET1, (b) SET2

In Fig. 18(a) and Fig. 18(b), actual turn off switching loss (E_{off}) is plotted as a function of I_0 and R_{gext} for SET1 and SET2 respectively. A close agreement between behavioural simulation and analytical results are observed. For low values of I_0, E_{off} is negligible as channel current collapses to zero at the beginning of voltage rise period. E_{off} is monotonically increasing function of both I_0 and R_{gext}. It is worthwhile to note that E_{off} can not be obtained from experimental waveforms and there is a significant difference between experimentally obtained loss $E'_{off(exp)}$ and actual switching loss ($E_{off(sim)}$ or $E_{off(anly)}$). In Fig. 19 (a) and (b), actual switching loss obtained from the proposed analytical model ($E_{off(anly)}$) using (6) and the experimentally measured loss ($E'_{off(exp)}$) (using (7)) is compared with the actual switching loss obtained from behavioural simulation ($E_{off(sim)}$) using (6) for ($V_{dc} = 600V$, $R_{gext} = 2.5\Omega$), ($V_{dc} = 800V$, $R_{gext} = 8.5\Omega$) and $I_0 = 5 - 15A$ for SET1 and $I_0 = 5 - 25A$ for SET2. $|E_{anly} - E_{sim}|(\mu J)$ and $|E'_{exp} - E_{sim}|(\mu J)$ is plotted for the aforementioned operating conditions where $E_{off(sim)}$ is used as the reference. It can be seen from Fig. 19 that there is a significant difference between $E_{off(sim)}$ and $E'_{off(exp)}$. The proposed analytical model estimates the actual turn off switching loss ($E_{off(anly)}$) which is close to $E_{off(sim)}$ and experimental measurement grossly overestimates the turn off switching loss. Estimation of actual turn off switching loss one of the contributions of this work.

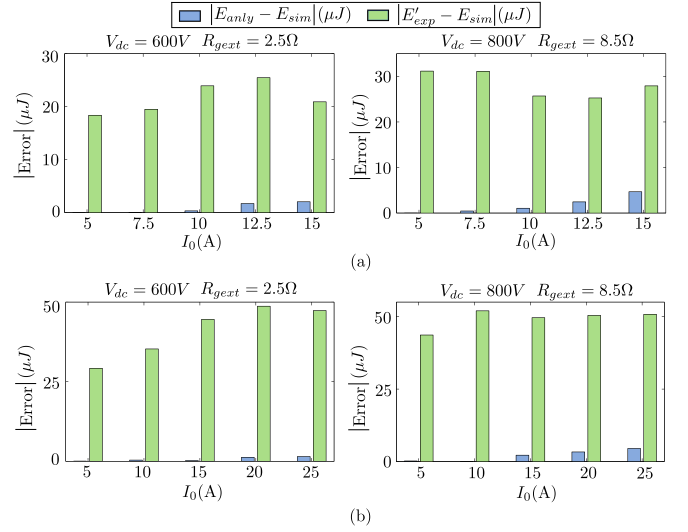


Fig. 19: $|Error|$ (μJ) vs $I_0(A)$ plot: (a) SET1, (b) SET2

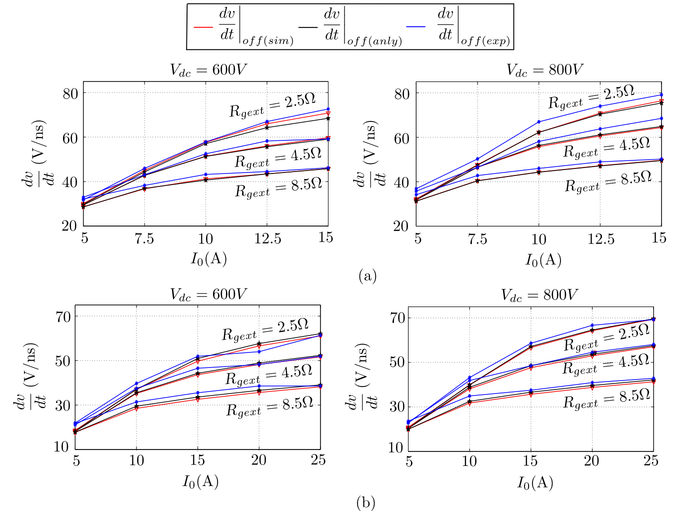


Fig. 20: Turn off (dv/dt): (a) SET1, (b) SET2

For both behavioural simulation and proposed analytical model, (dv/dt) is defined as the average rate of change in v_{ds}

TABLE VIII: Comparison of (di/dt) (A/ns)

	I_0 (A)	$R_{gext} = 2.5\Omega$ Sim	Anly	Exp	$R_{gext} = 8.5\Omega$ Sim	Anly	Exp
SET1	5	0.59	0.62	0.63	0.6	0.68	0.64
	10	1.7	1.55	1.78	1.36	1	1.25
	15	1.86	1.45	2	1.48	1.15	1.47
SET2	5	0.61	0.51	0.5	0.59	0.55	0.44
	15	2.5	1.81	2	1.66	1.22	1.5
	25	2.76	2.1	2.7	2	1.6	1.78

during voltage rise period (Mode II). It is difficult to define the start of voltage rise period from the experimental waveforms. So for experimentally measured (dv/dt), 10%-100% change in v_{ds} is considered. (dv/dt) is plotted as a function of I_0 for different values of R_{gext} and SET1 and SET2 in Fig. 20(a) and Fig. 20(b) respectively. Close agreement is observed between behavioural simulation, analytical and experimentally obtained results. (dv/dt) is a strong function of both I_0 and R_{gext}. It increases with I_0 for a fixed R_{gext} and reduces as R_{gext} increases. As previously mentioned, for low I_0 and /or R_{gext}, channel current i_{ch} collapses to zero at the beginning of voltage rise period. So for low I_0, (dv/dt) has a weak dependence on R_{gext}.

For experimental, behavioural simulation and proposed analytical model, (di/dt) is defined as the average rate of change in i_d during current fall period (Mode III). (di/dt) is given in Table VIII for $V_{dc} = 800V$, three values of I_0 and two values of R_{gext} for SET1 and SET2. Good agreement between simulation and experimental result is observed for most of the operating conditions. The analytical model estimates the (di/dt) with higher accuracy for lower I_0. But for higher I_0, proposed model slightly underestimates the (di/dt) rate. This is because there is a small difference between i_d and i_{ch} at the end of the current fall period and i_d crosses zero before i_{ch} (see Fig. 12). In the proposed model, $i_d \approx i_{ch}$ has been considered which results in a slight overestimation of current fall time and subsequently underestimate the (di/dt) rate. Also, it can infer from these results that the (di/dt) reduces with the increase in R_{gext} and it is prominent for higher values of I_0.

TABLE IX: Comparison of $V_{ds(max)}$ (V)

	I_0 (A)	$R_{gext} = 2.5\Omega$ Sim	Anly	Exp	$R_{gext} = 8.5\Omega$ Sim	Anly	Exp
SET1	5	848.56	848.54	880	847.4	851.65	864
	10	924.92	928.62	920	903.84	891.37	888
	15	957.9	951.5	1000	919	902.36	912
SET2	5	845.23	837.07	864	844	840.3	872
	15	985.24	971.86	990	931.15	910.38	944
	25	1030.6	1005.7	1020	961.75	927	964

Similar as (di/dt), $V_{ds(max)}$ is given Table IX for $V_{dc} = 800V$, three values of I_0 and two values of R_{gext} for SET1 and SET2. Simulation, analytical and experimental results match closely for most of the operating conditions. As I_0 increases, $V_{ds(max)}$ increases for a constant R_{gext}. Also for a constant I_0, $V_{ds(max)}$ reduces with the increase in R_{gext}. This observation is prominent for higher values of I_0.

VIII. Comparison between proposed analytical model and other existing models

This section presents a comparison of the proposed analytical model with known models available in the literature. It can be observed from Table I, there is no single work in the literature that provides superior performance in all three modes. So a mode by mode comparison is done. For a given mode, a particular existing work is selected that results in the best performance in that mode. Based on the observations in Table I, [26] is selected for delay period (Mode I) and [16] is chosen for the other two modes (Mode II and Mode III). The correctness of the behavioural model to capture turn off switching transient has already been verified through experiment. So the results obtained from the behavioural simulation are taken as the standard for this comparison. The comparison is done at $V_{dc} = 800V$ and $(R_{ext} = 2.5\Omega, I_0 = 5A)$, $(R_{ext} = 8.5\Omega, I_0 = 15A)$ for SET1 and $(R_{ext} = 2.5\Omega, I_0 = 5A)$, $(R_{ext} = 8.5\Omega, I_0 = 25A)$ for SET2. This set of results consist of both low I_0, R_{ext} and high I_0, R_{ext} case and encompasses all different possibilities.

In Mode I, delay time (t_1) estimated from the proposed analytical model is compared with the results of the existing model of [26] and behavioural mode in the following table for the above mentioned operating conditions (Mode I of Table X). It can be concluded from the comparison that the existing model grossly underestimates t_1 for both low I_0, R_{ext} and high I_0, R_{ext} condition and the error between estimated t_1 using behavioural model and existing approach lies between 62-70% for SET1 and 67-74.5% for SET2 for the entire operating conditions. On the other hand, proposed analytical model considers the coupled dynamics of the gate and the power loop and uses the detailed model of the miller capacitance and the channel current in ohmic region. This results in better estimation of t_1. In Mode II, important quantities for comparison are voltage rise time (t_2), actual switching loss (E_2) and (dv/dt). These quantities obtained from [16] is compared with the results obtained from behavioural model and the proposed analytical model (Mode II Table X). The proposed analytical model performs much better compared to the existing model and the error in estimation is more prominent for the high value of R_{gext}. Note, a nonlinear model of channel current is used and the external gate-drain parasitic capacitance effect is taken into account in proposed analytical model, which results in better estimation of the previously mentioned quantities. Important quantities of Mode III are current fall time (t_3), actual switching loss (E_3), (di/dt) and transient over-voltage $(V_{ds(max)})$. These quantities obtained from [16] are compared with the behavioural model and the proposed analytical model. Proposed analytical model performs better over the existing model throughout the operating range.

From the above discussion, it can be concluded that the proposed analytical model performs better compared to the existing model in all the modes of turn off switching transient and over the entire operating range.

IX. Conclusion

An analytical model to study the turn off switching dynamics of SiC MOSFET and Schottky diode pair using

TABLE X: Comparison of behavioural simulation (Sim), proposed analytical model (Anly) and existing model(Exst)

			Mode I	Mode II			Mode III			
			t_1 (ns)	t_2 (ns)	E_2 (μJ)	$\left(\frac{dv}{dt}\right)$ (V/ns)	t_3 (ns)	E_3 (μJ)	$\left(\frac{di}{dt}\right)$ (A/ns)	$V_{ds(max)}$ (V)
SET1	[2.5 Ω, 5A]	Sim	11.70	25.13	0.044	32.25	2.52	0	0.59	848.56
		Anly	11.94	25.55	0.034	32.07	2.15	0	0.62	848.54
		Exst	4.12	20.55	0.01	41.63	0.62	0	0.91	862.68
	[8.5 Ω, 15A]	Sim	15.31	17	48.79	49.66	7.85	28	1.48	919
		Anly	14.8	17.2	50.29	49.53	8.53	31.35	1.15	902.36
		Exst	5.05	11.27	16.41	79.76	3.7	10.08	1.67	939.26
SET2	[2.5 Ω, 5A]	Sim	18.58	21.07	0.28	39.83	2.54	0	1.06	884.55
		Anly	18.67	21.19	0.23	39.92	2.41	0	1.11	887.76
		Exst	5.49	18.36	0.08	47.103	1.22	0	1.09	879.93
	[8.5 Ω, 25A]	Sim	26.65	20.93	118.18	41.27	10.38	70.82	1.99	961.75
		Anly	26.06	20.77	121.65	42.11	10.94	72.18	1.6	927
		Exst	7.33	14.86	56.69	62.77	5.98	37.28	2.41	995.72

datasheet parameters and external circuit parasitics is presented in this paper. This model is derived from the behavioural model of the devices (SiC MOSFET and SBD) and the external circuit parasitics through approximations. First, the behavioural model is validated through experiment for two sets of 1200V SiC MOSFET and Schottky diode pair and a wide range of operating conditions. Then the behavioural model is used to verify the proposed analytical model. Important quantities related to turn off switching dynamics obtained from the experiment, behavioural simulation and the proposed analytical model are compared. Proposed model estimates the switching transition time accurately and numbers are close to behavioural simulation and experimental approach. It has been established in this paper that there is a significant difference between actual switching loss and experimentally measured loss. Experimental measurement grossly overestimates the turn off switching loss. On the other hand, turn off switching loss estimated using the proposed analytical technique closely matches with the actual loss obtained from behavioural simulation. For the low value of external gate resistance and/or load current, channel current collapses to zero before voltage rise period ends and gate looses its control over power circuit state variables. In this scenario, though the turn off switching loss is negligible, (dv/dt), (di/dt) and transient over-voltage have a weak dependence on external gate resistance. As external gate resistance and/or load current increases, channel current sustains during voltage rise period. This may result in a significant amount of switching loss. But the external gate resistance has better control over (dv/dt), (di/dt) and transient over-voltage. A transition mode is observed at the starting of the current fall period where the difference between drain current and channel current reduces to zero and it predicts the transient over-voltage.

In summary, the proposed analytical model provides a fast inexpensive method to accurately estimate the quantities related to turn off switching transient of SiC MOSFET and Schottky diode pair using datasheet parameters and external circuit parasitics which are important for power electronic converter design.

X. Appendix

$$\begin{pmatrix} \frac{dv_D}{dt} \\ \frac{dv_{ds}}{dt} \\ \frac{di_d}{dt} \\ \frac{dv_{gs}}{dt} \end{pmatrix} = \begin{pmatrix} \left(\frac{i_d - I_0}{C_{D(eq)}(v_D)}\right) \\ \left(\frac{i_d - i_{ch}}{C_{oss(eq)}(v_{dg}, v_{ds})}\right) \\ \left(\frac{V_{dc} - v_{ds} - v_D}{L_d + L_s}\right) \\ (A + B\,(v_{ds} + v_D) + C\,(i_d - i_{ch}) + Dv_{gs}) \end{pmatrix} \tag{35}$$

$$A = \left(\frac{V_{EE} - \frac{V_{dc}L_s}{L_d + L_s}}{\tau_1}\right),\ B = \left(\frac{L_s}{(L_d + L_s)\tau_1}\right),$$

$$C = \left(\frac{\tau_2}{\tau_1 C_{oss(eq)}(v_{dg}, v_{ds})}\right),\ D = -\frac{1}{\tau_1}$$

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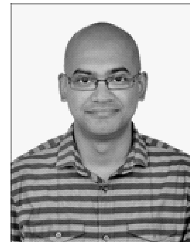

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