A Three-Phase Three-Level Isolated DC-AC Converter with Line Frequency Unfolding

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***Abstract*—A three-level three phase single-stage high frequency link (HFL) DC-AC converter is reported in this paper for grid integration of photovoltaic sources. The proposed topology employs two three-level neutral point clamp (NPC) half-bridge legs on the DC side. The advantages of using three-level legs over conventional two level are- (a) the three-level legs can be implemented with the devices with lower blocking voltage which are economical, (b) the low voltage blocking devices have lower on-state drop and lower turn ON-OFF energy losses compared to high voltage blocking devices used in a two level leg. These help to improve the converter efficiency. The sinusoidal pulse width modulation is implemented with the three-level NPC legs. The modulation strategy ensures reduced neutral current drawn by the NPC legs. The inner switches of the NPC legs are zero voltage switched (ZVS). The turn ON transitions of the outer switches are with zero current (ZCS). The proposed solution employs two high frequency transformers to provide galvanic isolation which results in compact, low cost isolated converter solution. The intermediate DC link is pulsating and does not require any filtering. A low frequency unfolder is employed to generate line frequency AC from pulsating DC. The switching loss of the unfolder is negligible. The proposed topology can support stand-alone load upto ± 0.866 PF. The converter operation is verified on a 2kW hardware prototype.**

***Index Terms*—Three-level NPC inverter, phase shift modulation, DC-AC converter, high frequency link, single-stage, zero voltage switching (ZVS), zero-current switching (ZCS), line frequency unfolding**

I. Introduction

THE pulse width modulated (PWM) single-stage high frequency link (HFL) DC-3ϕ AC converters are gaining attention for applications like grid integration of renewable energy sources [1], [2], energy storage system [3], electric or hybrid electric vehicle [4] etc. The single-stage converters do not use interstage bulky DC capacitors which are unreliable. To provide galvanic isolation high frequency transformers (HFT) are used which results in high power density, economical converter solution. In literature the PWM single-stage HFL DC-3ϕ AC converters are classified into two major categories- cyclo-converter type (CHFL) [5]–[7] and rectifier type (RHFL) [8], [9]. In CHFL topology, H-bridge is used to generate high frequency (HF) AC from input DC. The HF AC is fed to HFT. A cyclo-converter is employed in the secondary of the HFT to generate line frequency AC from the HF AC. In a RHFL topology, the cyclo-converter of the CHFL is replaced with an active rectifier followed by a voltage source inverter (VSI). The DC link between the rectifier and inverter stage is pulsating.

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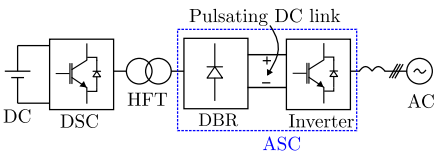


Fig. 1: A unidirectional single-stage RHFL inverter

In applications like grid integration of renewables or fuel cells, where the active power flow is mostly from input DC to AC, the unidirectional PWM RHFL DC-3ϕ AC topologies [10]–[15] are becoming popular. In an unidirectional RHFL topology the rectifier stage is implemented with diode bridge rectifier (DBR) instead of active switches (see Fig. 1) thus reduces active component count and additional driving circuitry. As seen in Fig. 1, these converters have three parts- DC side converter (DSC), AC side converter (ASC) and high frequency transformer (HFT). Though unidirectional, but these converters might need to support $\pm$ 0.9/0.95 PF operation at the grid end as per grid requirements [16]. The converter proposed in [10]–[13] support operation upto ± 0.866 PF. These converters employ a hybrid modulation strategy where the ASC inverter is high frequency switched for one third of the line cycle (partial unfolding). The unidirectional topologies presented in [14], [15], though achieves complete line frequency unfolding of the ASC, they can only support UPF operation. Additional shunt compensator is needed to support the reactive power demand at the grid end.

The unidirectional RHFL topologies discussed so-far employ two level structure on the DSC to generate high frequency AC from input DC. The three-level NPC converters are considered as an alternative to the standard two-level VSIs in low voltage applications [17], [18] because of increased efficiency at higher switching frequencies along with improved output harmonic spectrum and reduced EMI. With same input DC voltage, the three-level legs can be implemented with lower blocking voltage devices which are economical. The low blocking voltage devices have lower on-state drop and lower turn ON-OFF energy losses compared to high voltage blocking devices used in a two level leg [17] hence the improvement in the efficiency. The idea can be extended to isolated DC-DC and DC-AC converter topologies. A three-level ZVS PWM DC-DC converter was first introduced in [19], where the input two level H-bridge of a PSFB (phase shifted full bridge) converter is replaced with a three-level NPC leg. A passive auxiliary circuit is proposed in [20], which resets the primary circulating current in zero state hence improves

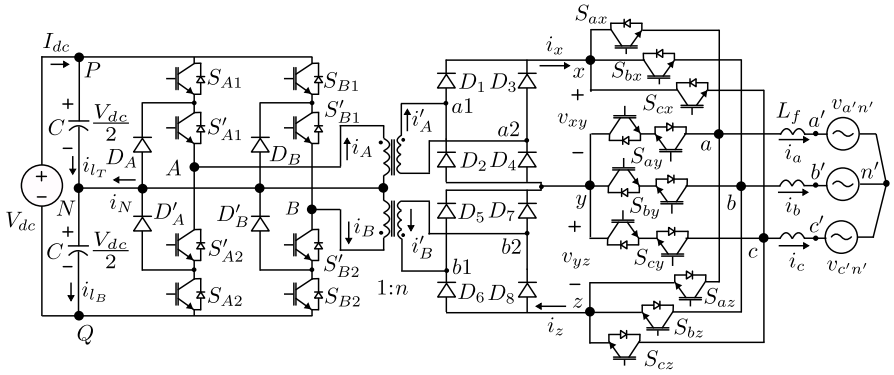


Fig. 2: Configuration of the proposed inverter

the efficiency. For high power application, three phase, three-level DC-DC converters are proposed in [21], [22]. Like a PSFB, the ZVS of a three-level DC-DC converter is also load dependent and at light load the converter is hard switched. Even hard switched, the light-load efficiency of a three level DC-DC converter is higher than a similarly rated two level counterpart as the blocking voltage of the devices are half and have better switching characteristics [23], [24]. In [25], a unidirectional RHFL inverter topology is reported where the DSC has three, three-level NPC legs. But the converter can only support UPF operation.

In this paper, a three-level three phase single stage high frequency link DC-AC converter is proposed (see Fig. 2). The proposed solution is unique w.r.t the above discussed topologies because it has all the following features together. i) On the DSC, the converter has two three level NPC half-bridge legs to generate high frequency AC from the input DC. ii) The ASC achieves line frequency unfolding. iii) The proposed topology can supply stand-alone load upto $\pm$ 0.866 power factor. Additionally, the converter has following key features. (a) Sinusoidal pulse width modulation (PWM) is implemented with the DC side three-level legs. But the modulation strategy and the switching scheme of the NPC legs are completely different from the conventional PWM strategy applied to a 3ϕ, three level NPC inverter which results in generation of line frequency AC from input DC. The proposed strategy generates PWM high frequency AC across the transformer primaries using the two three level, NPC legs. (b) Suggested modulation strategy ensures reduced neutral current drawn by the three-level legs. (c) The inner switches of the three-level legs are zero voltage switched (ZVS) over complete line cycle. (d) Zero current turn ON (ZCS) of the outer switches are ensured. (e) Interstage DC link is pulsating and does not employ filter capacitor. (f) Low frequency switching results in negligible switching loss of the unfolder. (g) The high frequency galvanic isolation provides high power density, economical converter solution.

The paper is organized as follows. The modulation strategy of the converter is discussed in section II. In section III the detailed switching process of the three level legs are described. Experimental validation of the converter operation is presented in section IV.

II. Converter Modulation Technique

As shown in Fig. 2, the proposed DC-AC converter employs two three-level neutral point clamp ($3L$-NPC) half-bridge legs on the DC side. Two high frequency transformers (HFT), each with a turns ratio $1:n$, provide the galvanic isolation. The primary windings of the HFTs are connected between the poles of the NPC half-bridge legs and the neutral point, N as seen in Fig. 2. The neutral point, N, is obtained by connecting two capacitors (C) in series across the input DC bus (V_{dc}). The secondary output of each HFT is fed to a full bridge rectifier. The output ports of the two rectifiers are connected in series to obtain a three-level DC link. The proposed topology does not employ DC link filter capacitors and hence the three-level DC link is pulsating. To obtain three phase line frequency AC from the pulsating DC link, an unfolder with six two-quadrant and three four-quadrant switches, is employed. The three phase output of the converter is connected to a balanced three phase source through line filters (L_f).

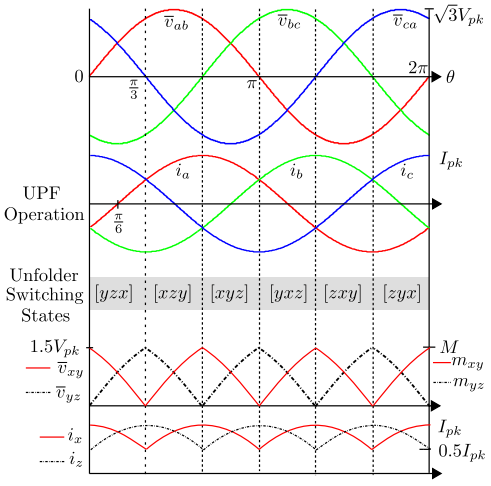


Fig. 3: Modulating strategy of the proposed converter

To generate the balanced three phase line frequency average pole voltages (Fig. 3), $\overline{v}_{ab} = \sqrt{3}V_{pk}\sin(\omega_o t{=}\theta)$, $\overline{v}_{bc} = \sqrt{3}V_{pk}\sin\left(\theta - \frac{2\pi}{3}\right)$ and $\overline{v}_{ca} = \sqrt{3}V_{pk}\sin\left(\theta + \frac{2\pi}{3}\right)$ with angular frequency $\omega_o = 2\pi f_o$, the unfolder is switched six times over a line cycle. The switching states of the unfolder is given in Table I. The unfolder poles (a, b, c) can be connected

to the node x through the switches $S_{(a,b,c)x}$, node y through the switches $S_{(a,b,c)y}$ and node z through the switches $S_{(a,b,c)z}$ respectively. Unfolder switching state $[yzx]$ indicates that the pole a is connected to node y through S_{ay}, the pole b is connected to node z through S_{bz} and the pole c is connected to node x through S_{cx}. Similarly the other states are also defined. Following the switching states, the unfolder two quadrant switches are switched at line frequency whereas the four quadrant switches are switched at twice of the line frequency hence incurring negligible switching loss.

TABLE I: Unfolder switching states

θ	$[0,\frac{\pi}{3}]$	$[\frac{\pi}{3},\frac{2\pi}{3}]$	$[\frac{2\pi}{3},\pi]$	$[\pi,\frac{4\pi}{3}]$	$[\frac{4\pi}{3},\frac{5\pi}{3}]$	$[\frac{5\pi}{3},2\pi]$
State	$[yzx]$	$[xzy]$	$[xyz]$	$[yxz]$	$[zxy]$	$[zyx]$

From the switching states of the unfolder, the rectifier average output voltages ($\overline{v}_{xy}$ and $\overline{v}_{yz}$) and currents i_x, i_z are obtained and are given in Table II. $i_{a,b,c}$ are the sinusoidal line currents with negligible ripple, supplied to the load. For example, when the switching state is $[yzx]$, the unfolder

TABLE II: Rectifier output voltages and currents

Unfolder State	$[yzx]$	$[xzy]$	$[xyz]$	$[yxz]$	$[zxy]$	$[zyx]$
$\overline{v}_{xy}$	$\overline{v}_{ca}$	-$\overline{v}_{ca}$	$\overline{v}_{ab}$	-$\overline{v}_{ab}$	$\overline{v}_{bc}$	-$\overline{v}_{bc}$
$\overline{v}_{yz}$	$\overline{v}_{ab}$	-$\overline{v}_{bc}$	$\overline{v}_{bc}$	-$\overline{v}_{ca}$	$\overline{v}_{ca}$	-$\overline{v}_{ab}$
i_x	i_c	i_a	i_a	i_b	i_b	i_c
i_z	-i_b	-i_b	-i_c	-i_c	-i_a	-i_a

switches S_{ay}, S_{bz} and S_{cx} are ON. Hence, the rectifier output port xy is connected across the pole terminals ca and yz is connected across ab. Thus $\overline{v}_{xy} = \overline{v}_{ca}$, $\overline{v}_{yz} = \overline{v}_{ab}$ and the rectifier output currents $i_x = i_c$ and $i_z = -i_b$. To generate the average output rectifier voltages as given in Table II, the modulation signals of the DC side $3L$-NPC legs, $m_{xy} = \dfrac{\overline{v}_{xy}}{n(V_{dc}/2)}$ and $m_{yz} = \dfrac{\overline{v}_{yz}}{n(V_{dc}/2)}$ are shown in Fig. 3. M is defined as $M = \dfrac{3V_{pk}}{nV_{dc}}$ and $M \in [0,1]$.

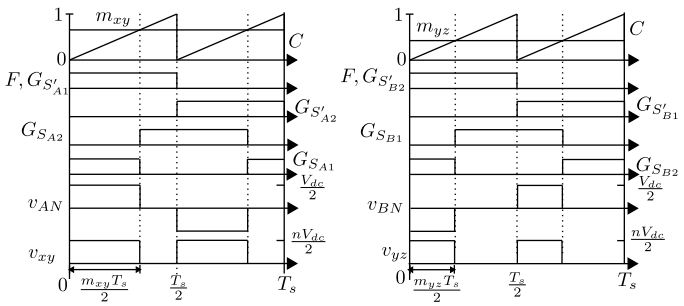


Fig. 4: Modulation of DC side three-level legs

The $3L$-NPC legs are high frequency switched to generate the sinusoidal pulse width modulated high frequency AC across the transformer primaries. The modulation strategy is shown in Fig. 4. A signal F with period T_s and 50% duty ratio is considered over which the transformer flux is balanced. F is assigned to be the gating signals of S'_{A1} ($G_{S'_{A1}}$) and S'_{B2} ($G_{S'_{B2}}$). S'_{A2} is switched complementary with S'_{A1}. Similarly, S'_{B1} is complementary switched with S'_{B2}. The outer switches of the legs, $(S_{A1} - S_{A2})$ and $(S_{B1} - S_{B2})$, are also complementary switched. A unipolar saw-tooth carrier, C, with period $\frac{T_s}{2}$ is considered which is aligned with F. The modulation signals m_{xy} and m_{yz} are compared with C to obtained the gating signals of S_{A2} and S_{B1} respectively. The gating pulses of S_{A2} and S_{B1} are also square wave with period T_s and 50% duty ratio. But these signals are phase shifted by $\frac{m_{xy}T_s}{2}$ and $\frac{m_{yz}T_s}{2}$ w.r.t $G_{S'_{A1}}$ and $G_{S'_{B2}}$ respectively. The modulation strategy applies high frequency AC (HFAC)

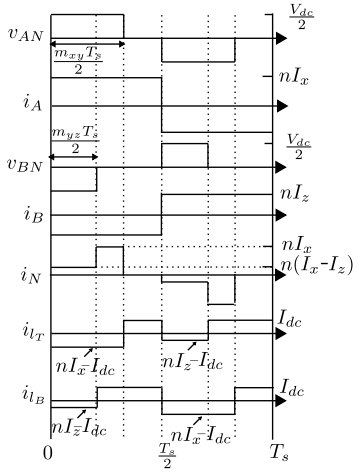


Fig. 5: Neutral and DC link capacitor currents of the DC side three-level NPC inverter

voltages, v_{AN} and v_{BN}, across the transformer primaries with voltage levels $\pm\frac{V_{dc}}{2}$ and 0 and pulse widths $\frac{m_{xy}T_s}{2}$ and $\frac{m_{yz}T_s}{2}$ respectively as seen in Fig. 4. In the secondary of the HFTs, the rectifiers rectify the HFAC inputs. The output of the rectifiers, v_{xy} and v_{yz} are pulsating DC with voltage levels $+\frac{nV_{dc}}{2}$ and 0.

The above switching scheme ensures reduced neutral current, i_N, drawn by the $3L$-NPC legs. The scheme helps to reduce the RMS current of the DC link capacitors. Fig. 5 shows the applied primary voltages, primary currents and the neutral link current, i_N over a switching cycle. The polarities of the applied voltages across the transformer primaries in a half switching cycle are opposite. Hence the transformer winding currents, i_A and i_B, also have opposite polarities. In Fig. 5, the waveforms are shown at a switching instant when $m_{xy} > m_{yz}$. i_A and i_B have magnitudes of nI_x and nI_z respectively. I_x and I_z are the magnitudes of rectifier output current i_x and i_z respectively and are considered as constant over a switching cycle. For UPF operation, in the switching state $[yzx]$ ($\theta \in 0, \frac{\pi}{3}$), $i_x = I_{pk}\cos\theta$ and $i_y = I_{pk}\sin\left(\theta + \dfrac{\pi}{6}\right)$ (see Fig. 3). As seen in Fig. 5, during $0 < t < \frac{m_{yz}T_s}{2}$, $i_N = i_A + i_B = n(I_x - I_y)$. During $\frac{m_{yz}T_s}{2} < t < \frac{m_{xy}T_s}{2}$, transformer terminals BN are shorted through leg B diode D'_B and switch S'_{B2} and hence $i_N = i_A = nI_x$. During $\frac{m_{xy}T_s}{2} < t < \frac{T_s}{2}$, both the transformer primary terminals are shorted through one diode and switch pair. Hence, $i_N = 0$. Similarly i_N can be derived in other half of the switching cycle. The waveform of i_N has symmetry over $\frac{\pi}{6}$. The RMS of neutral current $i_{N,RMS}$ at UPF operation of the converter

is given in (1).

$$i_{N,RMS} = \sqrt{\frac{6}{\pi}\int_0^{\frac{\pi}{6}} [n^2(i_x - i_z)^2 m_{yz} + (ni_x)^2(m_{xy} - m_{yz})]\, d\theta} = 0.709\sqrt{M} n I_{pk} \quad (1)$$

In the switching state $[yzx]$, $m_{xy} = 1.15M\cos(\theta + \frac{\pi}{6})$ and $m_{yz} = 1.15M\sin\theta$ (see Fig. 3).

Similarly, the DC link capacitor RMS currents at UPF operation is given as-

$$i_{l_T,RMS} = i_{l_B,RMS} = nI_{pk}\sqrt{(0.458 - 0.243M)M} \quad (2)$$

Though the proposed topology has diode rectifiers in the secondary and does not employ any DC link capacitor after the rectifier stage, it can support upto 30° leading and lagging power factor stand alone load. The rectifier output currents i_x and i_z are positive instantaneously. Following Table II and Fig. 3 in state $[xzy]$, it can be seen that $i_x(= i_a)$ becomes negative when i_a lags more than 30°. Similarly $i_z(= -i_b)$ becomes negative when i_b leads more than 30°. The negative link currents cannot be supported by the rectifiers and hence the converter operation is power factor restricted.

III. Operation of 3L-NPC legs

Though high frequency switched, the 3L-NPC legs are soft-switched without additional auxiliary circuits. The operation of the 3L-NPC legs are analysed in details over a switching cycle (T_s) for UPF operation of the converter. The operation of both the legs are independent but similar hence only leg A is considered for further discussion. The operation is described when the unfolder is in state $[yzx]$. Similar strategy is followed in other states. In state $[yzx]$, the rectifier output current $i_x = i_c$ (Fig. 3). As the line currents ($i_{a,b,c}$) are properly filtered and slowly varying, i_x can be considered as constant current sink over T_s. Hence after the rectifier stage, the unfolder can be modelled as current sinks. The converter operation is analysed considering the 3L-NPC leg device (C_s) and diode (C_d) capacitances and the transformer leakage inductance (seen from primary) L_{lk}. Simplified circuit associated with leg A operation is shown in Fig. 7. The key switching transition waveforms are shown in Fig. 6.

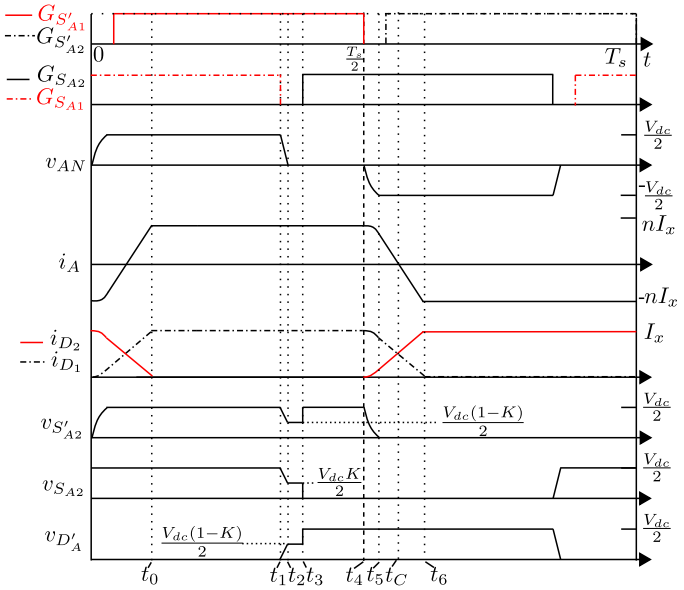


Fig. 6: Important switching waveforms over T_s

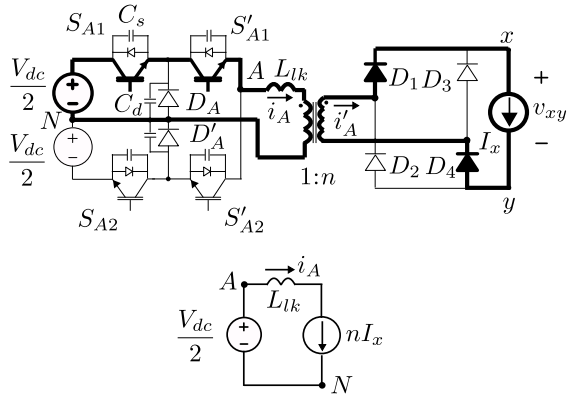


Fig. 7: Mode 1- circuit diagram and equivalent circuit

A. Mode 1 ($t_0 < t < t_1$, Fig. 7)

Top two switches, S_{A1} and S'_{A1}, of the 3L-NPC leg A are conducting which apply $\frac{V_{dc}}{2}$ across the transformer primary terminals AN. In the secondary the diodes D_1 and D_4 are conducting. The circuit is transferring active power from input to the load. The equivalent circuit is shown in Fig. 7. The primary current is $i_A = nI_x$. The diode D_A and bottom two switches S'_{A_2} and S_{A2} are blocking $\frac{V_{dc}}{2}$ (see Fig. 6).

B. Mode 2 ($t_1 < t < t_2$, Fig. 8)

This mode begins at t_1 when S_{A1} is turned OFF. The voltage across S_{A1} rises slowly due to device capacitance C_s. This helps to reduce turn OFF loss of S_{A1}. i_A charges the device and diode capacitances of S_{A1} and D'_A respectively. The capacitances of D_A, S'_{A2} and S_{A2} are being discharged. The equivalent circuit is shown in Fig. 8. The circuit equations are given in (3).

$$\begin{aligned} v_{S_{A1}} + v_{D_A} &= \frac{V_{dc}}{2} \\ v_{S_{A1}} + v_{S'_{A2}} + v_{S_{A2}} &= V_{dc} \\ v_{S_{A2}} + v_{D'_A} &= \frac{V_{dc}}{2} \\ C_s\frac{dv_{S_{A1}}}{dt} &= C_d\frac{dv_{D_A}}{dt} + C_s\frac{dv_{S'_{A2}}}{dt} + nI_x \\ C_s\frac{dv_{S'_{A2}}}{dt} + C_d\frac{dv_{D'_A}}{dt} &= C_s\frac{dv_{S_{A2}}}{dt} \end{aligned} \quad (3)$$

Solving (3), the voltage dynamics across the devices are given in (4).

$$\begin{aligned} v_{S_{A1}}(t) &= \left(\frac{2C_s + C_d}{C_s + C_d}\right)\frac{nI_x(t-t_1)}{3C_s + C_d} \\ v_{S'_{A2}}(t) &= \frac{V_{dc}}{2} - \frac{nI_x(t-t_1)}{3C_s + C_d} \\ v_{S_{A2}}(t) &= \frac{V_{dc}}{2} - \left(\frac{C_s}{C_s + C_d}\right)\frac{nI_x(t-t_1)}{3C_s + C_d} \end{aligned} \tag{4}$$

At t_2, $v_{S_{A1}} = \frac{V_{dc}}{2}$. The voltage across D_A is zero and is forward biased. The interval $(t_2 - t_1)$ is given in (5). At t_2 the blocking voltages across S'_{A2} and S_{A2} are given in (5). Where $K = \dfrac{C_s + C_d}{2C_s + C_d}$. If $C_s \gg C_d$, $K = 0.5$.

$$\begin{aligned} (t_2 - t_1) &= \frac{V_{dc}}{2}\left(\frac{C_s + C_d}{2C_s + C_d}\right)\frac{3C_s + C_d}{nI_x} \\ v_{S'_{A2}}(t_2) &= \frac{(1-K)V_{dc}}{2} \\ v_{S_{A2}}(t_2) &= \frac{KV_{dc}}{2} \end{aligned} \tag{5}$$

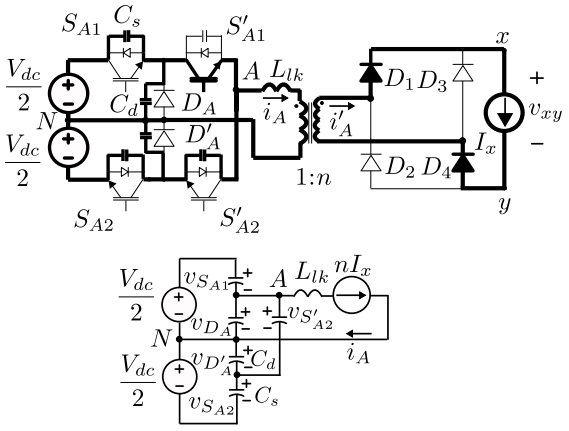


Fig. 8: Mode 2- circuit diagram and equivalent circuit

C. Mode 3 ($t_2 < t < t_4$)

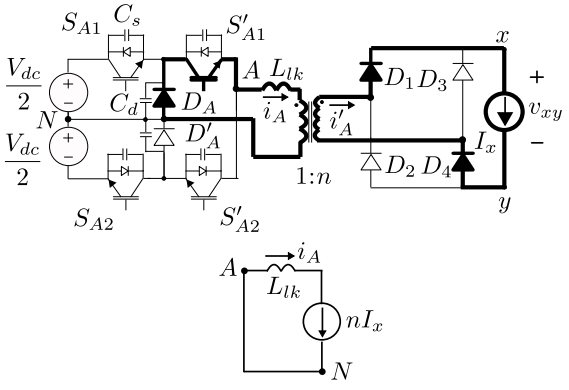


Fig. 9: Mode 3a- circuit diagram and equivalent circuit

1) Mode-3a ($t_2 < t < t_3$, Fig. 9): D_A and S'_{A1} are conducting. The transformer primary terminals A, N are shorted. In this mode, the load current free-wheels through the circuit and no active power is transferred from source to load. The mode is termed as zero state. Equivalent circuit is shown in Fig. 9. S_{A2} blocks $\frac{KV_{dc}}{2}$. The blocking voltage of S'_{A2} and D'_A is $\frac{(1-K)V_{dc}}{2}$. Currents through these devices and the diode are zero.

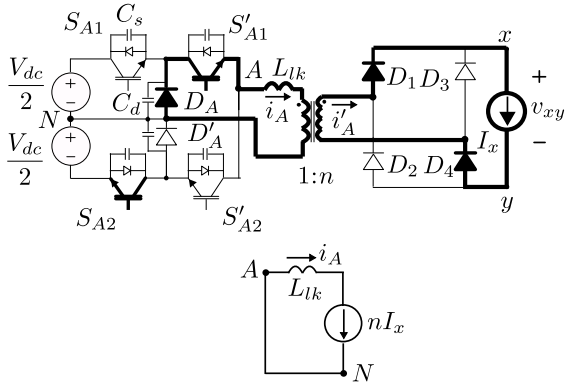


Fig. 10: Mode 3b- circuit diagram and equivalent circuit

2) Mode-3b ($t_3 < t < t_4$, Fig. 10): At t_3, S_{A2} is turned ON. As S_{A2} does not conduct current before and just after the switching transition, the turn ON of S_{A2} is a zero current transition (ZCS). The device parasitic capacitance C_s discharges through the channel of S_{A2}. As the blocking voltage was $\frac{KV_{dc}}{2}$ where $K < 1$ and C_s is only the parasitic capacitance with small value, the loss due to capacitive discharge is negligible. After t_3, the blocking voltage of S'_{A2} and D'_A is $\frac{V_{dc}}{2}$. The circuit continues to be in zero state with conducting D_A, S'_{A1} and the secondary diodes D_1, D_4.

D. Mode 4 ($t_4 < t < t_5$, Fig. 11)

At t_4, S'_{A1} is turned OFF. The voltage across S'_{A1} changes slowly due to device capacitance C_s which reduces the turn OFF loss of S'_{A1}. The pole current i_A starts charging the

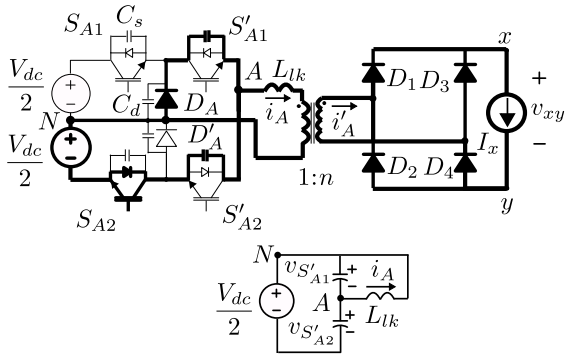


Fig. 11: Mode 4- circuit diagram and equivalent circuit

capacitance across S'_{A1} and discharging the capacitance across S'_{A2}. Appeared voltage polarity across the transformer primary, AN is negative which forward bias the rectifier diodes D_2, D_3.

Hence the transformer secondary is shorted through the rectifier bridge. The equivalent circuit is shown in Fig. 11. The circuit equations are given in (6).

$$\begin{aligned} v_{S'_{A1}} + v_{S'_{A2}} &= \frac{V_{dc}}{2} \\ v_{S'_{A1}} + L_{lk}\frac{di_A}{dt} &= 0 \\ C_s(dv_{S'_{A1}}/dt - dv_{S'_{A2}}/dt) &= i_A \end{aligned} \tag{6}$$

(6) is solved with initial conditions $v_{S'_{A1}}(t_4) = 0$, $v_{S'_{A2}}(t_4) = \frac{V_{dc}}{2}$ and $i_A(t_4) = nI_x$. The voltage across $v_{S'_{A1}}$ and the current i_A are given in (7).

$$\begin{aligned} v_{S'_{A1}}(t) &= n\omega_r L_{lk} I_x \sin\omega_r(t-t_4) \\ i_A(t) &= nI_x \cos\omega_r(t-t_4) \end{aligned} \tag{7}$$

Where $\omega_r = \dfrac{1}{\sqrt{2L_{lk}C_s}}$. At t_5 this mode ends when $v_{S'_{A1}} = V_{dc}/2$ and $v_{S'_{A2}} = 0$. To complete the charge-discharge of C_s across $S'_{A1,A2}$, the condition is given in (8). The duration $(t_5 - t_4)$ is given in (8).

$$\begin{aligned} nI_x &\geq \frac{V_{dc}}{2\omega_r L_{lk}} \\ (t_5 - t_4) &= \frac{1}{\omega_r}\sin^{-1}\left(\frac{V_{dc}}{2\omega_r L_{lk} nI_x}\right) \end{aligned} \tag{8}$$

Else the circuit enters into a resonating oscillation mode and successive turn ON of S'_{A2} results in hard switching.

E. Mode 5 ($t_5 < t < t_C$, Fig. 12)

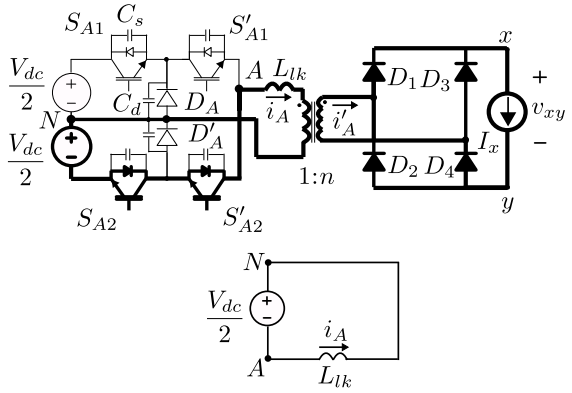


Fig. 12: Mode 5- circuit diagram and equivalent circuit

At t_5, when the voltage across S'_{A2} becomes zero, the anti-parallel diode across S'_{A2} is forward biased and starts conducting. The equivalent circuit is shown in Fig. 12. The applied voltage across the transformer primary, $v_{AN} = -\frac{V_{dc}}{2}$. i_A changes linearly in this mode as given in (9).

$$i_A = i_A(t_5) - \frac{V_{dc}}{2L_{lk}}(t - t_5) \tag{9}$$

i_A falls to zero and changes its direction at t_C. To ensure ZVS ON, S'_{A2} is turned ON when the anti-parallel diode is conducting. The duration $(t_C - t_5)$ is given in (10).

$$t_C - t_5 = \frac{2L_{lk}i_A(t_5)}{V_{dc}} \tag{10}$$

In secondary, linear current commutation between diode pairs $(D_{1,4})$, $(D_{2,3})$ takes place. Current through D_1 and D_2 are shown in Fig. 6.

F. Mode 6 ($t_C < t < t_6$, Fig. 13)

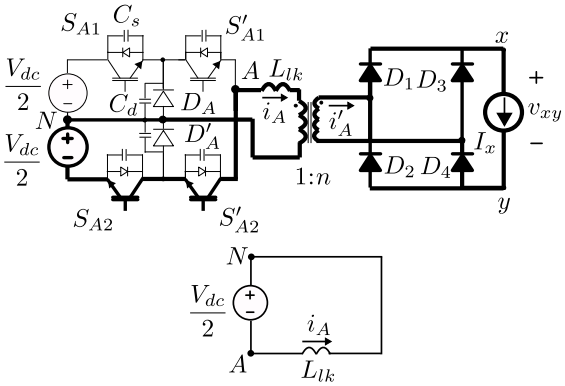


Fig. 13: Mode 6- circuit diagram and equivalent circuit

As S'_{A2} is turned ON in between t_5 and t_C, i_A can grow in the opposite direction after t_C. Current commutation continues between the diode pairs $(D_{1,4})$, $(D_{2,3})$. i_A changes linearly as expressed in (9). The mode ends at t_6 when $i_A = -nI_x$.

G. Mode 7 ($t > t_6$, Fig. 14)

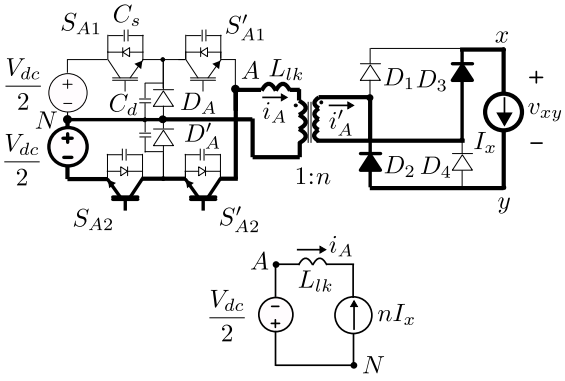


Fig. 14: Mode 7- circuit diagram and equivalent circuit

After t_6, D_1 and D_4 are reverse biased and stop conducting. D_2 and D_3 conduct I_x. In the primary S'_{A2} and S_{A2} are conducting i_A. The equivalent circuit is shown in Fig. 14. The converter is in next active state where the active power is transferred from DC source to load like in Mode 1.

The above discussion shows the operation of the $3L$-NPC leg over one half of a switching cycle. In the other half similar switching sequences are followed with other symmetrical switches and ZCS turn ON of S_{A1} and ZVS turn ON of S'_{A1} are ensured similar to S_{A2} and S'_{A2} respectively as discussed in modes 3 and 5.

H. Estimation of upper limit of dead time to ensure ZVS

As discussed above, the pole current i_A changes its direction during the switching transitions of $S'_{A1} - S'_{A2}$. To ensure zero

voltage turn ON of $S'_{A1} - S'_{A2}$, the switches must be gated ON when the anti-parallel diode is in conduction before the direction of i_A is changed. Hence the dead time between $S'_{A1} - S'_{A2}$ cannot be arbitrary and has upper and lower bounds. To allow the complete charge-discharge of the device capacitances, the dead time should be greater than the interval $(t_5 - t_4)$ as given in (8). The upper bound of dead time is $(t_C - t_4)$, where t_C is the zero cross over point of i_A. $(t_C - t_5)$ is given in (10). As seen in (8) and (10), the intervals are dependent on I_x which is the magnitude of i_x over a switching cycle. In Fig. 3, i_x over a line cycle is shown for UPF operation. The bounds on the dead time are most strict at the minimum value of i_x which is $0.5I_{pk}$. Hence replacing I_x with $0.5I_{pk}$, following limits on dead time DT are obtained.

$$DT \geq (t_5 - t_4)_{max} = \frac{1}{\omega_r} \sin^{-1}\left(\frac{V_{dc}}{n\omega_r L_{lk} I_{pk}}\right)$$

$$DT \leq (t_5 - t_4)_{max} + (t_C - t_5)_{min}$$

$$= \frac{1}{\omega_r}\left[\sin^{-1}\left(\frac{V_{dc}}{n\omega_r L_{lk} I_{pk}}\right) + \sqrt{\left(\frac{n\omega_r L_{lk} I_{pk}}{V_{dc}}\right)^2 - 1}\right] \quad (11)$$

(11) ensures ZVS turn ON of $S'_{A1} - S'_{A2}$ over the entire line cycle. For a given input V_{dc} and the circuit parasitics (C_s, L_{lk}), the bounds are dependent on I_{pk}, i.e output power P. For a given operation range of the converter if (11) is ensured for the minimum value of I_{pk}, ZVS of $S'_{A1} - S'_{A2}$ can be ensured for the complete range of operation.

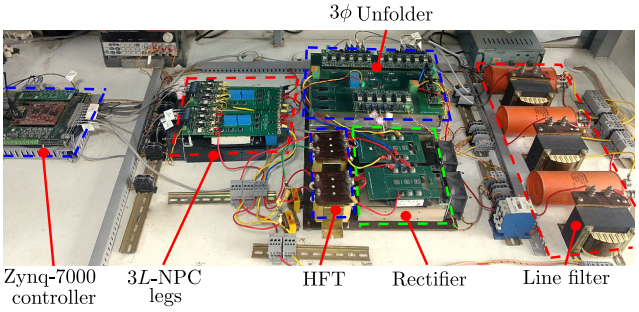


Fig. 15: Hardware prototype

IV. Experimental verification

A. Operating condition

To verify the operation of the proposed inverter a 2kW laboratory scale hardware prototype is built and tested. Fig. 15 shows the test setup. The operating condition of the converter is presented in Table III. The $3L$-NPC legs are implemented with 1200V, 75 A SEMIKRON IGBT modules, SKM75GB123D. The neutral clamp diodes are implemented with 1200V, 75A IXYS diode modules, MEE 75-12 DA. These diode modules are also used to build the secondary rectifiers. INFINEON IKW40N120H3 discrete IGBTs (1200V, 40A) are used in the secondary unfolder. All the IGBTs are driven with optically isolated gate drivers, ACPL 339J with gate voltage levels $\pm$15V. A 600 ns dead time is provided between to complementary switched devices in the $3L$-NPC legs. A 800 ns overlap time is given between to successive gating signals

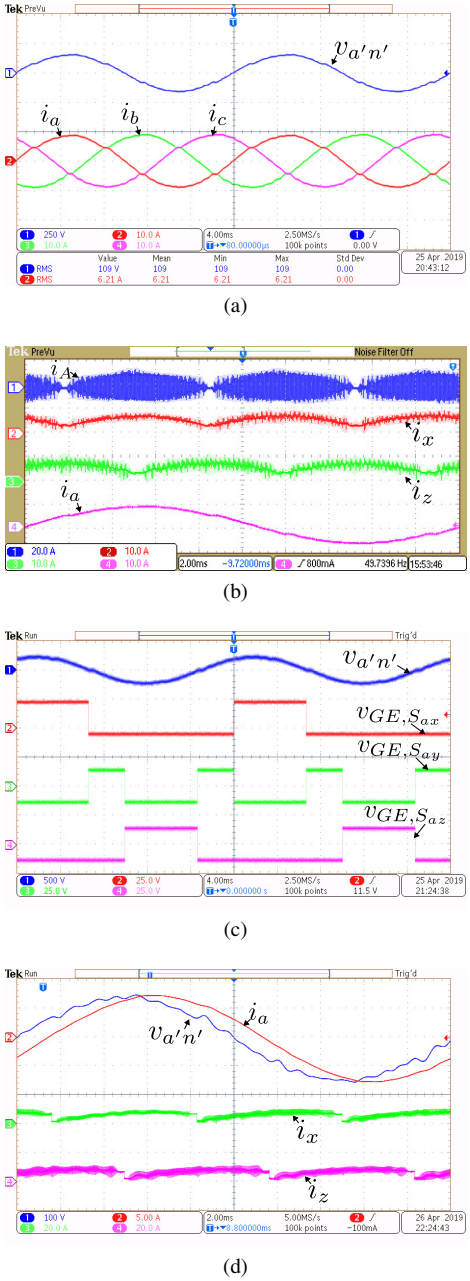
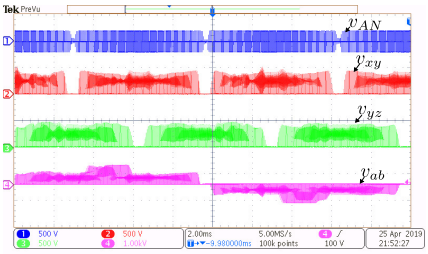


Fig. 16: (a) UPF operation- [CH1] $v_{a'n'}$ (250V/div.), [CH2]-[CH4]: line currents (10A/div.). (b) Current waveforms- [CH1]: i_A (20A/div.), [CH2]-[CH4]: i_x, i_z, i_a (10A/div.). (c) Unfolder switching- [CH1] $v_{a'n'}$ (500V/div.), [CH2]-[CH4]: Gate-emitter voltages of S_{ax}, S_{ay}, S_{az} (25V/div.). (d) Non UPF operation (PF-0.9 lagging)- [CH1]: $v_{a'n'}$ (100V/div.), [CH2]: i_a (5A/div.), [CH3]-[CH4]: i_x and i_z (20A/div.).

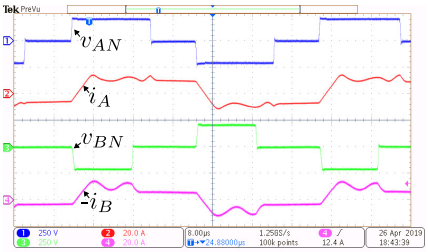
of an unfolder leg. The HFTs are implemented with EPCOS ferrite E cores (E80/38/20). The primary and secondary turns of a HFT are 51 and 68 respectively. The transformers have leakage inductances (seen from primary) in the order of 5-6 μH. To ensure ZVS turn ON of the $3L$-NPC leg switches, additional 36 μH inductance is connected in series with each primary winding. 2.5 mH inductors (L_f) are used as line filters to filter out the high frequency component from the line currents.

B. Experimental verification of modulation strategy

The balanced three phase output of the converter is shown in Fig. 16a. The converter is connected to a balanced three



(a)



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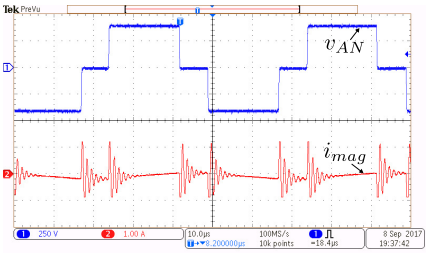
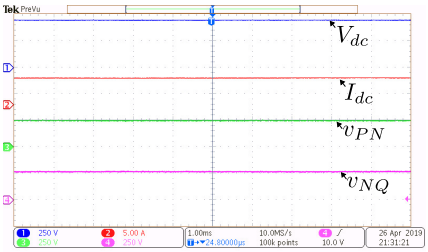


(c)

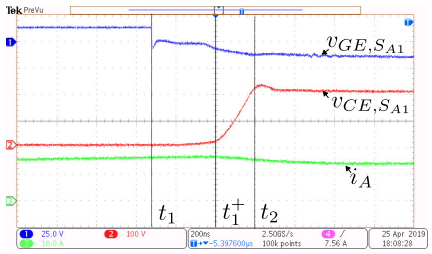


(d)

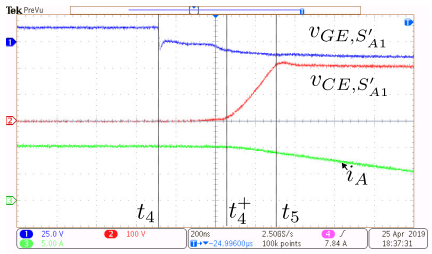
Fig. 17: (a) Pole voltages- [CH1]-[CH3]: v_{AN}, v_{xy}, v_{yz} (500V/div), [CH4] v_{ab} (1kV/div.). (b) Transformer waveforms over switching cycle- [CH1] v_{AN} (250V/div.), [CH2]: i_A (20A/div.), [CH3]: v_{BN} (250V/div.), [CH4]: $-i_B$ (20A/div.). (c) HFT magnetising current-[CH1]: v_{AN} (250V/div.), [CH2]: i_{mag} (1A/div.). (d) DC inputs- [CH1]: V_{dc} (250V/div.), [CH2]: I_{dc} (5A/div.), [CH3]: v_{PN} (250V/div.), [CH4]: v_{NQ} (250V/div.).

TABLE III: Operating condition

Output power (P)	2.05kW
DC input (V_{dc})	460V
Peak phase voltage (V_{pk})	156V
HFT turns ratio (n)	4/3
Switching frequency ($f_s = \frac{1}{T_s}$)	20kHz
Line frequency ($f_o = \frac{\omega_o}{2\pi}$)	50Hz



(a)



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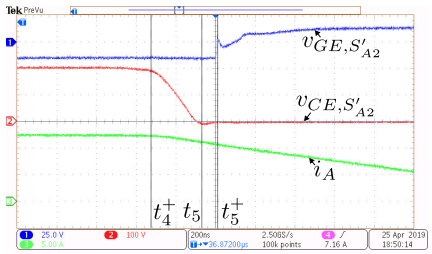
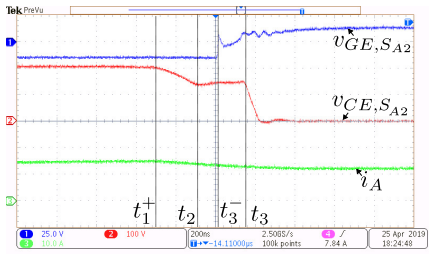


(c)



(d)

Fig. 18: Switching transition waveforms- (a) Turn OFF of S_{A1}. (b) Turn OFF of S'_{A1}. (c) Turn ON of S'_{A2}. (d) Turn ON of S_{A2}.

phase voltage source supplying 2.05 kW power (P) at UPF. Peak of the output phase voltage V_{pk} is 156 V. Balanced three-phase line currents with peak $I_{pk} = \dfrac{2P}{3V_{pk}} = 8.8$ A are shown in Fig. 16a.

Fig. 16b shows the transformer primary current i_A, the rectifier output currents i_x, i_z and the line current i_a. The transformer primary current, i_A, is high frequency square wave with sinusoidally varying magnitude. i_A has a peak magnitude of $nI_{pk} = 11.7$ A. The experimentally obtained rectifier output currents i_x and i_z have similar shapes as shown in Fig. 3 and have peak magnitude of $I_{pk} = 8.8$ A.

The unfolder switching strategy is shown in Fig. 16c. Based on the switching states given in Table I, gating signals of the unfolder are obtained. It is seen that the two quadrant switches ($S_{ax,az}$) are line frequency (50 Hz) switched whereas the four-

quadrant switch (S_{ay}) are switched twice of the line frequency (at 100 Hz). Hence the unfolder obtained negligible switching loss.

The proposed topology can support stand-alone load upto 30° leading and lagging power factor. Fig. 16d shows the converter operation supporting a 0.9 PF inductive load. The line current i_a lags $v_{a'n'}$ by 25.2°. The result also shows rectifier output currents i_x and i_z. Differences in shape of i_x and i_z at UPF (Fig. 16b) and at lagging PF operation are observable. For both the cases, i_x and i_z are always positive over the line cycle. Similarly other non-unity power factor operation of the converter can be verified.

The pulse width modulated HF AC (v_{AN}) applied across transformer primary is shown in Fig. 17a. v_{AN} has voltage levels of $\pm$230 V and 0 V. Fig. 17a also shows the rectifier output voltages v_{xy} and v_{yz} with voltage levels $0.5nV_{dc} =$ 307V and 0. As discussed in section II, the intermediate DC link xy and yz are pulsating as no filter capacitor is employed. The unfolder pole voltage v_{ab} is also shown in Fig. 17a.

The transformer primary voltages and primary currents over a switching cycle are shown in Fig. 17b. Experimentally measured applied voltages v_{AN} and v_{BN} are matched with the waveforms shown in Fig. 5. The polarity of applied voltages are opposite. This verifies the modulation strategy of the $3L$-NPC legs to ensure reduced neutral current as described in section II.

Fig. 17c shows the experimentally measured magnetising current waveform of the high frequency transformer and the transformer primary voltage over a switching cycle. As the transformer primary voltages have zero average over the switching cycle hence flux is balanced over the switching cycle. The high frequency oscillation observed in the magnetising current is due to parasitic ringing of the transformer during the switching transitions.

The Fig. 17d shows the input voltages and input current of the converter. The applied input voltage is 460 V and input current is 5 A. The input DC link voltages are $v_{PN} = v_{NQ} =$ 230 V. As seen in the figure v_{PN} and v_{NQ} have negligible ripple hence no neutral voltage unbalance is observed.

C. Experimental verification of soft-switching transitions of the 3L-NPC leg A

In this subsection, the experimental results are presented to verify following switching transitions of the $3L$-NPC leg A- turn OFF transitions of S_{A1}, S'_{A1} and the turn ON of S'_{A2}, S_{A2}.

Fig. 18a shows the turn OFF transition of S_{A1}. Before t_1, S_{A1} was ON and conducting i_A. At t_1, the gating pulse of S_{A1} is removed. After some time at t_1^+, when the gate emitter voltage of S_{A1}, $v_{GE,S_{A1}}$ becomes negative, the voltage across the device, $v_{CE,S_{A1}}$ starts to rise slowly and at t_2, S_{A1} blocks $0.5V_{dc}$. The slow rise of the voltage across the device is due to device capacitance (C_s) which helps to reduce the turn OFF loss of S_{A1}. The result verifies the switching process described in Mode 2 of section III.

Fig. 18b presents the turn OFF transition of S'_{A1}. At t_4 the gating pulse is removed. At t_4^+, when the gate emitter voltage of S'_{A1}, $v_{GE,S'_{A1}}$ is negative, the voltage across the device, $v_{CE,S'_{A1}}$ starts to rise slowly and at t_5, $v_{GE,S'_{A1}}$ rises to $0.5V_{dc}$. The slow change in $v_{CE,S'_{A1}}$ is due to device capacitance which helps to reduce turn OFF loss of S'_{A1}. After t_5, i_A falls linearly. The result verifies the switching process described in Mode 4 of section III.

The experimental result shown in Fig. 18c verifies the ZVS turn ON of S'_{A2} described in Mode 4-5 of section III. S'_{A2} was OFF and was blocking $0.5V_{dc}$. At t_4^+, i_A starts to discharge the capacitance across S'_{A2}. The voltage across the device, $v_{CE,S'_{A2}}$ falls to zero at t_5 and the anti-parallel diode of S'_{A2} starts conducting i_A. At t_5^+, before i_A changes its direction, the gating pulse of S'_{A2} is applied to ensure ZVS turn ON.

The turn ON process of S_{A2} is shown in Fig. 18d. At t_1^+, the voltage across S_{A2}, $v_{CE,S_{A2}}$ starts to fall from $0.5V_{dc}$. At t_2, $v_{CE,S_{A2}} = 0.5KV_{dc} = 140V$ and S_{A2} continues to block $0.5KV_{dc}$. At t_3^-, the gating pulse of S_{A2} is applied. When the gate emitter voltage, $v_{GE,S_{A2}}$ rises above the device threshold voltage at t_3, the device channel starts conducting. The device capacitance discharges through the channel. As the direction of i_A remains same, S_{A2} does not conduct even after turn ON. Hence the turn ON of S_{A2} is zero current transition (ZCS). The loss due to parasitic discharge into the channel is small as the blocking voltage ($0.5KV_{dc}$) and the capacitance both are small. The result verifies the process described in Mode 2-3 of section III.

D. Power loss and Efficiency

The converter power loss is analytically estimated assuming ripple free line currents. In the analysis only conduction loss is considered as the proposed topology is soft-switched. The experimentally measured power loss verifies the analysis.

1) Analytical loss expressions: The conduction loss in switch S_{A1} is given as-

$$P_{C_{S_{A1}}} = 0.25MV_{CE}(nI_{pk}) + 0.23MR_{CE}(nI_{pk})^2 \quad (12)$$

Where V_{CE} and R_{CE} are constant voltage drop and on state resistance respectively of the IGBT module. I_{pk} is the peak of the line current. The conduction loss in switch S'_{A1} is given as-

$$P_{C_{S'_{A1}}} = 0.41V_{CE}(nI_{pk}) + 0.35\,(nI_{pk})^2\,R_{CE} \quad (13)$$

The conduction loss in diode D_A is given as-

$$\begin{aligned} P_{C_{D_A}} &= (0.41 - 0.25M)V_{CE}(nI_{pk}) \\ &\quad + (0.35 - 0.23M)\,(nI_{pk})^2\,R_{CE} \end{aligned} \quad (14)$$

Where V_D and R_D are constant voltage drop and on state resistance respectively of the diode module. As the DSC is soft-switched, switching loss is negligible.

The conduction loss in a ASC diode of $D_1 - D_8$ is given as

$$P_{C_{D_1}} = 0.41V_DI_{pk} + 0.36R_DI_{pk}^2 \quad (15)$$

The conduction loss in a ASC two quadrant switch of $S_{a,b,c(x,z)}$ is given as

$$P_{C_{S_{ax}}} = 0.276V_{CE}I_{pk} + 0.235R_{CE}I_{pk}^2 \quad (16)$$

The conduction loss in a ASC four quadrant switch of $S_{a,b,c(y)}$ is given as

$$P_{C_{S_{ay}}} = 0.04 V_{CE} I_{pk} + 0.014 R_{CE} I_{pk}^2 \quad (17)$$

The conduction loss in an anti-parallel diode of the four quadrant switches $S_{a,b,c(y)}$ is given as

$$P_{C_{D_{S_{ay}}}} = 0.04 V_D I_{pk} + 0.014 R_D I_{pk}^2 \quad (18)$$

As ASC active switches are low frequency switched, the switching loss is negligible.

The copper loss of a HFT is given as $I_{A,RMS}^2(R_p + \frac{R_s}{n^2})$. Where $I_{A,RMS} = 0.84 n I_{pk}$ is the RMS current of the primary winding. R_p and R_s are resistance of the primary and secondary windings. At the switching frequency the HFT core loss is negligible.

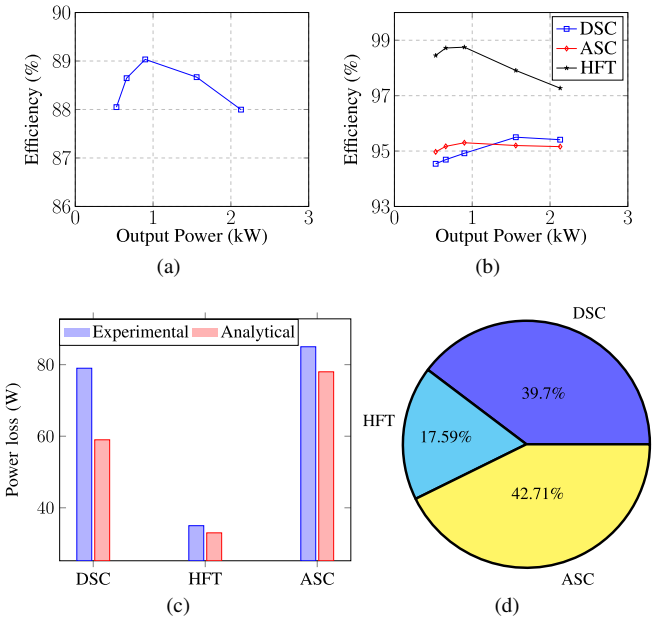


Fig. 19: (a) Variation of efficiency with load. (b) Stage wise efficiency of the converter. (c) Loss distribution estimated analytically and obtained experimentally at 1.54kW. (d) Share of loss at 1.54kW output power

2) Experimental measurement of converter power loss: The converter was operated with fixed input DC 420V, delivering a range of output power, 0.53kW to 2.13kW. The power loss of various stages of the converter was measured. The variation of efficiency with load power is shown in Fig. 19a. The hardware prototype has maximum efficiency 89% at 0.9kW output power. The efficiency of the three stages (DSC, ASC and HFT) of the converter are shown in Fig. 19b. The DSC and ASC stages have above 95% efficiency individually almost throughout the load range 19b. The efficiency of the DSC improves with higher power output as expected. Because at high power the DSC is soft-switched through out the line cycle. The low frequency switched ASC has almost constant efficiency profile with the variation of load. The HFT loss increases with increased load. The experimentally obtained and analytical estimated losses at the different stages of the converter at 1.56kW output power are shown in Fig. 19c. The analytically estimated power losses are closely matched with the experimentally obtained values. A pie chart showing the share of loss in different stages at 1.56kW output power is shown in Fig. 19d. The experimental prototype of the proposed topology is also not optimally designed for 2-3kW power level and hence has the relatively low peak efficiency of 89%. With an optimally designed converter at 2kW output powers, an analytically estimated overall efficiency of 95.5% can be achieved. The method of analytical estimation is verified with the existing hardware (Fig. 19c).

V. Comparison with other topologies

The proposed topology is compared with two single-stage unidirectional three phase high-frequency-link inverter topologies given in [12], [13]. Like the proposed topology, these selected topologies can support VAr upto ± 0.866 power factor. To perform the comparison fairly, all the topologies under consideration are designed for same operating conditions with given input and output voltages and output power. The switching frequency and modulation index (0.85) are considered same for all the topologies. All the topologies are modulated at the 85% of its maximum possible modulation index. For generalization, the parameters of the comparison are evaluated in terms of output power (P), input DC voltage (V_{dc}) or peak output voltage (V_{pk}) and switching frequency (f_s).

Table IV summarises the topology comparison. It presents the number of active and passive semiconductors employed, their blocking voltages (V_b), RMS (I_{RMS}) currents. S.F is the scaling factor. Total number of semiconductors employed in the proposed topology is same as [13]. Though the number of active devices used in the proposed topology is higher compared to [12], but majority of these switches are line frequency switched. The blocking voltage of the DSC devices of the proposed topology are half of [12], [13] and have relatively higher RMS currents. The ASC devices have similar RMS currents. The DSC of the proposed topology is soft-switched whereas the ASC is low frequency switched. In [12], [13], DSCs and ASCs are hard-switched.

The proposed solution has 2 high-frequency transformers (HFT), similar to the topology in [13] with comparable area product. [12] has 3 high-frequency transformers.

Table V summarises the power loss comparison. To perform a thorough comparison of the converter power losses, the conduction losses of the DSC switches are further expressed in terms of $\frac{V_{CE}P}{V_{dc}}$ and $\frac{R_{CE}P^2}{V_{dc}^2}$. For diodes R_{CE}, V_{CE} are replaced with R_D, V_D respectively. In case of ASC switches and diodes V_{dc} of the scaling factors are replaced with V_{pk}. The switching losses of the active switches are also expressed in terms of $\frac{f_s P E_R}{P_R}$ where $E_R = E_{ON_R} + E_{OFF_R}$ and $P_R = V_{CC} I_C$. E_{ON_R} and E_{OFF_R} are the turn ON and OFF energy losses of the devices given at rated conditions, V_{CC} and I_C.

The blocking voltage of DSC devices of the proposed topology, is half and the RMS current is more than twice of [12], [13]. V_{CE} and R_{CE} are the function of device blocking voltage and RMS currents. V_{CE} reduces with blocking voltage

TABLE IV: Topology comparison-devices and HFTs

		S.F	[12]	[13]	Proposed Topology
DSC	Switch count	—	6	8	8
	Diode count	—	—	—	4
	$V_{b,sw}$	V_{dc}	1	1	0.5
	$I_{RMS,sw}$	$\frac{P}{V_{dc}}$	0.58	0.49/0.43	1.0/ 1.4
	Switching	—	Hard-switched	Hard-switched	Soft-switched
ASC	switch count	—	6	12	12
	Diode count	—	6	14	8
	$V_{b,sw}$	V_{pk}	2.04	1.2	3.5/1.76
	$I_{RMS,sw}$	$\frac{P}{V_{pk}}$	0.33 / 0.302	0.33/ 0.414	0.323/ 0.396
	Switching	—	High-freq. hard-switched	High-freq. hard-switched	Line freq. switched
HFT	HFT count	—	3	2	2
	$I_{RMS,pri}$	$\frac{P}{V_{dc}}$	0.87	0.685	1.976
	$I_{RMS,sec}$	$\frac{P}{V_{pk}}$	0.43	0.58	0.56
	Area product	$\frac{P}{f_s J B_m K_w}$	0.2	0.3	0.42

of the devices and R_{CE} comes down with increased RMS current. Hence the DSC devices of the proposed topology have lower V_{CE} and R_{CE} compared to [12], [13].

Though the conduction loss factors of the DSC devices and diodes are higher, as these devices and diodes have lower V_{CE} and R_{CE} compared to [13], the DSC has comparable conduction loss. The conduction loss of the ASC devices are half of [13] and comparable with [12]. The ASC diodes have comparable conduction losses with [13]. ASC diode of [12] has lower conduction loss compared to the proposed solution.

The DSC of the proposed topology is soft-switched throughout the line cycle. The ASC is line frequency switched incurring negligible switching loss. As the topologies in [12], [13] are high frequency hard-switched, it incurs significant switching loss.

VI. Conclusion

A novel three-level three-phase high frequency link single stage DC-AC converter is presented in this paper for the applications like grid integration of photovoltaics. The proposed topology employs three-level NPC legs on the DC side of the converter. Hence the low voltage rating devices with lower on-state drop and lower E_{on} and E_{off} can be used to implement the DC side bridge compared to a two level based solution. Additionally, the inner switches of the three-level NPC legs are zero voltage switched (ZVS). Whereas the turn ON of the outer switches are zero current transitions (ZCS). Proposed modulation strategy of the three-level NPC legs ensures reduced neutral current. The pulse width modulation is implemented on the DC side bridge. The inter-stage DC link after the secondary rectifiers is pulsating as no filter capacitor is employed. The unfolder active switches are switched either at line frequency or twice of the line frequency hence incurring negligible switching loss. The converter can support stand-alone load upto 30° leading or lagging power factor. The detailed modulation strategy of the converter and switching process of the three-level NPC legs are discussed in the paper. Conditions ensuring ZVS operation over a complete line cycle are derived. A 2kW hardware prototype is built and tested. Experimental results are presented to verify the converter operation at UPF and 0.9 lagging PF operation. The proposed topology is compared with two other unidirectional single stage solutions. Compared to the other topologies, the proposed topology achieves complete unfolding of the AC side converter and soft-switching of the DC side converter. The proposed topology with high frequency galvanic isolation provides a compact, high power density, low cost converter solution.

TABLE V: Topology comparison- power loss

Topology			DSC			ASC	
		S.F.	Switch	Diode	S.F.	Switch	Diode
Proposed	P_C	$\frac{V_{CE}P}{V_{dc}}$	5.86	1.86	$\frac{V_{CE}P}{V_{pk}}$	1.26	2.347
		$\frac{R_{CE}P^2}{V_{dc}^2}$	12.1	3.42	$\frac{R_{CE}P^2}{V_{pk}^2}$	0.664	1.317
	P_S	$\frac{PE_R f_s}{P_R}$	0		$\frac{PE_R f_s}{P_R}$	0	
[12]	P_C	$\frac{V_{CE}P}{V_{dc}}$	2.25	0.25	$\frac{V_{CE}P}{V_{pk}}$	1.21	1.26
		$\frac{R_{CE}P^2}{V_{dc}^2}$	1.97	0.3	$\frac{R_{CE}P^2}{V_{pk}^2}$	0.65	0.853
	P_S	$\frac{PE_R f_s}{P_R}$	7.34		$\frac{PE_R f_s}{P_R}$	0.696	
[13]	P_C	$\frac{V_{CE}P}{V_{dc}}$	2.35	0.354	$\frac{V_{CE}P}{V_{pk}}$	2.45	2.434
		$\frac{R_{CE}P^2}{V_{dc}^2}$	1.654	0.17	$\frac{R_{CE}P^2}{V_{pk}^2}$	1.32	1.4
	P_S	$\frac{PE_R f_s}{P_R}$	5.4		$\frac{PE_R f_s}{P_R}$	1.26	

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