

A Single-Stage Soft-Switched Isolated Three-Phase DC-AC Converter with Three-Phase Unfolder

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Abstract—This paper proposes a unidirectional, single-stage, three-phase, high-frequency-link (HFL) DC-AC converter. The converter uses three high frequency transformers (HFT) to provide galvanic isolation. In the primary, the converter has three half-bridge legs. In secondary three diode-bridge rectifiers are used. Each rectifier is followed by a half-bridge (unfolder) leg. The modulation strategy proposed in this paper ensures zero voltage switching (ZVS) of all six primary side switches over the entire line cycle without additional snubber circuit. The secondary half-bridge legs are switched at line frequency, incurring negligible switching loss. The proposed converter does not require any inter-stage bulky DC-link filter capacitor. Thus, the overall filtering requirement is reduced, and the converter reliability is improved. The high frequency galvanic isolation improves the converter power density. In the paper, the modulation strategy and converter operation are described in detail. The operation is validated in a 3.7 kW hardware prototype. Key experimental results are presented in the paper.

Index Terms—DC-AC conversion, pulse-width modulation, high frequency link, single-stage, line frequency unfolding, zero-voltage-switching.

I. INTRODUCTION

HIGH frequency link, high power density DC-AC converters are gaining popularity for applications such as uninterrupted power supplies (UPS) [1], power supplies in electric and hybrid vehicle [2], grid integration of renewables [3] etc. In such converter topology, to provide galvanic isolation between DC and AC side, high frequency transformers (HFT) are employed. In literature, these converters are broadly classified into two groups- multi-stage and single-stage solution. A multi-stage topology has an isolated DC-DC converter, connected to a voltage source inverter (VSI) through inter-stage DC-link filter capacitor [4], [5]. Single-stage topologies avoid using inter-stage filter capacitor thus reducing the total filtering requirements as well as improving reliability. In a single-stage topology, high frequency AC (HFAC) is generated by the DC side bridge from the input DC and is fed to high frequency transformer. In the secondary, a cyclo-converter is used to generate controllable magnitude line frequency AC from the transformer output [6]–[8]. These single-stage converters are commonly known as cyclo-converter type HFL (CHFL) topology. Another well known single-stage topology is rectifier type HFL (RHFL), where the cyclo-converter operation is

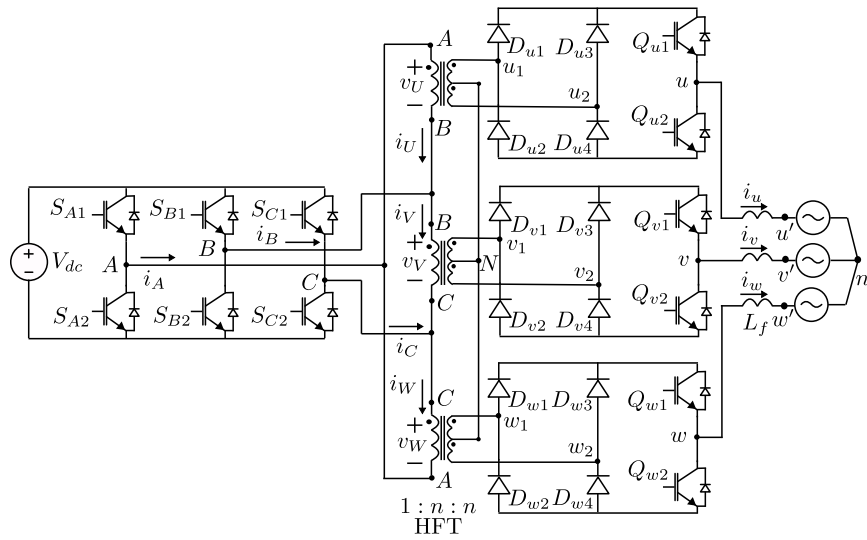
realized by an active rectifier stage connected to a VSI without any DC-link capacitor [9]–[11]. Here the inter-stage DC-link is pulsating and a synchronised modulation strategy is employed between the DC side bridge and the AC side inverter to generate line output.

In applications such as grid integration of photovoltaic, fuel cell and PMSG based wind turbine, the active power flows from DC source to AC grid. Unidirectional RHFL topologies [2], [12]–[15] are popular in such application. Here, the active rectifier is replaced by a diode bridge which reduces the active device count and associated control complexity. In [2], [12], [13], [15], a hybrid modulation (HM) strategy is discussed which results in reduction of high-frequency switching of the AC side inverter. Here, the switches of the AC side inverter is high frequency switched for one-third of a line cycle. Hence the efficiency of the converter is improved with reduced switching loss. A unidirectional three-phase HFL inverter is proposed in [14] where the AC side half-bridge legs are line frequency switched thus incurring negligible switching loss. The DC side has six half-bridge legs which are phase-shift modulated. These legs are zero-voltage switched (ZVS) only for some part of the line cycle. [16] presents an improvement of the topology presented in [14] with four half-bridge legs in the DC side converter. Here ZVS turn ON of one DC side converter leg is ensured over complete line cycle but the remaining three legs are partially soft-switched. AC side half-bridge legs are line frequency switched.

A widely used isolated DC-DC topology is Phase-shift modulated full bridge (PSFB) converter where the half-bridge legs are zero voltage switched (ZVS) using device capacitance and transformer leakage inductance [17]. But the ZVS is load dependent. The stored energy in the transformer leakage inductance is insufficient to completely charge or discharge the device capacitances at light or no load operation. Then the converter is hard-switched. Additional passive [18]–[20] and active [21]–[23] snubber circuits are proposed in literature to achieve ZVS independent of load. In literature, these ideas are also employed in isolated DC-AC converters with phase shift modulated DC side bridge. In such topology, without additional snubber, the DC side bridge is hard-switched near the zero crossing of line current even when the converter is operated at rated load. [24]–[26] use auxiliary inductor based passive snubber to increase ZVS range over a line cycle.

In this paper, a new isolated, single-stage, three-phase DC-AC converter topology (see Fig. 1) is introduced along with a novel modulation strategy. Some important features of the proposed converter are as follows. a) The converter has three half-bridge legs in the DC input side. These legs are phase-shift modulated like a conventional PSFB converter.

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 Fig. 1. Proposed 3 ϕ HFL DC-AC converter

The suggested modulation scheme results in zero-voltage-transitions of all six active switches of the half-bridge legs over complete line cycle without an additional snubber. b) The converter uses three high frequency (HF) transformer to provide galvanic isolation. The HF isolation provides a compact, high power density converter solution. c) Three diode-bridge rectifiers are employed on the AC side of the converter. Each rectifier is further connected to a half-bridge leg. These three half-bridge legs in the AC side, are switched at line frequency based on the direction of line currents. Thus, incurring negligible switching loss. Diodes in the diode bridge are soft-commutated. d) The converter does not require bulky, inter-stage, DC-link filter capacitor which improves the converter reliability. Though the AC side converter of the proposed topology has similarity with [16], the proposed topology employs less number of active switches with lower RMS current and associated gate drivers and control circuits compared to [16]. Unlike [16], all DC side converter switches have identical RMS current, blocking voltage and power loss, hence requires simpler mechanical heat-sink arrangement. The novel modulation strategy suggested for the proposed topology ensures ZVS turn ON of all active switches in the DC side converter over the entire line cycle which is not the case with [16]. The DC side converter of the proposed topology incurs lower conduction loss compared to [16].

The paper is organized as follows. Section II describes the modulation strategy of the converter. The operation of the converter is presented in section III with detailed circuit analysis. Key experimental results are given in section IV to verify the converter operation. Section V presents a comparison of the proposed topology with a multi-stage and a single-stage solutions.

II. PROPOSED CONVERTER AND MODULATION STRATEGY

A. Proposed topology

Fig. 1 shows the proposed isolated three-phase DC-AC converter. Input DC side converter (DSC) has three half-bridge legs (A, B, C) with six two-quadrant switches ($S_{A1} - S_{C2}$).

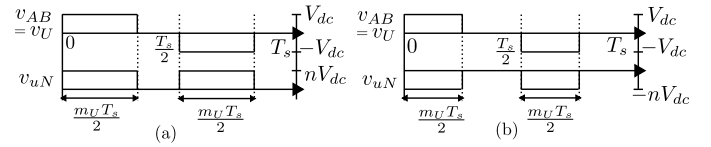
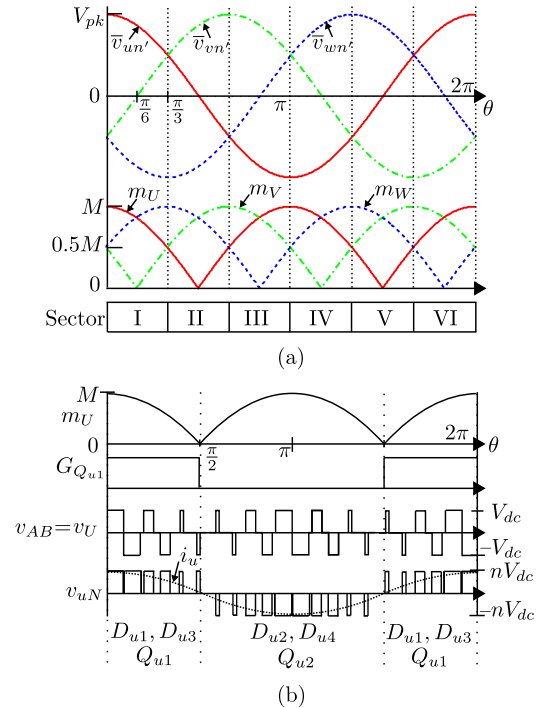

 Fig. 2. Transformer primary voltage v_{AB} and pole voltage v_{uN} over T_s - (a) when $\bar{v}_{un'} > 0$ (b) when $\bar{v}_{un'} < 0$


Fig. 3. (a) Phase voltages and the modulation signals, (b) Switching strategy of secondary side leg

Three high frequency transformers (HFT), each with one primary and two secondary windings are used. The turns ratio of each HFT is given as $1 : n : n$. The primary windings of the HFTs are connected in delta (see Fig. 1). The three terminals of the delta are connected to the poles of half-bridge legs A, B and C . In the secondary, in each HFT, the

finishing end of the first winding is connected to the starting end of the second identical winding and all these points of the three HFTs are shorted together to form the neutral point N . The secondary output of each HFT is fed to a diode bridge rectifier, $D_{l1} - D_{l4}$ followed by an half-bridge leg, $Q_{l1} - Q_{l2}$ where $l \in \{u, v, w\}$. These three half-bridge legs, $Q_{l1} - Q_{l2}$, are switched at line frequency and thus forming the three-phase unfolder. The converter is connected to a balanced three-phase voltage source $v(u', v', w')n'$ through line filters, L_f . The directions of currents, as shown in Fig. 1, are considered to be positive in the following discussion.

B. Modulation of AC side converter

Fig. 2 shows the voltage applied by the DSC across the transformer primary terminals AB , $v_{AB} = v_U$, over a switching cycle T_s . v_{AB} has voltage levels $\pm V_{dc}$ and zero with pulse width $\frac{m_U T_s}{2}$. Such waveform of v_{AB} ensures HFT flux balance over T_s . $m_U(t)$ is the time varying modulation signal to generate desired average phase voltage $\bar{v}_{un'} = V_{pk} \cos(\omega_o t + \theta)$ (see Fig. 3a). As the converter is connected to a balanced three phase load, $\bar{v}_{un'} = \bar{v}_{uN}$.

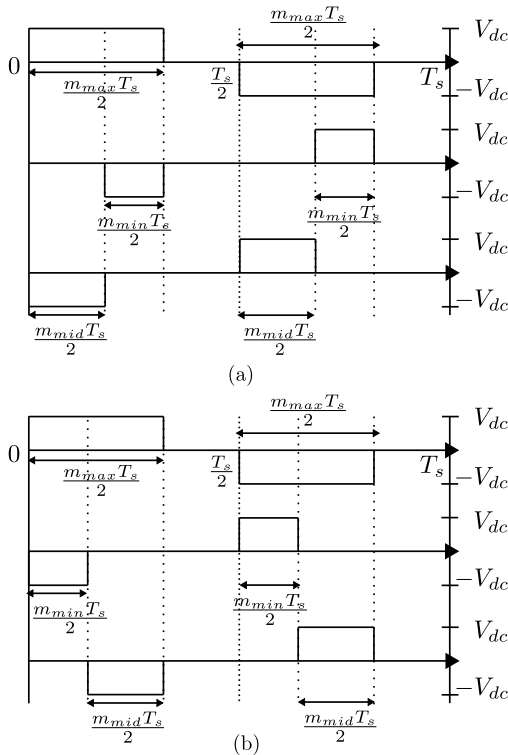


Fig. 4. Possible transformer primary voltages over T_s - (a) case I, (b) case II

In the transformer secondary, Q_{u1} is kept ON over one-half of the line cycle when $\bar{v}_{un'} \geq 0$. In one half of T_s when $v_U = V_{dc}$, D_{u1} conducts and $v_{uN} = v_{u1N} = nv_U = nV_{dc}$. In the next half when $v_U = -V_{dc}$, D_{u3} conducts and $v_{uN} = v_{u2N} = -nv_U = nV_{dc}$ (see Fig. 2a). Here, the average voltage, $\bar{v}_{uN} = \bar{v}_{un'} = nm_U V_{dc}$.

In the negative half of the line cycle i.e $\bar{v}_{un'} \leq 0$, Q_{u2} is kept ON and D_{u2} , D_{u4} take part in rectification (Fig. 2b). Here, $\bar{v}_{uN} = \bar{v}_{un'} = -nm_U V_{dc}$. Hence over a line cycle, $nm_U(\theta)V_{dc} = |\bar{v}_{un'}| = V_{pk} |\cos \theta|$. Thus the modulation

signal, m_U , is a rectified sine wave as seen in Fig. 3. The waveforms of v_U and v_{uN} over a line cycle are shown in Fig. 3b.

The suggested strategy results in line frequency switching of the half-bridge leg, $Q_{u1} - Q_{u2}$. In the similar way, other two phase voltages, $\bar{v}_{vn'} = V_{pk} \cos(\theta - \frac{2\pi}{3})$ and $\bar{v}_{wn'} = V_{pk} \cos(\theta + \frac{2\pi}{3})$, are generated. Thus all active switches in the secondary are line frequency switched, incurring negligible switching loss. Due to secondary diode bridges, the converter supports only instantaneous unidirectional power-flow from DC to AC side and hence the synthesized average phase voltage $\bar{v}_{un'}$ and line current i_u must be in phase.

C. Modulation of DC side converter

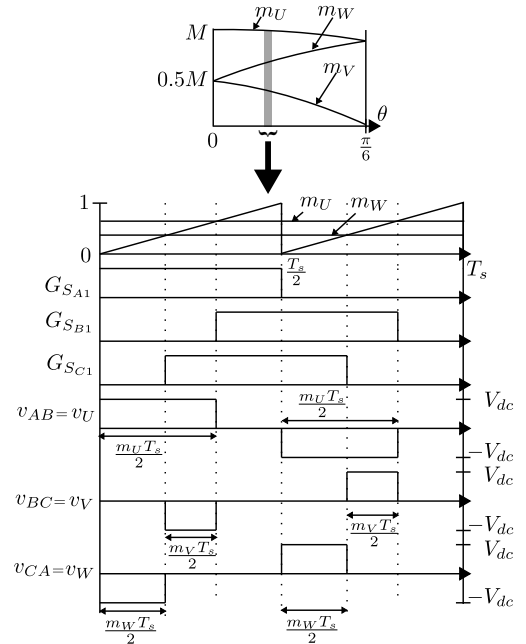


Fig. 5. DC side converter modulation in sector I

The three-phase modulation signals, m_U , m_V and m_W are given in (1) (see Fig. 3a).

$$m_j(\theta) = M \left| \cos \left(\theta + K_j \frac{2\pi}{3} \right) \right| \quad (1)$$

Where $j \in \{U, V, W\}$ and $K_U = 0$, $K_V = -1$ and $K_W = 1$ and $M = \frac{V_{pk}}{nV_{dc}}$. Let $m_{max} = \max(m_U, m_V, m_W)$, $m_{mid} = \text{mid}(m_U, m_V, m_W)$ and $m_{min} = \min(m_U, m_V, m_W)$. Using (1), the relation between m_{max} , m_{mid} and m_{min} is given in (2) (see Fig. 3a).

$$m_{max} = m_{mid} + m_{min} \quad (2)$$

Applying KVL across the HFT primary windings-

$$v_{AB} + v_{BC} + v_{CA} = v_U + v_V + v_W = 0 \quad (3)$$

Using the three legs of the DSC, we want to generate the voltage waveform like v_U (see Fig. 2) across each transformer primary terminals. Considering (2) and (3), there are two possible ways to apply the primary voltages over T_s as shown in Fig. 4.

TABLE I
 REFERENCE LEG IN DIFFERENT SECTORS

Sector	I	II	III	IV	V	VI
θ	$(0, \frac{\pi}{3})$	$(\frac{\pi}{3}, \frac{2\pi}{3})$	$(\frac{2\pi}{3}, \pi)$	$(\pi, \frac{4\pi}{3})$	$(\frac{4\pi}{3}, \frac{5\pi}{3})$	$(\frac{5\pi}{3}, 2\pi)$
Ref. Leg	A	C	B	A	C	B

In this paper, case I is considered for the DSC modulation. For example, when $\theta \in [0, \frac{\pi}{6}]$ (see Fig. 5), $m_{max} = m_U$, $m_{mid} = m_W$ and $m_{min} = m_V$. In the DSC, the two switches of a half-bridge leg are complementarily switched with a dead time. Each active switch of the DSC has a square wave gating pulse with 50% duty ratio and period T_s . When $\theta \in [0, \frac{\pi}{6}]$, leg A is considered as the reference leg. The gating pulse of S_{A1} , $G_{S_{A1}}$, is shown in Fig. 5. The gating signal S_{B1} , $G_{S_{B1}}$, is phase shifted w.r.t $G_{S_{A1}}$ by $\frac{m_U T_s}{2}$. The gating pulse of S_{C1} , $G_{S_{C1}}$ is phase shifted by $\frac{m_W T_s}{2}$ w.r.t $G_{S_{A1}}$. The phase shifts are obtained by comparing m_U and m_W with unity peak saw-tooth carrier of period $\frac{T_s}{2}$ (Fig. 5).

Following the above strategy, the reference leg needs to be changed every 60° as shown in Table I. These regions of θ are termed as sectors e.g. when $\theta \in [0, \frac{\pi}{3}]$, sector is I. In the next section, the selection of dead time of the DSC legs are described to achieve ZVS switching over complete line cycle.

III. STEADY STATE OPERATION OF THE DSC

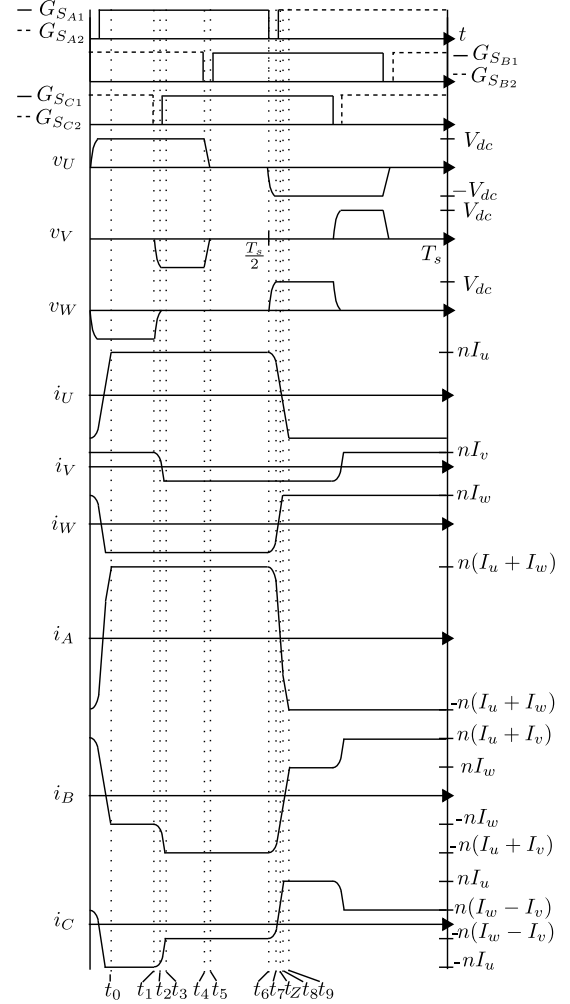
In this section, the steady state operation of the DSC over a switching cycle (T_s) is described in details. The operation presented here shows that all six active switches of the DSC are zero voltage switched (ZVS). For the switching analysis, the device capacitances C_s and leakage inductance of the HFTs seen from primary (L_{lk}) are considered. As the transformers are identical, the leakage inductances are considered to be equal. In the analysis, the conditions on dead-time are derived to ensure ZVS over a complete line cycle, $T_o = \frac{1}{f_o} = \frac{2\pi}{\omega_o}$. For ease of analysis, the slowly varying, properly filtered line currents $i_l = I_{pk} \cos(\theta + K_l \frac{2\pi}{3})$, ($l \in \{u, v, w\}$) and $K_u = 0$, $K_v = -1$ and $K_w = 1$) are assumed as constant current sinks over T_s with magnitudes I_l where I_{pk} is the peak of the line currents. The variations of I_l in sector I ($\theta \in [0, \frac{\pi}{3}]$) are given in (4) and (5).

$$\begin{aligned} I_u &= I_{pk} \cos \theta \\ I_w &= I_{pk} \cos \left(\frac{\pi}{3} - \theta \right) \end{aligned} \quad (4)$$

$$I_v = \begin{cases} I_{pk} \cos \left(\theta + \frac{\pi}{3} \right), & \theta \in [0, \frac{\pi}{6}] \\ I_{pk} \sin \left(\theta - \frac{\pi}{6} \right), & \theta \in [\frac{\pi}{6}, \frac{\pi}{3}] \end{cases} \quad (5)$$

The converter operation is described for the first half of sector I ($\theta \in [0, \frac{\pi}{6}]$) when $i_u = I_u$, $i_v = -I_v$ and $i_w = -I_w$ and $I_u > I_w > I_v$. For balanced operation, $I_u = I_v + I_w$, as can be seen from (4) and (5). Based on the directions of i_u , i_v and i_w , the line frequency switched Q_{u1} , Q_{v2} and Q_{w2} are kept ON throughout the switching cycle (T_s). In one half of a switching cycle, the converter goes through 9 distinct modes of operation. These modes can be divided as steady conduction

modes (mode 1, 4 and 6) and switching transition modes. As shown in Fig. 5, the DSC half-bridge legs are switched in the following order $C - B - A$ over one half of T_s . Mode 2 and 3 describe the transition of leg C. The transition of leg B is presented in mode 5. The switching process of leg A is divided into mode 7, 8 and 9. The circuit dynamics in the other half of T_s is similar. The switching waveforms in the first half of sector I are presented in Fig. 6.


 Fig. 6. DSC waveforms over T_s in sector I ($\theta \in [0, \frac{\pi}{6}]$)

A. Steady conduction mode I

Mode 1 ($t_0 < t < t_1$, Fig 6): In the DSC, S_{A1} , S_{B2} and S_{C2} are ON and thus the applied voltages across the HFT primary windings are $v_U = v_{AB} = V_{dc}$, $v_V = v_{BC} = 0$ and $v_W = v_{CA} = -V_{dc}$. Fig. 7a shows the circuit configuration in mode 1. Fig. 7b presents the simplified equivalent circuit. The primary currents in the HFTs are given as $i_U = nI_u$, $i_V = nI_v$ and $i_W = -nI_w$. The applied voltage polarity and the direction of currents shown in Fig. 7a and Fig. 7b indicate that the phases u and w are in active state, transferring power from DC to AC side, whereas the phase v is in zero state i.e. no active power is transferred from DC source to load. The

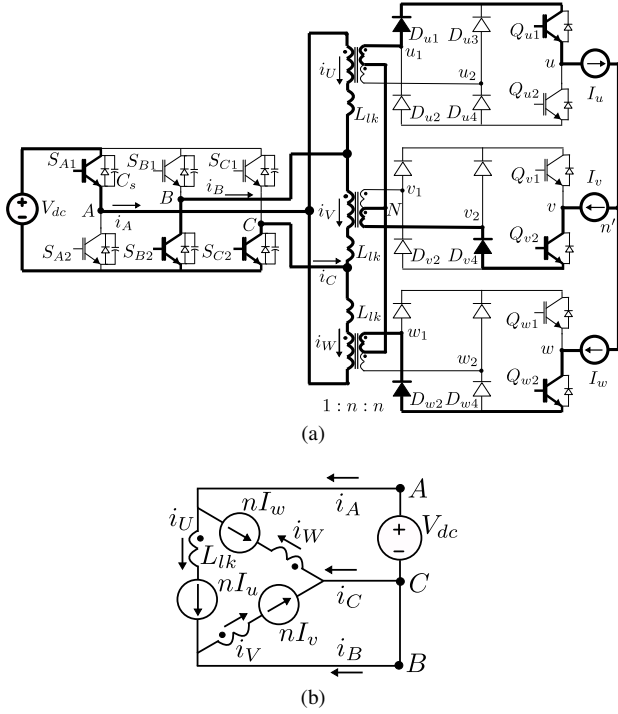


Fig. 7. Mode 1- (a) Circuit diagram, (b) Equivalent circuit

DSC pole currents $i_{A,B,C}$ are obtained by applying KCL at nodes A, B and C respectively.

$$\begin{aligned} i_A &= i_U - i_W = n(I_u + I_w) \\ i_B &= i_V - i_U = -n(I_u - I_v) = -nI_w \\ i_C &= i_W - i_V = -n(I_w + I_v) = -nI_u \end{aligned} \quad (6)$$

In secondary, (D_{u1}, Q_{u1}) , (D_{v4}, Q_{v2}) and (D_{w2}, Q_{w2}) are conducting the line currents.

B. Switching transition of leg C

Mode 2 ($t_1 < t < t_2$, Fig 6): The circuit configuration is shown in Fig. 8a and the simplified equivalent circuit is given in Fig. 8b. This mode starts at t_1 , when the gating pulse of S_{C2} is removed. The voltage across S_{C2} , $v_{S_{C2}}$, can not change abruptly due to device capacitance C_s . The slow rise of $v_{S_{C2}}$ helps to reduce turn OFF loss of S_{C2} . The pole current i_C starts charging the device capacitance (C_s) across S_{C2} and discharging the capacitance across S_{C1} . The applied voltage polarity across HFT terminals B and C , forward biases the secondary diode D_{v2} and hence the HFT secondary terminals v_1 and v_2 are shorted through the diode bridge (see Fig. 8a). This also shorts the current source I_v . As seen from Fig. 8b, the voltage polarity across C, B is against the direction of the primary current i_V and hence i_V falls (see Fig. 6). The applied voltage polarities across the HFT primary terminals- (A, B) and (C, A) are same as in mode 1 (see Fig. 7b and 8b). Hence the conduction states of secondary diode bridges $D_{u1} - D_{u4}$, $D_{w1} - D_{w4}$ and the half-bridge legs $Q_{u1} - Q_{u2}$, $Q_{w1} - Q_{w2}$ remain unchanged. The circuit equations in this

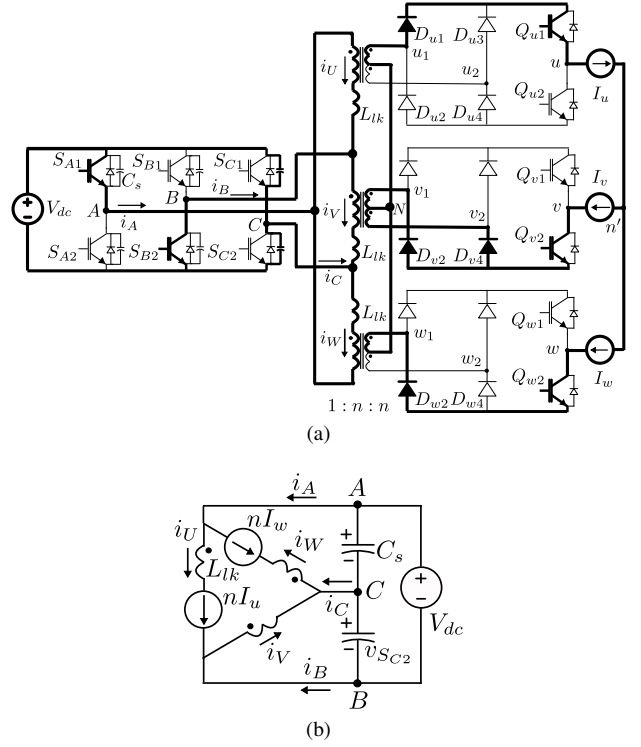


Fig. 8. Mode 2- (a) Circuit diagram, (b) Equivalent circuit

mode are shown in (7).

$$\begin{aligned} v_{S_{C2}} &= -v_V = n\omega_r L_{lk} I_u \sin \omega_r (t - t_1) \\ i_V &= nI_u \cos \omega_r (t - t_1) - nI_w \\ i_B &= -nI_u (1 - \cos \omega_r (t - t_1)) - nI_w \\ i_C &= -nI_u \cos \omega_r (t - t_1) \\ (t_2 - t_1) &= \frac{1}{\omega_r} \sin^{-1} \left(\frac{V_{DC}}{n\omega_r L_{lk} I_u} \right) \end{aligned} \quad (7)$$

Where $\omega_r = \frac{1}{\sqrt{2L_{lk}C_s}}$. At t_2 , $v_{S_{C2}}$ becomes equal to V_{DC} and this mode ends. To charge the $v_{S_{C2}}$ to V_{DC} , (8) needs to be satisfied. Otherwise the circuit goes into a resonating oscillation mode.

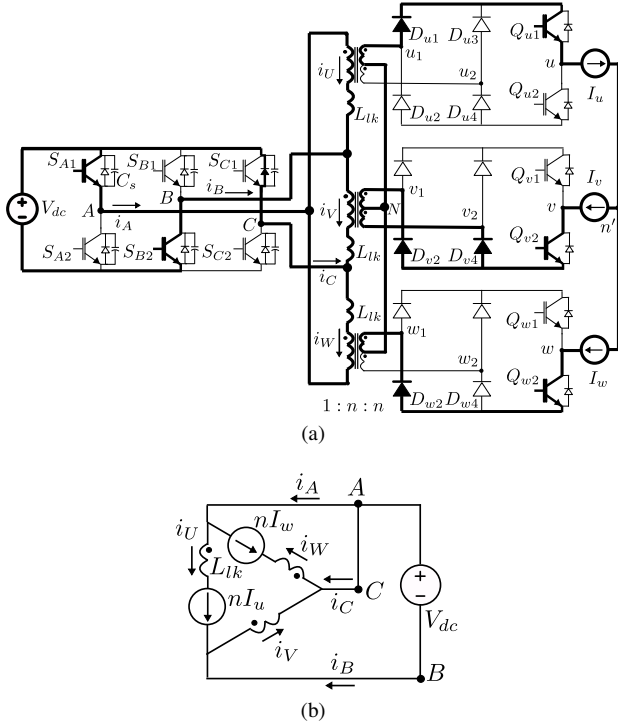
$$V_{dc} \leq n\omega_r L_{lk} I_u \quad (8)$$

The duration of mode 2, $(t_2 - t_1)$, is shown in (7). In our considered zone of operation, $\theta \in [0, \frac{\pi}{6}]$, $(t_2 - t_1)$ has maximum value at $\theta = \frac{\pi}{6}$ when $I_u (= 0.87I_{pk})$ is minimum.

Mode 3 ($t_2 < t < t_3$, Fig 6): After t_2 , the anti-parallel diode of S_{C1} comes in conduction as shown in Fig. 9a. The simplified equivalent circuit is shown in Fig. 9b. S_{C1} is turned ON after t_2 to achieve ZVS. To ensure ZVS ON throughout our considered zone of operation, the dead-time, DT_C , between $S_{C1} - S_{C2}$ should be greater than maximum value of $(t_2 - t_1)$ and the condition is given in (9).

$$DT_C \geq \frac{1}{\omega_r} \sin^{-1} \left(\frac{1.15V_{DC}}{n\omega_r L_{lk} I_{pk}} \right) \quad (9)$$

In this mode, the applied voltage across the primary terminals (B, C) is $v_V = v_{BC} = -V_{dc}$ and is against the direction of i_V . Hence i_V falls in this mode also. i_V becomes zero and changes its direction. In secondary, soft current commutation



between the diodes D_{v2} and D_{v4} takes place. The primary currents are given in (10).

$$\begin{aligned} i_V &= i_V(t_2) - \frac{V_{dc}}{L_{lk}}(t - t_2) \\ i_B &= i_B(t_2) - \frac{V_{dc}}{L_{lk}}(t - t_2) \\ i_C &= i_C(t_2) + \frac{V_{dc}}{L_{lk}}(t - t_2) \end{aligned} \quad (10)$$

At t_3 , $i_V = -nI_v$ and this mode ends. D_{v4} is reverse biased. The DSC pole currents are given as $i_A(t_3) = n(I_u + I_w)$, $i_B(t_3) = -n(I_u + I_w)$ and $i_C(t_3) = -n(I_w - I_v)$. In this mode only the HFT primary current i_V changes its direction. The directions of DSC pole currents $i_{A,B,C}$ remain same as in mode 1.

C. Steady conduction mode II

Mode 4 ($t_3 < t < t_4$, Fig 6): The circuit configuration in this mode is shown in Fig. 10a. In DSC, S_{A1} , S_{B2} and the anti-parallel diode of S_{C1} are in conduction. Thus the applied voltages across the primary windings are- $v_U = V_{AB} = V_{dc}$, $v_V = v_{BC} = -V_{dc}$ and $v_W = v_{CA} = 0$. The simplified equivalent circuit is shown in Fig. 10b. Shown voltage polarities and current directions in the equivalent circuit, indicate that the active power is transferred from DC to AC side via phase u and v . Whereas phase w is in zero state. The primary winding currents in this mode are given as $i_U = nI_u$, $i_V = -nI_v$ and $i_W = -nI_w$. The DSC pole currents are $i_A = n(I_u + I_w)$, $i_B = -n(I_u + I_v)$ and $i_C = -n(I_w - I_v)$ (see Fig. 6).

D. Switching transition of leg B

Mode 5 ($t_4 < t < t_5$, Fig 6): This mode begins at t_4 when the gating pulse of S_{B2} is removed. The circuit diagram

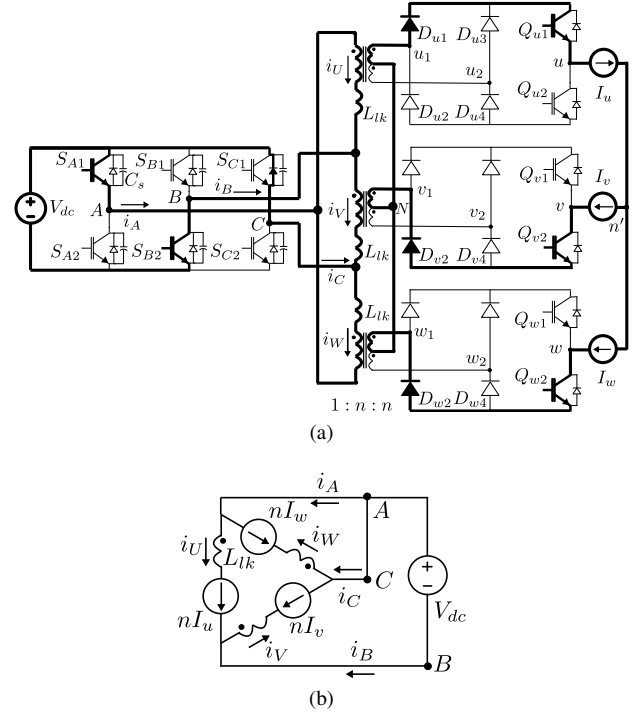


Fig. 10. Mode 4- (a) Circuit diagram, (b) Equivalent circuit

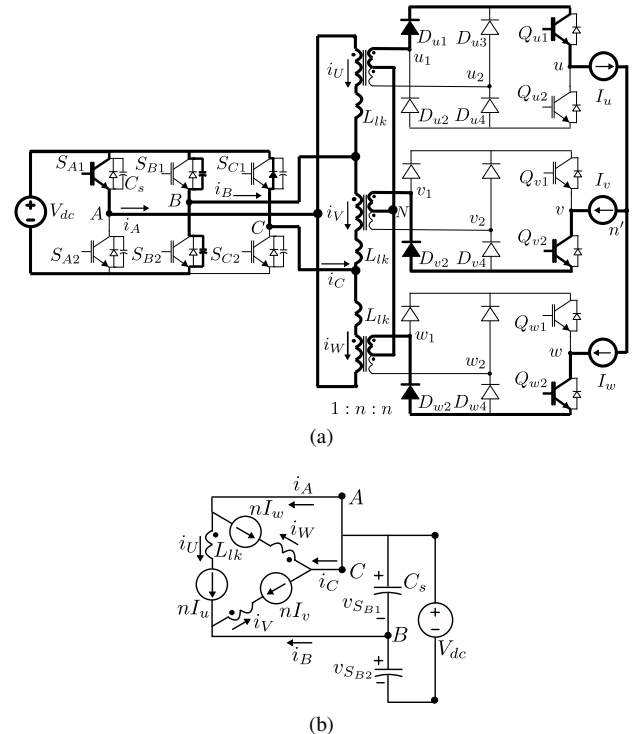


Fig. 11. Mode 5- (a) Circuit diagram, (b) Equivalent circuit

in this mode is shown in Fig. 11a. The device capacitance (C_s) slows down the voltage rise across S_{B2} and thus the turn OFF loss of S_{B2} is reduced. Fig. 11b presents the simplified equivalent circuit. The pole current i_B charges the capacitance across S_{B2} and discharges the capacitance across S_{B1} as shown in Fig. 11b. In this mode, the primary voltage polarities of the HFTs are same as in mode 4. Hence the conduction states of the secondary side diode bridges are unaltered. The primary winding currents ($i_{U,V,W}$) and the DSC pole currents ($i_{A,B,C}$) do not change in this mode. The circuit dynamics in this mode is shown in (11).

$$\begin{aligned} v_{S_{B1}} &= V_{dc} - \frac{n(I_u + I_v)}{2C_s}(t - t_4) \\ v_{S_{B2}} &= \frac{n(I_u + I_v)}{2C_s}(t - t_4) \\ t_5 - t_4 &= \frac{2C_s V_{dc}}{n(I_u + I_v)} \end{aligned} \quad (11)$$

$v_{S_{B1}}$ and $v_{S_{B2}}$ are voltages across S_{B1} , S_{B2} respectively. At $t = t_5$, $v_{S_{B2}} = V_{dc}$ and this mode ends. The duration ($t_5 - t_4$), is given in (11). In our considered range of $\theta \in [0, \frac{\pi}{6}]$, ($t_5 - t_4$) is maximum at $\theta = \frac{\pi}{6}$, when $(I_u + I_v)$ is minimum and is equal to $0.87I_{pk}$.

E. Steady conduction mode III

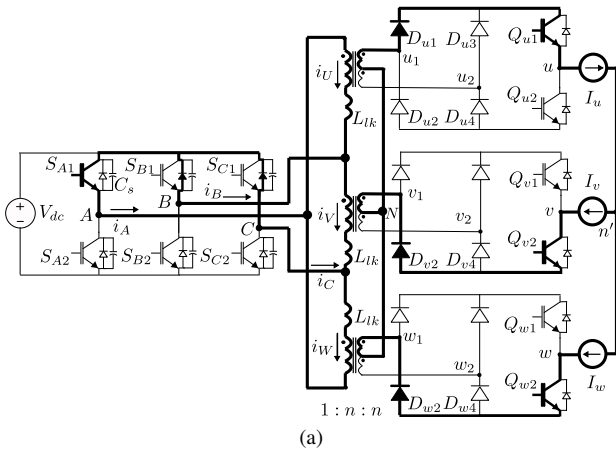


Fig. 12. Mode 6- (a) Circuit diagram, (b) Equivalent circuit

Mode 6 ($t_5 < t < t_6$, Fig 6): The circuit configuration of mode 6 is shown in Fig. 12a. As seen from the figure, in the DSC, S_{A1} and the anti-parallel diodes of S_{B1} , S_{C1} are in conduction. To achieve ZVS turn ON of S_{B1} , gating pulse of S_{B1} should be applied after t_5 when the anti-parallel diode is in conduction. To achieve soft turn ON through out the considered interval of $\theta \in [0, \frac{\pi}{6}]$, the dead-time between S_{B1} –

S_{B2} , DT_B , should be greater than the maximum duration of ($t_5 - t_4$). The condition is given in (12).

$$DT_B \geq \frac{2.3C_s V_{dc}}{nI_{pk}} \quad (12)$$

The applied primary voltages in this mode are $v_U = v_V = v_W = 0$. The simplified equivalent circuit is shown in Fig. 12b. In this mode, all three phases are in zero or free-wheeling state.

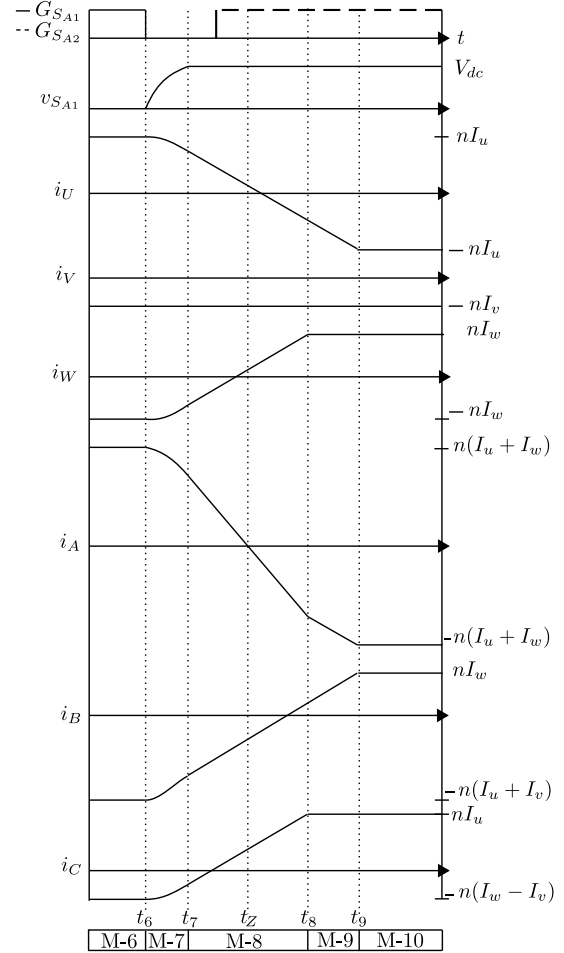


Fig. 13. Enlarged current wave forms in Mode 7-9

F. Switching transition of leg A

Mode 7 ($t_6 < t < t_7$, Fig 6 and Fig. 13): This mode begins at t_6 when S_{A1} is turned OFF. The circuit configuration is shown in Fig. 14a. As explained earlier, the device capacitance (C_s) across S_{A1} helps to reduce the turn OFF loss. The pole current i_A , begins to charge the capacitor across S_{A1} and discharge the capacitor across S_{A2} . The simplified equivalent circuit is shown in Fig. 14b. The voltage polarities across the primary terminals (A, B) and (C, A) forward bias the secondary diodes D_{u3} and D_{w4} respectively. And thus the secondary terminals of the two HFTs, (u_1, u_2) and (w_1, w_2) are shorted by the diode bridges $D_{u1} - D_{u4}$ and $D_{w1} - D_{w4}$ respectively. The current sinks I_u and I_w are also shorted. As seen in Fig. 14b, the applied voltage polarities are against the directions of the primary currents i_U and i_W . Hence i_U and

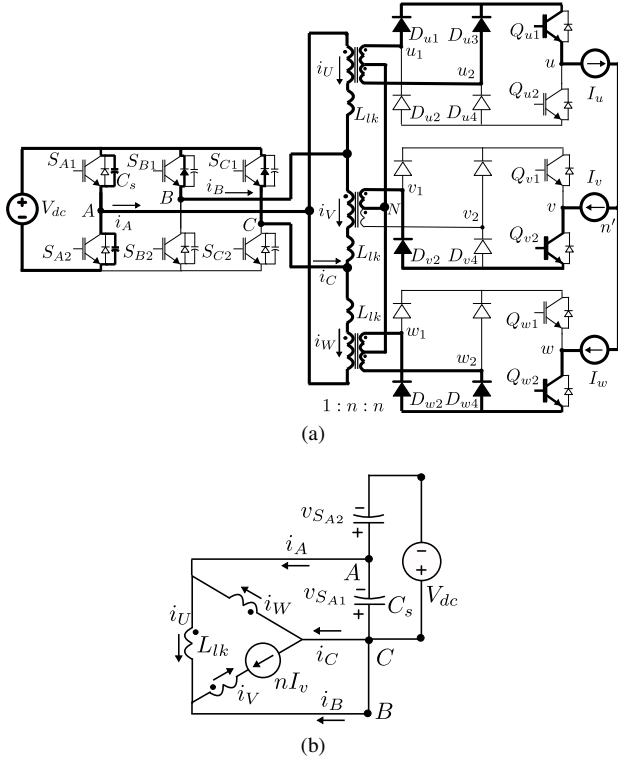


Fig. 14. Mode 7- (a) Circuit diagram, (b) Equivalent circuit

i_W starts to decrease in this mode whereas the primary current $i_V = -nI_v$ remains unchanged. The circuit equations in this mode are given in (13).

$$\begin{aligned}
 i_U &= nI_u - \frac{n(I_u + I_w)}{2}(1 - \cos \omega'_r(t - t_6)) \\
 i_W &= -nI_w + \frac{n(I_u + I_w)}{2}(1 - \cos \omega'_r(t - t_6)) \\
 i_A &= n(I_u + I_w) \cos \omega'_r(t - t_6) \\
 i_B &= -n(I_u + I_v) + \frac{n(I_u + I_w)}{2}(1 - \cos \omega'_r(t - t_6)) \\
 i_C &= -n(I_w - I_v) + \frac{n(I_u + I_w)}{2}(1 - \cos \omega'_r(t - t_6)) \\
 v_W &= -v_U = v_{SA1} = \frac{n(I_u + I_w)\omega'_r L_{lk}}{2} \sin \omega'_r(t - t_6)
 \end{aligned} \quad (13)$$

Where v_{SA1} is the voltage across S_{A1} and $\omega'_r = \frac{1}{\sqrt{L_{lk}C_s}}$. At the end of this mode at t_7 , $v_{SA1} = V_{dc}$ and $v_{SA2} = 0$. The anti-parallel diode of S_{A2} is forward biased. To charge the capacitor (C_s) across S_{A1} to V_{dc} , following condition should be satisfied, $n(I_u + I_w)\omega'_r L_{lk} \geq 2V_{dc}$. Otherwise, the circuit enters into a resonating oscillation mode with frequency ω'_r and remains there till S_{A2} is turned ON. Also this results in hard turn ON of S_{A2} . The interval $(t_7 - t_6)$, is given as, $(t_7 - t_6) = \frac{1}{\omega'_r} \sin^{-1} \left(\frac{2V_{dc}}{n(I_u + I_w)\omega'_r L_{lk}} \right)$. $(t_7 - t_6)$ has maximum value in sector I at $\theta = 0$ and $\theta = \frac{\pi}{3}$, where $(I_u + I_w) = 1.5I_{pk}$ is minimum. To achieve ZVS turn ON of S_{A2} , the gating pulse of S_{A2} should be applied after t_7 when the anti-parallel diode is conducting. Considering maximum value of $(t_7 - t_6)$, the

dead time between $S_{A1} - S_{A2}$, DT_A , should satisfy (14).

$$DT_A \geq \frac{1}{\omega'_r} \sin^{-1} \left(\frac{1.33V_{DC}}{n\omega'_r L_{lk} I_{pk}} \right) \quad (14)$$

The transformer primary currents, i_U and i_W along with the DSC pole currents, $i_{A,B,C}$ linearly change their directions in next two modes. S_{C1} and S_{B1} are already ON (ZVS) in mode 3 and mode 6 respectively. So, based on the direction of i_B and i_C , at first the anti-parallel diodes and then the switches S_{B1} and S_{C1} conduct respectively.

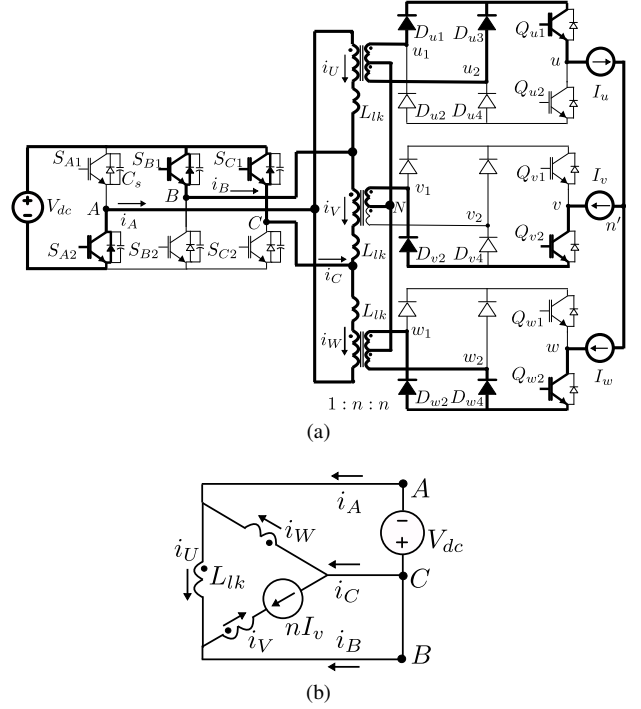


Fig. 15. Mode 8- (a) Circuit diagram, (b) Equivalent circuit

Mode 8 ($t_7 < t < t_8$, Fig 6 and Fig. 13): The circuit configuration is shown in Fig.15a and the corresponding simplified equivalent circuit is presented in Fig. 15b. As seen from these figures, the voltage applied across the primary terminals (A, B) and (C, A) are against the direction of primary currents i_U and i_W . Hence, i_U and i_W fall further in this mode. The circuit dynamics are given in (15).

$$\begin{aligned}
 i_U &= i_U(t_7) - \frac{V_{dc}}{L_{lk}}(t - t_7) \\
 i_W &= i_W(t_7) + \frac{V_{dc}}{L_{lk}}(t - t_7) \\
 i_A &= i_A(t_7) - \frac{2V_{dc}}{L_{lk}}(t - t_7) \\
 i_{B,C} &= i_{B,C}(t_7) + \frac{V_{dc}}{L_{lk}}(t - t_7)
 \end{aligned} \quad (15)$$

In secondary, I_u is transferred linearly from diode D_{u1} to D_{u3} . Similarly, I_w is also transferred from D_{w2} to D_{w4} . i_W changes its direction in this mode. At t_8 , $i_W = nI_w$ and $i_C = nI_u$ and this mode ends. At t_8 , I_w is completely transferred from D_{w2} to D_{w4} and D_{w2} is reverse biased.

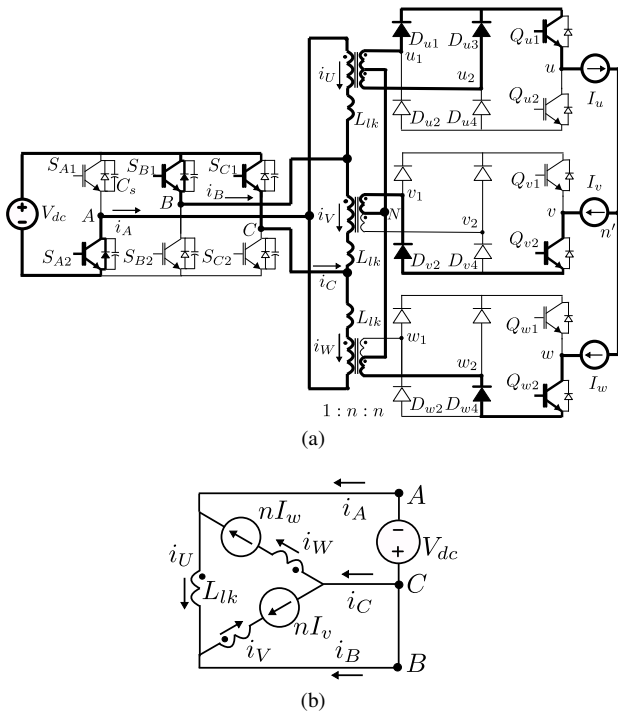


Fig. 16. Mode 9- (a) Circuit diagram, (b) Equivalent circuit

Mode 9 ($t_8 < t < t_9$, Fig 6 and Fig. 13): The circuit configuration is presented in Fig. 16a and the corresponding simplified equivalent circuit is shown in Fig. 16b. In this mode, the slope of the pole current i_A is changed from $\frac{2V_{dc}}{L_{lk}}$ to $\frac{V_{dc}}{L_{lk}}$, as the primary current i_W is clamped to nI_w . The slope of the primary current i_U and pole current i_B remain $\frac{V_{dc}}{L_{lk}}$. i_U and $i_{A,B}$ change their directions. At t_9 , $i_U = -nI_u$, $i_A = -n(I_u + I_w)$ and $i_B = nI_w$ and this mode ends. At t_9 , I_u is shifted completely to D_{u3} from D_{u1} and D_{u1} is reverse biased.

G. Steady conduction mode I

Mode 10 ($t > t_9$, Fig 6): The circuit configuration and simplified equivalent circuit are presented in Fig. 17a and Fig. 17b respectively. Phase u and phase w are in active power transfer mode whereas the phase v is in zero state as indicated by the voltage polarities and current directions in Fig. 17b. Mode 10 is equivalent to Mode 1.

H. Upper limit of DT_A to ensure ZVS

As we have seen, during the switching transition of leg B and C , respective pole currents i_B and i_C do not change their directions. But the pole current i_A changes its direction during the switching transition of leg A . To ensure ZVS turn ON of $S_{A1} - S_{A2}$ the gating signal should be applied before i_A becomes zero at t_Z and thereafter changes its direction and hence the anti-parallel diode stops conducting. So, there must be an upper limit of DT_A such that $DT_A < (t_Z - t_6) = \Delta t_Z$. To achieve ZVS ON over our considered range of $\theta \in [0, \frac{\pi}{6}]$, $DT_A < \Delta t_{Z,min}$. Here our objective is to find out $t_{Z,min}$. For the ease of estimation, the duration of mode 7,

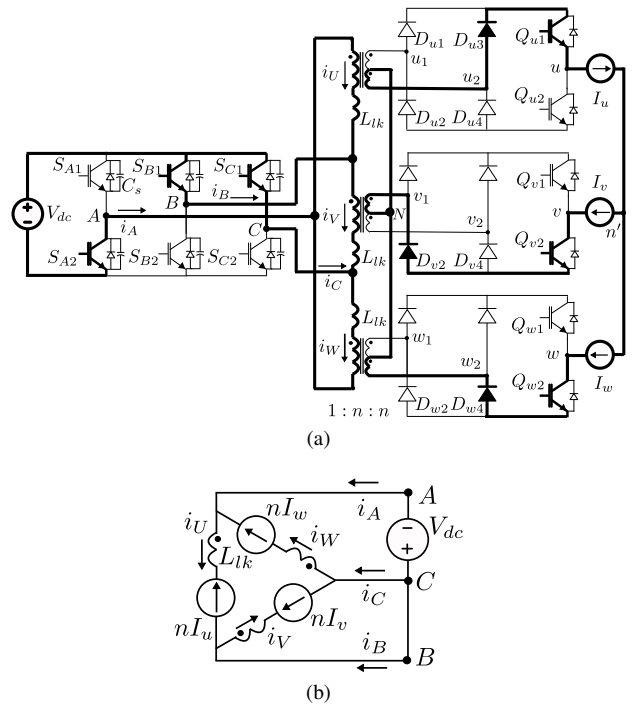


Fig. 17. Mode 10- (a) Circuit diagram, (b) Equivalent circuit

($t_7 - t_6$) and the change of current magnitudes in mode 7 are considered negligible. Hence, $i_A(t_6) \simeq i_A(t_7) = n(I_u + I_w)$ and $i_W(t_6) \simeq i_W(t_7) = -nI_w$. At the end of mode 8, at t_8 , $i_W(t_8) = nI_w$. In mode 8, i_A has a slope of $\frac{2V_{dc}}{L_{lk}}$ and in mode 9 the slope is $\frac{V_{dc}}{L_{lk}}$. It is important to find out the slope of i_A between t_6 and t_Z . Using (4), (5) and (15), The interval $(t_8 - t_6) = \frac{(i_W(t_8) - i_W(t_6))L_{lk}}{V_{dc}} = \frac{2nI_wL_{lk}}{V_{dc}}$ and $i_A(t_8) = i_A(t_6) - \frac{2V_{dc}}{L_{lk}}(t_8 - t_6) = -\frac{nI_{pk}}{2}(\cos\theta + 3\sqrt{3}\sin\theta)$. $i_A(t_8)$ is negative in our considered range of θ . So, i_A changes its direction in mode 8 with a slope $\frac{2V_{dc}}{L_{lk}}$. Hence Δt_Z is given in (16).

$$\Delta t_Z = \frac{n(I_u + I_w)L_{lk}}{2V_{dc}} = \frac{\sqrt{3}nI_{pk}L_{lk}}{2V_{dc}} \cos\left(\frac{\pi}{6} - \theta\right) \quad (16)$$

At $\theta = 0^\circ$, Δt_Z is minimum and $\Delta t_{Z,min} = \frac{0.75nI_{pk}L_{lk}}{V_{dc}}$. Combining with (14), the dead time, DT_A , between the gating signals of $S_{A1} - S_{A2}$ is given in (17).

$$\frac{1}{\omega_r'} \sin^{-1}\left(\frac{1.33V_{DC}}{n\omega_r'L_{lk}I_{pk}}\right) \leq DT_A \leq \frac{0.75nI_{pk}L_{lk}}{V_{dc}} \quad (17)$$

The above discussion presents the DSC operation in one half of T_s . Similar switching process is followed in the next half with other symmetrical switches. In the other half of sector I ($\theta \in [\frac{\pi}{6}, \frac{\pi}{3}]$), the DSC legs are switched in following order $B - C - A$ (over one half of T_s). The transition of leg B has two modes same as discussed in mode 2 and 3. The transition of leg C follows a similar process discussed in mode 5. The transition of leg A is same as discussed in mode 7-9. The DSC has a similar sequence of operation in other sectors. For

example, the DSC legs are switched in the order of $B-A-C$ over one half of T_s in sector II ($\theta \in [\frac{\pi}{3}, \frac{\pi}{2}]$). Here, the process of switching transitions of leg B and leg A are same as described in Mode 2-3 and in mode 5 respectively. leg C has similar switching transition as described in Mode 7-9.

IV. EXPERIMENTAL VALIDATION

A. Experimental set-up

The operation of the proposed converter is experimentally verified using a 3.7 kW hardware prototype (see Fig. 18). Table II presents the operating condition. 1200V, 75A SEMIKRON IGBT modules (SKM75GB123D) are used to implement the half-bridge legs of the converter. Secondary diode bridges use IXYS fast recovery 1200V, 75A diodes, MEE 75-12 DA. Optically isolated gate driver, ACPL 339J, with driving voltage level $\pm 15V$, is used to drive the IGBTs. The switching frequency of the DSC is 20kHz. A 600 ns dead-time that satisfies all the dead-time conditions derived in the last section is provided between two IGBTs of a half-bridge leg. Three ferrite core (E 80/38/20) HFTs with turns ratio 51:34:34 are used. The transformers have leakage inductance (seen from primary) in the order of 6-8 μ H. To satisfy the dead-time condition given in (17), an additional 48 μ H inductor is connected in series with each primary winding of the HFTs. To implement the modulation strategy and to generate gating signals of the IGBTs, an ARM-FPGA based system-on-chip (SoC) control platform, Xilinx Zynq-7000 is used.

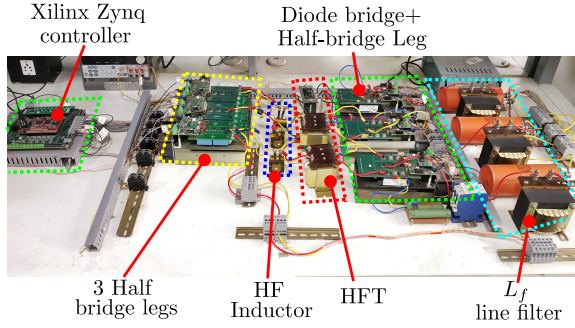


Fig. 18. Hardware prototype

TABLE II
OPERATING CONDITION

Output power (P_{out})	3.7kW
Output peak voltage (V_{pk})	190V
DC input (V_{dc})	350V
HFT turns ratio (n)	2/3
Line frequency ($f_o = \frac{\omega_o}{2\pi}$)	50Hz
Switching frequency ($f_s = \frac{1}{T_s}$)	20kHz

B. Experimental validation of modulation strategy

A balanced 3 ϕ , 50 Hz AC voltage source ($v_{(u'v'w')n'}$) is connected to the converter. Input DC bus voltage is 350 V. M is adjusted to get the peak of output phase voltage (V_{pk}) of 190 V. Fig. 19 shows the phase voltage $v_{u'n'}$ and line currents $i_{u,v,w}$. The experimentally measured peak value (I_{pk})

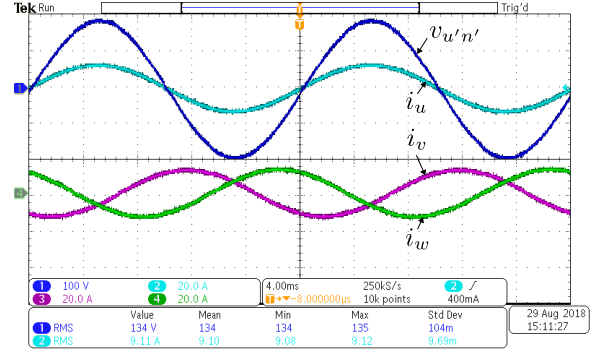


Fig. 19. Line output- [CH1] $v_{u'n'}$ (100V/div.), [CH2] i_u (20A/div.), [CH3] i_v (20A/div.), [CH4] i_w (20A/div.). Time scale 4ms/div.

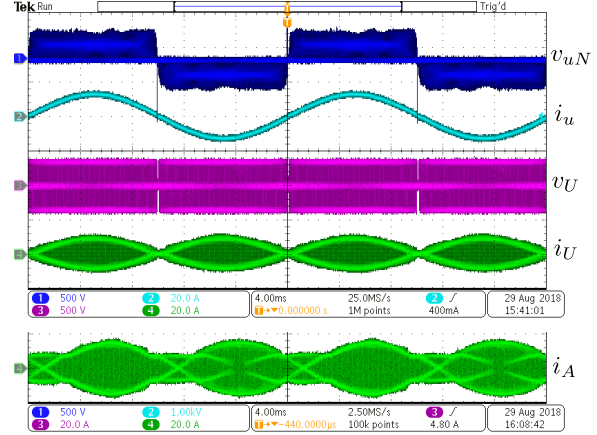


Fig. 20. Pole voltage and current waveforms- [CH1] v_{uN} (500V/div.), [CH2] i_u (20A/div.), [CH3] v_U (500V/div.), [CH4] i_U (20A/div.); [CH4] i_A (20A/div.). Time scale 4ms/div.

of the line currents is 12.9 A. The theoretically estimated $I_{pk} = \frac{P_{out}}{1.5V_{pk}} = 12.98$ A. At 50 Hz, the impedance of line filter ($L_f = 2.5$ mH) is relatively small. Hence $v_{u'n'}$ is almost in phase with the line current i_u .

The unipolar PWM pole voltage w.r.t HFT neutral, v_{uN} , is shown in Fig. 20. v_{uN} has voltage levels $nV_{dc} = 233V$ and zero. In this figure, in [CH3], the HFT primary voltage, v_U is shown. v_U is PWM high frequency AC with voltage levels of $\pm V_{dc} = \pm 350$ V and zero. The primary winding current i_U and the DSC pole current i_A are also shown in 20. The waveform of i_U , as seen in the figure, is high frequency square-wave with magnitude varied sinusoidally over a line cycle. The envelope of i_U has the experimentally measured peak of 8.6 A. The theoretically estimated peak is $nI_{pk} = 8.65A$. Unlike i_U , the envelope of i_A never touches time axis as seen in Fig. 20. This pole current envelope helps to achieve soft-turn ON of the leg switches $S_{A1} - S_{A2}$ over complete line cycle. The current envelope has a measured peak of $\sqrt{3}nI_{pk} = 14.9A$.

Switching cycle waveforms of the transformer primary voltages ($v_{U,V,W}$) and the primary currents (i_U, i_V) are shown in Fig. 21 (in sector I, $\theta \approx \frac{\pi}{90}$). Steady-state magnitude of primary currents, i_U and i_V , are $nI_u = 8.65 \cos(\frac{\pi}{90}) \approx 8.6$ A and $nI_v = 8.65 \cos(\frac{\pi}{90} + \frac{\pi}{3}) \approx 3.9$ A respectively. This result verifies the analytical voltage and current waveforms shown in Fig. 5 and Fig. 6. Hence, the modulation strategy and operation

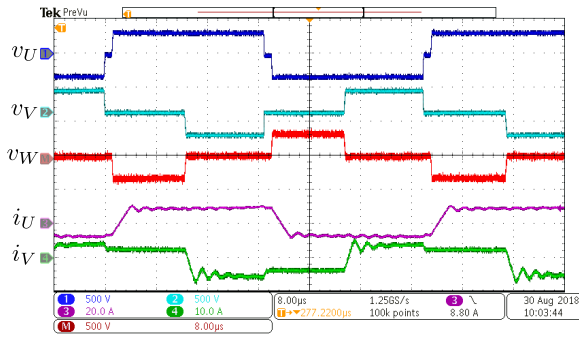


Fig. 21. Transformer primary voltages and primary currents (in sector I at $\theta \approx \frac{\pi}{90}$) - [CH1] v_U (500V/div.), [CH2] v_V (500V/div.), [M] v_W (500V/div.), [CH3] i_U (20A/div.), [CH4] i_V (10A/div.). Time scale $8\mu\text{s}/\text{div}$.

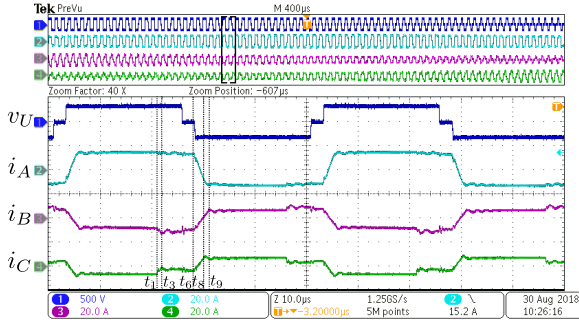


Fig. 22. Primary voltage and the DSC pole currents (in sector I at $\theta \approx \frac{\pi}{18}$) - [CH1] v_U (500V/div.), [CH2] i_A (20A/div.), [CH3] i_B (20A/div.), [CH4] i_C (20A/div.). Time scale $10\mu\text{s}/\text{div}$.

of the DSC described in Section II and III are also verified. As expected, it is seen that the polarity of primary winding current changes only when the applied primary voltage jumps to $\pm 350\text{V}$ from zero. Flux balance of HFT is achieved over T_s .

Fig. 22 presents the DSC pole currents $i_{A,B,C}$ in sector I at $\theta \approx \frac{\pi}{18}$. The experimental waveforms closely match with the analytical pole current waveforms in sector I shown in Fig. 6. The steady-state magnitude of i_A is 13.9 A. From the experimental result, the change in magnitude of pole currents i_B and i_C in Mode 2-3 ($t_1 < t < t_3$) are clearly observable. As discussed in section III, i_B and i_C do not change their direction in Mode 2-3. The pole currents change their direction in Mode 7-9 ($t_6 < t < t_9$) as seen in Fig. 22.

C. Experimental validation of ZVS of the DSC

Switching transition of leg A: The switching transition of leg A in sector I (at $\theta \approx \frac{\pi}{18}$) is presented in Fig. 23. This result verifies the switching process discussed in Mode 7-9 in section III. The gating pulse of S_{A1} , $G_{S_{A1}}$, is withdrawn at t_6^- . As seen in Fig. 23, at t_6 , $v_{S_{A1}}$ starts to build up. Due to device capacitance C_s , voltage changes slowly across S_{A1} and hence the turn OFF loss of S_{A1} has reduced. At t_7 , $v_{S_{A1}} = V_{dc} = 350\text{V}$, $v_{S_{A2}} = 0\text{V}$ and the pole current i_A is still positive i.e. flowing in the same direction. Hence the anti-parallel diode of S_{A2} is in conduction. To achieve ZVS turn ON, at t_7^+ , the gating pulse of S_{B2} , $G_{S_{B2}}$ is applied before i_A becomes zero. Sometime after, i_A becomes zero and then changes its direction at t_Z .

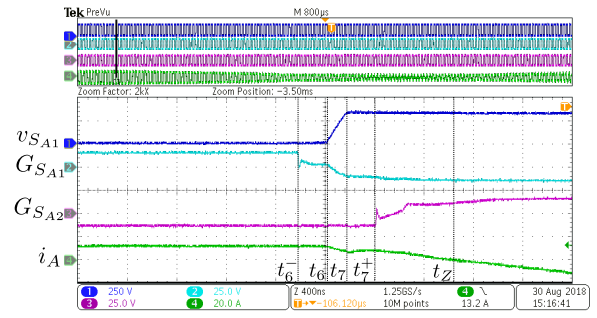


Fig. 23. Switching transition of leg A (in sector I at $\theta \approx \frac{\pi}{18}$) - [CH1] $v_{S_{A1}}$ (250V/div.), [CH2] $G_{S_{A1}}$ (25V/div.), [CH3] $G_{S_{A2}}$ (25V/div.), [CH4] i_A (20A/div.). Time scale $400\text{ns}/\text{div}$.

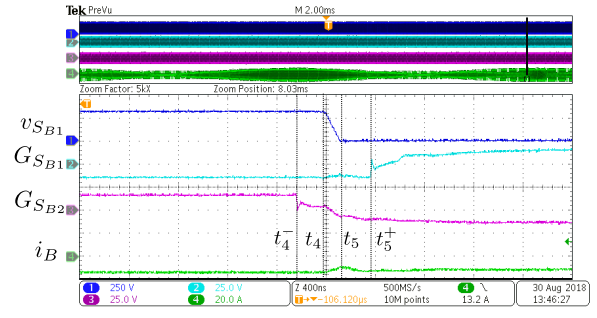


Fig. 24. Switching transition of leg B (in sector I at $\theta \approx \frac{\pi}{18}$) - [CH1] $v_{S_{B1}}$ (250V/div.), [CH2] $G_{S_{B1}}$ (25V/div.), [CH3] $G_{S_{B2}}$ (25V/div.), [CH4] i_B (20A/div.). Time scale $400\text{ns}/\text{div}$.

Switching transition of leg B: Fig. 24 shows the switching transition of leg B described in Mode 5-6 in section III. As seen in the figure, S_{B2} is ON and conducting initially. The gating pulse of S_{B2} is withdrawn at t_4^- . The voltage across $S_{B1} - S_{B2}$ starts changing slowly and linearly at t_4 . Due to device capacitance C_s , the slow change in voltage helps to reduce the turn OFF loss of S_{B2} . The voltage across S_{B1} , $v_{S_{V_T}}$, falls to zero at t_5 . Sometime after, at t_5^+ , S_{B1} is turned ON. Thus ZVS turn ON of S_{B1} is ensured.

Switching transition of leg C: Fig. 25 shows the switching transition of $S_{C1} - S_{C2}$ discussed in Mode 2-3 in section III. The gating pulse of S_{C2} is removed at t_1^- . As seen in the figure, sometime after, at t_1 , the voltages across $S_{C1} - S_{C2}$ start to change. Due to device capacitance C_s , the turn OFF loss of S_{C2} is reduced. The voltage across S_{C1} , $v_{S_{C2}}$, becomes zero at t_2 . The pole current (i_C) direction does not change.

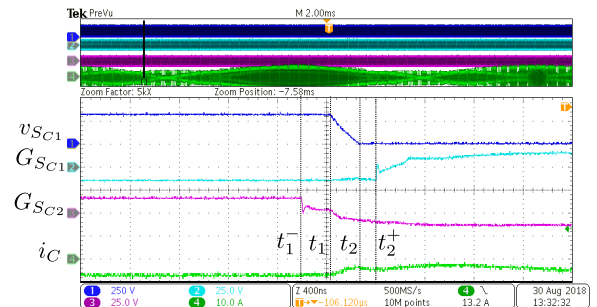


Fig. 25. Switching transition of leg C (in sector I at $\theta \approx \frac{\pi}{18}$) - [CH1] $v_{S_{C1}}$ (250V/div.), [CH2] $G_{S_{C1}}$ (25V/div.), [CH3] $G_{S_{C2}}$ (25V/div.), [CH4] i_C (10A/div.). Time scale $400\text{ns}/\text{div}$.

Hence the anti-parallel diode of S_{C1} is in conduction. At t_2^+ , gating pulse of S_{C1} is applied ensuring ZVS turn ON of S_{C1} .

D. Measured loss and efficiency

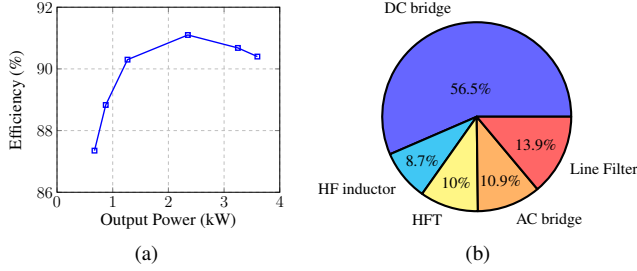


Fig. 26. (a) Efficiency of the proposed DC-AC converter, (b) Loss distribution at 2.35kW output power

Fig. 26a presents the experimentally measured efficiency of the converter with DC input 350V. The plot is given for a range of output power from 0.6kW to 3.7kW. As seen in the figure, the converter has a peak efficiency of 91.1% at 2.35kW output power. Fig. 26b shows the loss distribution of the converter at 2.35kW output. Out of total loss, The DSC has a loss of 56.5% and the line frequency switched secondary unfolded along with the diode-bridges has loss of only 11%.

V. TOPOLOGY COMPARISON

TABLE III
TARGET DESIGN SPECIFICATION

Parameter	Value
Output power (P)	200 kW
Input DC (V_{dc})	800V
Output phase AC peak (V_{pk})	339V (415V L-L RMS)
Switching frequency (f_s)	20kHz
Line frequency (f_o)	50Hz

The proposed topology is compared with a conventional multi-stage solution (a PSFB isolated DC-DC converter cascaded with 3ϕ VSI through a interstage LC filter) and a single-stage topology presented in [16]. To perform a fair comparison, the converters are designed for a target application of grid integration of solar with the specification shown in Table III. The converters are modulated at the 85% of the maximum possible modulation index. In multi-stage, 3ϕ VSI is modulated with standard conventional space vector PWM (CSVPWM).

In all the three topologies the diode bridges are implemented with IXYS diode MEO 450-12DA (1200V,450A). In the proposed topology, SEMIKRON IGBT SKM450GB12T4 (1200V,450A) are considered for all active switches. In multi-stage topology all active switches are implemented using SKM450GB12T4. In [16], SEMIKRON IGBT SKM450GB12T4 (1200V,450A) are considered for the DSC switches $S_1 - S_2$ and the ASC switches $Q_{a1} - Q_{c2}$ [16]. The switches $S_{A1} - S_{C2}$ are implemented with SKM400GB125D (1200V,300A).

The comparison is summarised in Table IV. The table shows the number of passive and active semiconductors used,

TABLE IV
TOPOLOGY COMPARISON

		S.F	Multi-stage Topology	[16]	Proposed Topology
DSC	Switch count	—	4	8	6
	$V_{b,sw}$	V_{dc}	1	1	1
	$I_{RMS,sw}$	$\frac{P}{V_{dc}}$	$0.83(S_{1,2}), 0.77(S_{3,4})$	$1.06(S_{1,2}), 0.33(S_{A1-C2})$	0.64
	$I_{P,sw}$	$\frac{P}{V_{dc}}$	1.2	$1.57(S_{1,2}), 0.79(S_{A1-C2})$	1.36
ASC	switch count	—	6	6	6
	Diode count	—	4	12	12
	$V_{b,sw}$	V_{pk}	2.0	2.35	2.35
	$V_{b,D}$	V_{pk}	2.35	2.35	2.35
	$I_{RMS,sw}$	$\frac{P}{V_{pk}}$	0.327	0.334	0.334
	$I_{P,sw}$	$\frac{P}{V_{pk}}$	0.667	0.667	0.667
	$I_{RMS,D}$	$\frac{P}{V_{pk}}$	0.35	0.236	0.236
$I_{P,D}$	$\frac{P}{V_{pk}}$	0.5	0.67	0.67	
HFT	HFT count	—	1	3	3
	$I_{RMS,pri}$	$\frac{P}{V_{dc}}$	1.2	0.557	0.557
	$I_{RMS,sec}$	$\frac{P}{V_{pk}}$	0.5	0.334	0.334
	Area product	$\frac{P}{f_s J B_m K_w}$	0.5	0.242	0.242

their blocking voltage (V_b), peak (I_P) and RMS (I_{RMS}) current. S.F is the scaling factor. The proposed topology uses 6 active switches in the DSC. The multi-stage topology and the topology in [16] employ 4 and 8 numbers of active switches, respectively. The DSC switches in the proposed topology have lower RMS current compared to the multi-stage topology and [16]. In all the solutions, blocking voltage of DSC switches is same as input DC bus voltage.

In ASC, all the three topologies have 6 active switches with similar RMS current and blocking voltage. Number of diodes in the secondary of the proposed solution is 12, same as in [16]. These diodes also have similar blocking voltage and RMS current. The multi-stage topology has 4 diodes in the secondary with higher RMS current.

The proposed solution employs 3 high-frequency transformers (HFT), similar to the topology in [16] with same area product and winding RMS currents. The multi-stage solution has one HFT with twice area product and winding RMS currents compared to the proposed solution.

DSC and ASC losses of the three topologies are presented in

TABLE V
LOSS COMPARISON (SCALING FACTOR $\frac{P}{100}$)

		Multistage Topology	[16]	Proposed Topology
DSC	P_{CL}	0.445	0.71	0.47
	P_{SL}	0	0.01	0
ASC	P_{CL}	1.03	1.14	1.14
	P_{SL}	2.353	0	0

Table V where P_{CL} and P_{SL} are the conduction and switching loss respectively. The conduction loss of the DSC of proposed topology is comparable with multi-stage solution and is almost half compared to [16]. In the proposed and multi-stage topologies, ZVS turn ON is ensured for all DSC switches over complete line cycle. Hence, the turn ON switching loss of DSC is zero. The DSC in [16] has small but finite turn ON switching loss as $S_{A1} - S_{C2}$ [16] are hard-switched for small parts of line cycle. The conduction losses in ASC of all the three topologies are comparable. Due to line frequency switching of the ASC, the proposed topology and the topology in [16] have negligible switching loss. The conventional multi-stage solution has high switching loss compared to the proposed solution due to hard-switching of the ASC 3ϕ VSI. In the proposed converter, decoupling of switching frequency from power loss provides an opportunity to push the switching frequency high which results in smaller magnetics.

TABLE VI
FILTER SIZE COMPARISON USING THD

Filter	Multistage topology	[16]	Proposed topology
Input	0.42 (THD_I)	0.55 (THD_I)	0.498 (THD_I)
Output	0.69 (THD_V)	0.6 (THD_V)	0.7 (THD_V)
Intermediate DC Link	0.42 (THD_V , PSFB), 0.48 (THD_I , 3ϕ VSI)	-	-

The voltage and current THDs are measures of the converter filtering requirements [16]. The filtering requirements are compared in Table VI for the target specification. The input and output filter requirements are comparable in all the three topologies. But the multi-stage solution requires additional filter at the interconnection of the DC-DC and the 3ϕ VSI. Overall capacitive and inductive filter requirement in the multi-stage solution is high when compared with the proposed solution. Hence, from the filter requirement perspective, the proposed solution is cost effective and will result in higher power density.

VI. CONCLUSION

This paper presents a unidirectional, isolated, high power density DC- 3ϕ AC converter solution for grid integration of renewable sources. The proposed converter topology has the following key features. All active switches in DC side converter are zero voltage switched (ZVS) over the entire line cycle without additional snubber circuit. Hence the power loss of the high frequency switched DC side converter is reduced

significantly. In the paper, a detailed analysis is presented showing the converter operation over a switching cycle and the conditions on dead-time between the switch-pair of a half-bridge leg are derived to ensure ZVS turn ON. The modulation strategy ensures soft commutation of the secondary diode bridges. The AC side half-bridge legs are line frequency switched incurring negligible switching loss. The converter does not require any inter-stage DC link filter capacitor and thus reducing overall filtering requirements. The converter operation is experimentally verified on a 3.7 kW hardware prototype. Experimental results are presented to show ZVS transitions of the DC side half-bridge legs. An in-depth topology comparison is presented to show the advantages of the proposed topology over the conventional multi-stage topology and one existing single-stage topology.

APPENDIX

VOLTAGE STRESS ON SECONDARY DIODES AND SWITCHES CONSIDERING PARASITIC CAPACITANCES

In the switching analysis of the proposed topology we have not considered the secondary diode and switch parasitic capacitances. These capacitances have no role in active power transfer. Like in a PSFB converter, at the end of zero to active state transition, these capacitances resonate with the transformer leakage inductances and cause voltage overshoot across the secondary diodes and devices. What follows is a brief discussion on the voltage overshoot caused at the end of zero to active state transition (Mode 9) in the secondary circuit of phase u (see Fig. 27a). At the end of mode 9 (Fig. 16a), D_{u1}

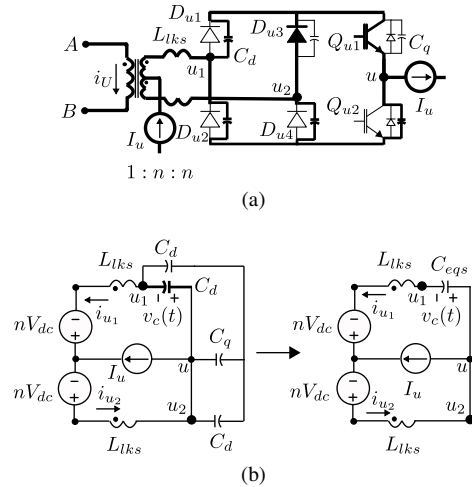


Fig. 27. (a) Secondary circuit of phase u after zero to active state transition (after Mode 9), (b) Equivalent Secondary circuit of phase u after zero to active state transition

stops conducting. The equivalent circuit is shown in Fig. 27b. In the circuit, secondary winding leakage inductances L_{lks} and diode (C_d) and device C_q capacitances are considered. The voltage across the diode D_{u1} , $v_c(t)$, starts ringing. By solving the equivalent circuit, $v_c(t)$ is given in (18).

$$v_c(t) = 2nV_{dc}(1 - \cos \omega_s t) \quad (18)$$

$$\text{Where } \omega_s = \frac{1}{\sqrt{2L_{lks}C_{eqs}}} \text{ and } C_{eqs} = \frac{3C_d^2 + 2C_qC_d}{C_q + 2C_d}.$$

Active [27], [28] or passive [29], [30] snubber suggested in the literature for PSFB can be used to mitigate the voltage stress. In the experimental set up, small RCD snubbers are used to reduce the voltage stress on the secondary diodes and devices.

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