A PWM ZVS High-Frequency-Link Three-Phase Inverter with T-type NPC Unfolder

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***Abstract*—In this paper a pulse width modulated (PWM) single-stage high frequency link (HFL) three-phase DC-AC converter is proposed for grid integration of solar and fuel cell based energy sources. On the DC side, the converter has three half-bridge legs which are zero-voltage switched (ZVS) over the entire line cycle without using any additional snubber circuit. On the AC side, two diode bridge rectifiers and one neutral point clamped (NPC) T-type three-level inverter are employed. The active switches in NPC inverter are switched either at line frequency or twice of it, incurring negligible switching loss. Modulation ensures soft commutation in the diode bridges. The intermediate three level DC bus is pulsating and does not require any DC filter capacitor and thus reduces overall filtering requirements. The high frequency galvanic isolation provides high power density, low cost converter solution. The converter operation is analysed in detail and verified on a 2 kW hardware prototype.**

***Index Terms*—Phase shift modulation, DC-AC power conversion, high frequency link, zero voltage switching, three-phase unfolder, NPC T-type three-level inverter, single-stage power conversion**

I. Introduction

SINGLE-stage high frequency link (HFL) DC-AC converters are becoming attractive solution for applications like grid integration of renewable energy sources [1]–[3], power train in electric and hybrid vehicle [4], battery based storage system [5], UPS [6] etc. These compact, high power density and low cost converters employ high frequency galvanic isolation instead of conventional line frequency transformers which are bulky and costly. These converters also avoid use of bulky interstage DC link filter capacitor and thus reduce overall filtering requirements and increase the system reliability.

The single-stage three-phase HFL inverter topologies discussed in literature can be broadly classified into two categories- resonant and PWM type. In [7], a three-phase bidirectional DC-AC converter is presented. It has two isolated dual-bridge series resonant converters (DBSRC) followed by a three-level unfolder. The dual bridge series resonant converter has following problems- high circulating current, load dependency of voltage gain and constant frequency duty modulation resulting in limited range of soft-switching [8]. To reduce tank current, [7] employs complex minimum current trajectory (MCT) technique. Small DC link filter capacitors are used to filter out the switching frequency components.

The PWM single-stage HFL converters are of two types- cyclo-converter type HFL (CHFL) [9]–[11] and rectifier type HFL (RHFL) [12], [13]. In a CHFL topology, high frequency (HF) AC is generated from DC input using H-bridge and is fed to HFT. In the secondary, cyclo-converter is used to get line frequency AC from HF AC. The operation of the cyclo-converter can be divided in two parts- first rectification of HF AC and then line frequency inversion [14]. In a RHFL topology, instead of using a cyclo-converter, a rectifier followed by a voltage source inverter (VSI) is used in the secondary. Here intermediate DC link is pulsating.

Unidirectional PWM RHFL DC-3ϕ AC converter topologies [15]–[20] are becoming popular in applications like grid integration of PV, fuel cell where the power flow is unidirectional (from source to grid). But in case of large scale PV plant, reactive power support with power factor $\pm$ 0.9/0.95 is essential at the grid end [21]. The unidirectional topologies can be broadly classified in two categories based on the ability to support limited amount (± 0.866 PF) of reactive power at the AC port.

In [15]–[18], the presented topologies can support upto ± 0.866 power factor load. These converters employ a hybrid modulation strategy. In [15]–[17], the AC side 3ϕ VSI is high frequency switched only for one third of the line cycle thus reducing the switching loss of the converter. In [15], the DC side high frequency inverter is also soft switched. In [18], the secondary has a three level NPC inverter where the active switches are high frequency switched for one sixth of the line cycle. The DC side converter is hard-switched and additional snubber circuits are used for transformer leakage energy commutation.

The topologies in [19], [20] can support only UPF load and require additional shunt compensator to support any reactive power demand by the load. Here all the active switches in the AC side are line frequency switched. But the high frequency switched DC side converters are partially soft-switched.

This paper introduces a unidirectional PWM high frequency link DC- 3ϕ AC converter (in Fig. 1) which can support upto $\pm$ 0.866 power factor operation. All active switches in the AC side NPC T-type three-level unfolder are low frequency (LF) switched, incurring negligible switching loss. Modulation strategy ensures zero voltage switching (ZVS) of all six active switches in the DC side bridge over complete line cycle without additional snubber. The proposed converter with suggested modulation scheme has following additional features. (i) PWM is implemented in the DC side bridge. (ii) The secondary diode bridges are soft commutated. (iii) Intermediate three level DC link is pulsating and does not

Manuscript received March 12, 2019; revised June 15, 2019 and August 22, 2019; accepted September 1, 2019. This work was supported by Department of Science and Technology, Government of India under the project titled “Development of an advanced System-On-Chip (SoC) based embedded controller for power electronic converters”. (*Corresponding author : Anirban Pal*).

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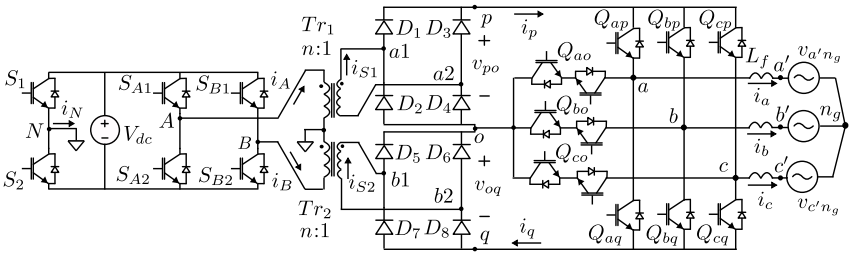


Fig. 1: Configuration of the proposed inverter

require any DC filter capacitor. (iv) High frequency galvanic isolation results in compact, low cost converter solution.

The organisation of this paper is as follows. The converter structure is described in section II. In section III modulation strategy is discussed. The steady state operation of the converter over a switching cycle along with soft-switching conditions are presented in section IV. Key experimental results are presented in section V. Converter power loss and measured efficiency are shown in section VI. Topology comparison is presented in section VII.

II. Proposed Inverter

The proposed inverter is shown in Fig. 1. In the DC side converter (DSC), a full bridge, $S_{A1}-S_{B2}$ along with a half bridge leg, S_1-S_2 are employed. The output of the full-bridge ($S_{A1}-S_{B2}$) is fed to two high frequency transformers (HFT), Tr_1 and Tr_2 with turns ratio $n:1$. The primary windings of Tr_1 and Tr_2 are connected in series and the common point is shorted with the pole (N) of S_1-S_2. The secondary windings of Tr_1 and Tr_2 are connected to two diode-bridge rectifiers D_1-D_4, D_5-D_8 respectively. The output terminals of the diode-bridges are connected in series. A three-level T-type neutral point clamp (NPC) 3ϕ inverter is used to generate the line frequency AC voltages from the rectifier output. The converter is connected to a balanced 3ϕ voltage source through filter inductors L_f as shown in Fig. 1.

III. Modulation Strategy

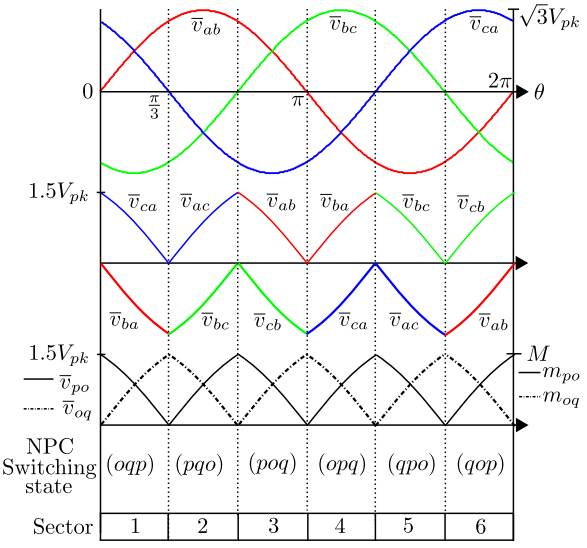


Fig. 2: Switching states of NPC inverter

The pole a can be connected to the nodes p, o and q through the NPC inverter leg a (Q_{ap}, Q_{ao}, Q_{aq}) (see Fig. 1). The switching state of the NPC inverter, (pqo), implies

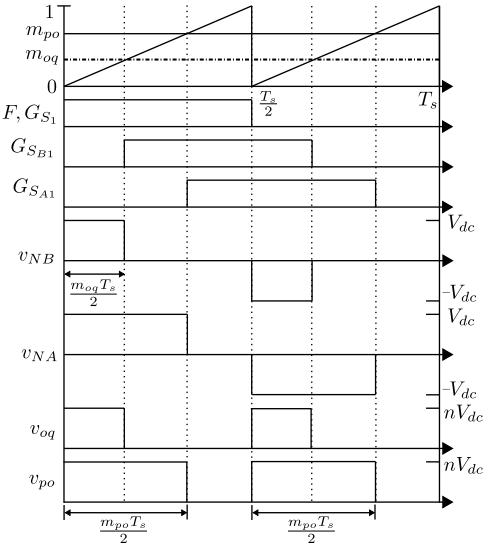


Fig. 3: Modulation of DC side bridge

leg a is connected to p, leg b to q and leg c to o, i.e. Q_{ap}, Q_{bq}, Q_{co} are ON. To generate balanced three-phase average line to line voltages, $\overline{v}_{ab} = \sqrt{3}V_{pk}\sin(\omega_o t{=}\theta)$, $\overline{v}_{bc} = \sqrt{3}V_{pk}\sin\left(\theta - \frac{2\pi}{3}\right)$ and $\overline{v}_{ca} = \sqrt{3}V_{pk}\sin\left(\theta + \frac{2\pi}{3}\right)$ with angular frequency $\omega_o = \frac{2\pi}{T_o}$, the operation of the converter is divided into six equal sectors over a line cycle, ($\theta \in [0, 2\pi]$), as shown in Fig. 2. In each sector, the two line-line voltages with non-maximum magnitudes are plotted with respect to (w.r.t) a common phase (see Fig. 2) e.g. $\overline{v}_{ac}$ and $\overline{v}_{bc}$ in sector 2. Here c is the common phase and w.r.t c, $\overline{v}_{ac} > 0$ and $\overline{v}_{bc} < 0$. In sector 2, the average rectifier output voltages are $\overline{v}_{po} = \overline{v}_{ac}$ and $\overline{v}_{oq} = -\overline{v}_{bc}$ as shown in Fig. 2. Hence, in this sector, the common phase c should be connected to node o and phase a and b should be connected to nodes p and q respectively through the NPC inverter legs. Thus the switching state of the NPC inverter in sector 2 is (pqo). Similarly, the switching states in other sectors can be obtained and are shown in Fig. 2. As the switching states are changed at the beginning of each sector and remain same throughout a sector, the NPC inverter is low frequency switched incurring negligible switching loss. Following the switching states, two quadrant switches ($Q_{ap}-Q_{cq}$) are line frequency switched and the four quadrant switches ($Q_{ao}-Q_{co}$) are switched at twice of the line frequency.

The DSC is phase shift modulated (PSM) to generate average rectifier output voltages $\overline{v}_{po} = \frac{m_{po}V_{dc}}{n}$ and $\overline{v}_{oq} = \frac{m_{oq}V_{dc}}{n}$. m_{po} and m_{oq} are the modulation signals as shown in

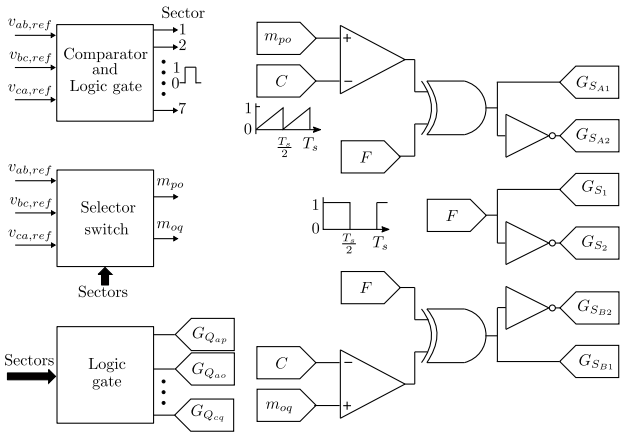


Fig. 4: Control circuit of the converter

Fig. 2 with peak $M = \dfrac{1.5nV_{pk}}{V_{dc}}$. The modulation strategy over a switching cycle T_s is shown in Fig. 3. F is a high frequency (HF) square wave signal with period T_s and 50% duty ratio. T_s is considered to be flux balance cycle of the HFTs. A unity magnitude, unipolar saw-tooth carrier (C) with period $\dfrac{T_s}{2}$, aligned with F is considered. Two switches in each half-bridge leg of the DSC are complementary switched with a dead time to avoid short circuit of the DC source, V_{dc}. F is assigned to be the gating signal of S_1, G_{S_1}. The modulation signals m_{po} and m_{oq} are compared with the saw-tooth carrier to generate the gating signals of $S_{A1} - S_{A2}$ and $S_{B1} - S_{B2}$ respectively. Slowly varying modulation signals are approximated as constant over a switching cycle T_s. The gating signal of S_{A1}, $G_{S_{A1}}$ is (a square wave with period T_s and 0.5 duty ratio) phase shifted by $\dfrac{m_{po}T_s}{2}$ w.r.t F. Similarly, the gating signal of S_{B1}, $G_{S_{B1}}$ is phase shifted by $\dfrac{m_{oq}T_s}{2}$ w.r.t F as shown in Fig. 3. The suggested modulation strategy generates pulse width modulated (PWM) high frequency AC voltages v_{NA} and v_{NB} with voltage levels $\pm V_{dc}$ and 0 which are fed to Tr_1 and Tr_2 respectively. In the secondary, the diode bridges $D_1 - D_4$ and $D_5 - D_8$ rectify the high frequency AC and generate pulsating DC voltages v_{po} and v_{oq} with required average $\overline{v}_{po}$, $\overline{v}_{oq}$ respectively. The control circuit of the proposed converter is shown in Fig. 4. The controller gives the three phase reference voltage signals $v_{ab,ref} = \frac{\overline{v}_{ab}}{\frac{V_{dc}}{n}}$, $v_{bc,ref}$ and $v_{ca,ref}$. Using the reference voltages, the sector signals can be generated. Using sector informations and voltage references, gating pulses of NPC inverter and the modulations signals m_{po} and m_{oq} are obtained. The gating signals of the DSC are generated by employing comparators and logic gates as shown in Fig. 4.

Fig. 5 shows the properly filtered, ripple free line currents $i_a = I_{pk}\sin\left(\theta - \dfrac{\pi}{6}\right)$, $i_b = I_{pk}\sin\left(\theta - \dfrac{5\pi}{6}\right)$ and $i_c = I_{pk}\sin\left(\theta + \dfrac{\pi}{2}\right)$ for unity power factor (UPF) operation of the converter. i_p and i_q are the output currents of the rectifiers $D_1 - D_4$ and $D_5 - D_8$ respectively at UPF operation. Following the NPC inverter switching state in sector 2 $\left(\dfrac{\pi}{3} \le \theta \le \dfrac{2\pi}{3}\right)$,

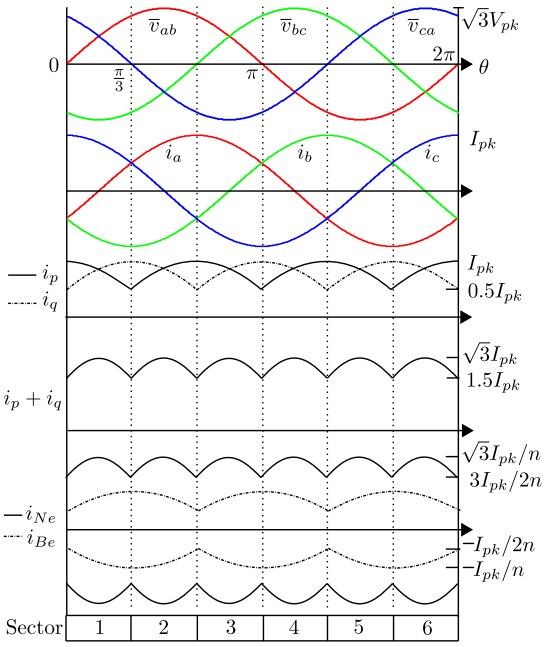


Fig. 5: Converter current waveforms at UPF operation

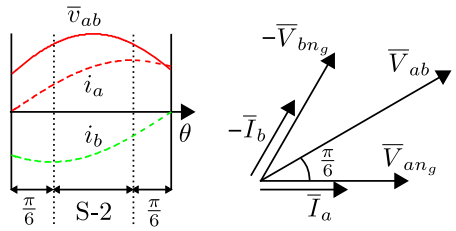


Fig. 6: Phasor diagram at UPF operation

$i_p = i_a = I_{pk}\sin\left(\theta - \dfrac{\pi}{6}\right)$ and $i_q = -i_b = I_{pk}\sin\left(\theta + \dfrac{\pi}{6}\right)$. Similarly, in other sectors i_p and i_q can be defined. As seen in Fig. 5, i_p and i_q have maximum values of $I_{pq_{max}} = I_{pk}$ and minimum values of $I_{pq_{min}} = 0.5I_{pk}$. Fig. 5 also shows the waveform of $(i_p + i_q)$ with maximum value $I_{(p+q)_{max}} = \sqrt{3}I_{pk}$ and minimum value $I_{(p+q)_{min}} = 1.5I_{pk}$ respectively.

Due to diode bridges, i_p and i_q have to be positive instantaneously, in each sector. Let us consider sector 2, where $i_p = i_a$ and $i_q = -i_b$. $\overline{V}_{ab}$, $\overline{V}_{an_g}$, $\overline{V}_{bn_g}$, $\overline{I}_a$ and $\overline{I}_b$ are the phasor quantities of $\overline{v}_{ab}$, $\overline{v}_{an_g}$, $\overline{v}_{bn_g}$, i_a and i_b respectively. As seen in Fig. 6, in sector 2 (S-2), i_p becomes negative, if i_a lags more than 30° and $i_q < 0$, if i_b leads more than 30°. Which cannot be supported by the diode bridges. Due to waveform symmetry, similar observations can be made in other sectors also. Thus the converter can support upto ±30° leading and lagging power factor operation.

IV. Steady State Operation and Soft-Switching

The converter operation at UPF, over one switching cycle T_s, is described in detail when the converter is in sector 1. In other sectors, similar switching strategy is followed. In the analysis, DSC device capacitances (C_s) and the leakage inductances (seen from primary) L_{lk_1}, L_{lk_2} of Tr_1 and Tr_2 respectively are considered. Considering the leakage inductances of the transformers are of same order, $L_{lk_1} \simeq L_{lk_2} = L_{lk}$. The DSC active switches are zero voltage switched (ZVS) over complete line cycle (T_o). ZVS is achieved using C_s

and L_{lk}. Following the switching state in sector 1, the NPC inverter switches Q_{ao}, Q_{bq} and Q_{cp} are kept ON (see Fig. 2). Hence, $i_p = i_c = I_{pk}\cos\theta$ and $i_q = -i_b = I_{pk}\sin\left(\theta + \frac{\pi}{6}\right)$. As the switching state of the NPC inverter remains same over the sector, it can be replaced by two current sinks I_p and I_q at the rectifier output stage (see Fig. 8a). I_p and I_q are the rectifier output currents, i_p, i_q, respectively, over T_s and can be considered as constant current sinks, if $i_{a,b,c}$ are properly filtered with negligible ripple. In the following analysis $I_p > I_q$ is considered ($\theta \in [0, \frac{\pi}{6}]$). Thus $m_{po} > m_{oq}$ as seen in Fig. 2. The analysis will be similar in the other half of the sector 1, when $I_p < I_q$. What follows is a detailed description of the switching process of the DC side bridge and current commutation of AC side diode bridges in one half of the switching cycle. In the other half cycle, circuit evolves in similar fashion. Fig. 7 presents key waveforms during switching transitions.

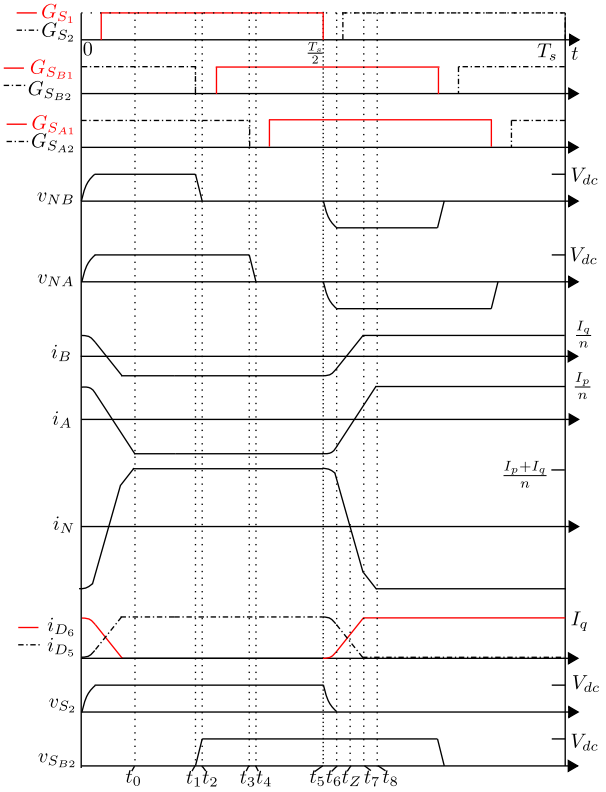


Fig. 7: Important switching waveforms over T_s

A. Mode I ($t_0 < t < t_1$ Fig. 8)

S_1, S_{A2} and S_{B2} are conducting in the DSC. V_{dc} is applied across HFT primary terminals NA and NB. In the secondary, D_2, D_3 and D_5, D_8 are conducting I_p and I_q respectively. Reflected transformer primary currents $i_{A,B}$ are shown in Fig. 7. $i_A = -\frac{I_p}{n}$, $i_B = -\frac{I_q}{n}$ and $i_N = \frac{I_p + I_q}{n}$. Equivalent circuit is shown in Fig. 8b. The voltage polarity and current directions indicate the active power transfer from DC source to load through both the transformers and diode bridges.

B. Mode II ($t_1 < t < t_2$ Fig. 9)

At t_1, S_{B2} is turned OFF. Due to C_s voltage across S_{B2} changes slowly which reduces turn OFF loss. i_B starts charging the capacitance across S_{B2} and discharging the capacitance

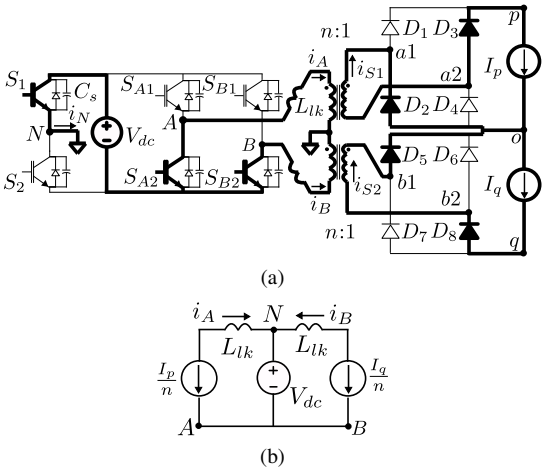


Fig. 8: Mode I-(a) circuit diagram, (b) equivalent circuit

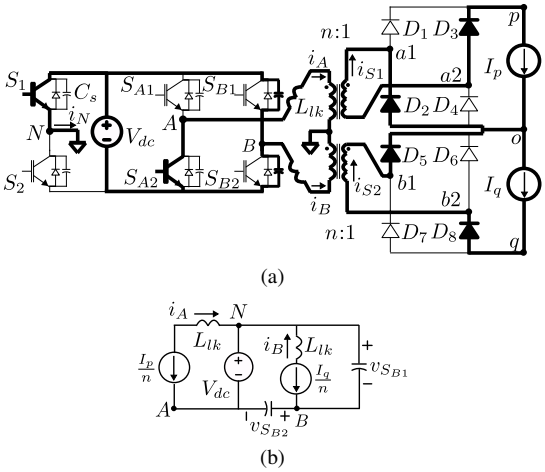


Fig. 9: Mode II-(a) circuit diagram, (b) equivalent circuit

across S_{B1}. The equivalent circuit is shown in Fig. 9b. The voltage dynamics across $S_{B1} - S_{B2}$ can be described by (1).

$$\begin{aligned} v_{S_{B1}} &= V_{dc} - \frac{I_q}{2nC_s}(t - t_1) \\ v_{S_{B2}} &= \frac{I_q}{2nC_s}(t - t_1) \end{aligned} \tag{1}$$

At t_2, $v_{S_{B1}} = 0$. The anti-parallel diode across S_{B1} is forward biased.

C. Mode III ($t_2 < t < t_3$ Fig. 10)

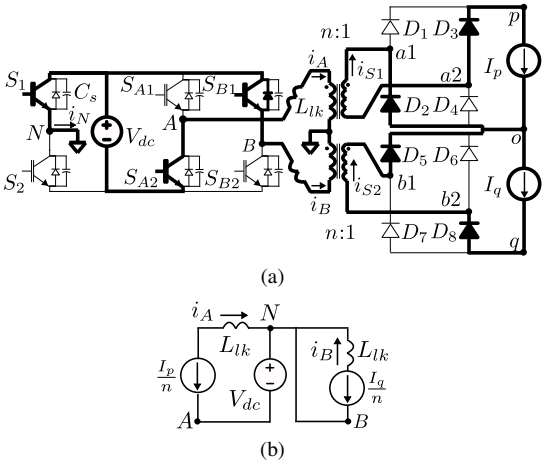


Fig. 10: Mode III-(a) circuit diagram, (b) equivalent circuit

The anti-parallel diode of S_{B1} is conducting. The primary terminals N, B of Tr_2 is shorted. In this mode, no active power is transferred from source to load through Tr_2 and the diode bridge $D_5 - D_8$. The voltage across NA is V_{dc}. Active power is transferred from source to load trough Tr_1 and diode bridge $D_1 - D_4$. Equivalent circuit is shown in Fig. 10b. Gating pulse of S_{B1} is applied in this mode to achieve ZVS turn ON of S_{B1} when the anti-parallel diode is conducting. To achieve ZVS turn ON of S_{B1} the dead time (DT_B) between the gating signals of $S_{B1} - S_{B2}$ is given in (2).

$$DT_B \geq \frac{2nC_sV_{dc}}{I_q} \tag{2}$$

$\frac{2nC_sV_{dc}}{I_q}$ is maximum when I_q is minimum i.e. $I_q = I_{pq,min} = 0.5I_{pk}$ at $\theta = 0$. So, to achieve ZVS turn ON through out the line cycle $DT_B \geq \frac{2nC_sV_{dc}}{I_{pq,min}} = \frac{4nC_sV_{dc}}{I_{pk}}$.

D. Mode IV ($t_3 < t < t_4$)

At t_3, S_{A2} is turned OFF. Due to device capacitance the voltage across S_{A2} changes slowly thus reduces turn OFF loss. In this mode the circuit dynamics is similar as discussed in Mode II. At the end of this mode the anti-parallel diode of S_{A1} is forward biased.

E. Mode V ($t_4 < t < t_5$ Fig. 11)

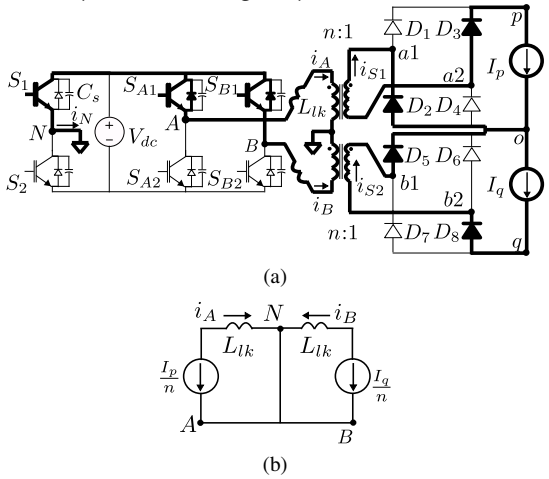


Fig. 11: Mode V-(a) circuit diagram, (b) equivalent circuit

After t_4, the anti-parallel diode of S_{A1} is conducting. Now both transformer primaries are shorted by S_1 and anti-parallel diodes of $S_{A1,B1}$. The converter is in zero state and no active power is transferred from DC source to load. The equivalent circuit is shown in Fig. 11b. Gating signal of S_{A1} is applied in this state to ensure ZVS turn ON. Like $S_{B1} - S_{B2}$, dead time between the gating signals of $S_{A1} - S_{A2}$ should be $DT_A \geq \frac{4nC_sV_{dc}}{I_{pk}}$.

F. Mode VI ($t_5 < t < t_6$ Fig. 12)

At t_5, S_1 is turned OFF. The device capacitance helps to reduce turn OFF loss by slowing down the rise of voltage across S_1. The pole current i_N starts charging the capacitance across S_1 and discharging the capacitance across S_2. Appeared voltage polarity across NA and NB forward bias D_1, D_4 and D_6, D_7. Secondary windings of Tr_1 and Tr_2 are shorted

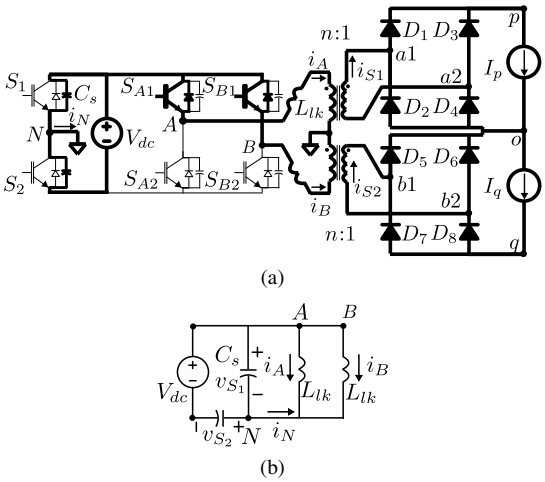


Fig. 12: Mode VI-(a) circuit diagram, (b) equivalent circuit

through diode bridges. The equivalent circuit is shown in Fig. 12b. The transition can be described by (3).

$$\begin{aligned} &i_A + i_B + i_N = 0 \\ &v_{S_1} + v_{S_2} = V_{dc} \\ &C_s(dv_{S_1}/dt - dv_{S_2}/dt) = i_N \\ &v_{S_1} = L_{lk}\frac{di_A}{dt} = L_{lk}\frac{di_B}{dt} \end{aligned} \tag{3}$$

Equation (3) is solved with initial conditions $v_{S_1}(t_5) = 0$, $i_N(t_5) = \frac{(I_p + I_q)}{n}$, $i_A(t_5) = -\frac{(I_p)}{n}$ and $i_B(t_5) = -\frac{(I_q)}{n}$. The voltage across S_1, v_{S_1} and currents are given in (4).

$$\begin{aligned} v_{S_1}(t) &= \frac{\omega_r L_{lk}}{2n}(I_p + I_q)\sin\omega_r(t - t_5) \\ i_N(t) &= \frac{(I_p + I_q)}{n}\cos\omega_r(t - t_5) \\ i_A(t) &= -\frac{I_p}{n} + \frac{I_p + I_q}{2n}(1 - \cos\omega_r(t - t_5)) \\ i_B(t) &= -\frac{I_q}{n} + \frac{I_p + I_q}{2n}(1 - \cos\omega_r(t - t_5)) \end{aligned} \tag{4}$$

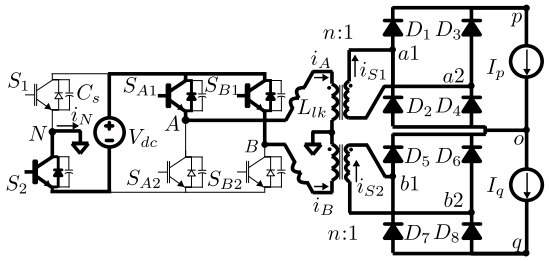
Where $\omega_r = \frac{1}{\sqrt{L_{lk}C_s}}$. This mode ends at t_6 when $v_{S_1} = V_{dc}$ and $v_{S_2} = 0$. From (4), to completely charge C_s across S_1 to V_{dc}, following condition needs to be satisfied- $(I_p + I_q) \geq \frac{2nV_{dc}}{\omega_r L_{lk}}$. Otherwise, the circuit enters into a resonating oscillation mode and results in hard turn ON of S_2. As seen in Fig. 5, the minimum value of $(I_p + I_q)$ over a line cycle is $I_{(p+q),min} = 1.5I_{pk}$. So, the condition on I_{pk} is given in (5).

$$I_{pk} \geq \frac{4nV_{dc}}{3\omega_r L_{lk}} \tag{5}$$

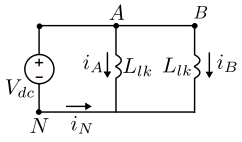
G. Mode VII ($t_6 < t < t_7$ Fig. 13)

After t_6, the anti-parallel diode across S_2 starts conducting i_N. To achieve ZVS ON, gating pulse of S_2 is applied when the anti-parallel diode is conducting. The dead time DT_N between the gating pulses of $S_1 - S_2$ should satisfy (6).

$$DT_N \geq (t_6 - t_5)_{max} = \frac{1}{\omega_r}\sin^{-1}\left(\frac{4nV_{dc}}{3\omega_r L_{lk} I_{pk}}\right) \tag{6}$$



(a)



(b)

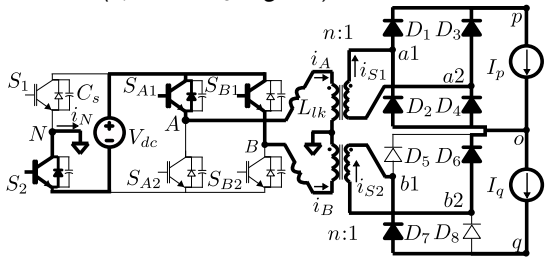
Fig. 13: Mode VII-(a) circuit diagram, (b) equivalent circuit

The equivalent circuit in this mode is shown in Fig. 13b. The primary currents, i_A and i_B are changed linearly. $i_{A,B,N}$ are given in (7).

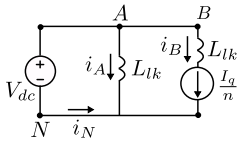
$$\begin{aligned} i_A &= i_A(t_6) - \frac{V_{dc}}{L_{lk}}(t - t_6) \\ i_B &= i_B(t_6) - \frac{V_{dc}}{L_{lk}}(t - t_6) \\ i_N &= i_N(t_6) - \frac{2V_{dc}}{L_{lk}}(t - t_6) \end{aligned} \tag{7}$$

In the secondary, current changes linearly between diode pairs $(D_{1,4})$, $(D_{2,3})$ and $(D_{5,8})$, $(D_{6,7})$. Current through D_5 and D_6 are shown in Fig. 7. As S_2, $S_{A1,B1}$ are ON, i_A, i_B and i_N can change their direction and build up in the opposite directions. At t_7, when $i_B = \frac{I_q}{n}$, this mode ends.

H. Mode VIII ($t_7 < t < t_8$ Fig. 14)



(a)



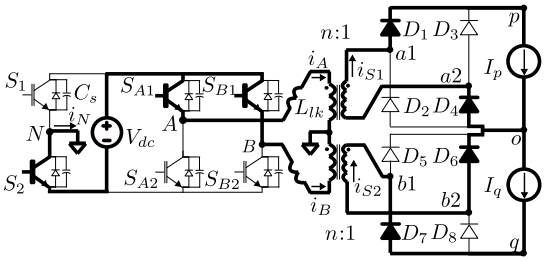
(b)

Fig. 14: Mode VIII-(a) circuit diagram, (b) equivalent circuit

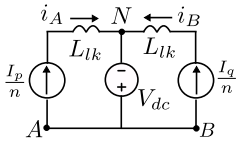
D_5 and D_8 are reverse biased and stop conducting whereas D_6 and D_7 are conducting I_q. The equivalent circuit is shown in Fig. 14b. i_A and i_N changes linearly with slope $\frac{V_{dc}}{L_{lk}}$. At t_8, $i_A = \frac{I_p}{n}$, $i_N = -\frac{I_p + I_q}{n}$ and this mode ends.

I. Mode IX ($t_8 < t < t_9$ Fig. 15)

After t_8, D_2, D_3 are reverse biased. D_1 and D_4 conduct I_p. In the primary, S_2, S_{A1} and S_{B1} are conducting. The converter is in next active state. Active power is transferred from DC source to load through both the transformers and the diode bridges. The equivalent circuit is shown in Fig. 15b. The circuit condition is similar as in $Mode\ I$.

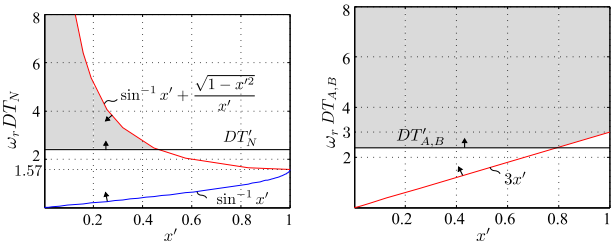


(a)



(b)

Fig. 15: Mode IX-(a) circuit diagram, (b) equivalent circuit



(a) (b)

Fig. 16: (a) ZVS bound of leg N (b) ZVS bound of leg A, B

J. Estimation of ZVS bounds of the DSC

During the switching transitions of leg A and B, the pole currents $i_{A,B}$ do not change direction. Whereas the pole current i_N changes its direction during the switching transition of $S_{1,2}$. Which puts a strict upper limit on dead time (DT_N) to achieve ZVS turn ON of $S_{1,2}$. What follows is a procedure to find out the upper limit of DT_N. Let, $R = \frac{nV_{dc}}{I_{pk}}$, $R_o = \sqrt{\frac{L_{lk}}{C_s}}$ and $x' = \frac{4R}{3R_o}$. As in Fig.7, at t_5, $i_N(t_5) = \frac{I_p + I_q}{n}$. The minimum value of $I_p + I_q$ is $1.5I_{pk}$ (at $\theta = 0$ and $\frac{\pi}{3}$ in sector 1, Fig. 5). Hence $i_N(t_5)_{min} = \frac{1.5I_{pk}}{n}$. Using (4), $i_N(t_6)_{min} = \frac{1.5I_{pk}}{n}\sqrt{(1 - x'^2)}$. It can be shown that, i_N falls to zero at t_Z with a slope $\frac{2V_{dc}}{L_{lk}}$. Hence, $(t_Z - t_6)_{min} = \frac{L_{lk}}{2V_{dc}} i_N(t_6)_{min} = \frac{1}{\omega_r}\frac{\sqrt{1-x'^2}}{x'}$. From (6), at $\theta = 0$ and $\frac{\pi}{3}$ in sector 1, $(t_6 - t_5) = \frac{1}{\omega_r}\sin^{-1} x'$, which is also the lower limit of DT_N. Hence, at $\theta = 0$ and $\frac{\pi}{3}$, $(t_Z - t_5) = (t_6 - t_5) + (t_Z - t_6)_{min} = \frac{1}{\omega_r}\sin^{-1} x' + \frac{1}{\omega_r}\frac{\sqrt{1-x'^2}}{x'}$. Combining (6), the limits on DT_N is expressed as (8) and is shown in Fig.

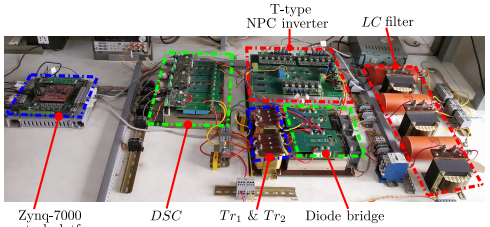


Fig. 17: Hardware prototype

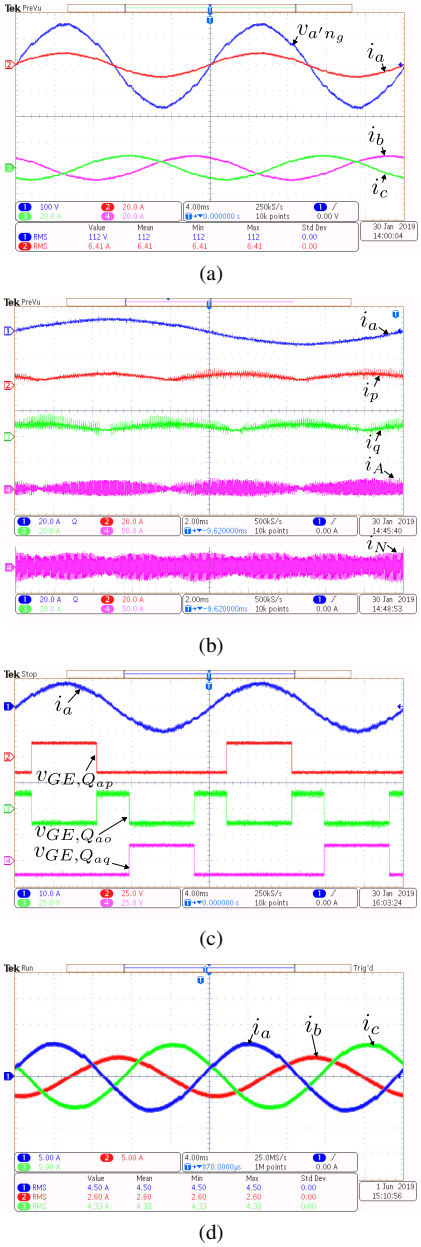


Fig. 18: (a) UPF operation- [CH1] $v_{a'n_g}$ (100V/div.), [CH2]-[CH4]: line currents (20A/div.). (b) [CH1]-[CH4]: i_a, i_p, i_q (20A/div.), DSC pole currents $i_{A,N}$ (50A/div.) . (c) Line switching of NPC leg- [CH1] i_a (20A/div.), [CH2]-[CH4]: Gate-emitter voltages of Q_{ap}, Q_{ao}, Q_{aq} (25V/div.). (d) Unbalance operation- [CH1]-[CH3]: i_a, i_b and i_c (5A/div.).

16a. DT'_N is device technology imposed minimum required dead time. When $x' << 1$, $DT_N \leq \frac{1}{\omega_r x'} = \frac{0.75 I_{pk} L_{lk}}{n V_{dc}}$. Similarly, the lower limit of the dead times of leg $A-B$, ($DT_{A,B} \geq \frac{4nC_s V_{dc}}{I_{pk}}$) is given in (8) and is shown in Fig. 16b. $DT'_{A,B}$ is the minimum dead time requirement imposed by the device technology.

$$\sin^{-1} x' \leq \omega_r DT_N \leq \sin^{-1} x' + \frac{\sqrt{1-x'^2}}{x'} \qquad (8)$$
$$\omega_r (DT_{A,B}) \geq 3x'$$

In this section, the soft-switching conditions of the DSC are derived for UPF operation of the converter. At UPF, soft-switching can be achieved for all the switches of the DSC over the complete line cycle. Similar conditions can be derived for other power factor operation. It can be shown that at $\pm 30°$ PF operation, soft turn ON of $S_1 - S_2$ can be achieved over the

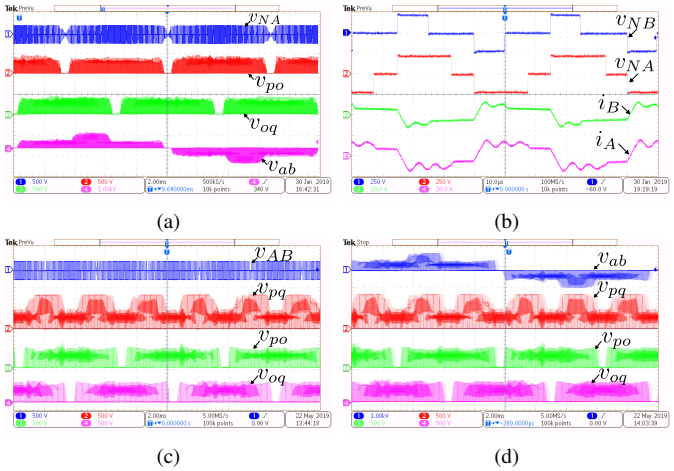


Fig. 19: (a) [CH1] HFT primary voltage- v_{NA}, rectifier output voltages- [CH2] v_{po}, [CH3] v_{oq} (500V/div), [CH4] NPC inverter pole voltage- v_{ab} (1kV/div.). (b) Waveforms over switching cycle- [CH1]-[CH2]: v_{NB}, v_{NA} (250V/div.) and [CH3]-[CH4]: i_B, i_A (20A/div.). (c) [CH1] v_{AB}, [CH2]-[CH4]: v_{pq}, v_{po}, v_{oq} (500V/div). (d) [CH1] v_{ab} (1kV/div)., [CH2]-[CH4]: v_{pq}, v_{po}, v_{oq} (500V/div).

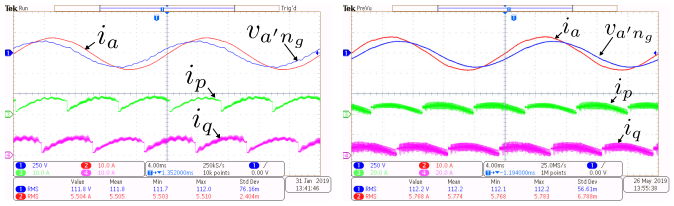


Fig. 20: (a) Non UPF operation (PF-0.89 lagging)- [CH1]: $v_{a'n_g}$ (250V/div.), [CH2]-[CH4]: i_a, i_p and i_q (10A/div.), (b) Non UPF operation (PF-0.896 leading)- [CH1]: $v_{a'n_g}$ (250V/div.), [CH2]-[CH4]: i_a, i_p and i_q (10A/div.)

complete line cycle whereas $S_{A1} - S_{B2}$ are hard-switched in some small durations of the line cycle.

The above discussion shows the switching process of the converter in one half of the switching cycle T_s in sector 1. In next half of the switching cycle, similar switching sequences are followed with other symmetrical switches. In other sectors, though the switching states of the NPC inverter will change, still the NPC inverter can be modelled as two current sources I_p and I_q connected across the rectifier outputs. So, similar circuit dynamics as discussed above, will be observed through out the line cycle.

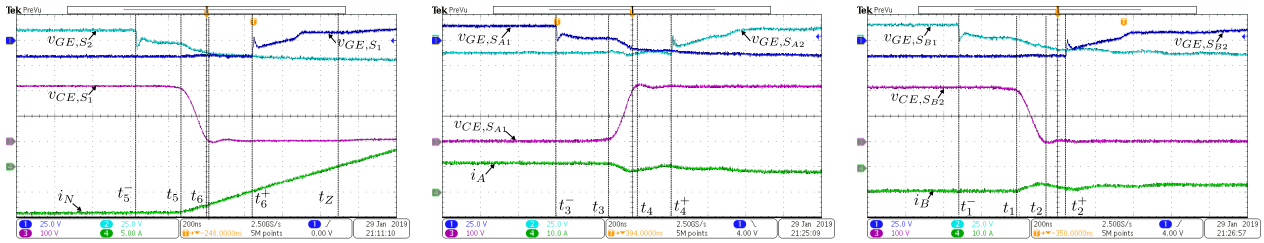
V. Experimental Results

A. Setup and operating condition

TABLE I: Operating condition

Output power (P)	2.15kW
DC input (V_{dc})	230V
HFT turns ratio (n)	3/4
L-L peak voltage ($\sqrt{3}V_{pk}$)	270V
Switching frequency ($f_s = \frac{1}{T_s}$)	20kHz
Line frequency ($f_o = \frac{\omega_o}{2\pi}$)	50Hz

The operation of the converter discussed so far is experimentally verified in a 2kW hardware prototype. The experimental hardware is shown in Fig. 17. Table I presents the operating condition. The active switches in DSC are implemented with 1200V, 75 A SEMIKRON IGBT modules and are switched at 20kHz. IXYS 1200V, 75A diode modules



(a) (b) (c)

Fig. 21: Switching transition waveforms- (a) Turn OFF of S_2 and turn ON of S_1. (b) Turn OFF of S_{A1} and turn ON of S_{A2}. (c) Turn OFF of S_{B1} and turn ON of S_{B2}.

MEE 75-12 DA are used in the secondary rectifiers. The NPC inverter is implemented with INFINEON IKW40N120H3 discrete IGBTs (1200V, 40A). Optically isolated gate drivers ACPL-339J are used to drive all the IGBTs with gate-emitter voltage levels $\pm 15V$. The dead-time provided between two active switches in a leg of DSC is 600 ns which satisfies all the dead-time limits derived in last section. An overlap time of 800ns is provided between two consecutive gating signals of the NPC inverter. The turns ratio of Tr_1 and Tr_2 are selected as $51:68$. EPCOS ferrite E cores (E80/38/20) are used. The leakage inductances seen from primary of Tr_1 and Tr_2 are 6.5 μH and 5.3 μH respectively. Additional series inductance of 36 μH is connected in series with each primary winding to achieve soft-switching of the DSC and hence $L_{lk} \simeq 42\mu$H. 2.5 mH inductance is used as line filter (L_f) at the converter output. Xilinx Zynq-7010 based control platform is used to implement the modulation strategy.

B. Verification of modulation strategy

The converter is connected to a balanced 3ϕ voltage source $v_{(a'b'c')n_g}$ with line-line peak ($\sqrt{3}V_{pk}$) 270V. The input DC supply is 230 V. Fig. 18a presents the UPF operation of the converter with an output power (P) of 2.15 kW. The phase voltage $v_{a'n_g}$ and line current i_a are in same phase as seen in Fig. 18a. The peak of the line current $I_{pk} = \dfrac{2P}{3V_{pk}} = 9.1$ A. 3ϕ balanced line currents $i_{a,b,c}$ are shown in Fig. 18a.

The rectifier output currents i_p, i_q and DSC pole currents i_A and i_N are shown in Fig. 18b over a line cycle. i_p and i_q have the peak of 9.1 A (I_{pk}) and the experimental waveforms are matched as shown in Fig. 5. The envelope of i_A and i_N have peak values of $\dfrac{\sqrt{3}I_{pk}}{n} = 21$A and $\dfrac{3I_{pk}}{2n} = 18.2$A respectively. Experimentally obtained envelops of i_A and i_N are similar to what is analytically predicted in Fig. 5.

Fig. 18c presents the line current i_a and gate emitter voltages of Q_{ap}, Q_{ao} and Q_{aq} of the NPC inverter. Q_{ap} and Q_{aq} are switched at line frequency (50 Hz) whereas Q_{ao} are switched at twice of the line frequency. This result verifies the low frequency switching strategy of NPC inverter.

Experimental result of the converter supporting unbalanced load is shown in Fig. 18d. The three phase unbalanced line currents ($i_a - i_c$) have peak values of 6.36A, 3.68A and 6.12A respectively. The Phase angles between $i_{a,b}$, $i_{b,c}$ and $i_{c,a}$ are 116°, 102° and 142° respectively.

Fig. 19a shows the pulse width modulated high frequency AC (v_{NA}) applied across Tr_1 primary. The voltage levels of v_{NA} are ± 230 V and 0. The rectifier output voltages v_{po} and v_{oq} are shown in [CH2] and [CH3] respectively. The pulsating v_{po} and v_{oq} have voltage levels $\dfrac{V_{dc}}{n} = 307$ V and 0. Thus Fig. 19a verifies pulsating intermediate DC link without any capacitor. In [CH4], the NPC inverter pole voltage v_{ab} is shown. v_{ab} has steady state voltage levels- ± 307 V (V_{dc}/n), ± 614 V ($2V_{dc}/n$) and 0.

The primary voltages ($v_{NA,NB}$) and currents ($i_{A,B}$) of Tr_1 and Tr_2 are shown in Fig. 19b. This result verifies the transformer voltage and current waveforms presented in Fig. 7. Transformer flux balance is achieved over one switching cycle. From the figure, across the primary windings, 0 to $\pm V_{dc}$ transitions happen simultaneously in both the transformers. At these instants, $S_1 - S_2$ are switched and $i_{A,B}$ change directions. But $\pm V_{dc}$ to 0 transitions are not synchronised.

Fig. 19c shows the pulse width modulated high frequency AC voltage, v_{AB}. The voltage levels of v_{AB} are ± 230 V and 0. The secondary DC link voltage v_{pq} is shown in [CH2]. The pulsating v_{pq} has voltage levels $\dfrac{2V_{dc}}{n} = 614$ V, $\dfrac{V_{dc}}{n} = 307$ V and 0 V. The rectifier output voltages v_{po} and v_{oq} are shown in [CH3] and [CH4] respectively.

Fig. 19d shows the pulse width modulated pole voltage, v_{ab}. v_{ab} has steady state voltage levels- ± 307 V (V_{dc}/n), ± 614 V ($2V_{dc}/n$) and 0. v_{pq}, v_{po} and v_{oq} are shown in [CH2]-[CH4] respectively.

Fig. 20a shows the lagging power factor operation of the proposed converter. From the figure, i_a lags $v_{a'n_g}$ by 26.7°. The converter is supplying $\cos 26.7° = 0.89$ lagging power factor load. This figure also shows rectifier output currents i_p and i_q and they are positive over the line cycle. The converter operation supplying 0.896 power factor leading load is shown Fig. 20b. The line current i_a leads the output voltage by 26.4°. The rectifier output currents i_p and i_q are shown in Fig. 20b.

C. Verification of soft-switching of the DSC legs

In the following discussion turn ON transitions of S_1, S_{A2} and S_{B2} and turn OFF of S_2, S_{A1} and S_{B1} are described.

Fig. 21a shows the switching transition of leg $S_1 - S_2$. S_2 was ON and conducting pole current i_N. S_1 was blocking $v_{CE,S_1} = V_{dc}$. At t_5^-, the gating pulse of S_2 is withdrawn. After sometime at t_5, voltages across $S_1 - S_2$ start changing. Slow change in voltage across S_2 due to device capacitance helps to reduce turn OFF loss of S_2. During this time i_N changes as per (4) in Mode VI of section IV. At t_6, $v_{CE,S_1} = 0$ and after that i_N changes linearly as per (7) in Mode VIII of section IV. At t_6^+, gating pulse of S_1, v_{GE,S_1} is applied (before i_N changes its direction). As $v_{CE,S_1} = 0$, zero voltage turn

ON (ZVS) of S_1 is ensured. At t_Z, i_N becomes zero and changes its direction.

Switching transition of $S_{A1} - S_{A2}$ is shown in Fig. 21b. Before t_3^-, S_{A1} was conducting i_A and S_{A2} was blocking V_{dc}. At t_3^-, gating pulse of S_{A1} is removed. After sometime at t_3, voltages across $S_{A1} - S_{A2}$ begin to change. Voltage across S_{A1}, $v_{CE,S_{A1}}$, slowly builds upto V_{dc} and the voltage across S_{A2} becomes zero at t_4. Slow change in voltage across S_{A1} due to device capacitance helps to reduce turn OFF loss of S_{A1}. As i_A does not change its direction, the anti-parallel diode of S_{A2} is in conduction after t_4. At t_4^+, gating pulse of S_{A2}, $v_{GE,S_{A2}}$ is applied when $v_{CE,S_{A2}} = 0$ and thus ZVS turn ON is achieved. This transition verifies the operation in Mode IV of section IV.

Switching transition of $S_{B1} - S_{B2}$ is presented in Fig. 21c. The switching process is similar to the transition of $S_{A1} - S_{A2}$. The switching process verifies the converter operation in Mode II and III of section IV. Due to device capacitance, slow rise in voltage across S_{B1} helps to reduce turn OFF loss of S_{B1}. From Fig. 21c, it is clearly seen that the gating signal of S_{B2} is applied when the voltage across S_{B2}, $v_{CE,S_{B2}}$ is zero and thus ensuring ZVS turn ON of S_{B2}.

VI. Power Loss and Efficiency

The converter power loss is analytically estimated assuming ripple free line currents. In the analysis only conduction loss is considered as the proposed topology is soft-switched. Power loss is also obtained experimentally.

A. Analytical loss estimation

The conduction loss in switch S_1 and S_{A1} are given in (9). Due to operation symmetry, leg A and B switches have same loss. The conduction loss in anti-parallel diode of S_{A1} is given in (9). V_{CE}, V_D and R_{CE}, R_D are the constant voltage drop and on state resistance of the IGBT switches and diodes respectively.

$$\begin{aligned} P_{C_{S_1}} &= \frac{0.83 V_{CE,S_1} I_{pk}}{n} + 1.37 \frac{R_{CE,S_1} I_{pk}^2}{n^2} \\ P_{C_{S_{A1}}} &= \frac{M V_{CE,S_{A1}} I_{pk}}{4n} + \frac{5\sqrt{3}M}{12\pi n^2} R_{CE,S_{A1}} I_{pk}^2 \\ P_{C_{D,SA1}} &= (0.41 - 0.254M) \frac{V_{D,SA1} I_{pk}}{n} \\ &+ (0.353 - 0.23M) \frac{R_{D,SA1} I_{pk}^2}{n^2} \end{aligned} \tag{9}$$

The conduction loss in ASC diode D_1, NPC inverter switch Q_{ap} and Q_{ao} are given in (10).

$$\begin{aligned} P_{C_{D_1}} &= 0.41 V_{D_1} I_{pk} + 0.36 R_{D_1} I_{pk}^2 \\ P_{C_{Q_{ap}}} &= 0.276 V_{CE_{ap}} I_{pk} + 0.235 R_{CE_{a1}} I_{pk}^2 \\ P_{C_{Q_{ao}}} &= 0.04 V_{CE_{ao}} I_{pk} + 0.014 R_{CE_{ao}} I_{pk}^2 \end{aligned} \tag{10}$$

The conduction loss of HFT is given as $I_{p,HFT}^2 (R_p + n^2 R_s)$. Where $I_{p,HFT} = \frac{0.84 I_{pk}}{n}$ is the RMS current of the primary winding. R_p and R_s are primary and secondary winding resistance. At the switching frequency the HFT core loss is negligible.

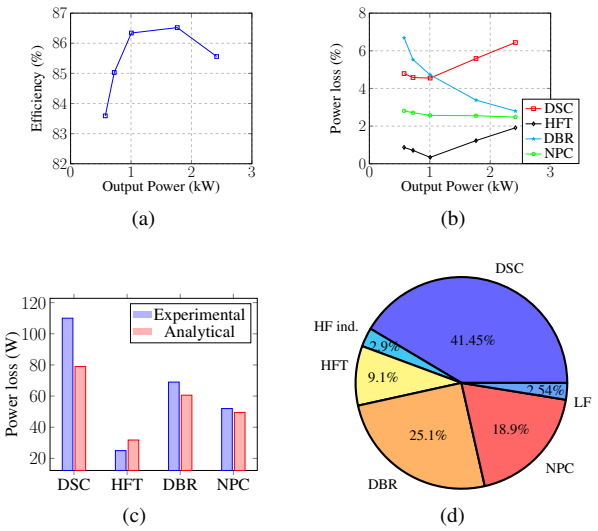


Fig. 22: (a) Efficiency of the proposed 3ϕ HFL inverter, (b) Power loss at different stages of 3ϕ HFL inverter. (c) Power loss break down and (d) Percentage loss distribution at 1.76kW output power.

B. Experimentally measured power loss

The converter is operated with input 230V DC for a variation of output load 0.57kW to 2.42kW. The power loss is measured at different stages of the converter. Fig. 22a shows the measured efficiency of the converter. The prototype has maximum efficiency 86.52 % at 1.76kW output power. The experimentally obtained power losses in different stages of the converter are shown in Fig. 22b. The experimental and analytical loss distribution of the converter at 1.76kW output power is shown in Fig. 22c. As seen from the figure, the analytically estimated power losses at the different stages of the converter are closely matched with the experimentally obtained losses. A pie chart showing the share of loss in different stages at 1.76kW output power is shown in Fig. 22d.

TABLE II: Topology Comparison

	Proposed topology	[17]	[20]	PSFB+ 3ϕ VSI
Active switch count	18	12	14	10
No. of diodes	8	6	12	4
Load support (PF)	± 0.866	± 0.866	UPF	Any
DSC	ZVS	Hard-switched	Partially ZVS	ZVS
ASC	LF switched	Partially HF Switched	LF switched	HF Switched
Intermediate DC link Filter	No	No	No	Yes

TABLE III: Devices used in experiment and optimal design

		Part No.	V_{CE}/V_D	R_{CE}/R_D
DSC	Used	SKM75GB123D (1200V, 75A)	1.8V	38 mΩ
	Optimal Design	IRFP4137PbF (300V, 38A)	-	56mΩ
DBR	Used	MEE 75-12 DA (1200V, 75A)	1.5V	3.65mΩ
	Optimal Design	DPG20C400PC (400V, 20A)	0.77V	19.8mΩ
NPC	Used	IKW40N120H3 (1200V, 40A)	2.05V	-
	Optimal Design	IKP28N65ES5 (650V, 28A)	1.06V	14mΩ

The experimental prototype is not optimally designed for

2-3kW power level and hence has the relatively low peak efficiency of 86.52%. We have optimally designed the converter at 2.15kW with the devices listed in Table III. The design has an analytically estimated efficiency of 94.7%. The method of analytical estimation is already verified with the existing hardware. As the chosen devices in the optimal design has better conduction loss parameters as shown in Table III and as the loss is primarily due to conduction, the optimal design has better efficiency.

VII. Topology comparison

The proposed topology is compared with the single stage topologies presented in [17], [20] and a conventional multi-stage topology (PSFB followed by a 3ϕ VSI). Key features are summarised in Table II. The multi-stage topology uses minimum number of semiconductors. But it requires intermediate DC filter capacitor which reduces reliability and the 3ϕ VSI is hard switched impacting efficiency. [17] can support reactive power flow upto ± 0.866 PF at the AC port but the converter is hard-switched. In [20], the DSC is partially soft-switched and ASC is line frequency switched but the converter can supply load only at UPF. Though the proposed topology uses higher number of low frequency switched active devices, the converter support reactive power upto ± 0.866 PF and the power loss of the converter is independent of switching frequency, which helps to increase the converter switching frequency and hence reduces the size of the magnetics.

VIII. Conclusion

This paper presents a novel PWM high frequency link three-phase DC-AC converter for grid integration of photovoltaic and fuel cell energy sources. The converter also supports upto 30° leading and lagging power factor standalone load. The converter has following features. The active switches of DC side converter are zero voltage switched over complete line cycle. Intermediate DC link is pulsating and the use of bulky DC link filter capacitor is avoided. The AC side NPC three level inverter is switched at low frequency and thus incurring negligible switching loss. The high frequency galvanic isolation provides compact, high-power density converter solution. The converter operation is analysed and switching process is described. The analysis determines proper dead time selection for switching of the DC side converter to ensure soft-switching. The converter can supply a single phase load connected between any two poles. Converter operation is validated on a 2kW hardware prototype. Experimental results verifying the steady state operation of the converter at UPF and 0.89 lagging power factor are presented. ZVS switching of DC side converter is experimentally validated.

Appendix
Estimation of conduction loss in S_1

The conduction loss of switch S_1 is expressed as $P_{C_{S_1}} = V_{CE,S_1} I_{S_1,avg} + R_{CE,S_1} I^2_{S_1,rms}$. Where $I_{S_1,avg}$ and $I_{S_1,rms}$ are the average and RMS current through S_1 respectively. The current through S_1, i_{S_1} is a switching frequency current with magnitude (I_{S_1}) varying sinusoidally over line cycle. I_{S_1} has similar wave shape as $(i_p + i_q)$, shown in Fig. 5. I_{S_1} has a periodicity over $\frac{\pi}{3}$ and it is defined as $I_{S_1} = \frac{\sqrt{3} I_{pk}}{n} \cos\left(\frac{\pi}{6} - \theta\right)$ over $0 < \theta < \frac{\pi}{3}$. In a switching cycle ($T_s$), S_1 conducts half of T_s. The RMS current, average current and the conduction loss $P_{C_{S_1}}$ of S_1 are given in (11).

$$
\begin{aligned}
I^2_{S_1,rms} &= \frac{3}{2\pi} \int_0^{\frac{\pi}{3}} \frac{3 I^2_{pk}}{n^2} \cos^2\left(\frac{\pi}{6} - \theta\right) d\theta = 1.37 \frac{I^2_{pk}}{n^2} \\
I_{S_1,avg} &= \frac{3}{2\pi} \int_0^{\frac{\pi}{3}} \frac{\sqrt{3} I_{pk}}{n} \cos\left(\frac{\pi}{6} - \theta\right) d\theta = 0.83 \frac{I_{pk}}{n} \\
P_{C_{S_1}} &= \frac{0.83 V_{CE,S_1} I_{pk}}{n} + 1.37 \frac{R_{CE,S_1} I^2_{pk}}{n^2}
\end{aligned}
\tag{11}
$$

Following similar process, the losses in other switches and diodes are obtained.

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