# Power Electronic Converter-based Flexible Transmission Line Emulation

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***Abstract*—A power electronic converter-based Transmission Line Emulator (TLE) is presented in this paper. The TLE can emulate medium and long lines in steady state and symmetrical faults occurring at any point in the line. A travelling wave based numerical scheme for the emulation of the line is identified and then implemented on a novel digital architecture in the FPGA part of a System on Chip platform. The proposed architecture meets the real-time computation constraints through parallel processing and optimal use of hardware resources (DSP slices, block RAMs etc.). A comprehensive analysis to determine the two important parameters of the TLE: the power converter switching frequency and observer update period while satisfying a number of constraints coming from the numerical scheme, power and embedded hardware, has been presented. Finally, relevant simulation and experimental results on a developed 400 V, 15 kVA TLE prototype have been presented for validation.**

***Index Terms*—long transmission line, hardware emulation, SoC, real-time simulation, 3-phase VSI, current control**

## NOMENCLATURE

| | |
|---|---|
| $\Delta t_{obs}$ | Transmission line observer solution update period. |
| $F_{sw}$ | Power electronic converter switching frequency. |
| $T_{sw}$ | Power electronic converter switching period. |
| $l$ | Length of emulated transmission line. |
| $n$ | No. of line sub-divisions. |
| $\Delta x$ | Length of each line sub-division. |
| $\Delta x_{des}$ | Desired minimum length resolution on the line. |
| $R, L, G, C$ | Per-unit length line resistance, inductance, conductance and capacitance, respectively. |
| $Z_0$ | Characteristic impedance of line. |
| $c$ | Wave propagation velocity along line. |
| $f_{i,max}$ | Maximum frequency component in emulated line current signal. |
| $t_{comp,PS}$ | Required observer computation time in PS. |
| $t_{comp,PL}$ | Required observer computation time in PL. |
| $t_{clk,PS}$ | Instruction clock period in PS. |
| $t_{clk,PL}$ | Instruction clock period in PL. |
| $t_f$ | Time required by processor to perform tasks other than observer computation. |
| $F_{limit}$ | Maximum operating switching frequency of power converter. |
| $\delta_P$ | Power angle between two ends of transmission line. |

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## I. INTRODUCTION

REAL-TIME simulation of power systems, electromechanical energy conversion systems, various power sources and loads in steady and transient conditions play a vital role in the testing of industry manufactured control, protection and power equipment [1]–[8]. A digital platform emulating a test environment in real time can be connected to a control or protection device under test (DUT) through digital to analog (DAC) and analog to digital (ADC) conversion interface. This is called hardware in loop (HIL) testing [3]–[8]. Here the digital platform is called the observer (OBS), Fig.1(a). For example, the controller of a grid tied solar inverter can be tested in a HIL platform. Where the observer has to emulate solar PV, grid and the inverter. Note in HIL simulation the DUT does not exchange real power with the observer. Now to test the solar inverter along with the controller, the emulated test environment (the utility grid and solar PV) needs to exchange electric power with DUT. This is achieved by adding a power amplifier (PA) in the real time emulator. This power amplifier is implemented with a power electronic converter. So here we need a power electronic converter based PV and grid emulators. This test set up is known as power hardware in loop (PHIL, Fig. 1(b)), [9]–[15]. Hardware emulators, in PHIL testing, are used to replace any costly or physically unavailable component and produce a diverse set of test conditions through an user-friendly interface.

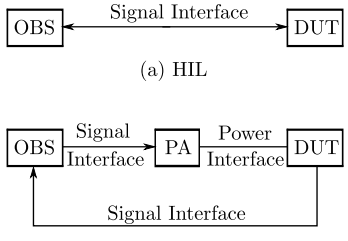


Fig. 1. Conceptual diagram of (a) HIL, (b) PHIL simulation.

Applying above concept in developing a representative power grid system for laboratory based testing of control, protection and power equipment and communication interfaces,

autonomous emulators of every component in the system are developed which are electrically interconnected following the intended network [14]–[17]. Following a similar idea, Field Programmable Gate Array (FPGA) based generator, power converter and transmission line models have been developed in [18]–[20]. But these platforms are incapable of exchanging power with any external hardware. On the contrary, in a test-bed built using power converter-based emulators, every node inside the emulated network is physically accessible to a power hardware under test and insertion of custom designed power amplifiers are no longer required. Power converter-based emulation of synchronous generators has been reported in [17]. In this paper we address similar emulation of transmission lines.

The general architecture of a Transmission Line Emulator (TLE) as shown in Fig. 2, has two main components- the observer and the power hardware. Sending end (S.E) and receiving end (R.E) bus voltages $(v_{SE}(t), v_{RE}(t))$ are physically fed to the observer which solves the emulated line model in

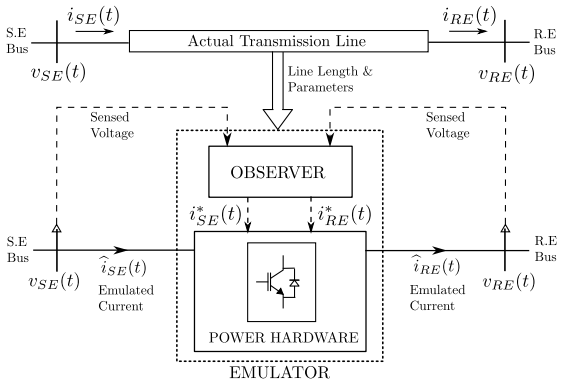


Fig. 2. General architecture of a Transmission Line Emulator (TLE).

real-time and estimates the S.E and R.E currents of the line $(i^*_{SE}(t),\ i^*_{RE}(t))$. The estimated currents work as references and the power hardware output currents $(\widehat{i}_{SE}(t),\ \widehat{i}_{RE}(t))$ are controlled to track them. Leveraging high switching frequencies and flexible control of power electronic converters, the power hardware is comprised of 3-phase Voltage Source Converters (VSCs). [21]–[24] have extensively dealt with the design and development of a TLE based on a similar architecture. [21], [22] have addressed line emulation in case of steady state and [23], [24] have emulated 3-phase short-circuit faults on a transmission line. However, the scope in all these works is limited to short lines only, where a simple lumped R-L model of the line is sufficient for emulation. In this paper, we address the problem of hardware emulation of medium and long transmission lines in steady state as well as 3-phase faults occurring at any intermediate point on the line. Following are the contributions of this work.

- We have investigated the applicability of different transmission line models for the stated purpose and identified a travelling wave based numerical solution suitable to be solved by the observer in real-time.
- Two key parameters in the design of programmable TLE are the power converter switching frequency $(F_{sw})$ and observer solution update period $(\Delta t_{obs})$. Once selected, these parameters are not changed for varying cases of line length, line parameters and emulated transient dynamics. The desired space resolution on the emulated line, accuracy of the numerical scheme and frequency content of the line current signal directly influence the choice of $\Delta t_{obs}$. The choice of $F_{sw}$ depends on the maximum possible switching frequency of the power electronic converter and the minimum controller bandwidth required to track the current references. Further the constraint of real-time computation based on the chosen embedded platform also influence the selection of these parameters. In this work, we have provided a comprehensive analysis of all these determining factors and have laid out simple guidelines to choose the correct values of $F_{sw}$ and $\Delta t_{obs}$ to make the TLE platform independent of emulated line length and parameters.
- Due to the complexity of the chosen travelling wave based transmission line model which captures the distributed nature of the line, the real-time computation needed in the observer is significantly high when compared with the previous works [21]–[24]. We show, how to compute the observer computation time if implemented in a sequential processor. The ARM Cortex A9 of Zynq 7000 System on Chip (SoC) is used as an example.
- A novel digital architecture for real-time implementation of the observer in the FPGA part of SoC has been provided which uses parallel computation and optimal number of digital resources (DSP slices, block RAMs etc.) and thereby drastically reduces the computation time.
- An experimental test-bed for TLE with Grid or Bus emulators are presented that draws only the losses in the power converters.

The paper is organized as follows. Section II provides the modelling and solution of AC transmission lines suitable for long line emulation. Section III describes the design and embedded implementation details of the observer. Section IV describes the power hardware topology and associated controls. Relevant simulation and experimental results are given in Section V followed by the conclusion in Section VI.

## II. Modelling & Solution of Transmission Lines

The complexity of the mathematical model of the line to be solved in the observer depends on the nature of the emulated event (frequency content, location) as well as the characteristics of the emulated line (line length $(l)$, arrangement). A very detailed model can give accurate results in any case while incurring a large computational overhead in real-time whereas, a simplified model may fail to generate the desired output. Thus, this section is dedicated towards finding out the applicability of different transmission line models and their solutions for real-time emulation of steady state and symmetrical faults in medium and long lines. For simplicity of understanding, it is assumed that the lines are 3-phase single circuit, fully transposed in nature and the conductors are symmetrically spaced, maintaining an uniform height over the ground.

A simple series model of total line resistance and inductance (R-L model) is fairly accurate for short lines ($l < 80$ km), as emulated in [21]–[24], but not sufficient for long lines as the shunt admittance of the line becomes significant. For

medium (80 km $< l <$ 250 km) and long ($l >$ 250 km) lines, nominal-pi lumped parameter model can be used for sinusoidal steady state analysis. However, this model is not accurate for faults and other high frequency transients due to the inherent lumpedness of the line parameters [25]. Fig. 3(a) shows the mismatch in one phase of the S.E currents during steady state as well as a 3-phase fault at R.E of a 132 kV, 500 km long line for 3 different models - a lumped R-L model, a nominal pi-model and the PSCAD frequency dependent model (PSCAD FDM) [26]. Fig. 3(b) compares the same result between PSCAD Bergeron model and PSCAD FDM model. The transient performance can be improved by

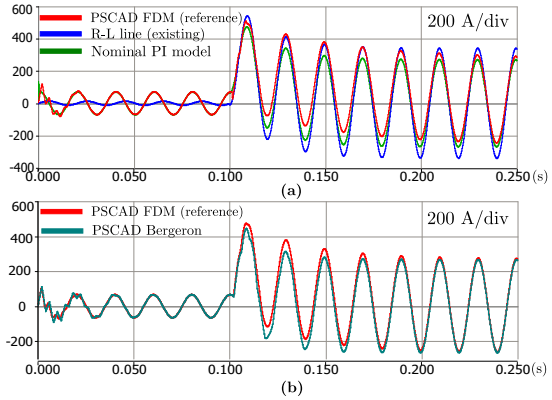


Fig. 3. Comparison of S.E currents during steady state and fault transient of a 500 $km$ long line: (a) Comparison of PSCAD FDM, lumped R-L model and nominal PI model, (b) Comparison of PSCAD FDM and PSCAD Bergeron.

cascading several pi-sections to better represent the distributed nature of the line parameters, but that increases computation time and complexity so greatly that it becomes very difficult to implement on a digital platform. Moreover, for longer lines, nominal pi-model needs be replaced with long line corrected equivalent pi-model for better results [25].

The above observations inspire us to consider the general distributed model of a transmission line for emulation purpose, as dictated by the following governing equations,

$$\frac{\partial v(x,t)}{\partial x} + L\frac{\partial i(x,t)}{\partial t} + Ri(x,t) = 0 \quad (1)$$

$$\frac{\partial i(x,t)}{\partial x} + C\frac{\partial v(x,t)}{\partial t} + Gv(x,t) = 0 \quad (2)$$

where, $v(x,t)$ and $i(x,t)$ are respectively the voltage and current at a distance $x$ from the S.E of the line at time $t$. To ensure modular and autonomous operation of the line emulators, our goal here is to develop a solution of (1)-(2) that solves the terminal currents only based on the information of individual line parameters and local bus voltages. Another important objective is that the solution must be capable of estimating fault currents for faults occurring anywhere along the line, which also inspires us to preserve the distributedness of the line unlike it's lumped approximations. In addition, the solution time should be small enough to aid real-time emulation. Based on Fig. 4 and discussion above, the problem statement for the observer can be formulated as-

Given, a) Initial condition of voltage and current along the line: $v(x,0)$, $i(x,0)$, and b) Boundary condition of terminal

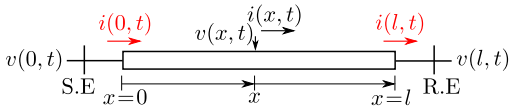


Fig. 4. Problem addressed by the observer.

voltages: $v_{SE}(t) = v(0,t)$ and $v_{RE}(t) = v(l,t)$, solve the terminal currents: $i_{SE}(t) = i(0,t)$ and $i_{RE}(t) = i(l,t)$.

A potential candidate for the solution of the above problem is the Bergeron model [25] as it considers uniform distribution of the line inductance and capacitance while lumping the total line resistance at three places. The solution is much faster and accurate and better suited for digital implementation than cascaded pi-circuits. However, to get accurate results, the wave travel time ($\tau$) has to be an integral multiple ($m_1$) of the time interval $\Delta t_{obs}$ at which the observer solves the model and updates the solution or, $\tau = m_1 \times \Delta t_{obs}$. This essentially avoids the need for using complex interpolation algorithms to compensate the timing mismatch [25]. Further, as will be seen later, for discrete-time implementation, $\Delta t_{obs}$ must be an integral multiple ($m_2$) of the power converter switching period ($T_{sw}$). Therefore,

$$\tau = m_1 \times m_2 \times T_{sw}, \quad (\because \Delta t_{obs} = m_2 \times T_{sw}) \quad (3)$$

As $\tau$ varies with line parameters, (3) implies that if Bergeron model is used, the power converter switching frequency ($F_{sw} = 1/T_{sw}$) needs to be changed every time a new line is emulated which will impede flexibility of implementation. This also presents difficulty to emulate a fault at an intermediate point on the line, as the line needs to be divided into two segments which have different values of $\tau$ parameter, requiring two different time steps in observer computation. Further, the pre-fault voltage and current information at the intermediate point needs to be known to calculate the fault currents, which are also not available with the Bergeron model since it solves only the terminal quantities of a line.

To overcome above difficulties in digital implementation and fault emulation, in this work a numerical method known as the 'Method of Characteristics'(MOC) [27], used for solving hyperbolic partial differential equations like (1)-(2), is adopted. Unlike Bergeron model, MOC uniformly distributes the line resistance and also considers the shunt conductance of the line. The MOC converts (1) and (2) into ordinary differential equations that can be integrated only along a family of straight lines (see Fig. 5) with slopes $\frac{dx}{dt} = \pm\frac{1}{\sqrt{LC}} = \pm c$ in the $x$-$t$ plane [27]. $c$ is the wave propagation velocity. The intersection

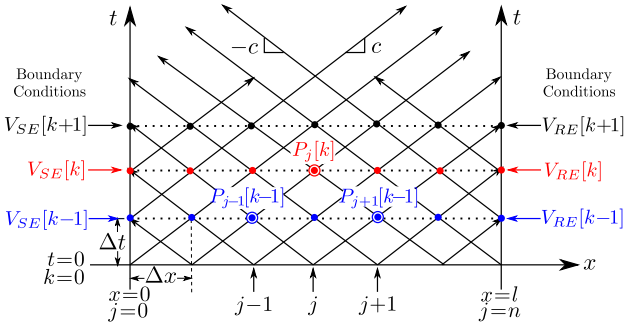


Fig. 5. Numerical scheme implemented in observer, $P \in \{V, I\}$.

of these lines on the $x$-$t$ plane form the solution points for

$v(x,t)$ and $i(x,t)$ at a regular space interval of $\Delta x$ and time interval of $\Delta t$ such that, $\left|\frac{\Delta x}{\Delta t}\right| = c$. Hence, we discretize a continuous quantity $p \in \{v, i\}$ in space and time as,

$$p(x,t) = p(j\Delta x, k\Delta t) = P_j[k], \qquad P \in \{V, I\} \tag{4}$$

In our case, $\Delta t = \Delta t_{obs}$, $\Delta x = c\Delta t_{obs}$ and $j = 0, 1, .., n$ where, $l = n\Delta x$. Also, for S.E, $V_{SE}[k] = V_0[k]$, $I_{SE}[k] = I_0[k]$ and for R.E, $V_{RE}[k] = V_n[k]$, $I_{RE}[k] = I_n[k]$. At every $k^{th}$ time step, to solve $P_j[k]$ at any internal point on the line, the observer solves equations (5)-(6) using previous step information at two adjacent points $P_{j-1}[k-1]$ and $P_{j+1}[k-1]$ while, to find out current at a boundary point it solves either (7) or (8) using previous step data at one adjacent point and sampled value of the terminal voltage $V_{SE}[k]$ or $V_{RE}[k]$. The solved $k^{th}$ step data are stored and used to solve the $(k+1)^{th}$ step in the next computation cycle and in this way the numerical scheme advances in real-time. For, $1 \leq j \leq n-1$,

$$\begin{aligned} V_j[k] = C_4 \left(V_{j-1}[k-1] + V_{j+1}[k-1]\right) \\ + C_5 \left(I_{j-1}[k-1] - I_{j+1}[k-1]\right) \end{aligned} \tag{5}$$

$$\begin{aligned} I_j[k] = C_6 \left(V_{j-1}[k-1] - V_{j+1}[k-1]\right) \\ + C_7 \left(I_{j-1}[k-1] + I_{j+1}[k-1]\right) \end{aligned} \tag{6}$$

$$I_{SE}[k] = C_1 V_{SE}[k] - C_2 V_1[k-1] + C_3 I_1[k-1] \tag{7}$$

$$I_{RE}[k] = -C_1 V_{RE}[k] + C_2 V_{n-1}[k-1] + C_3 I_{n-1}[k-1] \tag{8}$$

$C_1, ..., C_7$ are constants for a particular line whose formulae in terms of line parameters are given in the Appendix. For steady state and symmetrical fault analysis, only two phases of a 3-phase line needs to be solved using (5)-(8) as the line is in balanced conditions.

## III. Embedded Implementation of the TLE

One important question that needs to be answered is how to choose the power converter switching frequency $(F_{sw})$ along with the observer update interval $(\Delta t_{obs})$ in order to make the TLE platform independent of the emulated line length and parameters for a range of transients, keeping practical limitations of the digital hardware and power hardware into consideration. We will be answering this question at first.

A power electronic converter through closed loop feedback control ensures that the emulator currents track the S.E and R.E currents computed by the observer. As in this case, the actuator or power converter is updated only at every switching period $T_{sw}$, there is no need to update the observer computation faster than that. So, $\Delta t_{obs} \geq T_{sw}$. Also for digital implementation, it is convenient to set $\Delta t_{obs}$ as an integral multiple of $T_{sw}$ or,

$$\Delta t_{obs} = m_2 \times T_{sw}, \qquad m_2 \in \{1, 2, 3, ...\} \tag{9}$$

So, determination of $\Delta t_{obs}$ and $T_{sw}$ is same as finding $m_2$ and $T_{sw}$. In the following analysis, we consider a case in which the line parameters of the chosen set of emulated transmission lines vary within $\pm 10\%$ of a nominal value $(X_{nom})$ as, $0.9X_{nom} \leq X \leq 1.1X_{nom}$ where, $X \in \{L, C, R, G\}$ and the maximum length of any emulated line $(l_{max})$ is $1000\,km$. The considered range of variation of the line parameters and $l_{max}$ are however design parameters which are specific to a TLE platform. The nominal values of the line parameters in our case, are given in Table-III. From there, we obtain, minimum surge impedance $Z_{0,min} = \sqrt{L_{min}/C_{max}} = 485\ \Omega$ and likewise the minimum and maximum wave velocity $c_{min} = 2.26 \times 10^5\ km/s$ and $c_{max} = 2.76 \times 10^5\ km/s$, respectively.

$\Delta t_{obs}$ determines the number of line subdivisions $(n)$ by, $n = l/\Delta x = l/(c\Delta t_{obs})$ and thereby the computational load on the digital platform. The choice of $\Delta t_{obs}$ depends on several factors, as- (a) Since the transmission line is considered uniform and continuous, the incremental resistance $R\Delta x$ in MOC should be small enough compared to the surge impedance $Z_0$, not to cause discontinuity in wave propagation. Therefore, to get accurate results, $R\Delta x << Z_0$. To satisfy for any line, it is recommended to keep,

$$(R\Delta x)_{max} \leq \frac{Z_{0,min}}{10} \ \text{ or, } \ \Delta t_{obs} \leq \frac{Z_{0,min}}{10(Rc)_{max}} \tag{10}$$

since, $(R\Delta x)_{max} = (Rc)_{max}\Delta t_{obs}$. (b) For proper reconstruction of the estimated line current signal we ensure the observer samples the signal at least at 10 times the maximum frequency component $(f_{i,max})$ present in it. Hence, $f_{obs} = 1/\Delta t_{obs} \geq 10 f_{i,max}$. As this paper addresses the emulation of steady state and symmetrical fault dynamics, it is sufficient to take, $f_{i,max} = 100$ Hz. (c) Value of $\Delta x$ should be chosen lesser than the desired minimum space resolution $\Delta x_{des}$, so that fault points can be located more precisely. Therefore, $\Delta x \leq \Delta x_{des}$ or, $\Delta t_{obs} \leq \Delta x_{des}/c_{max}$. As a choice we take $\Delta x_{des} = 15\,km$.

Above 3 factors constitute the upper limit $(\alpha)$ of $\Delta t_{obs}$ as,

$$\Delta t_{obs} \leq \alpha = \min\left\{\frac{Z_{0,min}}{10(Rc)_{max}}, \frac{1}{10 f_{i,max}}, \frac{\Delta x_{des}}{c_{max}}\right\} \tag{11}$$

which satisfies the requirements of numerical solution related constraint, signal reconstruction and space resolution for emulation of any line within the considered range of parameters and length. Putting the values in (11) for the present case we obtain, $\alpha = 54\,\mu s$.

Next, from (5)-(8) we can infer that, to solve 2 phases of a 3-phase line with $n$ sub-divisions, at each computation step the observer performs, $\phi(n) = 12 + 8(n-1)$ multiplications and $\psi(n) = 9 + 12(n-1)$ additions along with move and shift operations. Xilinx make Zynq System-on-Chip (SoC) has been selected as the embedded platform which has an ARM Cortex-A9 based Processing System (PS) and Xilinx Programmable Logic (PL) on a single chip (Fig. 7(a)). The required number of Instruction Cycles for Multiplication $(ICM)$ and Addition $(ICA)$ are 5 and 4 respectively for floating point operation in Zynq PS which has an instruction clock period, $t_{clk,PS} = 6\,ns$. Therefore, the required computation time of the observer $(t_{comp})$ in PS can be roughly estimated as,

$$\begin{aligned} t_{comp,PS} &\approx \left[\phi(n) \times ICM + \psi(n) \times ICA\right] t_{clk,PS} \\ &\approx (88n + 8) t_{clk,PS} \ \approx (88n) t_{clk,PS} \end{aligned} \tag{12}$$

To achieve a much faster rate of computation using parallel multiplier and adder blocks, a Zynq PL-based implementation

of the observer has been proposed later by which it takes fixed 8 PL clock cycles ($1\,t_{clk,PL} = 10\,ns$) to compute each line sub-division. Thus, for $n$ sub-divisions,

$$t_{comp,PL} \approx (8n) t_{clk,PL} \tag{13}$$

For both PS and PL, $t_{comp}$ is an increasing function of $n\left(=\frac{l}{c\Delta t_{obs}}\right)$ which is maximum when, $l = l_{max}$ and $c = c_{min}$. Therefore we can write,

$$t_{comp,max} = k_z/\Delta t_{obs}, \quad z \in \{PS, PL\} \tag{14}$$

$$\text{where, } k_z = \left(88\, l_{max} t_{clk,PS}\right)/c_{min}, \quad \text{for } PS \tag{15}$$

$$= \left(8\, l_{max} t_{clk,PL}\right)/c_{min}, \quad \text{for } PL$$

In power converter control, one switching period is divided to perform 4 main tasks as - (a) Sensing and signal filtering, (b) Observer computation, (c) Control and modulation and (d) Communication. Let the total time required to perform tasks (a), (c) and (d) be denoted as $t_f$, which is around $20\,\mu s$ in our case for Zynq PS. Since, $\Delta t_{obs}$ can span over $m_2$ number of switching periods, at least $(1/m_2)$th fraction of the observer computation task must be completed in one $T_{sw}$. Hence, $T_{sw}$ should be chosen so that,

$$T_{sw} \geq \frac{t_{comp,max}}{m_2} + t_f \tag{16}$$

Using (9) and (14), (16) forms a quadratic inequality of $\Delta t_{obs}$,

$$\Delta {t_{obs}}^2 - m_2 t_f \Delta t_{obs} - k_z \geq 0 \tag{17}$$

Solving (17) we get $\beta_z\left(z \in \{PS, PL\}\right)$, a function of $m_2$ as the lower limit of $\Delta t_{obs}$,

$$\Delta t_{obs} \geq \beta_z(m_2) = \frac{m_2 t_f + \sqrt{(m_2 t_f)^2 + 4k_z}}{2} \tag{18}$$

Note that, $\beta_z(m_2)$ is influenced by the maximum line length and the computation speed of the digital platform. From (11) and (18), we conclude $\Delta t_{obs}$ should be chosen so that,

$$\beta_z(m_2) \leq \Delta t_{obs} \leq \alpha, \quad z \in \{PS, PL\} \tag{19}$$

As $\beta_z(m_2)$ increases with $m_2$, it's minimum value is obtained for $m_2 = 1$. However, for the TLE platform being designed, (18) gives, $\beta_{PS}(1) = 59\,\mu s$ and $\beta_{PL}(1) = 31\,\mu s$. Therefore, the observer cannot be implemented in the Zynq PS as $\beta_{PS}(m_2) > \alpha (= 54\,\mu s)$ for all $m_2$, violating (19). Hence, for further analysis we will consider only $\beta_{PL}(m_2)$.

*1) Determination of power converter switching period ($T_{sw}$):* Putting, $\Delta t_{obs} = m_2 T_{sw}$ in (19), we get for PL,

$$\beta'(m_2) = \frac{\beta_{PL}(m_2)}{m_2} \leq T_{sw} \leq \frac{\alpha}{m_2} = \alpha'(m_2) \tag{20}$$

The choice of $T_{sw} = 1/F_{sw}$ depends on the maximum switching frequency at which the designed power converter can be operated, denoted as $F_{limit}$ (30 kHz, in our case). Further, to ensure proper switching frequency noise attenuation, $F_{sw}$ is kept at least 10 times higher than the control bandwidth, which is again kept at 10 times the maximum frequency current signal to be tracked ($f_{i,max}$). Therefore,

$$100 f_{i,max} \leq F_{sw} \leq F_{limit} \tag{21}$$

$$\text{or, } \delta = 1/F_{limit} \leq T_{sw} \leq \gamma = 1/100 f_{i,max} \tag{22}$$

Combining inequalities (20) and (22) we conclude,

$$\max\left\{\beta'(m_2), \delta\right\} \leq T_{sw} \leq \min\left\{\alpha'(m_2), \gamma\right\} \tag{23}$$

$\alpha'(m_2)$, $\beta'(m_2)$, $\gamma\,(=100\,\mu s)$ and $\delta\,(=33.33\,\mu s)$ are plotted in Fig.7(b) with respect to $m_2$ for the TLE under design and the line segment(s) corresponding to $T_{sw}$ and $m_2$ choices that satisfy (23) is shown. In the present case, we get the following range: $33.33\,\mu s \leq T_{sw} \leq 56\,\mu s$ and $m_2 = 1$. Hence, $\Delta t_{obs} = T_{sw} = 50\,\mu s$ and corresponding $F_{sw} = 20$ kHz is chosen for the TLE platform designed in this work. Thus, using inequality (23), one can determine correct values of $\Delta t_{obs}$ and $F_{sw}$ to be used in order to make the emulator independent of the emulated line length and parameter variation while satisfying all the digital and power hardware constraints.

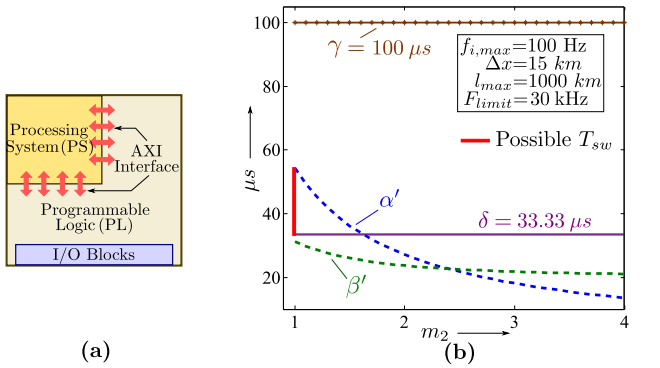


Fig. 7. (a) PS and PL in Zynq SoC architecture. (b) Determination of $T_{sw}$ for the designed TLE platform.

*2) Implementation of Observer in Zynq PL:* Referring to Fig. 8, to find terminal currents $\left(j \in \{0, n\}\right)$ of one phase of the line we solve (7) and (8) using Op-1a, Op-2, Op-3 and Op-6. For other values of $j$ (intermediate points), (5) and

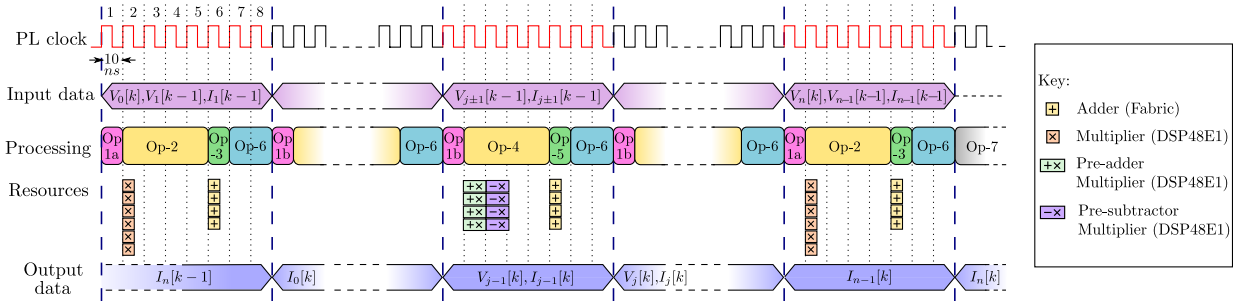


Fig. 6. Resource utilization and timing diagram of observer operation in Zynq PL for solving a 3-phase transmission line with $n$ sub-divisions.

(6) are solved using Op-1b, Op-4, Op-5 and Op-6. These 4 operations for each $j$ takes 8 PL clocks (Fig. 6). Thus, sequential evaluation of $V_j[k]$ and $I_j[k]$ at an observer time step $k$ from $j = 0$ to $j = n - 1$ requires $8n$ PL clock cycles. For Op-2 to Op-5, operands are fetched using multiplexers $M_1$-$M_5$ based on the value of $j$, from 32 bit wide memory buffers that store previous time step data. To solve 2 phases of the line simultaneously, 6 DSP48E1 slices and 4 logic fabric adders in the Zynq PL are used to perform Op-2 and Op-3 while for Op-4 and Op-5, 4 pre-adder DSP48E1 multipliers, 4 pre-subtractor DSP48E1 multipliers and 4 logic fabric adders are used. The detailed timing diagram of the operation is shown in Fig. 6 and PL resource utilization is given in Table-I.

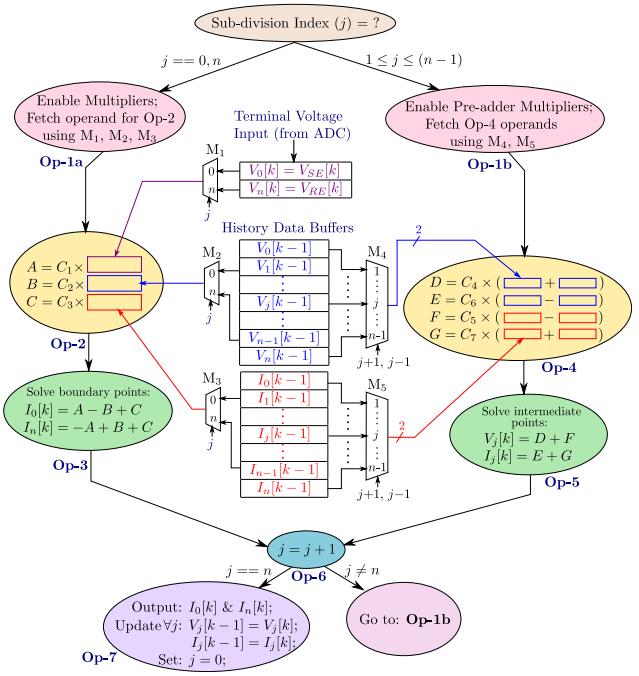


Fig. 8. Observer algorithm to solve one phase of a line in Zynq PL.

TABLE I
FPGA RESOURCE UTILIZATION

| Item | Available | Used | % Utilization |
|---|---|---|---|
| Slice LUTs | 17600 | 1931 | 10.97 % |
| Slice Registers | 35200 | 1674 | 4.76 % |
| F7 Multiplexers | 8800 | 396 | 4.50 % |
| Block RAM Tile | 60 | 8 | 13.33 % |
| DSP slices (DSP48E1) | 80 | 14 | 17.5% |
| Bonded IO Blocks | 100 | 12 | 12 % |

*3) Comparison of model computation tasks and memory utilization:* In comparison to the proposed MOC based method, the Bergeron model results in much less computation only when the line is emulated in steady state. However, for fault emulation Bergeron model results in more computation and requires larger memory. The computation details and memory required for a processor based implementation of Bergeron method for line emulation purpose is outlined in the Appendix. A comparison of MOC with Bergeron for solving a long line with $n$ sub-divisions is presented in Table-II.

TABLE II
COMPARISON OF COMPUTATION LOAD AND MEMORY REQUIREMENT (*SPECIFIC TO ZYNQ PS)

| # | MoC | Bergeron (In Appendix B) |
|---|---|---|
| Multiplication | $12 + 8(n-1)$ | $20(n-1) + 20$ |
| Addition | $9 + 12(n-1)$ | $192(n-1) + 16$ |
| Move | $9 + 8n$ | $4n(n+1)$ |
| Compare | $2n$ | $n$ |
| Shift | 0 | $96(n-1)$ |
| Total computation time* | $(588n + 102)\ ns$ | $(4n^2 + 313n - 272)\ ns$ |
| Memory | $8(n+1)\times$ 32 bits | $4n(n+1)\times$ 32 bits |

## IV. TLE POWER HARDWARE TOPOLOGY AND CONTROL

One 3-phase Voltage Source Inverter (VSI) emulates the S.E and simultaneously another VSI is used to emulate the R.E of the line. These VSIs are connected in a back-to-back fashion through a common DC link (P-N) as shown in Fig. 9 [21].

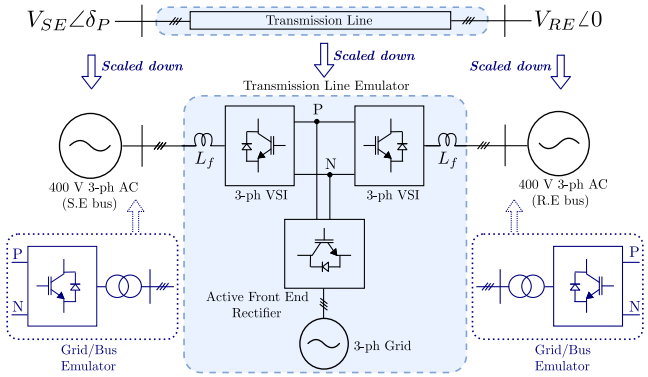


Fig. 9. Power hardware topology inside the TLE.

*1) Scaling of the actual system:* In order to emulate any transmission line using laboratory-scale power electronic hardware, the actual power and voltage level of the line needs to be scaled down to the power and voltage level of the 3-phase VSIs in the emulator. For example, for the TLE designed in this work, the VSIs are rated for 15 kVA and 400 V (L-L). To preserve system equivalence, the scaling should be done keeping the per-unit (p.u) values of power, voltage and line parameters $(R, L, C, G)$ unchanged. The nominal values of the line parameters are given in Table-III. If the nominal voltage

TABLE III
ACTUAL AND SCALED DATA OF EMULATED LINE

| Quantity (nominal) | In actual line | In TLE |
|---|---|---|
| Power | 50 MVA | 15 kVA |
| Voltage (L-L) | 132 $kV_{rms}$ | 400 $V_{rms}$ |
| RMS line current | 218.7 A | 21.65 A |
| $L$ | 2.16 mH/$km$ | 66.13 $\mu$H/$km$ |
| $C$ | 7.512 nF/$km$ | 245.4 nF/$km$ |
| $R$ | 105.8 m$\Omega$/$km$ | 3.24 m$\Omega$/$km$ |
| $G$ | $1.05\times10^{-8}$ mho/$km$ | $3.43\times10^{-7}$ mho/$km$ |
| $c$ | $2.483\times10^{5}\ km/s$ | $2.483\times10^{5}\ km/s$ |

and current of the actual line are scaled down by factors $K_v$ and $K_i$ respectively, to keep the p.u values unaltered, parameters $R, L, C, G$ scale as $kR, kL, C/k, G/k$ respectively, where, $k = K_v/K_i$. However, the wave propagation velocity

and travel time remain unaltered even after scaling for a given length of the line. During fault in the actual system the current becomes almost 5 times its rated value (218.7 A). For fault emulation,in order to limit the current in the TLE to its rated value of 21.65 A, $K_i$ is reduced by a factor of 5.

*2) Emulation of transmission line losses:* The source controlling the DC bus (P-N) needs to sink the power loss in the emulated transmission line. It also needs to support the actual losses (switching and conduction loss in the switching devices and losses in the filter inductor). An Active Front-End Rectifier (AFE) is used to support the bi-directional power flow requirement while maintaining constant output DC voltage using conventional inner current and outer voltage loop control method [28].

The scaled down S.E and R.E bus can be emulated with VSIs, also known as grid emulators. If connected through isolation transformers, these bus emulator VSIs can be connected to the same DC link (P-N). This will result in circulation of active power at both ends of the emulated line. In this way, the AFE only needs to support the converter losses and hence can be of low power rating. The proposed test-bed with grid or bus emulator and line emulator VSIs along with the AFE is shown in Fig. 9.

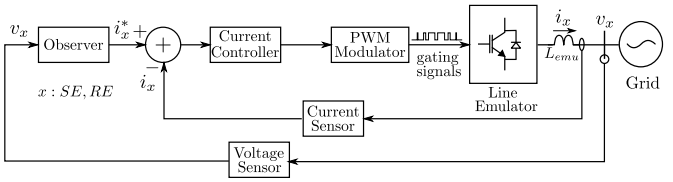


Fig. 10. Control block diagram of the line emulators ($x \in \{SE,\ RE\}$).

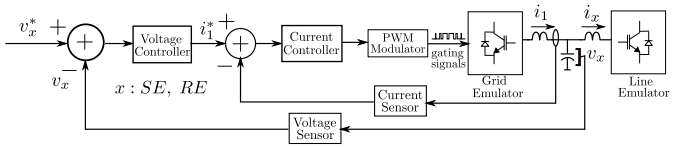


Fig. 11. Control block diagram of the grid emulators ($x \in \{SE,\ RE\}$).

*3) Control Implementation:* The two VSIs used for emulating the transmission line are controlled in current control mode in order to track the observer generated current references. The system level control block diagram is shown in Fig. 10. The controllers have been designed in the rotating $dq0$ frame so that the reference currents appears as DC in steady state and can be tracked using simple PI controllers. The VSIs' are synchronized with the grid voltages using Synchronous Reference Frame - PLL (SRF-PLL) [28]. The open-loop control bandwidth is kept at 500 Hz and the achieved phase margin is around 80°. The converters in the grid bus emulator have been controlled in voltage-frequency control mode using conventional inner current and outer voltage loop control method. In this way, the filter capacitor voltage is controlled to act as the grid for the subsequent line emulator (Fig. 10).

## V. Simulation and Experimental Results

To verify the proposed emulation scheme, a TLE prototype is designed and fabricated as shown in Fig. 13. The details of the power and embedded hardware of the designed TLE are listed in Table-IV. As a case study, a 500 $km$ long transmission line having $R, L, G, C$ parameters as listed in Table-III is considered for emulation.

TABLE IV
Design Details of the TLE Power and Embedded Hardware

| Item | Value/Part No. |
|---|---|
| VSI power rating | 15 kVA |
| VSI voltage rating (L-L) | 400 $V_{rms}$ |
| Nominal DC bus voltage | 800 V |
| Line filter ($L_f$) | 6 mH |
| IGBT Switches | SKM50GB12T4 (half-bridge module) |
| Gate Driver | ACPL-339J |
| Controller | Zynq SoC: XC7Z010-1CLG400C |
| Switching Frequency ($F_{sw}$) | 20 kHz |
| Observer update period ($\Delta t_{obs}$) | 50 $\mu s$ |

Based on above data and chosen $\Delta t_{obs}$, the observer based on the chosen numerical scheme (MOC) was coded in Matlab/Simulink and compared against the most accurate transmission line model available in PSCAD - the Frequency Dependent Phase model (PSCAD FDM). Current error in existing R-L model based approach in Fig. 12 confirm the validity of the proposed method in steady-state ($\delta_P$ kept at 0°) and during fault transients (at 210 $km$ of a 500 $km$ line).

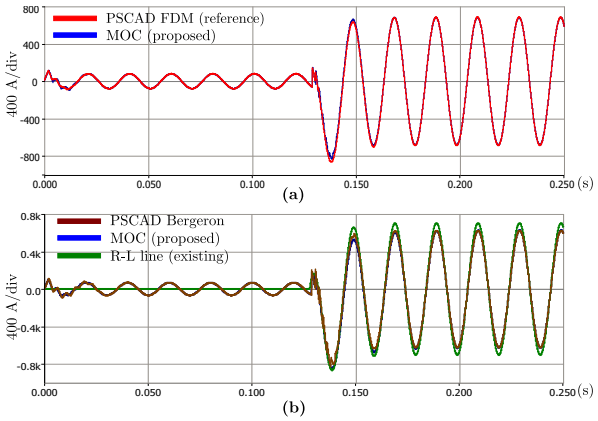


Fig. 12. Validation of developed observer for steady state and 3-phase fault emulation: **(a)** Comparison with PSCAD FDM, **(b)** Comparison of proposed method with existing method and PSCAD Bergeron model.

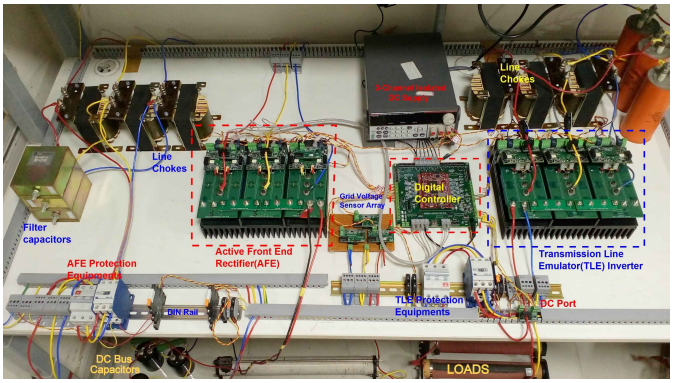


Fig. 13. Experimental set-up of the TLE system.

For experimental validation, the experiments were performed keeping the grid voltages at 1 p.u in the emulator base as per Table-III and DC bus voltage regulated at 800 V. In each experiment, the emulated event is also simulated in PSCAD using the Frequency Dependent Phase model of the

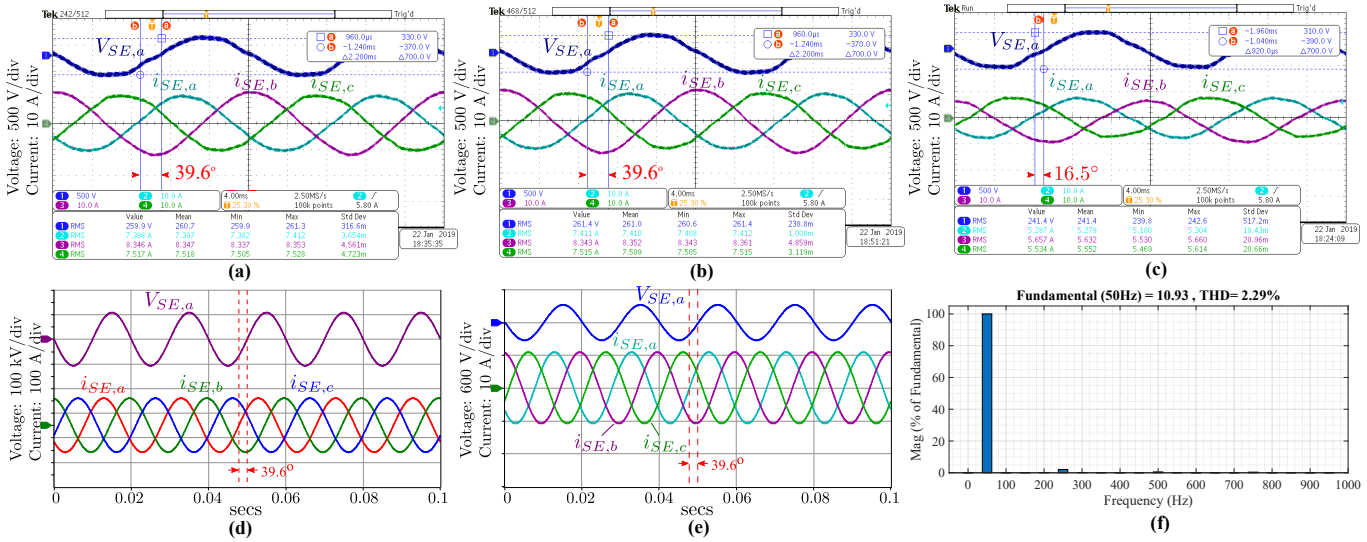


Fig. 14. Steady state emulation: (a) TLE using proposed method, (b) TLE using Bergeron method, (c) TLE using existing method (R-L line), (d) PSCAD simulation of steady state at actual power level, (e) PSCAD simulation at TLE power level, (f) Harmonic analysis of steady state current.

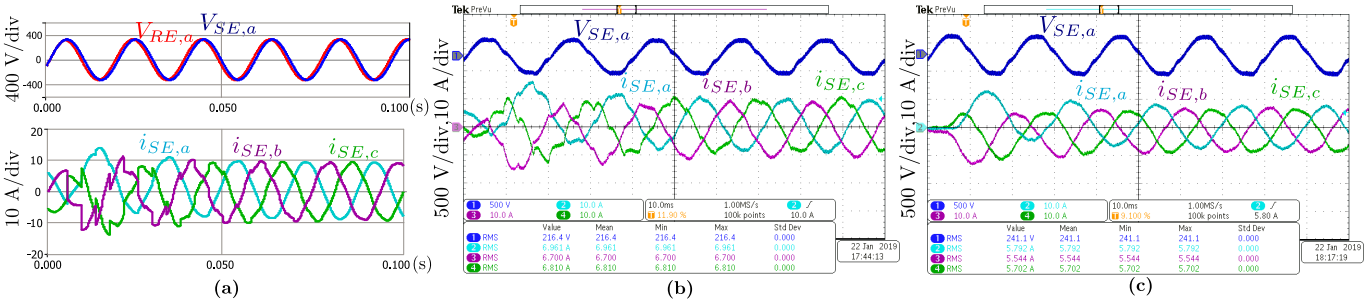


Fig. 15. (a) PSCAD simulation of step change in $\delta_P$ (Bergeron), (b) TLE result using proposed method, (c) TLE result using existing method (R-L).

line for validating the obtained experimental result. The events observed have been divided into 3 cases-

*1) Steady state:* Fig. 14(a) shows PSCAD simulation of 3-phase S.E currents of the actual transmission line when the power angle $\delta_P$ between the S.E voltage $(V_{SE})$ and R.E voltage $(V_{RE})$ is fixed at +15°. Fig. 14(b) shows the PSCAD simulation of the line when scaled down to the emulator level following conversion in Table-III. Fig. 14(c) shows the experimental result from the developed emulator. Active power flow = 4 kW and reactive power flow = +3.3 kVAR.

*2) Step change in power angle & bus voltage:* Fig. 15(a)-(b) and Fig. 15(c) respectively show the PSCAD simulation and the hardware emulation result of the 3-phase S.E currents of the line when $\delta_P$ is changed from 0° to -15°. Note the 90° phase difference between the a-phase voltage and current as, the line draws only reactive power in steady state when $\delta_P = 0°$. Similarly, Fig. 16(a)-(b) and Fig. 16(c) respectively show the simulation and the hardware emulation result of the S.E currents when the R.E voltage $(V_{RE})$ is stepped up from 0.8 p.u to 1 p.u keeping $\delta_P$ fixed at +15°. It can be observed that the developed TLE based emulation very closely matches the PSCAD line simulation in all cases.

*3) Symmetrical faults:* Fig. 17(a) and (b) respectively show the PSCAD simulated and TLE emulated phase-$a$ S.E current response when the line is subjected to a 3-phase symmetrical fault at the R.E bus for 10 line cycles. In this case, the fault is triggered when the S.E voltage $(V_{SE})$ is passing through it's $+ve$ zero crossing. Fig. 18 demonstrate the emulator's ability to emulate faults occurring at any intermediate point on the line with a max. error of $\pm\frac{\Delta x}{2} = \pm\frac{c\Delta t_{obs}}{2} = \pm 6.2\ km$. Fig. 18(a) and (b) respectively show the PSCAD simulated and TLE emulated transient S.E and R.E currents when a 3-phase fault occurs at $174\,km$ from S.E of the $500\,km$ line.In all the cases, the captured fault dynamics in the TLE exhibit a high degree of matching with the PSCAD simulations.

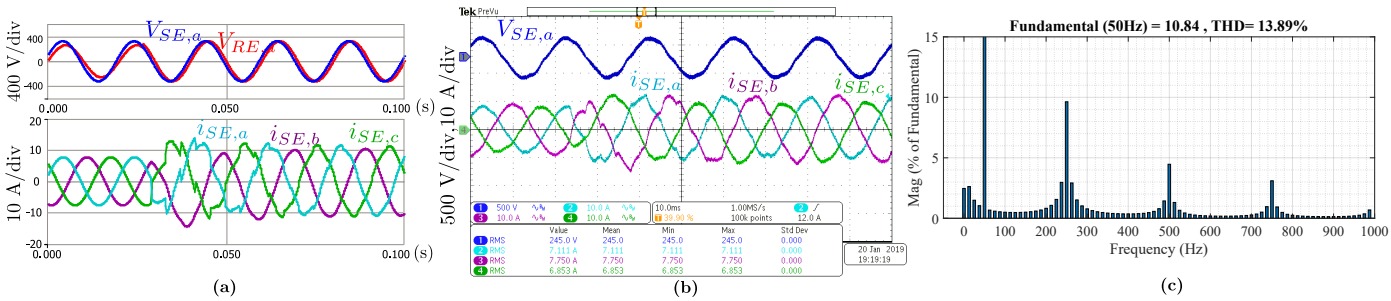


Fig. 16. (a) PSCAD simulation of step change in $V_{RE}$ (Bergeron), (b) TLE result using proposed method, (c) Harmonic analysis in line currents.

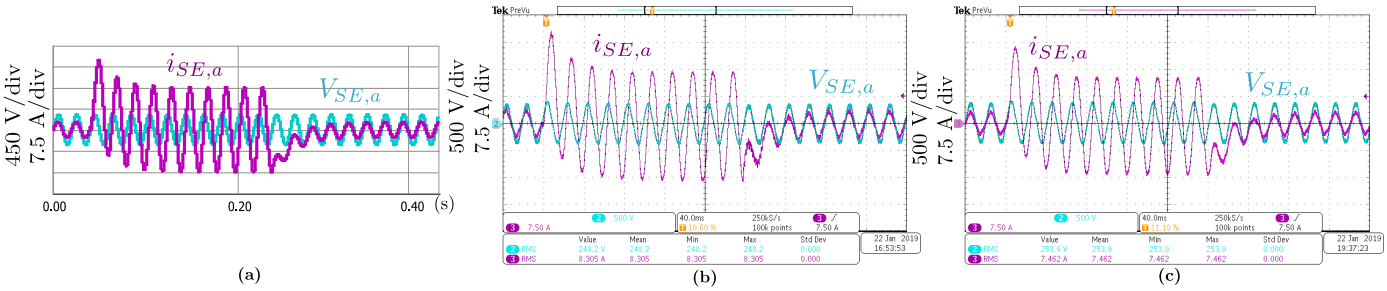


Fig. 17. Phase-$a$ current & voltage during 3-phase fault at R.E triggered at $+ve$ zero crossing of $V_{SE}$: (a) PSCAD simulation (Bergeron), (b) TLE emulation using proposed method, (c) TLE emulation using existing method.

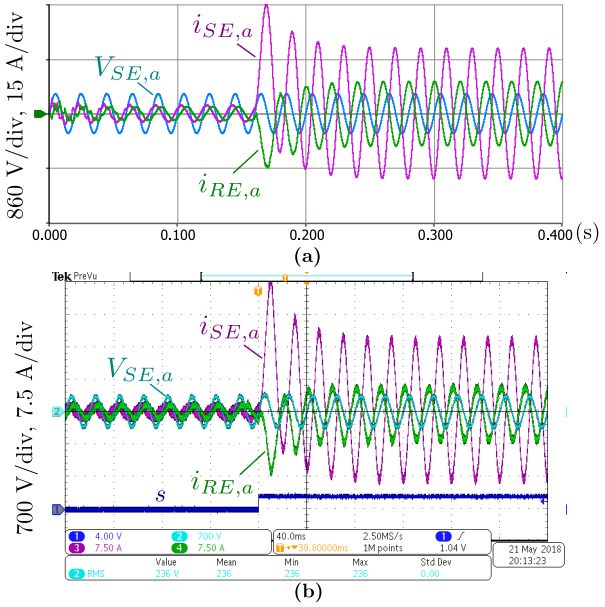


Fig. 18. Phase-$a$ S.E & R.E currents during a 3-phase fault at $174\ km$ from S.E of the $500\ km$ line: (a) PSCAD simulation, (b) TLE emulation.

## VI. Conclusion

The problem of medium and long transmission line emulation in steady state and symmetrical faults using power electronic converters has been addressed in this paper. Applicability of various line models for long line emulation in real-time has been investigated and a travelling wave-based numerical solution has been adopted which considers the uniform distribution of all line parameters as opposed to simple lumped models adopted in all previous attempts of line emulation. The developed emulator can also emulate faults occurring at an intermediate point on the line. Further, comprehensive analysis has been presented that helps the user to decide the correct power converter switching frequency and line model solution interval to be used to emulate a large set of lines with varying parameters and length while paying consideration to the power and digital hardware constraints of the emulator. Moreover, a novel digital architecture to implement the adopted numerical scheme in real-time on Zynq SoC-based digital platform has been outlined. The proposed emulation scheme along with the analysis provided, makes the developed platform (400 V, 15 kVA) an advanced and versatile transmission line emulator.

## Appendix

### A. Line Constants

$C_1 = A/B,\ C_2 = A'/B,\ C_3 = B'/B,\ C_4 = A'/(2A),\ C_5 = B'/(2A),\ C_6 = 0.5C_2,\ C_7 = 0.5C_3,$ where,

$$A = \left[\sqrt{LC} + \frac{G}{2}\sqrt{\frac{L}{C}}\Delta t_{obs}\right],\ B = \left[L + \frac{R\Delta t_{obs}}{2}\right]$$

$$A' = \left[\sqrt{LC} - \frac{G}{2}\sqrt{\frac{L}{C}}\Delta t_{obs}\right],\ B' = \left[L - \frac{R\Delta t_{obs}}{2}\right]$$

### B. Required computation load of observer using Bergeron method

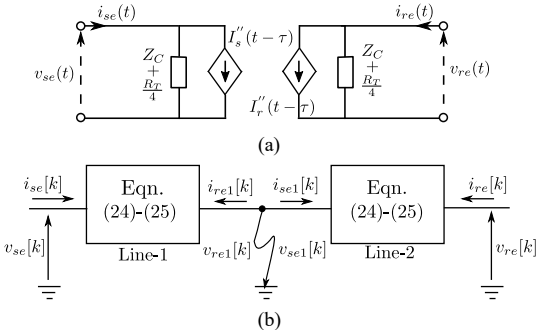


Fig. 19. (a) Bergeron model of a long transmission line, (b) Original line segmented into two parts at the fault point.

Referring to Fig. 19(a), prior to fault, the equations needed for solving the line end currents by Bergeron's Model are,

$$i_{se}(t) = K_1 v_{se}(t) + K_2 v_{se}(t-\tau) + K_3 i_{se}(t-\tau) + K_4 v_{re}(t-\tau) + K_5 i_{re}(t-\tau) \quad (24)$$

$$i_{re}(t) = K_1 v_{re}(t) + K_2 v_{re}(t-\tau) + K_3 i_{re}(t-\tau) + K_4 v_{se}(t-\tau) + K_5 i_{se}(t-\tau) \quad (25)$$

The constants $K_{1-5}$ depends on the line parameters. For two phases, the number of multiplications and additions involved are 20 and 16 respectively. In addition we need 8 FIFO buffers. The size of each buffers is $N = \left(\frac{\tau}{\Delta t_{obs}}\right)$. As $\Delta x = c\Delta t_{obs}$, $l = n\Delta x$ and $l = c\tau$, we have $N = n$. Now say, the fault has ocurred at $x = j\Delta x$. Hence the line will be segmented in two sections which will be solved using two separate Bergeron's Model (Fig.19(b)). To do this, the information of the voltage and current at the fault location prior to fault instant must be available. Since, the fault location can be chosen arbitrarily by the user, we need to solve and store pre-fault values of $v_j$ and $i_j$, $\forall\ j \in \{1, n-1\}$ to facilitate the fault computations. This is done using (26).

$$\begin{bmatrix} v_j[k] \\ i_j[k] \end{bmatrix} = \begin{bmatrix} \cosh\gamma(j\Delta x) & Z_c \sinh\gamma(j\Delta x) \\ \frac{1}{Z_c}\sinh\gamma(j\Delta x) & \cosh\gamma(j\Delta x) \end{bmatrix} \begin{bmatrix} v_{se}[k] \\ i_{se}[k] \end{bmatrix} \quad (26)$$

Therefore for each location, we need to maintain 2 FIFO buffers with size $n$. So total $4(n+1)$ buffers (each of size $n$) needs to be used and each buffer requires $n$ move operations to update it's contents. Further, using Cordic algorithm,

evaluation of each complex $\cosh$ and $\sinh$ function requires $2$ multiplications, $94$ additions and $48$ data shift operations. Hence, approximately $20(n-1)$ number of multiplications and $192(n-1)$ number of additions are required.

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