A Reduced Switch Count Single-Stage Three-Phase Bidirectional Rectifier With High-Frequency Isolation

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***Abstract*—Dual active bridge (DAB) based converters offer the benefit of smaller volume due to high-frequency isolation and controllability of active power flow, making them attractive for various applications, such as renewable energy generation, plug-in hybrid vehicles, and distribution systems. This paper presents a novel converter topology along with a modulation strategy for a DAB-based three-phase ac to dc converter. The major benefits are single-stage conversion, no unreliable intermediate dc-link capacitor, reduced number of switches, i.e., only two active switches on the ac side, simple control scheme, open-loop unity power factor operation, bidirectional power flow, and partial soft-switching. This paper presents the analysis of all the operating modes of the converter, resulting in the analytical estimation of power transfer and rms winding current and investigation of soft-switching conditions for the power devices. Simulation and experimental results have been presented to demonstrate the advantages of the proposed technique and accuracy of the analysis.[1]**

***Index Terms*—Dual active bridge (DAB), high-frequency (HF) link, isolated converter, power electronic transformer (PET), single stage, soft switching, solid-state transformer (SST), unity power factor, zero current switching (ZCS), zero voltage switching (ZVS).**

I. Introduction

GALVANIC isolation is a basic requirement when power converters are employed with different voltage levels, such as in grid integration of renewable energy generation systems. Fig. 1(a) shows a typical dc to three-phase ac conversion with a line frequency transformer (LFT) isolation. In a system like this, the LFT is one of the most expensive components and has a large footprint. The size and the cost of the isolation transformer can be reduced by increasing the frequency. In recent years, the solid-state transformer (SST) has been identified as a promising technology [2], [3] to replace LFTs. An SST is essentially an ac–ac converter with a high-frequency (HF) link and finds applications in ac motor drives [4], [5], power distribution systems [6], etc. An isolated HF-link ac–dc converter can replace few stages in a multistage SST in order to achieve higher power density and better reliability. These converters can be used for the integration of renewable energy sources, such as solar photovoltaics [7]–[9], energy storage [10], fuel cells [11], [12], chargers for electric vehicles [13], [14], rectification [15], and ac motor drives [16].

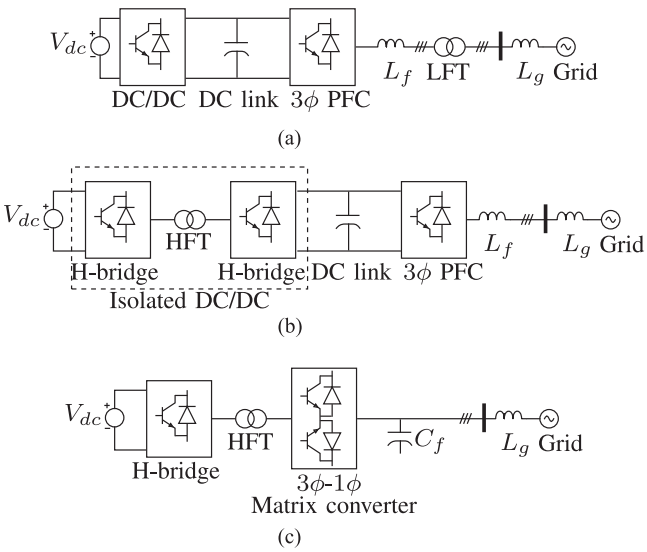

Fig. 1. (a) Conventional two-stage ac–dc converter with LFT. (b) Two-stage ac–dc converter with HFT. (c) Single-state ac–dc converter with HFT [14].

Isolated HF-link ac–dc converters proposed in the literature can be divided into two groups: multistage and single stage. Multi- or two-stage topologies typically involve a stage converting line frequency ac to a dc link followed by an isolated bidirectional dc–dc converter, as shown in Fig. 1(b). The isolated

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[1]This work was originally reported in [1]. Following improvements have been made 1) Extended the operation from only a single mode to four modes to get more utilization. 2) A detailed analysis for additional modes have been added 3) An entire section have been added to analyze softswitching conditions 4) Additional simulation results have been provided 4) Experimental results have been added.

dc–dc converter can either be dual active bridge (DAB) [17] based or may involve resonant power conversion [18]. Single-stage topologies provide a direct conversion of line frequency ac to dc without an intermediate dc link. Major advantage of a single-stage power conversion is the elimination of electrolytic dc-link capacitance and, thereby, increasing reliability and power density [19], [20].

Pulse width modulation (PWM) based single-stage three-phase HF-link bidirectional converters have been discussed in literature [19]–[25]. A DAB-based power conversion has significant advantage over PWM-based methods in high-power and high-voltage applications. In DAB-based solutions, the leakage inductance of the HF transformer (HFT) can be used for active power transfer.

In classical dc–dc DAB, two full-bridge inverters are modulated in a square wave mode with a phase shift, and active power is being transferred through the leakage inductance of the HFT [26]. A three-phase dc–dc version was first introduced in [27]. In [28], the dual-phase-shift modulation was introduced where both the bridges had been modulated with the same duty cycle. Considerable effort had been made to minimize conduction losses and to increase soft-switching range for single-phase [29]–[34] and three-phase dc–dc DAB [35].

A single-stage single-phase DAB-based ac–dc converter was first introduced in [36]. A full-bridge [36], [37] or a push–pull based matrix converter [38] can be used as the line frequency ac (LFac) to HFac converter. In [39] the LFac to HFac conversion was done with only two active switches. A multistage DAB-based single-phase ac–dc converter was proposed in [40]. It has a line-rectified double-frequency voltage link. In [14] and [41], a single-stage three-phase ac to dc DAB-based converter has been analyzed. As shown in Fig. 1(c), this converter employs a three-phase to single-phase matrix converter requiring 12 two-quadrant or active switches (a MOSFET or IGBT with an antiparallel diode) on the ac side and an H-bridge on the dc side of the single-phase HFT. The ac-side matrix converter converts the three-phase LFac to a quasi-square wave single-phase ac and applies it to the HFT. The dc-side H-bridge is operated to generate a duty cycle modulated square wave at the same frequency but with a phase shift to transfer active power. This paper proposes a novel single-stage DAB-based three-phase ac–dc converter that require only two active switches for three-phase LFac to HFac conversion. The proposed topology employs a three-phase voltage source inverter (VSI) in the dc side. This paper also presents a novel modulation strategy that results in bidirectional power flow, partial soft-switching, and power factor correction.

The paper is organized in nine sections. Section II introduces the topology and provides a detailed description of the proposed modulation technique, along with the operating modes that result from the proposed switching strategy. Section III presents the switching frequency analysis of the converter for the computation of active power flow and rms winding current. The results in Section III are used to obtain line frequency quantities presented in Section IV. Soft switching has been discussed in Section V. Section VI describes a design procedure for the proposed converter and provides an estimate of converter losses. A comparison with two other topologies has been presented in Section VII, based on the analysis done in Section VI. In Section VIII, simulation and experimental results have been presented to validate the analysis. Section IX concludes this paper.

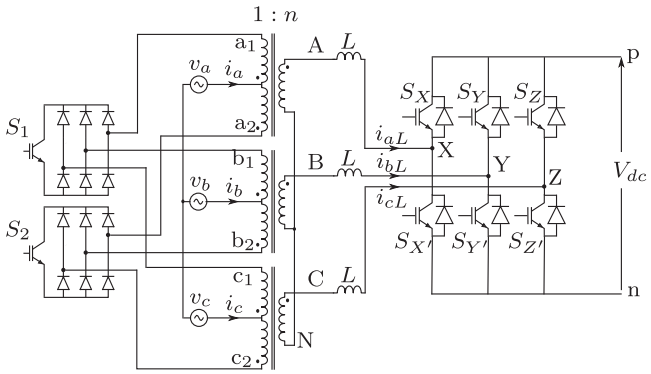


Fig. 2. Topology of the ac–dc converter.

II. Topology Description and Modulation Technique

The proposed topology is shown in Fig. 2. For each phase, it employs one three-winding transformer with turns ratio $1:n$. The common terminal of the two primary windings of each transformer is connected to one of the three input phases v_a, v_b, and v_c. The other terminals of each primary winding are connected in a push–pull configuration with two active switches S_1 and S_2 through a three-phase diode bridge.

The inductance L on the secondary side of the transformer represents the total leakage inductance of the transformer ($L = n^2 L_p + L_s$). If the designed value of L is larger than the leakage inductance, we need to add external inductance in series with the primary or secondary winding. The secondary-side converter is a two-level VSI. It is connected to a dc source with voltage $V_{\rm dc}$.

The primary-side voltages are assumed to be sinusoidal and balanced with frequency $\omega = 2\pi f = \frac{2\pi}{T}$ and amplitude $V_{\rm grid}$, with phase a voltage defined in (1). The primary-side switches S_1 and S_2 are switched in a complimentary manner with a 50% duty ratio at a frequency $f_s = 1/T_s$, such that $f_s >> f$. Thus, the secondary-side voltages are HF square waves with a line frequency sinusoidal envelope, as defined in (2). The switching signals q_{S_1} and q_{S_2} of S_1 and S_2, respectively, phase a, and secondary winding voltage v_{AN} are shown in Fig. 3(a)

$$v_{\rm a} = V_{\rm grid} \sin(2\pi f t) \tag{1}$$

$$v_{AN} = \pm n v_{\rm a} = \pm n V_{\rm grid} \sin(2\pi f t) \quad (+ \text{ with } S_1 \text{ ON}, - \text{ with } S_2 \text{ ON}). \tag{2}$$

The secondary-side VSI is space vector modulated to generate phase voltages v_{XN}, v_{YN}, and v_{ZN}, which have the same average value as voltages v_{AN}, v_{BN}, and v_{CN}, respectively, over one half of switching period T_s. The space vector diagram of a two-level VSI is shown in Fig. 3(b). The figure shows six active vectors $\mathbf{U_1}$–$\mathbf{U_6}$ and two zero vectors $\mathbf{U_0}$ and $\mathbf{U_7}$. The vector $\mathbf{U_1}$ corresponds to the switching state (100), meaning that top switch of phase X and bottom switches of phases Y and Z are ON. Note that in each VSI leg, the top and bottom switches are switched in a complimentary fashion. $\mathbf{V_o}$ is the vector formed

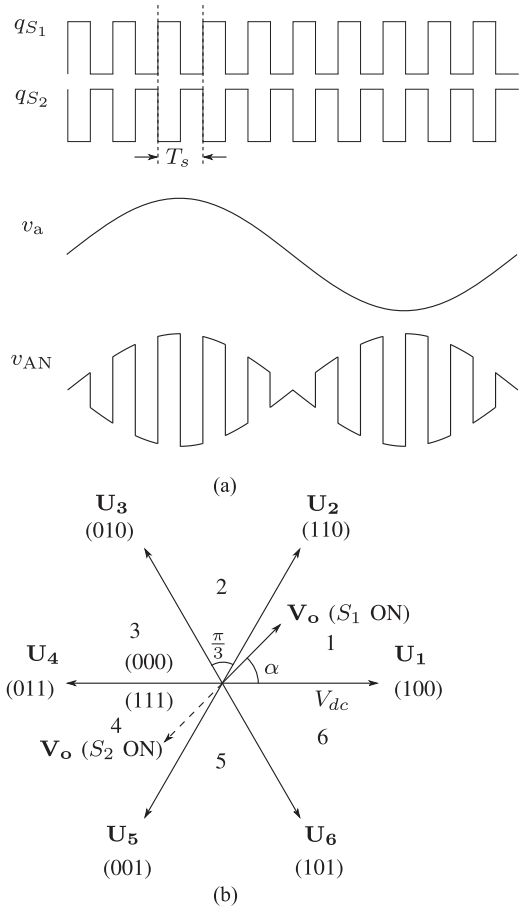


Fig. 3. (a) Primary-side modulation, phase a. (b) Space vectors of a two-level VSI.

by the transformer secondary voltages v_{AN}, v_{BN}, and v_{CN}

$$\mathbf{V_o} = v_{AN} + v_{BN}e^{j\frac{2\pi}{3}} + v_{CN}e^{-j\frac{2\pi}{3}}. \tag{3}$$

The VSI is PWM controlled to synthesize this vector in an average sense over each half of a switching period. In Fig. 3(b), $\mathbf{V_o}$ is in sector 1 when primary-side switch S_1 is ON. When the switch S_2 is ON, the secondary voltage polarity is reversed and the voltage vector, therefore, is rotated by 180° and is in sector 4.

The VSI pole voltages v_{Xn}, v_{Yn}, and v_{Zn} and phase voltages v_{XN}, v_{YN}, and v_{ZN} are related as follows:

$$v_{kN} = v_{kn} - \frac{1}{3}\sum_{j=X,Y,Z} v_{jn} \quad (k = X, Y, Z). \tag{4}$$

The pole and phase voltages of all three phases corresponding to each switching state of the VSI are given in Table I. Assume that the voltage vector $\mathbf{V_o}$ is in sector 1 when primary-side switch S_1 is turned ON, as shown in Fig. 3(b). The vector $\mathbf{V_o}$ is synthesized on an average over $\frac{T_s}{2}$ by applying VSI vectors $\mathbf{U_1}$ and $\mathbf{U_2}$ for time periods $\frac{d_1}{2}T_s$ and $\frac{d_2}{2}T_s$, respectively. Duty ratios d_1 and d_2 are defined in (5), and m is the modulation index defined in (6). The turns ratio n is adjusted such that $0 \le m < \frac{1}{\sqrt{3}}$. α is the angle between $\mathbf{V_o}$ and $\mathbf{U_1}$. For the rest of the first-half switching period $\frac{T_s}{2}$, the zero vector $\mathbf{U_0}$ is applied. When S_2 is ON, the vector $-\mathbf{V_o}$ is synthesized in an average sense over $\frac{T_s}{2}$ by applying vectors $\mathbf{U_4}$ and $\mathbf{U_5}$ for time periods $\frac{d_1}{2}T_s$ and $\frac{d_2}{2}T_s$, respectively. Note that $\mathbf{U_0}$ is again applied as zero state for the rest of the second-half switching period. The sequence of application of these vectors is $\mathbf{U_0}$-$\mathbf{U_1}$-$\mathbf{U_2}$-$\mathbf{U_1}$-$\mathbf{U_0}$-$\mathbf{U_5}$-$\mathbf{U_4}$-$\mathbf{U_5}$-$\mathbf{U_0}$, and the corresponding line to neutral voltage v_{XN} for phase X is given in Fig. 4

TABLE I
POLE AND PHASE VOLTAGES FOR DIFFERENT AVAILABLE SPACE VECTORS OF A VSI

Space Vector	Pole Voltages			Phase Voltages		
	v_{Xn}	v_{Yn}	v_{Zn}	v_{XN}	v_{YN}	v_{ZN}
$\mathbf{U_1}$	$V_{\rm dc}$	0	0	$\frac{2V_{\rm dc}}{3}$	$-\frac{V_{\rm dc}}{3}$	$-\frac{V_{\rm dc}}{3}$
$\mathbf{U_2}$	$V_{\rm dc}$	$V_{\rm dc}$	0	$\frac{V_{\rm dc}}{3}$	$\frac{V_{\rm dc}}{3}$	$-\frac{2V_{\rm dc}}{3}$
$\mathbf{U_3}$	0	$V_{\rm dc}$	0	$-\frac{V_{\rm dc}}{3}$	$\frac{2V_{\rm dc}}{3}$	$-\frac{V_{\rm dc}}{3}$
$\mathbf{U_4}$	0	$V_{\rm dc}$	$V_{\rm dc}$	$-\frac{2V_{\rm dc}}{3}$	$\frac{V_{\rm dc}}{3}$	$\frac{V_{\rm dc}}{3}$
$\mathbf{U_5}$	0	0	$V_{\rm dc}$	$-\frac{V_{\rm dc}}{3}$	$-\frac{V_{\rm dc}}{3}$	$\frac{2V_{\rm dc}}{3}$
$\mathbf{U_6}$	$V_{\rm dc}$	0	$V_{\rm dc}$	$\frac{V_{\rm dc}}{3}$	$-\frac{2V_{\rm dc}}{3}$	$\frac{V_{\rm dc}}{3}$
$\mathbf{U_0}$	0	0	0	0	0	0
$\mathbf{U_7}$	$V_{\rm dc}$	$V_{\rm dc}$	$V_{\rm dc}$	0	0	0

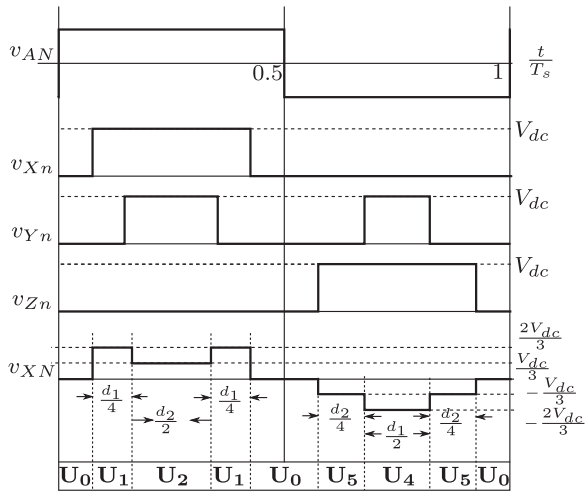


Fig. 4. Transformer secondary voltage v_{AN} followed by VSI pole voltages and phase voltage v_{XN} when $\mathbf{V_o}$ is in sector 1 (with S_1 on), over a switching cycle T_s.

$$d_1 = \sqrt{3}m\sin\left(\frac{\pi}{3} - \alpha\right)$$
$$d_2 = \sqrt{3}m\sin\alpha$$
$$d_z = 1 - d_1 - d_2 = 1 - \sqrt{3}m\cos\left(\alpha - \frac{\pi}{6}\right) \tag{5}$$
$$m = \frac{nV_{\rm grid}}{V_{\rm dc}}. \tag{6}$$

A phase shift between the voltages v_{AN} and v_{XN}, as shown in Fig. 5, (and corresponding voltages for other two phases)

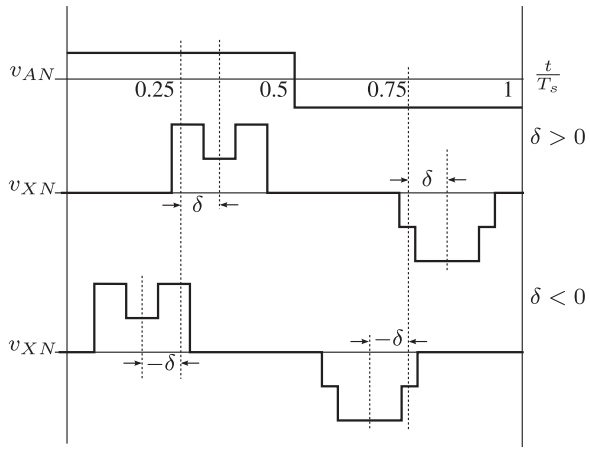


Fig. 5. Voltages in Mode I for positive and negative δ.

results in power flow. A positive time shift of δT_s results in power flow from ac to the dc source. A negative δ causes power flow in the opposite direction. δ lies in the range $(-\frac{1}{2}, \frac{1}{2})$. δ in the range $(-\frac{1}{4}, \frac{1}{4})$ results in the same power flow as in the range $(-\frac{1}{2}, -\frac{1}{4})$ and $(\frac{1}{4}, \frac{1}{2})$ but with a higher current in the latter range. Therefore, the range in which δ is controlled is restricted to $(-\frac{1}{4}, \frac{1}{4})$. For a given m, α, and δ, the converter may operate in five different modes, namely Mode I, Mode II, Mode IIIA, Mode IIIB, and Mode IV. These modes are illustrated in Fig. 6. The conditions for different modes is better understood in terms of a new variable $\delta' = 1 - 4\delta$. The range $(0, \frac{1}{4})$ of δ is mapped to a range of $(1, 0)$ (see Fig. 7). For a given m, α (hence d_1 and d_2), and δ', Table II presents the conditions for which the converter operates in these five modes. It should be noted that Mode IIIA occurs in first-half of sector when $d_2 < \delta' \leq d_1$, whereas Mode IIIB occurs in the second-half of the sector when $d_1 < \delta' \leq d_2$.

Fig. 8 shows plots d_1, d_2, and $d_1 + d_2$ for a given m as a function of α. If δ' is considered on the vertical axis, for a given m, each point in the δ'–α plane in Fig. 8 represents a specific operating point (m, δ', and α). The different shaded regions of the δ–α plane in Fig. 8(a) represent different modes. Fig. 8(a) also shows a graphical representation of Table II. It can be seen from this figure that for $\delta' > \sqrt{3}m$, the converter operates only in Mode I.

If $\frac{3}{2}m < \delta' \leq \sqrt{3}m$, the converter operates in Mode I for $\alpha\epsilon[0, \phi] \cup [\frac{\pi}{3} - \phi, \frac{\pi}{3}]$, with $\phi = \sin^{-1}(\frac{\delta'}{\sqrt{3}m}) - \frac{\pi}{3}$. For the rest of the values of α, the converter operates in Mode II. The conditions on δ' for a given value of m divide the possible range of $\delta'\epsilon(0, 1)$ in four distinct regions, namely R1, R2, R3, and R4. These regions are shown in Fig. 8(b). For a given value of δ' and m, the transition between different modes as α changes from 0 to $\frac{\pi}{3}$ is given in Table III.

III. Analysis in One Switching Period

The objective of this and the next section is the computation of two important quantities related to the operation and performance of the converter in terms of control variable δ. For

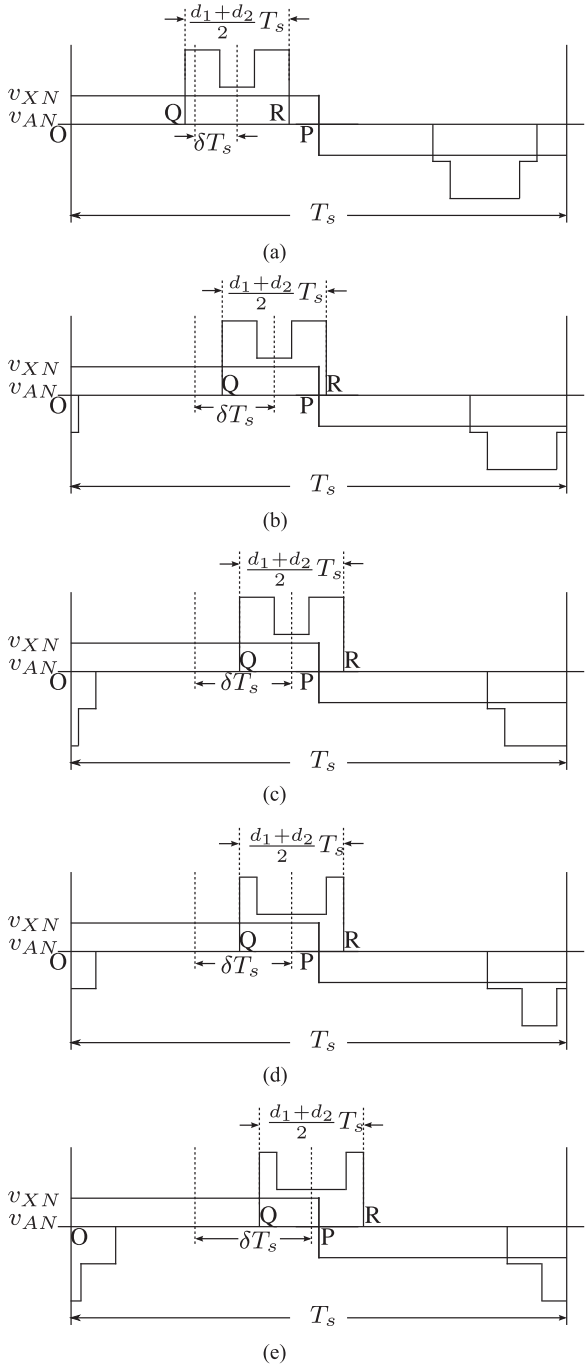


Fig. 6. Phase a voltage waveforms ($\mathbf{V_o}$ in sector 1 with S_1 ON): (a) Mode I, (b) Mode II, (c) Mode IIIA, (d) Mode IIIB, and (e) Mode IV.

Fig. 7. δ' versus δ.

TABLE II
CONDITIONS FOR DIFFERENT MODES FOR A GIVEN m, α, AND δ'

Mode	I	II	IIIA and IIIB	IV
Condition	$d_1 + d_2 < \delta' \leq 1$	$\max(d_1, d_2) < \delta' \leq d_1 + d_2$	$\min(d_1, d_2) < \delta' \leq \max(d_1, d_2)$	$0 < \delta' \leq \min(d_1, d_2)$

TABLE III
CONDITIONS FOR DIFFERENT REGIONS AND MODES FOR A GIVEN m AND δ' AS α MOVES FROM 0 TO $\pi/3$ IN A SECTOR

Region	Condition	ϕ	Modes		
			$0 < \alpha \leq \phi$	$\phi < \alpha \leq \frac{\pi}{3} - \phi$	$\frac{\pi}{3} - \phi < \alpha \leq \frac{\pi}{3}$
R1	$\sqrt{3}m < \delta' \leq 1$	0	I	I	I
R2	$\frac{3}{2}m < \delta' \leq \sqrt{3}m$	$\sin^{-1}\left(\frac{\delta'}{\sqrt{3}m}\right) - \frac{\pi}{3}$	I	II	I
R3	$\frac{\sqrt{3}}{2}m < \delta' \leq \frac{3}{2}m$	$\frac{\pi}{3} - \sin^{-1}\left(\frac{\delta'}{\sqrt{3}m}\right)$	IIIA	II	IIIB
R4	$0 < \delta' \leq \frac{\sqrt{3}}{2}m$	$\sin^{-1}\left(\frac{\delta'}{\sqrt{3}m}\right)$	IIIA	IV	IIIB

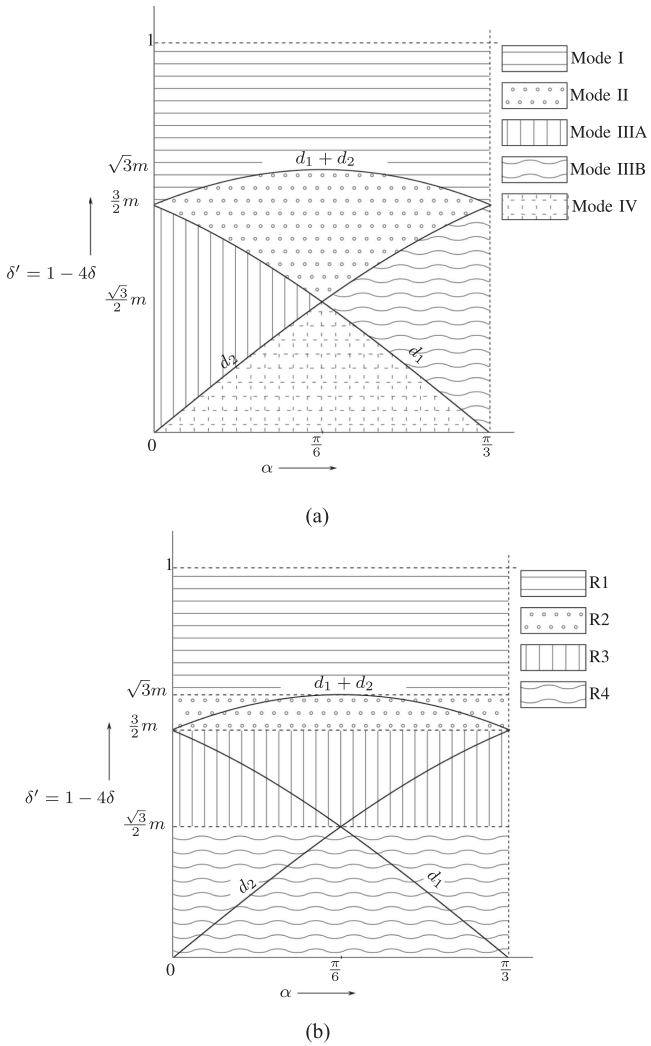


Fig. 8. Representation of (a) modes and (b) regions in the δ'–α plane for a given m.

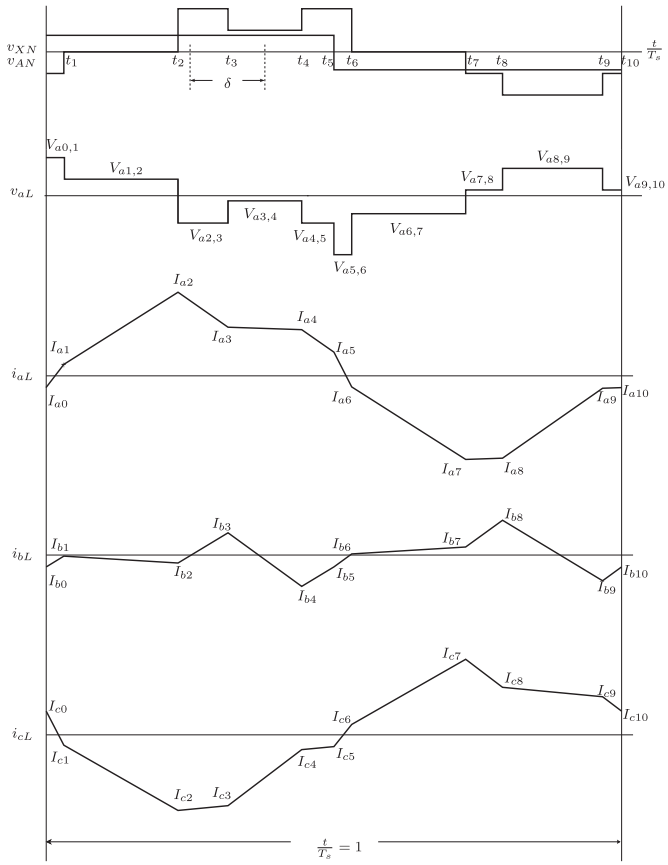


Fig. 9. Waveforms over one switching cycle in Mode II and $\delta > 0$.

a given m, these quantities are the rms of the transformer winding currents and the average active power transferred over a line cycle. To do this, first these quantities need to be computed over a switching cycle of period T_s. This section presents an outline for this computation.

TABLE IV
TIME INSTANTS AT WHICH VOLTAGE TRANSITIONS HAPPEN OVER A SWITCHING PERIOD IN MODE II AND POSITIVE δ

t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
$\left(\delta - \frac{d_z}{4}\right)$	$\left(\delta + \frac{d_z}{4}\right)$	$\left(\delta + \frac{(1-d_2)}{4}\right)$	$\left(\delta + \frac{(1+d_2)}{4}\right)$	$\frac{1}{2}$	$t_1 + \frac{1}{2}$	$t_2 + \frac{1}{2}$	$\left(\frac{1}{2} + \delta + \frac{(1-d_1)}{4}\right)$	$\left(\frac{1}{2} + \delta + \frac{(1+d_1)}{4}\right)$	1

TABLE V
INDUCTOR VOLTAGE EXPRESSIONS FOR PHASE a IN A SWITCHING PERIOD IN MODE II AND POSITIVE δ

$V_{a0,1}$	$V_{a1,2}$	$V_{a2,3}$	$V_{a3,4}$	$V_{a4,5}$	$V_{a5,6}$	$V_{a6,7}$	$V_{a7,8}$	$V_{a8,9}$	$V_{a9,10}$
$\left(nv_{\rm a} + \frac{V_{\rm dc}}{3}\right)$	$nv_{\rm a}$	$\left(nv_{\rm a} - \frac{2V_{\rm dc}}{3}\right)$	$\left(nv_{\rm a} - \frac{V_{\rm dc}}{3}\right)$	$V_{a2,3}$	$\left(-nv_{\rm a} - \frac{2V_{\rm dc}}{3}\right)$	$-nv_{\rm a}$	$\left(-nv_{\rm a} + \frac{V_{\rm dc}}{3}\right)$	$\left(-nv_{\rm a} + \frac{2V_{\rm dc}}{3}\right)$	$V_{a7,8}$

Given a phase-shift parameter δ and the applied input voltage vector, the waveforms of $v_{(A,B,C)N}$ and $v_{(X,Y,Z)N}$ can be determined over a switching cycle. The voltage across the inductor of each phase can be determined by taking the difference $v_{(A,B,C)N} - v_{(X,Y,Z)N} = v_{(a,b,c)L}$. Fig. 9 shows the voltage waveforms of v_{AN}, v_{XN}, and v_{aL} in Mode II. The various time instants t_1–t_{10} at which voltage transitions happen are given in Table IV. The levels of the voltage across the inductor in phase a are given in Table V

$$v_{aL} = L\frac{di_{aL}}{dt}. \tag{7}$$

By integrating (7), one can determine the inductor current from the inductor voltage v_{aL}. Note that in this case, a stepped v_{aL} waveform results in a piecewise linear waveform for current i_{aL}, which is given as

$$I_{ak} = I_{a(k-1)} + \frac{V_{a(k-1),k}}{L}(t_k - t_{k-1}), \quad k \epsilon [1,2,3,...,10]. \tag{8}$$

Assuming a quasi-steady-state operation, the volt-seconds across the inductor and the average current through inductor are zero

$$\int_0^{T_s} v_{aL}\,dt = 0$$
$$\int_0^{T_s} i_{aL}\,dt = 0. \tag{9}$$

Using (8) and (9), the current across the inductor can be completely determined and the waveform is illustrated in Fig. 9. This enables us to determine the square of rms of the inductor current (10) and the average active power transferred through phase a (11), over a switching cycle

$$< i_{aL,\rm RMS}^2 >_{T_s} (m,\delta,\alpha) = \frac{1}{T_s}\int_0^{T_s} i_{aL}^2\,dt \tag{10}$$

$$< P_a >_{T_s} (m,\delta,\alpha) = \frac{1}{T_s}\int_0^{T_s} v_{AN} i_{aL}\,dt. \tag{11}$$

The total power transferred through all three phases is given as

$$< P >_{T_s} (m,\delta,\alpha) = \sum_{j=a,b,c} < P_j >_{T_s} (m,\delta,\alpha). \tag{12}$$

A per unit system with base voltage $V_{\rm base} = V_{\rm dc}$ and base impedance $Z_{\rm base} = 2\pi f_s L$ is used for all the current and power expressions. The total average power transferred through the three phases in Mode II is given in (13) as shown at the bottom of this page. The rms currents through the three phases are given in (14) as shown at the bottom of the next page. for Mode II. Note that these quantities are function of the phase-shift parameter δ, along with the magnitude and position of the applied input voltage vector (m and α).

IV. POWER TRANSFER AND CURRENTS IN ONE LINE FREQUENCY PERIOD

In this section, the rms of transformer winding currents or the inductor currents and the average active power transferred over a line-cycle period T are presented. The square of rms of a phase current over a line cycle is the average of the square of rms of one-phase current computed over six sectors (15). The rms of the current over a line cycle is same for all three phases

$$< i_{L,\rm RMS}^2 >_T (m,\delta) = \frac{1}{6}\sum_{k=1,2...,6} < i_{a,\rm RMS}^2 >_{\text{Sector } k} (m,\delta). \tag{15}$$

Due to symmetry, the computed rms squared value is same over two diametrically opposite sectors, e.g., $< i_{a,\rm RMS}^2 >_{\text{Sector 1}}$

$$< P_{II} >_{T_s} (m,\delta,\alpha) = \frac{m\pi}{64}(24(m+4\delta m) - 3(4(1-4\delta)^2 + 9m^2)\cos(\alpha) + 12(1-4\delta)m\cos(2\alpha) - \sqrt{3}(4(1-4\delta)^2 + 15m^2 + 12m((-2+8\delta)\cos(\alpha) + m\cos(2\alpha)))\sin(\alpha)) \tag{13}$$

$(m,\delta) =< i^2_{a,\text{RMS}} >_{\text{Sector 4}} (m,\delta)$. Thus, the square of rms current is rewritten as

$$< i^2_{L,\text{RMS}} >_T (m,\delta) = \frac{1}{3} \sum_{k=1,3,5} < i^2_{a,\text{RMS}} >_{\text{Sector } k} (m,\delta). \tag{16}$$

Due to the three-phase symmetry, we have

$$\begin{aligned} &< i^2_{a,\text{RMS}} >_{\text{Sector 3}} (m,\delta) = < i^2_{b,\text{RMS}} >_{\text{Sector 1}} (m,\delta) \\ &< i^2_{a,\text{RMS}} >_{\text{Sector 5}} (m,\delta) = < i^2_{c,\text{RMS}} >_{\text{Sector 1}} (m,\delta). \end{aligned} \tag{17}$$

From (16) and (17), we get

$$< i^2_{L,\text{RMS}} >_T (m,\delta) = \frac{1}{3} \sum_{j=a,b,c} < i^2_{j,\text{RMS}} >_{\text{Sector 1}} (m,\delta). \tag{18}$$

The line-cycle rms currents are obtained by performing an rms calculation on the sector 1 rms currents for phase a, b, and c, as given by (18). A switching cycle "representative rms" defined in (19) is calculated by applying an rms calculation on the switching cycle rms currents for phase a, b, and c

$$< i^2_{L,\text{RMS}} >_{T_s} (m,\delta,\alpha) = \frac{1}{3} \sum_{j=a,b,c} < i^2_{jL,\text{RMS}} >_{T_s} (m,\delta,\alpha). \tag{19}$$

Given m and δ, the converter operates in one of the four regions, as given in Table III. For a given region, the converter operates in Mode X when $\alpha\epsilon[0,\phi] \cup [\frac{\pi}{3}-\phi, \frac{\pi}{3}]$, where Mode X and expression for ϕ are given in Table III for each region. For the rest of the sector, i.e., $\alpha\epsilon(\phi, \frac{\pi}{3}-\phi)$, the converter operates in Mode Y, again given in Table III. For example, when the region is R2, then $\phi = \sin^{-1}\left(\frac{\delta'}{\sqrt{3}m}\right) - \frac{\pi}{3}$, Mode X = Mode I, and Mode Y = Mode II. Thus, the rms of the transformer current over a line cycle is computed as given in (20) as shown at the bottom of this page and is the same as that of the ac line current where Ψ = R1, R2, R3, and R4. The expressions for per unit rms of the inductor current over a line cycle for all four regions are given in (21) as shown at the bottom of the next page. Note that the expressions for regions R3 and R4 are identical.

$$\begin{aligned}
< i_{aL,\text{RMS}_{II}} >_{T_s} (m,\delta,\alpha) = \frac{\pi}{24\sqrt{2}} [&m(3m(-20+96\delta(3+2\delta)+9m^2) - 12(4(-1+4\delta)^3 \\
&+ 3(-1+30\delta)m^2)\cos(\alpha) + m(3(-20+96\delta(3+2\delta)+9m^2)\cos(2\alpha) \\
&- 216\delta m\cos(3\alpha) + \sqrt{3}(24(2-9\delta)m\sin(\alpha) - 9(4(1-4\delta)^2+3m^2)\sin(2\alpha) \\
&+ 8(4-27\delta)m\sin 3\alpha])))]^{\frac{1}{2}} \\
< i_{bL,\text{RMS}_{II}} >_{T_s} (m,\delta,\alpha) = \frac{m\pi}{24} [&-(-54m^2 + 36m\cos(\alpha) + 3(4+192\delta^2+9m^2)\cos(2\alpha) \\
&- 2\sqrt{3}m(8-27m\cos(\alpha)+28\cos(2\alpha))\sin(\alpha) + 12(1+48\delta^2)(-2 \\
&+ \sqrt{3}\sin(2\alpha)))]^{\frac{1}{2}} \\
< i_{cL,\text{RMS}_{II}} >_{T_s} (m,\delta,\alpha) = \frac{\pi}{24\sqrt{2}} [&m(3m(-20+96\delta(3+2\delta)+9m^2) - 6(4(-1+4\delta)^3 \\
&+ 3(-5+48\delta)m^2)\cos(\alpha) - 6m(4+192\delta^2+9m^2)\cos(2\alpha) + 216\delta m^2\cos(3\alpha) \\
&- 6\sqrt{3}(4(-1+4\delta)^3 + (1+72\delta)m^2)\sin(\alpha) + 48\sqrt{3}(-1+12\delta)m\sin(2\alpha) \\
&+ 8\sqrt{3}(4-27\delta)m^2\sin(3\alpha))]^{\frac{1}{2}}
\end{aligned} \tag{14}$$

$$\begin{aligned}
< i^2_{L,\text{RMS}_\Psi} >_T (m,\delta) &= \frac{6}{T}\left(\int_0^{\frac{\phi}{\omega}} < i^2_{L,\text{RMS}_{\text{Mode } X}} >_{T_s} (m,\delta,\alpha)dt + \int_{\frac{\phi}{\omega}}^{\frac{\frac{\pi}{3}-\phi}{\omega}} < i^2_{L,\text{RMS}_{\text{Mode } Y}} >_{T_s} (m,\delta,\alpha)dt \right. \\
&\quad \left. + \int_{\frac{\frac{\pi}{3}-\phi}{\omega}}^{\frac{\frac{\pi}{3}}{\omega}} < i^2_{L,\text{RMS}_{\text{Mode } X}} >_{T_s} (m,\delta,\alpha)dt \right) \\
&= \frac{3}{\pi}\left(\int_0^{\phi} < i^2_{L,\text{RMS}_{\text{Mode } X}} >_{T_s} (m,\delta,\alpha)d\alpha + \int_{\phi}^{\frac{\pi}{3}-\phi} < i^2_{L,\text{RMS}_{\text{Mode } Y}} >_{T_s} (m,\delta,\alpha)d\alpha \right. \\
&\quad \left. + \int_{\frac{\pi}{3}-\phi}^{\frac{\pi}{3}} < i^2_{L,\text{RMS}_{\text{Mode } X}} >_{T_s} (m,\delta,\alpha)d\alpha \right)
\end{aligned} \tag{20}$$

Due to symmetry, the average active power transferred over a sector is same as that over a line cycle. The average active power transferred over a line cycle for a particular region is computed by integrating the switching cycle average power (22) as shown at the bottom of this page.

The expressions for average power transferred over a line cycle are given in (23) as shown at the bottom of this page for all four regions.

An analysis for current total harmonic distortion (THD) is now done. The rms current in the primary side is given as

$$< i_{\mathrm{pr,RMS}} >_T (m,\delta) = n < i_{L,\mathrm{RMS}} >_T (m,\delta) \tag{24}$$

The primary-side rms voltage in per unit is given in (25), and the rms value of fundamental component of primary-side current is given in (26)

$$< v_{\mathrm{pr,RMS}} >_T (m,\delta) = \frac{V_{\mathrm{pr}}}{\sqrt{2}}\frac{1}{V_{\mathrm{dc}}} = \frac{m}{n\sqrt{2}} \tag{25}$$

$$\begin{aligned} < i_{\mathrm{pr,1,RMS}} >_T (m,\delta) &= \frac{< P >_T (m,\delta)}{3 < v_{\mathrm{pr,RMS}} >_T (m,\delta)} \\ &= \frac{n\sqrt{2} < P >_T (m,\delta)}{3m}. \end{aligned} \tag{26}$$

The ripple current is given in (27) as shown at the bottom of the next page. Using (26) and (27), the current THD is computed in (28) as shown at the bottom of the next page. It should be noted that while the analysis done so far is only for positive values of δ, it can be extended to the negative range of δ. For negative values of δ, the power transferred is of the same magnitude, but

$$\begin{aligned} < i_{L,\mathrm{RMS}_{R1}} >_T (m,\delta) &= \frac{m\sqrt{\pi}}{48}\sqrt{-560\sqrt{3}m + 27m^2(3\sqrt{3}+8\pi) + 96(\pi + 48\delta^2\pi)} \\ < i_{L,\mathrm{RMS}_{R2}} >_T (m,\delta) &= \frac{\sqrt{\pi}}{48}\Bigg[m\Bigg((48(1-4\delta)^3 + 936m^2(1-4\delta))\sqrt{3-\left(\frac{1-4\delta}{m}\right)^2} \\ &\quad + m(\sqrt{3}m(-560+81m) + 24(4+9m^2)\pi + 4608\delta^2\pi) - 216m(4(1-4\delta)^2 \\ &\quad + 3m^2)\cos^{-1}\left(\frac{1-4\delta}{\sqrt{3}m}\right)\Bigg)\Bigg]^{\frac{1}{2}} \\ < i_{L,\mathrm{RMS}_{R3,R4}} >_T (m,\delta) &= \frac{\sqrt{\pi}}{24}\Bigg((6m(1-4\delta)^3 + 117m^3(1-4\delta))\sqrt{3-\left(\frac{1-4\delta}{m}\right)^2} + 2\sqrt{3}((1-4\delta)^4 - 2(17 \\ &\quad + 72\delta)m^3) + 48(-1+12\delta)m^2\pi + 27m^2(4(1-4\delta)^2 + 3m^2)\sin^{-1}\left(\frac{1-4\delta}{\sqrt{3}m}\right)\Bigg)^{\frac{1}{2}} \end{aligned} \tag{21}$$

$$\begin{aligned} < P_{R\Psi} >_T (m,\delta) = \frac{3}{\pi}\Bigg(&\int_0^{\phi} < P_{\text{Mode } X} >_{T_s} (m,\delta,\alpha)d\alpha + \int_{\phi}^{\frac{\pi}{3}-\phi} < P_{\text{Mode } Y} >_{T_s} (m,\delta,\alpha)d\alpha \\ &+ \int_{\frac{\pi}{3}-\phi}^{\frac{\pi}{3}} < P_{\text{Mode } X} >_{T_s} (m,\delta,\alpha)d\alpha\Bigg) \end{aligned} \tag{22}$$

$$\begin{aligned} < P_{R1} >_T (m,\delta) &= 3\delta m^2\pi \\ < P_{R2} >_T (m,\delta) &= -\frac{m\pi}{12}\Bigg((6m^2 + (1-4\delta)^2)\sqrt{3-\left(\frac{1-4\delta}{m}\right)^2} - 12\delta m\pi \\ &\quad - 9(1-4\delta)m\cos^{-1}\left(\frac{1-4\delta}{\sqrt{3}m}\right)\Bigg) \\ < P_{R3,R4} >_T (m,\delta) &= \frac{\pi}{72}\Bigg((-3m(1-4\delta)^2 - 18m^3)\sqrt{3-\left(\frac{1-4\delta}{m}\right)^2} - \sqrt{3}((1-4\delta)^3 + 9m^3) \\ &\quad + 18m^2\pi + 27(-1+4\delta)m^2\sin^{-1}\left(\frac{1-4\delta}{\sqrt{3}m}\right)\Bigg) \end{aligned} \tag{23}$$

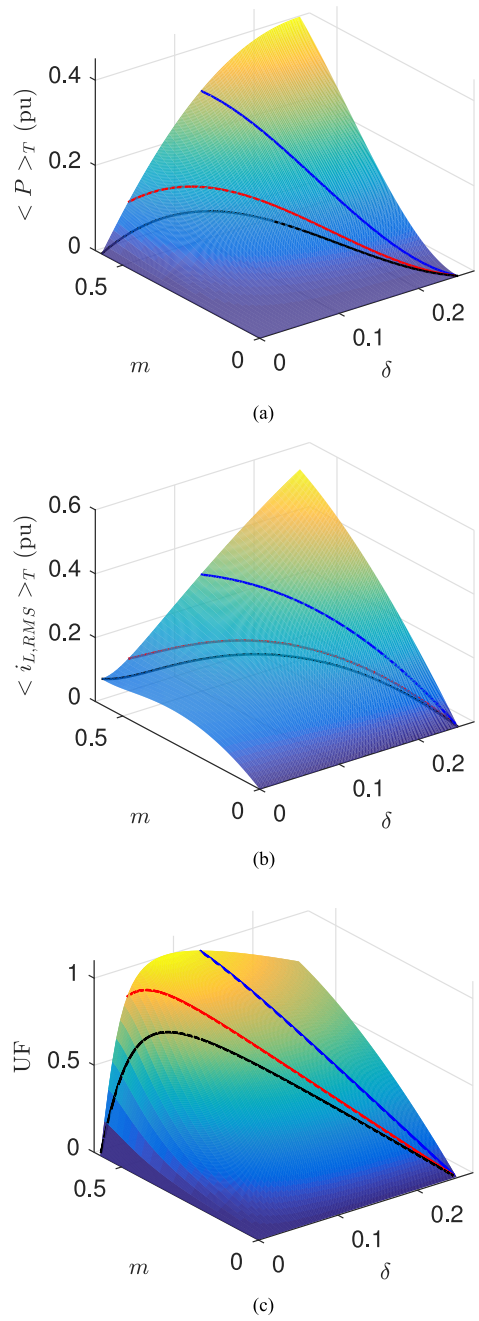


Fig. 10. (a) Average power versus δ and m. (b) Transformer secondary rms current versus δ and m. (c) Utilization factor versus δ and m (black, red, and blue curves on plots indicate R1, R2, and R3 boundaries, respectively).

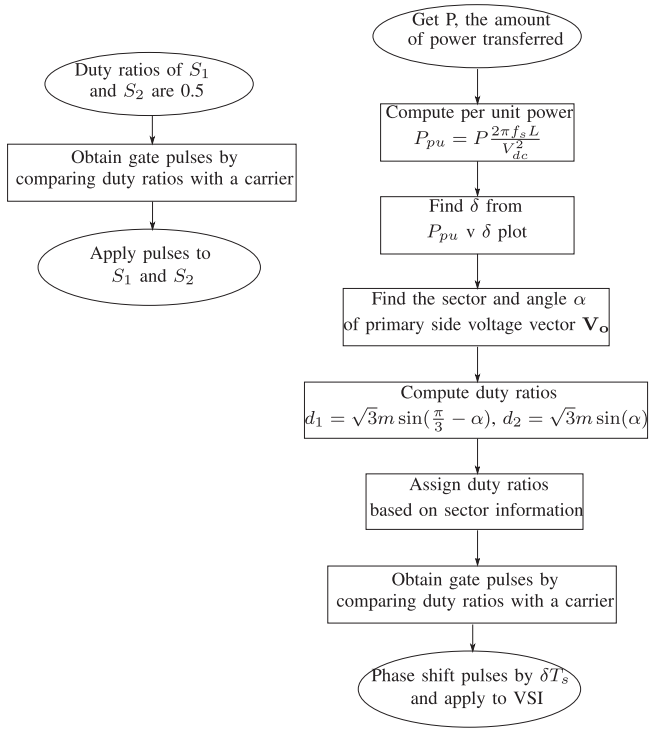


Fig. 11. Flowchart of the proposed modulation strategy.

changes sign (i.e., instead of flowing from ac to the dc, it flows in the opposite direction). Also, the rms quantities retain their expressions for negative δ.

The average power and transformer secondary rms current are plotted against δ and m in Fig. 10(a) and (b), respectively. The utilization factor of the converter is defined as UF $= \frac{<P>_T}{<i_L>_T}$. This is plotted against δ and m in Fig. 10(c). In each of the figures, the dashed lines denote the boundary between various regions of operation. From Fig. 10(a), it is observed that the maximum power transfer in Region R4 is approximately 0.41 p.u., which is more than three times the maximum power transfer of 0.12 p.u. in Region R1. The maximum utilization factor in Region R4 is 1.035 at $m = \frac{1}{\sqrt{3}}$ and $\delta = 0.08$, which is about 40% more than the utilization factor of 0.734 at $\delta = 0.0505$ and $m = 0.461$ that in Region R1, as shown in Fig. 10(c). Fig. 11 shows a flowchart describing how the gating signals for primary (q_{S_1}, q_{S_2}) and secondary (q_X, $q_{X'}$, q_Y, $q_{Y'}$, q_Z, $q_{Z'}$) side converters are generated for a given power transferred P and by sensing the ac and dc voltages.

$$< i_{\text{pr,rpl}} >_T (m,\delta) = \sqrt{< i^2_{\text{pr,RMS}} >_T (m,\delta) - < i^2_{\text{pr,1,RMS}} >_T (m,\delta)} \tag{27}$$

$$< \text{THD} >_T (m,\delta) = \frac{\sqrt{< i^2_{\text{pr,RMS}} >_T (m,\delta) - < i^2_{\text{pr,1,RMS}} >_T (m,\delta)}}{< i_{pr,1,\text{RMS}} >_T (m,\delta)}$$

$$= \sqrt{\frac{9m^2 < i^2_{L,\text{RMS}} >_T (m,\delta)}{2 < P^2 >_T (m,\delta)} - 1} = \sqrt{\frac{9m^2}{2\text{UF}^2} - 1} \tag{28}$$

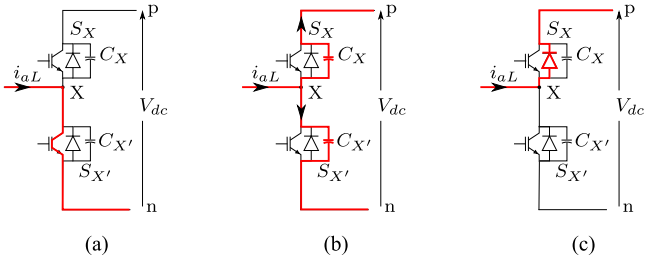


Fig. 12. Circuit diagrams to illustrate ZVS: (a) $S_{X'}$ conducting, (b) $S_{X'}$ and S_X capacitor charging and discharging, and (c) antiparallel diode of S_X conducting.

V. Soft Switching

The primary-side switches S_1 and S_2 undergo soft switching during dead time [zero current switching (ZCS)] in Mode I, as discussed in [1]. The waveform of i_{aL} is shown in Fig. 9 for Mode II with positive δ. It is observed that the current i_{aL} has a nonzero value I_{a5} when the primary switches S_1 and S_2 are switching. This also holds true for phases b and c currents in Mode II. Therefore, the current through the primary-side switches S_1 and S_2 is not zero when they switch. This implies they undergo hard switching in Mode II. This is also true for Modes IIIA, IIIB, and IV.

What follows next is a discussion on the switching of the secondary-side VSI. Consider the case when $\delta > 0$ and the converter is operating in Mode II, as shown in Fig. 9. Consider the transition at time t_2. Prior to time t_2, the switch $S_{X'}$ is ON and the current i_{aL} has a positive value I_{a2}, as shown in Fig. 12(a). At time t_2, switch $S_{X'}$ is turned OFF. The current then starts to flow through the capacitors C_X and $C_{X'}$. The initial voltage across C_X is equal to the dc voltage $V_{\rm dc}$ and it is discharged toward zero, whereas the capacitor $C_{X'}$ is charged toward $V_{\rm dc}$ from zero, as shown in Fig. 12(b). Since it takes some time to charge the capacitor $C_{X'}$, the turn OFF of $S_{X'}$ happens almost at zero voltage [zero voltage switching (ZVS)]. When the charging and discharging of the capacitors is complete, the antiparallel diode of S_X starts to conduct, as shown in Fig. 12(c). If the turn ON of S_X happens after the discharging of C_X is complete, then the turn ON of S_X is ZVS as the antiparallel diode is conducting. Thus, if the current in a phase is positive when transition from lower switch to upper switch happens, ZVS occurs in that phase. Similarly, if the current in a phase is negative when transition happens from upper to lower switch, ZVS occurs in that phase. It should be noted that whether the capacitors are discharged or charged in time to facilitate ZVS depends on the magnitude of the current, the value of capacitors C_X and $C_{X'}$, and the dc bus voltage. Thus, while the current being positive when the bottom switch turns OFF and the top switch is turns ON after a deadtime is a prerequisite for ZVS, it does not guarantee it.

In the notation used here, $I_{\rm X}$ is the phase current when switch $S_{\rm X}$ turns ON and $I_{\rm X'}$ is the phase current when switch $S_{\rm X'}$ turns ON. For example, in Mode II for positive δ, $I_{\rm X} = I_{a2}$ and $I_{\rm X'} = I_{a6}$ in Fig. 9. The switching transition currents for phase Z are similarly called $I_{\rm Z}$ and $I_{\rm Z'}$. In Sector 1, the phase Y of the inverter generates one pulse when S_1 is ON, with the switching currents labeled $I_{\rm Y,1}$ and $I_{\rm Y',1}$. This phase generates another pulse when S_2 is ON, with the switching currents labeled $I_{\rm Y,2}$ and $I_{\rm Y',2}$. See v_{YN} waveform in Fig. 4.

In general, $I_{\rm X}$ and $I_{\rm X'}$ are functions of δ, α, and m. Tables VI and VII are used to describe these functions in Sector 1 for positive values of δ. For example, in Mode II, $I_{\rm X} = f_1(k=0)$ and $I_{\rm X'} = -f_1(k=1)$ for positive values of δ. For ZVS turn off of $S_{\rm X'}$ and ZVS turn on of $S_{\rm X}$, $I_{\rm X}$ must be positive. Plots for $I_{\rm X}$ are given for entire range of positive δ, $0 \le \alpha < \frac{\pi}{3}$ and three values of m are given in Fig. 13. This shows that $I_{\rm X}$ is positive in all modes for $\delta > 0$ in Sector 1. Similarly, it is possible to show that the soft-switching condition is met for leg current in phases X and Z for $\delta > 0$ in Sector 1. The soft-switching condition for phase Y is met for entire Sector 1 and $\delta > 0$ only for top to bottom switch transition. The bottom to top switch transition in phase Y meets the soft-switching condition for a range of α as follows:

$$I_{\rm Y1} > 0 \quad \text{if} \quad \alpha \epsilon \left(\alpha^*, \frac{\pi}{3}\right)$$
$$I_{\rm Y2} > 0 \quad \text{if} \quad \alpha \epsilon \left(0, \frac{\pi}{3} - \alpha^*\right). \tag{29}$$

The angle α^* is given by the solution of

$$(3m\sin(\alpha^*) - 4\sqrt{3}\delta)\cos\left(\alpha^* + \frac{\pi}{3}\right) + \sin(\alpha^*) = 0. \tag{30}$$

For $\delta < 0$, the expressions for currents at switching transitions are given in Table VIII. The plots of $I_{\rm X}$ are given for entire range of negative δ, $0 \le \alpha < \frac{\pi}{3}$, and three values of m in Fig. 14, showing that the soft-switching condition is met for bottom to top transition when $\delta < 0$. Similarly, it is possible to show that all switching transitions in phases X and Z (top to bottom and bottom to top) and the bottom to top transitions in phase Y meet the soft-switching condition for $\delta < 0$. For the top to bottom transition in phase Y, soft-switching condition is met only for a certain range of α. Due to symmetry, similar conclusions can be drawn for other sectors. For example, in Sector 2, the middle phase X is partially soft switched, whereas the other two phase legs Y and Z meet the soft-switching criterion for all switching transitions for the entire range of m, δ, and α.

VI. Design and Loss Computation

A. Converter Design

In this section, a design method for the proposed converter is provided. The given specifications for the design are the following:

1) peak ac voltage $V_{\rm pr}$;
2) dc voltage $V_{\rm dc}$;
3) rated power P;
4) switching frequency $f_s = \dfrac{1}{T_s}$.

The operating point should be chosen to minimize the rms current, as discussed in the Section IV. The highest utilization factor occurs at $m = \frac{1}{\sqrt{3}}$ and $\delta = 0.08$. Therefore, the turns ratio of the transformer should be $n = \frac{V_{\rm dc}}{\sqrt{3}V_{\rm pr}}$. At $m = \frac{1}{\sqrt{3}}$ and $\delta = 0.08$, the per unit power is $< P >_T \ (m = \frac{1}{\sqrt{3}}, \delta = 0.08) = 0.226$. The required inductance L is given in (31). Note that

TABLE VI
FUNCTIONS DESCRIBING CURRENTS AT SWITCHING INSTANTS IN SECTOR 1

Function	Expression
$f_1(k)$	$\frac{\pi m \cos(\alpha)}{2}\left((-1)^k\left(1-\sqrt{3}m\cos\left(\alpha-\frac{\pi}{6}\right)\right)+4\delta\right)$
$f_2(k)$	$\frac{\pi m}{6}\left(3((-1)^k\sqrt{3}m\sin(\alpha)-4\delta)\cos\left(\alpha+\frac{\pi}{3}\right)+(-1)^k\sqrt{3}\sin(\alpha)\right)$
$f_3(k)$	$\frac{\pi m}{6}\left(3\cos\left(\alpha+\frac{\pi}{3}\right)\left(4\delta-(-1)^k\sqrt{3}m\sin\left(\frac{\pi}{3}-\alpha\right)\right)+(-1)^k\sqrt{3}\sin\left(\frac{\pi}{3}-\alpha\right)\right)$
$f_4(k)$	$\frac{\pi m}{2}\left((-1)^k\left(1-\sqrt{3}m\cos\left(\alpha-\frac{\pi}{6}\right)\right)+4\delta\right)\sin\left(\alpha+\frac{\pi}{6}\right)$
$f_5(k)$	$\frac{m\pi}{6}\left(3\left(\sqrt{3}m\cos\left(\alpha+\frac{\pi}{6}\right)+(-1)^k 4\delta\right)\sin\left(\alpha-\frac{\pi}{6}\right)+3\cos\left(\alpha+\frac{\pi}{3}\right)-\sqrt{3}\sin(\alpha)\right)$
$f_6(k)$	$\frac{m\pi}{6}\left(3(\sqrt{3}m\sin(\alpha)+(-1)^k 4\delta)\cos\left(\alpha+\frac{\pi}{3}\right)+4\sin\left(\alpha-\frac{\pi}{6}\right)-\cos(\alpha)\right)$

TABLE VII
SWITCHING TRANSITION CURRENT EXPRESSIONS IN SECTOR 1 FOR POSITIVE δ

Current \ Mode	Mode I	Mode II	Mode III A	Mode III B	Mode IV
I_{X}	$f_1(k=0)$	$f_1(k=0)$	$f_1(k=0)$	$f_1(k=0)$	$f_1(k=0)$
$I_{\mathrm{X}'}$	$f_1(k=1)$	$-f_1(k=1)$	$-f_1(k=1)$	$-f_1(k=1)$	$-f_1(k=1)$
$I_{\mathrm{Y}1}$	$f_2(k=0)$	$f_2(k=0)$	$f_2(k=0)$	$f_2(k=0)$	$f_2(k=0)$
$I_{\mathrm{Y}'1}$	$f_2(k=1)$	$f_2(k=1)$	$f_2(k=1)$	$f_6(k=0)$	$f_6(k=0)$
$I_{\mathrm{Y}2}$	$f_3(k=0)$	$f_3(k=0)$	$f_3(k=0)$	$f_3(k=0)$	$f_3(k=0)$
$I_{\mathrm{Y}'2}$	$f_3(k=1)$	$f_3(k=1)$	$f_5(k=0)$	$f_3(k=1)$	$f_5(k=0)$
I_{Z}	$f_4(k=0)$	$f_4(k=0)$	$f_4(k=0)$	$f_4(k=0)$	$f_4(k=0)$
$I_{\mathrm{Z}'}$	$f_4(k=1)$	$-f_4(k=1)$	$-f_4(k=1)$	$-f_4(k=1)$	$-f_4(k=1)$

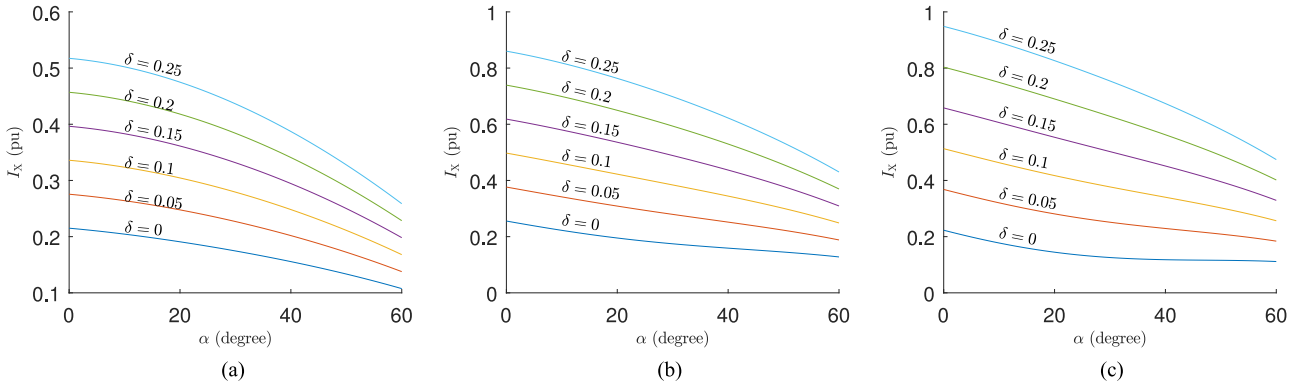


Fig. 13. I_{X} versus α for various values of $\delta \geq 0$ in Sector 1: (a) $m = \frac{1}{3\sqrt{3}}$, (b) $m = \frac{2}{3\sqrt{3}}$, and (c) $m = \frac{4}{5\sqrt{3}}$.

TABLE VIII
SWITCHING TRANSITION CURRENT EXPRESSIONS IN SECTOR 1 FOR NEGATIVE δ

Current \ Mode	Mode I	Mode II	Mode III A	Mode III B	Mode IV
I_{X}	$f_1(k=0)$	$-f_1(k=0)$	$-f_1(k=0)$	$-f_1(k=0)$	$-f_1(k=0)$
$I_{\mathrm{X}'}$	$f_1(k=1)$	$f_1(k=1)$	$f_1(k=1)$	$f_1(k=1)$	$f_1(k=1)$
$I_{\mathrm{Y}1}$	$f_2(k=0)$	$f_2(k=0)$	$f_2(k=0)$	$-f_6(k=1)$	$-f_6(k=1)$
$I_{\mathrm{Y}'1}$	$f_2(k=1)$	$f_2(k=1)$	$f_2(k=1)$	$f_2(k=1)$	$f_2(k=1)$
$I_{\mathrm{Y}2}$	$f_3(k=0)$	$f_3(k=0)$	$-f_5(k=1)$	$f_3(k=0)$	$-f_5(k=1)$
$I_{\mathrm{Y}'2}$	$f_3(k=1)$	$f_3(k=1)$	$f_3(k=1)$	$f_3(k=1)$	$f_3(k=1)$
I_{Z}	$f_4(k=0)$	$-f_4(k=0)$	$-f_4(k=0)$	$-f_4(k=0)$	$-f_4(k=0)$
$I_{\mathrm{Z}'}$	$f_4(k=1)$	$f_4(k=1)$	$f_4(k=1)$	$f_4(k=1)$	$f_4(k=1)$

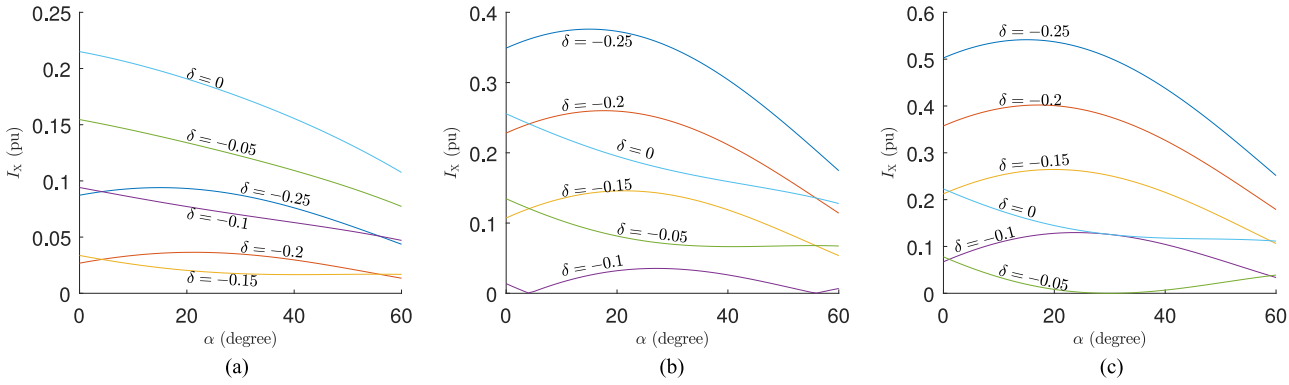


Fig. 14. I_X versus α for various values of $\delta \leq 0$ in Sector 1: (a) $m = \frac{1}{3\sqrt{3}}$, (b) $m = \frac{2}{3\sqrt{3}}$, and (c) $m = \frac{4}{5\sqrt{3}}$.

the inductance L represents the total leakage inductance of the transformer ($L = n^2 L_p + L_s$). If the designed value of L is larger than the leakage inductance, we need to add external inductance in series with the primary or secondary winding

$$0.226 = \frac{P}{\left(\frac{V_{\rm dc}^2}{2\pi f_s L}\right)}$$
$$\Rightarrow L = \frac{0.226}{P} \times \frac{V_{\rm dc}^2}{2\pi f_s}. \tag{31}$$

In the primary converter, the blocking voltage of the switches S_1 and S_2 is twice of maximum line–line voltage, i.e., $2\sqrt{3}V_{\rm pr}$, due to the push–pull action. The blocking voltage of the devices on the secondary side is $V_{\rm dc}$. The inductor rms current is computed as follows:

$$I_{2,\rm RMS} = \frac{V_{\rm dc}}{2\pi f_s L} < i_L >_T \left(m = \frac{1}{\sqrt{3}}, \delta = 0.08\right)$$
$$= \frac{V_{\rm dc}}{2\pi f_s L} \frac{< P >_T}{\rm UF} = \frac{P}{V_{\rm dc}} \frac{1}{\rm UF} = \frac{0.966P}{V_{\rm dc}}. \tag{32}$$

Due to the push–pull configuration, the primary-side rms current is given as follows:

$$I_{1,\rm RMS} = n\frac{I_{2,\rm RMS}}{\sqrt{2}} = \frac{V_{\rm dc}}{\sqrt{3}V_{\rm pr}} \frac{0.966P}{V_{\rm dc}} \frac{1}{\sqrt{2}} = \frac{0.394P}{V_{\rm pr}}. \tag{33}$$

In the primary-side converter, the diodes in each leg of the diode rectifiers will share the winding current equally over a line fundamental frequency period. Therefore, the rms current through the diodes in the primary-side converter is obtained as

$$I_{\rm pri,diode,RMS} = \frac{I_{1,\rm RMS}}{\sqrt{2}} = \frac{0.279P}{V_{\rm pr}}. \tag{34}$$

The rms currents through the primary-side converter switches and the upper and lower devices in the secondary-side VSI are obtained using simulations and given in the following equations:

$$I_{\rm pri,switch,RMS} = \frac{0.543P}{V_{\rm pr}} \tag{35}$$

$$I_{\rm sec,switch,upper,RMS} = \frac{0.648P}{V_{\rm dc}} \tag{36}$$

$$I_{\rm sec,switch,lower,RMS} = \frac{0.711P}{V_{\rm dc}}. \tag{37}$$

The peak current through the devices is equal to the maximum turn on current for the VSI in any given phase. Using Table VII, this is given as

$$I_{\rm sec,switch,peak} = \frac{mV_{\rm dc}}{4Lf_s}(1 - 1.5m + 4\delta) = \frac{1.823P}{V_{\rm dc}}$$
$$I_{\rm pri,switch,peak} = \frac{1.052P}{V_{\rm pr}}. \tag{38}$$

1) Conduction Losses: For estimating the device conduction losses, all devices are assumed as a resistor during ON state, with values $R_{\rm ON,pr}$ and $R_{\rm ON,sec}$ for primary- and secondary-side converters, respectively. The conduction losses are computed in (39) and (40).

$$P_{\rm pri,cond\text{-}loss} = (12I_{\rm pri,diode,RMS}^2 + 2I_{\rm pri,switch,RMS}^2)R_{\rm ON,pr}$$
$$= 1.524\frac{P^2}{V_{pr}^2}R_{\rm ON,}_{pr.} \tag{39}$$

$$P_{\rm sec,cond\text{-}loss} = 2(I_{\rm sec,switch,upper,RMS}^2 + I_{\rm sec,switch,lower,RMS}^2)R_{\rm ON,sec}$$
$$= 2.799\frac{P^2}{V_{\rm dc}^2}R_{\rm ON,sec.} \tag{40}$$

2) Switching Losses: The proposed converter would be designed at $m = \frac{1}{\sqrt{3}}$ and $\delta = 0.08$. With the chosen design parameters, the primary-side switches S_1 and S_2 undergo hard switching at turn off instants, while their turn on instants are soft switched because the currents in the corresponding primary-side windings start to build up from zero when they turn ON. The switching loss for the primary-side switch S_1 averaged over one switching period is

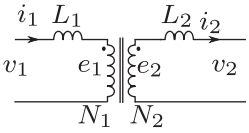


Fig. 15. Transformer equivalent circuit.

given as

$$< P_{\text{sw,loss},S_1} >_{T_s} (m,\delta,\alpha) = \frac{f_s}{2} V_{\text{clamp}} I_{S_1,\text{OFF}}(m,\delta,\alpha) t_{\text{sw,pr}} \tag{41}$$

where V_{clamp} is the clamp voltage, $t_{\text{sw,pr}}$ is the turn off time for S_1 (assumed fixed for different current values), and $I_{S_1,\text{OFF}}(m,\delta,\alpha)$ is the turn off current for S_1, which varies with α, m, and δ.

The switching loss in S_1 averaged over a sector is also equal to the switching loss averaged over a line frequency fundamental period, because of symmetry (42).

$$\begin{aligned} <P_{\text{sw,loss},S_1}>_T (m,\delta) &= \frac{3}{\pi}\int_0^{\frac{\pi}{3}} < P_{\text{sw,loss},S_1} >_{T_s} (m,\delta,\alpha) d\alpha \\ &= \frac{3}{\pi}\frac{f_s}{2} V_{\text{clamp}} t_{\text{sw,pr}} \int_0^{\frac{\pi}{3}} I_{S_1,\text{OFF}}(m,\delta,\alpha) d\alpha. \end{aligned} \tag{42}$$

The current flowing through the primary-side devices is equal to the absolute maximum of the three-phase ac currents. For $m = \frac{1}{\sqrt{3}}$ and $\delta = 0.08$, the following integral is obtained:

$$\int_0^{\frac{\pi}{3}} I_{S_1,\text{OFF}} \left(m = \frac{1}{\sqrt{3}}, \delta = 0.08, \alpha \right) d\alpha = n \frac{V_{\text{dc}}}{2\pi L f_s} 0.2919. \tag{43}$$

Hence, the total switching loss for both switches in the primary-side converter is obtained from (31), (42), and (43) and given in (44). Note that $V_{\text{clamp}} = 2\sqrt{3} V_{\text{pr}}$.

$$\begin{aligned} &< P_{\text{sw,loss,pri}} >_T \left(m = \frac{1}{\sqrt{3}}, \delta = 0.08 \right) \\ &= 2 < P_{\text{sw,loss},S_1} >_T \left(m = \frac{1}{\sqrt{3}}, \delta = 0.08 \right) \\ &= 1.2334 n \frac{V_{\text{clamp}} t_{\text{sw},pr} P f_s}{V_{\text{dc}}} = 2.467 t_{\text{sw},pr} P f_s \end{aligned} \tag{44}$$

For the secondary-side VSI, the phase with midvoltage has one hard switched transition per switching period when transitioning from bottom to top switch, for $0 \le \alpha \le \left(7.3\frac{\pi}{180}\right)$ and $\left(\frac{\pi}{3} - 7.3\frac{\pi}{180}\right) \le \alpha \le \frac{\pi}{3}$. For example, in Sector 1, the top switch phase Y of the secondary-side VSI undergoes hard switching for the range of α mentioned above. The switching loss for midphase of the secondary-side converter is similarly computed, first averaged over a switching period

$$< P_{\text{sw,loss,mid}} >_{T_s} (m,\delta,\alpha) = \frac{f_s}{2} V_{\text{dc}} I_{\text{mid,ON}}(m,\delta,\alpha) t_{\text{sw,sec}}. \tag{45}$$

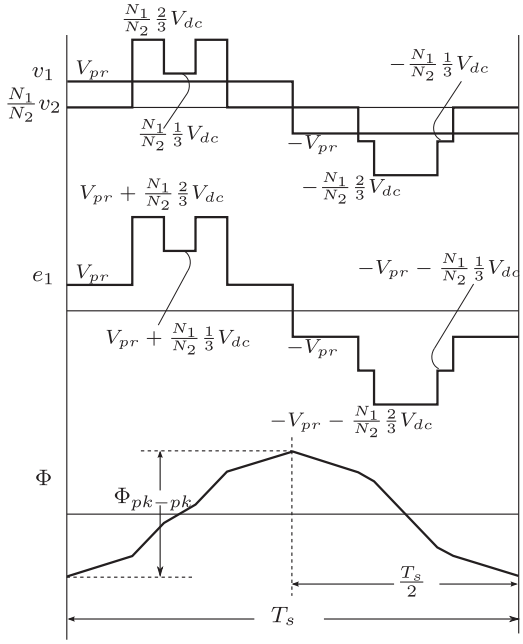


Fig. 16. Transformer voltages and flux.

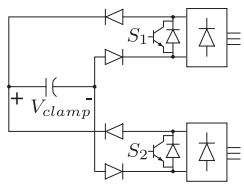


Fig. 17. Clamp circuit for a primary-side converter.

The quantity $t_{\text{sw,sec}}$ is the turn on time for VSI devices. The following integral is obtained for midphase turn on current:

$$\int_0^{\frac{7.3\pi}{180}} I_{\text{mid,ON}} \left(m = \frac{1}{\sqrt{3}}, \delta = 0.08, \alpha \right) d\alpha = \frac{V_{\text{dc}}}{2\pi L f_s} 0.0009. \tag{46}$$

The above-mentioned integral is for $0 \le \alpha \le 7.3\frac{\pi}{180}$. The integral for $\frac{\pi}{3} - 7.3\frac{\pi}{180} \le \alpha \le \frac{\pi}{3}$ is also obtained numerically and turns out to be same as that in (46); hence, the aforementioned expression will be multiplied by two for calculating total switching loss in the secondary-side converter. The total switching loss for the secondary-side converter averaged over a line frequency period (which is same as that averaged over a sector) is given in (47) as shown at the bottom of next page.

B. Transformer Design

A method for designing the transformer is discussed. In Fig. 15, a two-winding transformer is presented and is used to estimate the flux in the three-winding transformer used in the proposed topology.

TABLE IX
TOPOLOGY COMPARISON

		Scaling Factor	PFC+DAB	[14]	Proposed Topology
AC-side converter	no. of switches	–	10	12	2
	no. of diodes	–	–	–	12
	Blocking voltage	$V_{\rm pr}$	$\sqrt{3}$	$\sqrt{3}$	$2\sqrt{3}$
	RMS current through switches	$\frac{P}{V_{\rm pr}}$	0.333 (PFC), 0.667 (DAB)	0.651	0.543 (Switch), 0.279 (Diode)
	Peak current through switches	$\frac{P}{V_{\rm pr}}$	0.667 (PFC), 1.155 (DAB)	2.496	1.052
DC-side converter	no. of switches	–	4	4	6
	Blocking voltage	$V_{\rm dc}$	1	1	1
	RMS current through switches	$\frac{P}{V_{\rm dc}}$	1.155	1.376, 2.095	0.648, 0.711
	Peak current through switches	$\frac{P}{V_{\rm dc}}$	2.000	5.547	1.823
	no. of dc electrolytic capacitor	–	1	0	0
	no. of transformers	–	1	1	3

TABLE X
CONVERTER LOSS COMPARISON

		Scaling Factor	PFC+DAB	[14]	Proposed Topology
AC-side converter	Conduction loss	$\left(\frac{P}{V_{\rm pr}}\right)^2 R_{{\rm ON},pr}$	2.447	5.086	1.524
	Switching loss	$Pf_s t_{\rm sw,pr}$	1.104	0	2.467
DC-side converter	Conduction loss	$\left(\frac{P}{V_{\rm dc}}\right)^2 R_{\rm ON,sec}$	5.336	12.560	2.799
	Switching loss	$Pf_s t_{\rm sw,sec}$	0	0	0.004

Assuming that the transformer in Fig. 15 is ideal, the following equations hold:

$$\begin{aligned} v_1 &= L_1 \frac{di_1}{dt} + e_1 \\ e_2 &= L_2 \frac{di_2}{dt} + v_2 \\ e_2 &= \frac{N_2}{N_1} e_1 \\ I_1 &= \frac{N_2}{N_1} I_2. \end{aligned} \tag{48}$$

These equations can be solved to obtain e_1

$$e_1 = \frac{1}{2}\left(v_1 + \frac{N_1}{N_2} v_2\right) + \left(\left(\frac{N_1}{N_2}\right)^2 L_2 - L_1\right)\frac{di_1}{dt}. \tag{49}$$

If it is assumed that the series inductance L is equally distributed on the primary and secondary side, then $\left(\frac{N_1}{N_2}\right)^2 L_2 - L_1 = 0$. This gives

$$e_1 = \frac{1}{2}\left(v_1 + \frac{N_1}{N_2} v_2\right) = \left(\frac{v_1 + \frac{1}{n} v_2}{2}\right). \tag{50}$$

The voltage v_1, applied by the primary converter, has an amplitude V_1 equal to the instantaneous magnitude of primary-side ac voltage, while the voltage v_2 is generated by the secondary-side converter so that its average value is equal to v_1 in one half of switching period. Thus, the sum of v_1 and v_2 is largest when $\delta = 0$ and the primary-side voltage is at its peak value, i.e., $V_{\rm pr}$. Under these conditions, the transformer will have maximum flux buildup over a switching period. This corresponds to Mode I operation, with $\delta = 0$ and $V_1 = V_{\rm pr}$, shown in Fig. 16 for phase a.

$$\begin{aligned} < P_{\rm sw,loss,sec} >_T \left(m = \frac{1}{\sqrt{3}}, \delta = 0.08\right) &= 2\frac{3}{\pi}\frac{f_s}{2} V_{\rm dc} t_{\rm sw,sec} \int_0^{\frac{7.3\pi}{180}} I_{\rm mid,ON}\left(m = \frac{1}{\sqrt{3}}, \delta = 0.08, \alpha\right) d\alpha \\ &= 2\frac{3}{\pi}\frac{f_s}{2} V_{\rm dc} t_{\rm sw,sec} \frac{V_{\rm dc}}{2\pi L f_s} 0.0009 = 0.004 t_{\rm sw,sec} P f_s \end{aligned} \tag{47}$$

TABLE XI
TRANSFORMER COMPARISON

	Scaling Factor	PFC+DAB	[14]	Proposed Topology
RMS winding current (primary)	$\frac{P}{V_{\rm pr}}$	0.943	1.128	0.394
RMS winding current (secondary)	$\frac{P}{V_{\rm dc}}$	1.633	2.506	0.966
Maximum applied volt-seconds	$\frac{V_{\rm pr}}{f_s}$	1.732	1.732	1
Area product	$\frac{P}{f_s J B_{\max} K_w}$	0.817	0.977	0.336
Loss per transformer	K	0.859	0.983	0.441
no. of transformers	–	1	1	3
Turns ratio	–	$1:\left(\frac{0.577V_{\rm dc}}{V_{\rm pr}}\right)$	$1:\left(\frac{0.45V_{\rm dc}}{V_{\rm pr}}\right)$	$1{:}1{:}\left(\frac{0.577V_{\rm dc}}{V_{\rm pr}}\right)$

TABLE XII
THD VALUES (FOR FILTER COMPARISON)

PFC+DAB	[14]	Proposed Topology
THD_V	THD_I	THD_I
52.5%	167.03%	62.47%

TABLE XIII
CIRCUIT PARAMETERS FOR THREE-PHASE PET SIMULATION AND EXPERIMENTS

Parameter	Value
DC-link voltage ($V_{\rm dc}$)	135 V
Modulation index (m)	0.2, 0.35, 0.5
Line voltage rms	33.07 V, 57.87 V, 82.67 V
AC voltage frequency (f)	60 Hz
Switching period (T_s)	200 μs
δ	[−0.25,0.25] (steps of 0.05)
Secondary-side inductance (L)	480 μH
DC-link capacitor ($C_{\rm dc}$)	1.3 mF

The peak–peak flux and the average applied volt-seconds seen from the primary side in this scenario are found as follows:

$$\Phi_{\text{pk–pk,max}} = \frac{1}{N_1}\int_0^{\frac{T_s}{2}} e_1\,dt = \frac{T_s}{2N_1}V_{\rm pr} \tag{51}$$

$$< \text{VS} > = 2\Phi_{\text{pk–pk,max}} N_1 f_s = V_{\rm pr}. \tag{52}$$

The peak flux density $B_{\max}$ is related to the peak–peak flux through the transformer core area A_c

$$A_c B_{\max} = \frac{1}{2}\Phi_{\text{pk–pk,max}}. \tag{53}$$

The window area A_w, along with the window fill factor K_w, is related to the primary and secondary currents through the current density J. This is shown in (54) for the three-winding transformer

$$A_w K_w = 2\frac{N_1 I_{1,\rm RMS}}{J} + \frac{N_2 I_{2,\rm RMS}}{J} = (1+\sqrt{2})\frac{N_2 I_{2,\rm RMS}}{J}. \tag{54}$$

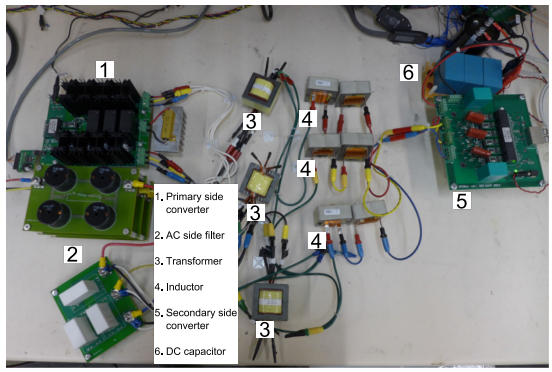


Fig. 18. Experimental setup.

Using (32) and (51)–(54), the product of core and window areas is then computed as follows:

$$A_c A_w = \frac{1}{2}\frac{\Phi_{\text{pk–pk,max}}}{B_{\max}} \times \frac{1}{K_w}(1+\sqrt{2})\frac{N_2 I_{2,\rm RMS}}{J}$$

$$\Rightarrow A_c A_w = \frac{m}{\rm UF}\frac{(1+\sqrt{2})}{4}\frac{P}{B_{\max}K_w J f_s} = \frac{0.336P}{B_{\max}K_w J f_s}. \tag{55}$$

The area product is a representation of the size of the core. It is possible to show that for a given core type and choices of J, $B_{\max}$, f_s core material, and volume of the core, the core and copper losses are proportional to ${A_c A_w}^{0.75}$ [42]. Thus, the losses can be written as $K(0.336)^{0.75} = 0.441$ K.

The primary-side switches S_1 and S_2 are not soft switched or zero current switched over a wide range of operating points and we need to add a clamping circuit shown in Fig. 17, to operate the two switches with a dead time. When one switch say S_1 is turned OFF,the upper halves of the primary winding currents circulate through the clamp circuit, when the bottom switch S_2 is turnedON after a dead time, the clamp circuit helps in commutation of the primary leakage inductance, for example, in this case the currents through the leakage inductance of the upper half of the primary winding becomes zero while the current

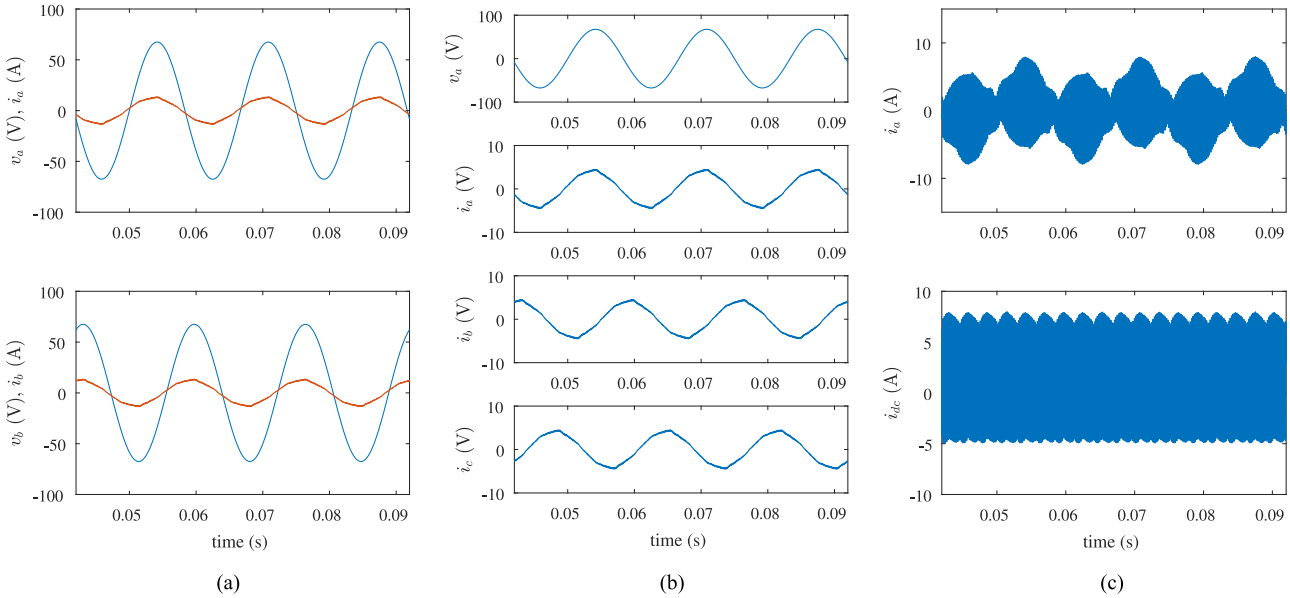


Fig. 19. Simulation results for three-phase PET for power transfer from ac to dc side. (a) Phase a voltage and filtered current (zoomed by three times) (top) and phase b voltage and filtered current (zoomed by three times) (bottom). (b) Phase a voltage (top) and filtered currents in three phases (bottom three waveforms). (c) Phase a unfiltered current (top) and unfiltered dc-link current (bottom).

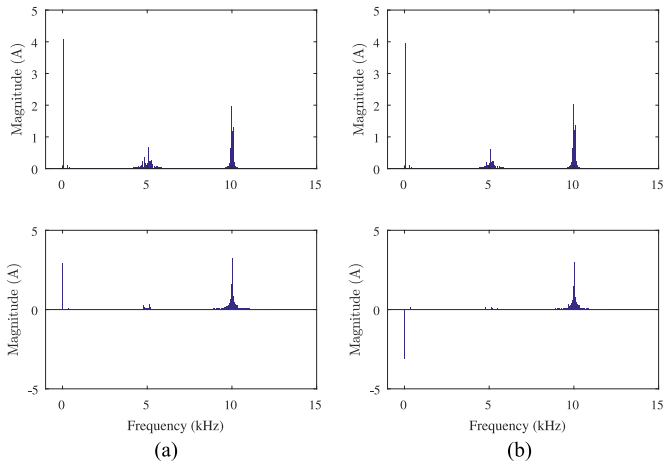


Fig. 20. Simulation results for (a) positive δ: frequency spectrum of unfiltered phase a current (top) and unfiltered dc-link current (bottom) and (b) negative δ: frequency spectrum of unfiltered phase a current (top) and unfiltered dc-link current (bottom).

through the lower half is build up to the corresponding secondary winding current.

VII. Comparison With Other Topologies

This section presents a detailed comparison of the proposed solution with 1) the standard two-stage solution of a three-phase active rectifier (PFC) followed by a DAB-based isolated dc–dc converter, shown in Fig. 1(b), and 2) the single-stage three-phase ac to dc DAB-based solution presented in [14], shown in Fig. 1(c).

The peak of the balanced input three-phase voltage is $V_{\rm pr}$ and its frequency is f, dc-side voltage is $V_{\rm dc}$. All comparisons are given at rated power P. The switching frequency of all switches are assumed to be f_s. Actual switching and conduction loss depends on on-state voltage drop across the switches and switching transition time ($t_{\rm sw}$) along with the electrical variables at the rated operating point. For simplicity of comparison, in the on state the conducting device is assumed to be a resistance same for all devices (switches and diodes) in the primary- or ac-side converter ($R_{{\rm ON},pr}$) and dc-side converter ($R_{\rm ON,sec}$). The turn on and turn off transition times are assumed to be equal and called $t_{\rm sw,pr}$ and $t_{\rm sw,sec}$ for the primary-side and secondary-side devices, respectively. Here, switch implies a power semiconductor device that can block voltage in one direction and allow current to flow in both directions, typically an IGBT or a power MOSFET with an antiparallel diode.

We have assumed the following.

1) The PFC is controlled with space vector PWM (SVPWM), and at full power (P), it is drawing current at unity power factor at maximum modulation index, $1/\sqrt{3}$. This implies that the dc-link voltage is $\sqrt{3}V_{\rm pr}$.

2) The DAB is modulated with phase-shift control and operated at $90^{\rm o}$ phase shift (one quarter of switching period) where transferred power is maximum. The turns ratio is set at $\frac{V_{\rm dc}}{\sqrt{3}V_{\rm pr}}$. This ensures soft switching (ZVS) in both bridges.

3) The solution given in [14] is designed to operate at rated condition with maximum utilization UF $= 0.399$, which occurs at $m = 0.45$ and $\delta = 0.0183$. Section VI provides the details of the design and computation of various performance related quantities used for comparison. The computation of these quantities for dc–dc DAB and the solution presented in [14] can be done in a similar way and are not included in this paper due to

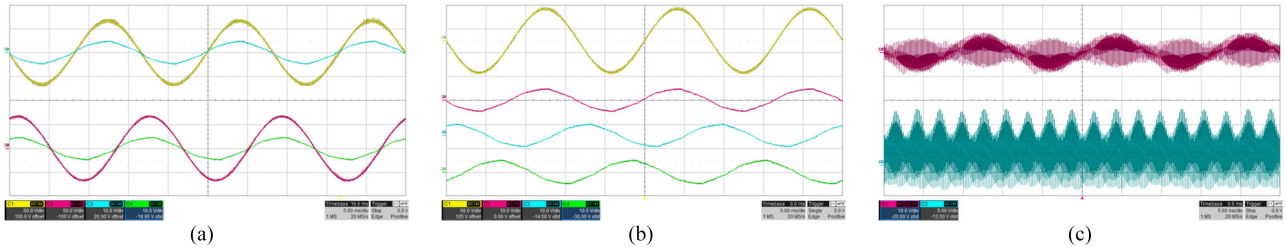


Fig. 21. Experimental results for three-phase PET for power transfer from ac to dc side: (a) phase a voltage and filtered current (top) and phase b voltage and filtered current (bottom) [50 V/div, 10 A/div], (b) phase a voltage (top) and filtered currents in three phases (bottom three waveforms) [50 V/div, 10 A/div], and (c) phase a unfiltered current (top) [10 A/div] and unfiltered dc-link current (bottom) [5 A/div].

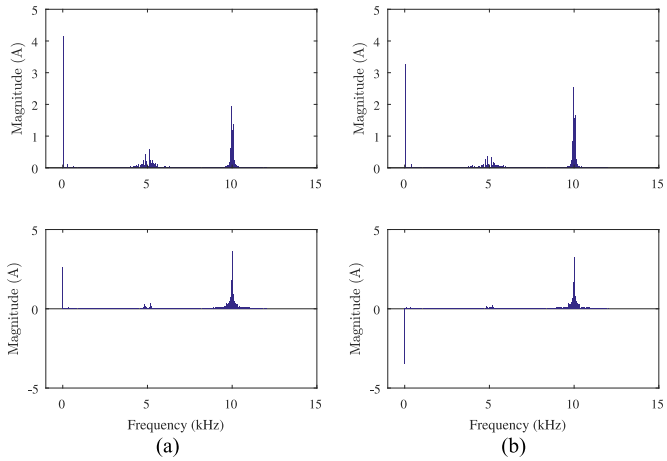


Fig. 22. Experimental results for (a) positive δ: frequency spectrum of unfiltered phase a current (top) and unfiltered dc-link current (bottom), and (b) negative δ: frequency spectrum of unfiltered phase a current (top) and unfiltered dc-link current (bottom).

size constraints. Appendix IX presents the computational details of the quantities given in this section that correspond to the PFC.

The ac-side converter for PFC+DAB solution consists of a three-phase (PFC) and single-phase bridge (part of DAB). Weise *et al.* [14] deploy a three-phase bridge with bidirectional switches, in this comparison, we have assumed that each of these switches are realized with the common emitter or common source connection of two regular switches. For PFC+DAB, [14], and dc-side converter of the proposed solution, a switch implies a MOSFET or an IGBT with an antiparallel diode. From Table IX, it can be seen that the proposed topology uses only 2 controlled switches along with 12 diodes. Although the blocking voltage is twice when compared with other two solutions, this is expected for push–pull configuration. While the rms currents are comparable, peak current in [14] is quite high. The dc-side converter in the proposed topology is a three-phase bridge, while that of the other two solutions is a single-phase bridge. Although the blocking voltage is same, the rms switch current is low for the proposed solution. Both peak and rms currents are high in [14]. The proposed topology uses minimum number of controlled switches without employing any electrolytic dc capacitor.

For the ac-side converter, the conduction loss is high in [14] but the switching loss is zero due to ZCS (see Table X). While the switching loss is higher in the proposed solution when compared with PFC+DAB solution, the conduction loss is lower. All three solutions achieve negligible switching loss in the dc-side converter due to ZVS. The conduction loss is much lower for the proposed solution.

The proposed topology deploys three HFTs where the primary has two equal windings. The other two solutions use a single two-winding transformer. As in the proposed solution, the entire power flow gets equally divided into three transformers, the rms winding currents are low in comparison with other solutions (see Table XI). Note that the rms current in the secondary winding in [14] is quite high. The maximum applied volt-seconds is comparatively low for the proposed solution. The area product is a representation of the overall size of the transformer. The value of this product for the proposed solution is approximately one third of that of other solutions. The overall loss in the transformer (both core and copper loss) is slightly higher in case of the proposed solution.

A. AC-Side Filter Comparison

Let us assume that at rated condition, the peak of the fundamental component of the input ac current be $I_{\rm pr}$, thus $I_{pr} = \frac{2P}{3V_{\rm pr}}$, because we assume unity power factor. The base impedance Z_b and base admittance Y_b are given as $Z_b = \frac{V_{\rm pr}}{I_{\rm pr}} = \frac{1}{Y_b}$. Also, $\omega_s = 2\pi f_s$. For the PFC+DAB solution, L_f can be used to filter out the HF components present at the switched output voltage of the inverter (PFC) [see Fig. 1(b)]. Let the voltage THD in the output line to neutral voltage of the inverter under SVPWM operation at maximum modulation index (i.e., the dc-link voltage of PFC is $V_{\rm dc,PFC} = \sqrt{3}V_{\rm pr}$) be $\text{THD}_v = \frac{\tilde{V}}{V_{\rm pr}}$, where $\frac{\tilde{V}}{\sqrt{2}}$ is the rms of the ripple component of the voltage.

Now, if we assume that all the ripple is at the switching frequency f_s (this leads to slight overdesign of the filter [43]), the ripple component of the line current will be $\tilde{I} = \frac{\tilde{V}}{\omega_s L_f}$. If we want to keep $\tilde{I}$ to be λ fraction ($<5\%$) of $I_{\rm pr}$, i.e., $\tilde{I} = \lambda I_{pr}$, then per unit filter impedance at the switching frequency will be inductive and is given as

$$Z_{f,\text{pu}} = \frac{\omega_s L_f}{Z_b} = \frac{\text{THD}_V}{\lambda}. \tag{56}$$

Similarly, for the proposed topology, if we want the ripple voltage $\tilde{V}$ to be a fraction λ of $V_{\rm pr}$, then the per unit capacitive

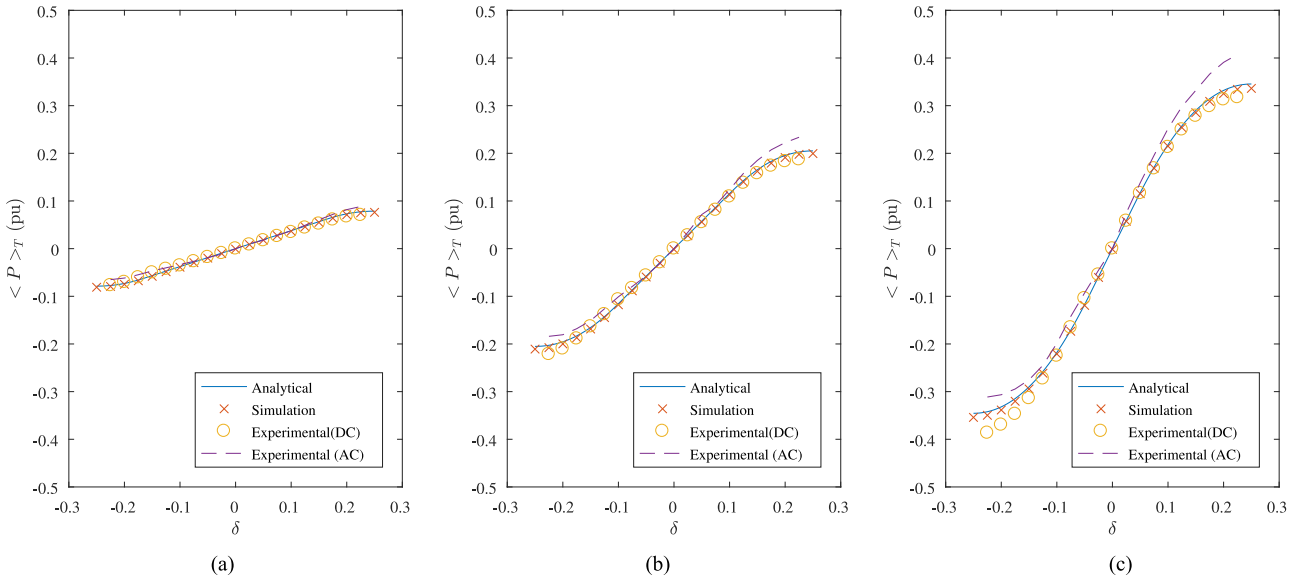


Fig. 23. Comparison of analytical, simulation, and experimental results for power transfer: (a) $m = 0.2$, (b) $m = 0.35$, and (c) $m = 0.5$.

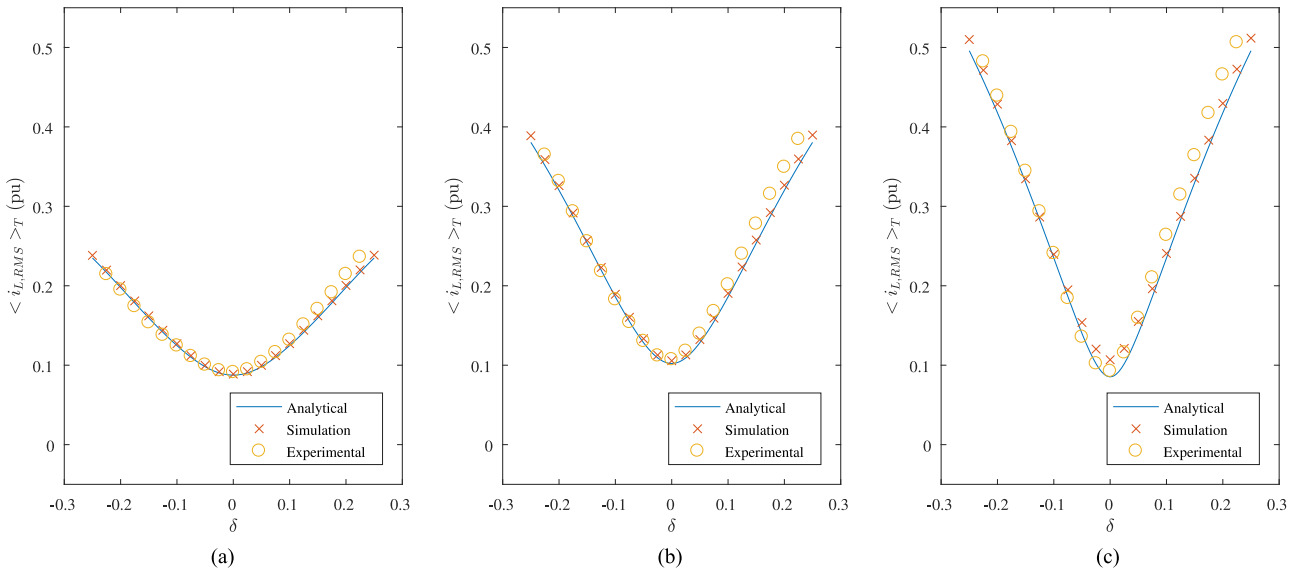


Fig. 24. Comparison of analytical, simulation, and experimental results for inductor rms current: (a) $m = 0.2$, (b) $m = 0.35$, and (c) $m = 0.5$.

filter admittance is given as [C_f is shown in Fig. 1(c)]

$$Y_{f,\text{pu}} = \frac{\omega_s C_f}{Y_b} = \frac{\text{THD}_I}{\lambda}. \tag{57}$$

So, the THD is a direct measure of the input ac-side per unit filter impedance for a given specified λ. The THD values for the three compared topologies are given Table XII.

VIII. Simulation and Experimental Results

The operation of the proposed converter was simulated using MATLAB–Simulink with PLECS blockset. The circuit parameters are given in Table XIII. The dc-link voltage V_{dc} was held fixed at 135 V, and the power transfer was observed at different values of modulation index m and phase-shift parameter δ. The turns ratio of the transformer is unity.

A laboratory hardware prototype has been developed. A photograph of the setup is shown in Fig. 18. In the primary push–pull converter, IXFX20N120 MOSFETs and C4D20120A diodes are used, whereas in the secondary-side VSI, the APTGF50TA120PG IGBT module is used. Concept 2SD106AI and 6SD106AI drivers are used for driving the power devices in the primary- and secondary-side converters, respectively. The dSPACE DS1103 control platform was used in conjunction with a Xilinx XC3S500E FPGA board to generate the gating signals. An *L*–*C* filter ($L = 820\,\mu$H and $C = 30\,\mu$F) is used to filter out HF components from the ac line current. A clamp circuit is included in the primary-side converter in Fig. 18 for

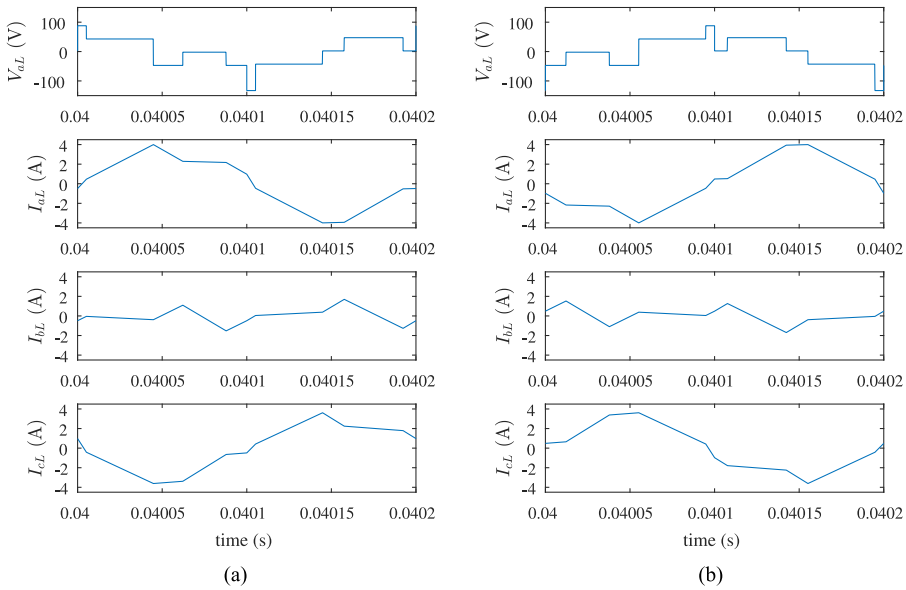


Fig. 25. Simulation results for soft switching for secondary VSI. (a) Positive δ, Mode II: Voltage across inductor in phase a (top figure) and current through inductor in phases a, b, and c (bottom three figures). (b) Negative δ, Mode II: Voltage across inductor in phase a (top figure) and current through inductor in phases a, b, and c (bottom three figures).

TABLE XIV
EXPERIMENTAL EFFICIENCY

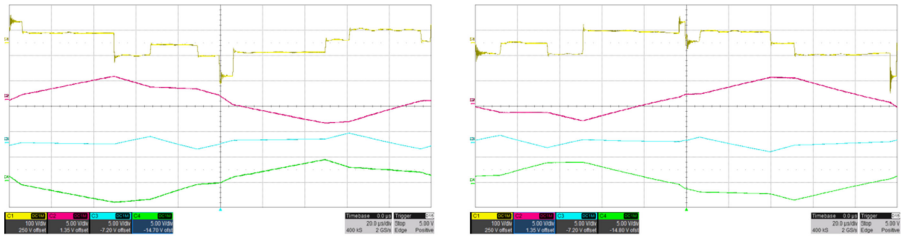
AC power (W)	442	360	304	166	−112	−295	−376
Efficiency (%)	81.5	83.8	84	84.1	88.9	89.7	80.5

preventing voltage spikes across S_1 and S_2 during switching transitions.

The simulation and experimental results corresponding to $m = 0.5$ and $\delta = 0.2$ (active power transfer from ac to dc) are given in Figs. 19 and 21, respectively. It is observed from Fig. 19(a) and 21(a) that the filtered ac line currents are nearly in phase with the input ac line voltages, confirming open-loop unity power factor operation. A small phase difference exists between the currents and voltages due to the effect of the input *L–C* filter. Figs. 19(b) and 21(b) confirm balanced three-phase operation. Figs. 19(c) and 21(c)show the unfiltered ac and dc currents. Figs. 20 and 22 show the spectrum of these currents. From Figs. 20 and 22, it is possible to see that the ac currents have the frequency components at the fundamental frequency and multiples of switching frequency. Similarly, the dc-side current has the dc component along with components at twice of the switching frequency. The experimental and the simulation results show a close correspondence, confirming the proposed operation.

In order to validate the analysis done in Sections III and IV, the rms value of the inductor current and the active power transferred over a line cycle for various values of m and δ are observed both in simulation and experiment and compared with the prediction of (21) and (23). The dc power is computed by taking the average of observed product of dc current and dc voltage both in case of simulation and experiment. Similarly, the ac power is computed by taking the product of the instantaneous input ac current and the ac line voltage. In case of simulation, both the ac and the dc powers are observed to be the same and match closely with corresponding analytical prediction, as shown in Fig. 23. In case of experiment, the observed ac and dc powers are not the same due to losses in the system, which include losses in the converter, in the transformer windings, etc. As in case of ac to dc power flow, the losses are supplied from the ac source, the input ac power is higher than the output dc power. Similarly, for negative values of δ, the ac power is lower than the dc power. In Fig. 22, it is possible to see the fundamental component of the ac line current is bigger in case of ac to dc power flow and the dc component of the dc-link current is bigger when δ is negative. In Fig. 23, it can be observed that the difference between the experimental ac and dc powers increases and diverges from the analytically predicted value in the active power for higher values (magnitude) of δ. This is because for higher values of δ, more active power is transferred and the rms inductor current is high, resulting in higher power loss. Fig. 24 showsw that both simulated and experimentally observed rms values of the inductor current for various values of m and δ match closely with the corresponding analytical prediction. The efficiency results for ac voltage with 82.67 V line–line rms and dc voltage of 135 V are provided in Table XIV.

In order to demonstrate soft switching in the secondary-side VSI, simulation results are presented in Fig. 25(a) at $m = 0.35$, $\alpha = 25^\circ$ in Sector 1, and $\delta = 0.125$, a Mode II operating condition. The voltage across the inductor for phase a and the currents through the three-phase inductors are shown for one switching period. Based on the discussion done in Section V and a comparison with Fig. 9, it can be deduced that all three phases undergo soft switching. The simulation results for $m = 0.35$, $\alpha = 25^\circ$ in



(a) (b)

Fig. 26. Experimental results, soft switching for secondary VSI. (a) Positive δ, Mode II: Voltage across inductor in phase a (top figure) and current through inductor in phases a, b, and c (bottom three figures) [100 V/div, 5 A/div]. (b) Negative δ, Mode II: Voltage across inductor in phase a (top figure), and current through inductor in phases a, b, and c (bottom three figures) [100 V/div, 5 A/div].

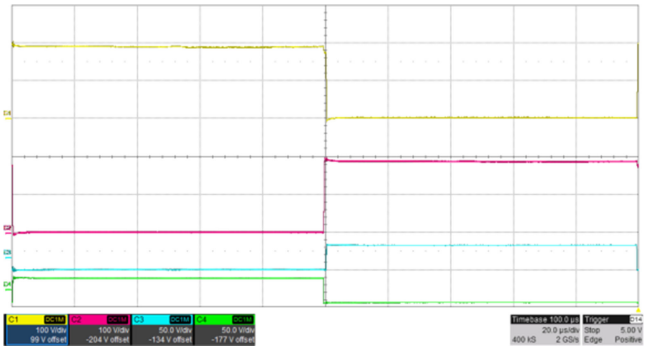


Fig. 27. Experimental result showing primary-side switches voltages: Collector emitter voltages of S_1 and S_2 (top two graphs [50 V/div] and gate emitter voltages of S_1 and S_2 (bottom two graphs [50 V/div]).

Sector 1, and $\delta = -0.125$ are shown in Fig. 25(b), and it can be similarly concluded that all three phases undergo soft switching. The experimental results for these operating conditions are shown in Fig. 26. The experimentally observed waveforms show close correspondence with the simulated waveforms in Fig. 25, confirming soft switching. Finally, Fig. 27 shows the collector emitter and gate emitter voltages of primary-side switches S_1 and S_2 during a switching transition in Mode II.

IX. Conclusion

This paper presents a single-stage isolated ac–dc converter. The proposed scheme results in the following advantages:

1) HFT operation: high power density and reduced cost for iron and copper;

2) open-loop ac-side power factor correction;

3) partial soft-switching; and

4) control of bidirectional active power flow.

The chosen topology has only two active switches in the ac-side converter, whereas the dc-side converter is a VSI. The paper identifies four possible modes of operation and then derives a closed-form analytical estimation of the transferred active power and rms of the transformer winding currents. Subsequent analysis shows partial soft-switching over a wide range of operating conditions. Simulation results show a close agreement with analytical predictions, while experimental results slightly differ due to power loss. However, with increasing frequency, transformer losses may increase and to counter this effect a successful design will require better core material and better winding structure. Experimental results showing active power flow in both directions are presented at steady-state operating conditions under open-loop control. Closed-loop control of this converter will be a part of the future work.

Appendix A
PFC Loss Computation

The PFC is assumed to be conventional space vector modulated, with unity power factor. Thus, the voltage on the dc side is $V_{\mathrm{dc,PFC}} = \sqrt{3}V_{\mathrm{pr}}$. The rms phase current is given as follows:

$$I_{\mathrm{RMS,PFC}} = \frac{\sqrt{2}P}{3V_{\mathrm{pr}}}. \tag{58}$$

The devices share the current equally, and thus, the device rms current is given as follows:

$$I_{\mathrm{RMS,switch,PFC}} = \frac{P}{3V_{\mathrm{pr}}} = \frac{0.333P}{V_{\mathrm{pr}}}. \tag{59}$$

The peak current in devices is

$$I_{\mathrm{peak,switch,PFC}} = \frac{2P}{3V_{\mathrm{pr}}} = \frac{0.667P}{V_{\mathrm{pr}}}. \tag{60}$$

The conduction losses are given as

$$P_{\mathrm{PFC,cond\text{-}loss}} = 6I^2_{\mathrm{RMS,switch,PFC}}R_{\mathrm{ON,pr}} = \frac{0.667P^2}{V^2_{\mathrm{pr}}}R_{\mathrm{ON,pr}}. \tag{61}$$

Now, the peak of the sinusoidal current flowing between the grid and the PFC is given as follows:

$$I_{\mathrm{peak,PFC}} = \frac{2P}{3V_{\mathrm{pr}}}. \tag{62}$$

Since it is assumed that the conventional two-level SVPWM is used, it means that there are two switching transitions in each phase leg, per switching period; one top to bottom switch transition and one bottom to top switch transition. Depending on the direction of the current, exactly one of these transitions will be hard switched. Therefore, the switching losses in all three

phases are computed, as given in (63)

$$P_{\mathrm{PFC,phase,sw\text{-}loss}} = 3\frac{1}{\pi}\frac{1}{2}\sqrt{3}V_{\mathrm{pr}}f_s t_{\mathrm{sw,pr}} \times \int_0^{\pi} I_{\mathrm{peak,switch,PFC}} \sin\theta d\theta = 1.104 P f_{s,\mathrm{PFC}} t_{\mathrm{sw,pr}}. \quad (63)$$

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