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A Bidirectional Soft-switched DAB based Single Stage Three Phase AC-DC Converter for V2G Application

Dibakar Das, Nathan Weise, *Member, IEEE*, Kaushik Basu, *Senior Member, IEEE*, Rohit Baranwal, *Member, IEEE* and Ned Mohan, *Life Fellow, IEEE*

***Abstract*—In vehicle to grid (V2G) applications, the battery charger of the electric vehicle (EV) needs to have a bidirectional power flow capability. Galvanic isolation is necessary for safety. An AC-DC bidirectional power converter with high-frequency isolation results in high power density, a key requirement for an on-board charger of an EV. Dual active bridge (DAB) converters are preferred in medium power and high voltage isolated DC/DC converters due to high power density and better efficiency. This paper presents a DAB based three-phase AC-DC isolated converter with a novel modulation strategy that results in 1) single stage power conversion with no electrolytic capacitor, improving the reliability and power density 2) open loop power factor correction 3) soft switching of all semi-conductor devices 4) a simple linear relationship between control variable and transferred active power. The paper presents a detailed analysis of the proposed operation, along with simulation results and experimental verification.**

***Index Terms*—Dual Active Bridge (DAB), Single stage AC-DC Converter, Soft switching, High frequency link**

I. Introduction

There is a growing interest towards development of converters for hybrid electric vehicle charging systems due to increasing awareness about global warming [1]. Hybrid electric vehicle (EV) chargers can be broadly classified into two groups: on-board and off-board chargers. On board chargers have the necessary power electronics on the vehicle to enable charging from a conventional utility power outlet. Typical power level of an on-board charger is limited to few tens of kW by size and weight constraints. The on board charger system must be highly efficient and must have high power density and reliability. For Vehicle to Grid (V2G) applications, the charger must be able to support bidirectional power flow [2], [3]. Conventional EV chargers at this power level have two stage architecture as shown in Fig.1(a) which uses an AC-DC rectifier followed by an isolated DC-DC converter [4], [5]. The AC-DC converter is modulated to draw sinusoidal grid currents. The DC-DC converter is used for voltage matching and providing isolation at high frequency which results in transformer size reduction. In this topology, an electrolytic capacitor is used to support the intermediate DC link which reduces the reliability of the overall system. Moreover, multiple stages of power conversion reduce overall power density of the system.

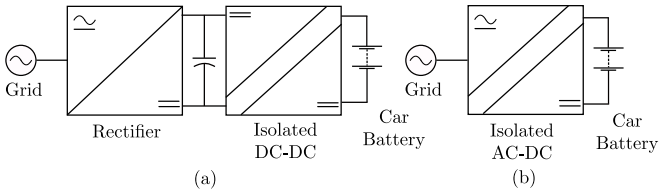

Fig. 1. (a) Typical power architecture of a two stage battery charger (b) Conceptual Diagram of the proposed single stage battery charger

The relative drawbacks of multi-stage topologies have led to development of single stage topologies which transfer active power without any intermediate stage. They have a better power density and reliability due to the exclusion of the DC link electrolytic capacitor [6]. Several single stage isolated EV charger topologies have been proposed in literature [7]–[9]. The focus of this work is on a single stage three phase isolated AC-DC converter. The proposed modulation strategy is based on Dual Active Bridge (DAB) principle that meets the essential requirements of an on board EV charger.

DAB based DC-DC power converter was proposed in [10]. This type of power conversion is suited for high voltage and medium power applications where isolation is required and high power density is important [5], [11], [12]. Two single phase full bridge converters are operated in square wave modulation with a phase shift to transfer active power.

Later it was found that one can also control the duty cycle of the two square waves by introducing zero states. So in total there are three degrees of freedom: two duty cycles and the phase shift. A large body of literature exists that tries to answer the following question: For a given active power how to set these three degrees of freedom so that RMS of the winding currents or the conduction loss in the bridges and transformer can be minimized while satisfying the soft-switching conditions [13]–[16]. Some authors aimed at the minimisation of the reactive component of power which is

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D. Das and K. Basu are with the Department of Electrical Engineering, Indian Institute of Science, Bangalore, India (email: dibakard@iisc.ac.in; kbasu@iisc.ac.in).

N. Weise is with the Department of Electrical and Computer Engineering, Marquette University, Milwaukee, USA (email: nathan.weise@mu.edu).

R. Baranwal is with the MTS Systems Corporation, Eden Prairie, MN 55344 USA (e-mail: baran065@umn.edu).

N. Mohan is with the University of Minnesota, Minneapolis, MN 55455 USA (e-mail: mohan@umn.edu).

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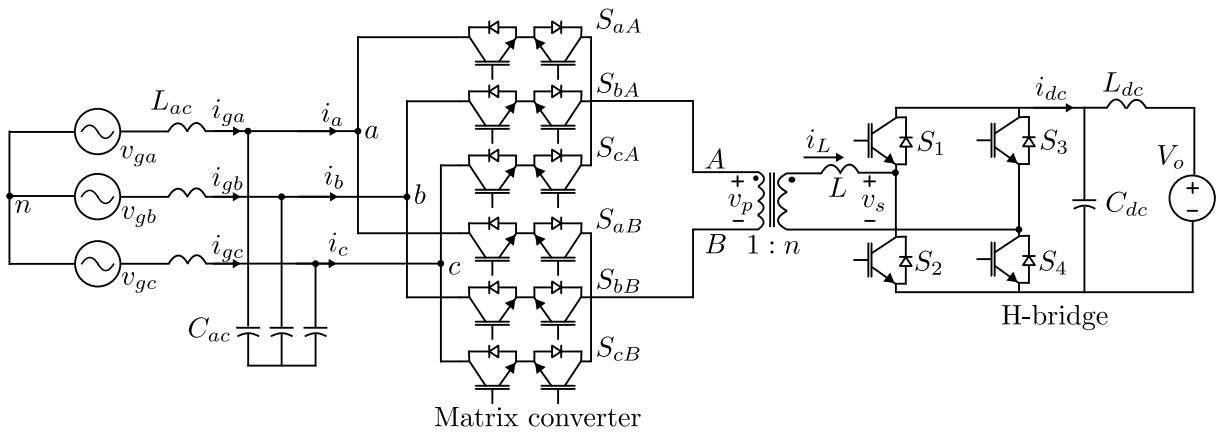

Fig. 2. Topology of the single stage AC-DC Converter

closely related to the conduction loss [17]–[19].

DAB based single stage single phase AC-DC converters have been discussed in [20]–[23]. In [21], a modulation strategy is proposed which achieves open-loop power factor correction and soft switching. An extension of the modulation strategy has beeen discussed in [22]. In [23], a variable switching frequency based modulation strategy has been proposed. The DAB based AC-DC converters described in [24] employs a line frequency switched rectifier followed by DAB converter stage. The intermediate DC input to the DAB converter is the rectified version of the line frequency AC.

DAB based single stage three phase converters have been discussed in [25]–[28], where [25] supports uni-directional power flow. A single stage reduced switch count converter is proposed in [26] where the AC-AC converter on primary is realized using a push pull structure. The paper presents a space vector modulation strategy for the DAB converter. Soft switching analysis in the paper shows that the primary side switches do not receive soft switching for most of the operating modes, whereas one of the transitions in the secondary bridge is partially hard switched. The two switches in the primary has high RMS and peak current rating. Different modulation strategies based on the topology shown in Fig.2 have been proposed in [27], [28]. In [27], The DC side H bridge is operated with square wave modulation and a quasi square wave is applied from the AC side with the max and the mid AC line-line voltage. The HF inductor current is assumed to be a square waveform for determination of duty cycles of the primary voltages and the power. This results in low frequency harmonics on the AC input current waveform. A soft switching analysis is presented. However, ensuring proper current polarities which gives soft switching over entire line cycle is not discussed. A modulation strategy which alleviates the low frequency harmonic problem is described in [28]. The AC side matrix converter is used to apply sequentially two square waveforms formed by the max and mid AC line-line voltages. A phase shifted square waveform is applied from the secondary for each of the square waveform applied from the primary. Although the low frequency harmonic problem is addressed, the paper does not discuss soft switching.

A three phase single stage DAB based AC-DC converter as shown in Fig.2 was proposed in [29]. The paper discusses a modulation strategy achieving input power factor correction and soft switching. The proposed modulation strategy is an extension of the modulation scheme proposed in [21]. However no detailed analysis and experimental results have been provided. In this paper, a DAB based modulation strategy has been proposed for the converter shown in Fig. 2 that results in a) Loss less switching: zero current switching (ZCS) in the AC side bridge and zero voltage switching in the DC side bridge b) Open loop input power factor correction without DC side load current sensing c) A simplified plant for closed loop control, as the phase shift or control input is proportional to the transferred active power.

The paper is organized in four sections. After the introductory first section, the Section II describes the analysis of the proposed modulation for the converter over a switching period and from that, derives the line frequency quantities for DC power transferred and RMS current in the transformer windings. The design procedure of the converter and filter is discussed in detail. A detailed analysis on soft switching of the converter has been provided. Section III contains simulation and experimental results showing the operation of the proposed modulation and the Section IV concludes the paper.

II. Analysis

This section presents the proposed modulation scheme, derivation of closed form expressions of important quantities such as DC power transferred and soft switching mechanism. The topology of the converter is shown in Fig. 2. The AC-side converter, the left side of Fig 2, is comprised of six four-quadrant switches $[S_{aA} - S_{cC}]$. They are realised using two emitter tied IGBT's with their respective anti-parallel diodes. These switches create a three-phase to single-phase matrix converter (MC). The single-phase side of the matrix converter is connected to the primary winding of a single-phase high frequency transformer (HFT). The AC input side has a low pass LC filter (C_{ac} and L_{ac}) between the source and the three phase to single phase matrix converter to suppress current harmonics drawn from the grid. The turns ratio of the single-phase transformer is $1 : n$. In this analysis, the magnetizing inductance, winding resistance and core losses are

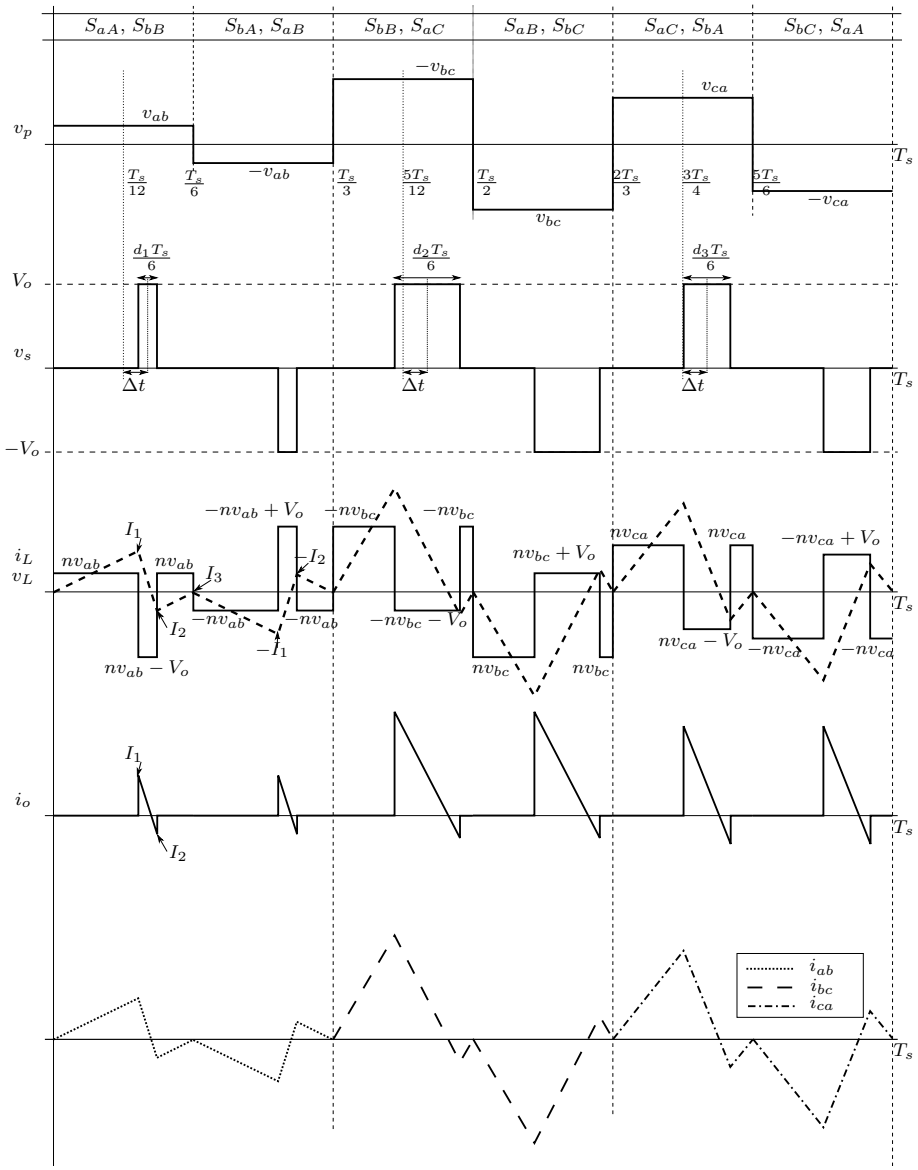

Fig. 3. Typical waveforms over a switching cycle T_s ($-\frac{\pi}{6} < \omega_i t < 0$)

neglected. The primary and secondary leakage inductances are lumped together on the secondary as L. The secondary of the single-phase transformer is connected to a H-bridge converter comprised of four two-quadrant switches $[S_1 - S_4]$. The current on the DC side of the converter is filtered with an LC filter (C_{dc} and L_{dc}). Finally, the H-bridge is connected to a DC source of voltage V_o. In the following analysis, all switches are considered ideal.

A. Modulation

1) Input Voltages: For analysing the modulation of the converter, it is assumed that the filter inductance L_{ac} offers negligible impedance at line frequency. Thus, the utility voltages v_{ga}, v_{gb} and v_{gc} directly appear at the converter input terminals. Assuming the three phase voltages to be balanced, the voltages to the input of the converter can be expressed as,

$$v_{jn}(t) = V_i \sin(\omega_i t + m_j) \tag{1}$$

where $j \in \{a, b, c\}$ and $m_a = 0$, $m_b = -2\pi/3$, $m_c = 2\pi/3$. The peak of the input line to neutral voltage is defined as V_i and the frequency of the three phase input voltages is $\omega_i = 2\pi/T_i$.

2) Matrix Converter: Fig. 3 shows typical primary voltage waveform v_p (v_{AB}), over one switching cycle of period T_s when $\left(-\frac{\pi}{6} < \omega_i t < 0\right)$. In this period, $|v_{bc}| > |v_{ca}| > |v_{ab}|$ and $v_{ab} > 0$, $v_{ca} > 0$ and $v_{bc} < 0$. T_s is the switching period of the matrix converter. The period T_s is divided into three equal times. The first third of the period alternates at 50% between a positive and negative value of the line to line voltage v_{ab}. Similarly, during the second third of T_s, the primary voltage of the transformer alternates between negative and positive v_{bc} for equal time and the primary voltage of the transformer alternates between positive and negative v_{ca} for equal time during the last third of T_s. The voltages applied

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over a cycle of T_s are given in (2).

$$v_p(t) = \begin{cases} |v_{ab}|, & 0 < t \leq T_s/6 \\ -|v_{ab}|, & T_s/6 < t \leq T_s/3 \\ |v_{bc}|, & T_s/3 < t \leq T_s/2 \\ -|v_{bc}|, & T_s/2 < t \leq 2T_s/3 \\ |v_{ca}|, & 2T_s/3 < t \leq 5T_s/6 \\ -|v_{ca}|, & 5T_s/6 < t \leq T_s \end{cases} \tag{2}$$

3) H-bridge Modulation: The H-bridge converter is comprised of switches $[S_1 - S_4]$ and produces a voltage (v_s in Fig. 2) pulse in each respective sixth of a cycle. The width of the pulse depends on current pair of input voltages being applied by the matrix converter. Additionally, these pulses are phase shifted with respect to v_p. The duty ratios of each third of the cycle of v_s are defined in (3)-(5) and depend on the voltage currently applied by the matrix converter. The duty ratios are shown in Fig. 3. The first third of the cycle the duty ratio is $d_1(t)$, the second third of the cycle the duty ratio is $d_2(t)$, and the final third of a cycle the duty ratio is $d_3(t)$. These duty ratios are calculated using the measured line to line input voltages, the DC bus voltage, and the turns ratio. Given the peak of the input line-line voltage $\sqrt{3}V_i$, the DC voltage V_o, the choice of the turns ratio should be such that the duty ratio never goes above one. The polarity of the generated pulses are same as the polarity of the applied voltage v_p of the matrix converter.

$$d_1(t) = \frac{n|v_{ab}(t)|}{V_o} \tag{3}$$

$$d_2(t) = \frac{n|v_{bc}(t)|}{V_o} \tag{4}$$

$$d_3(t) = \frac{n|v_{ca}(t)|}{V_o} \tag{5}$$

The time shift of the pulses produced by the H-bridge is denoted as Δt and is shown in Fig. 3. This modulation scheme imposes limits on the time shift. The pulse produced by the H-bridge will not be allowed to move outside of its respective one sixth of the modulation cycle (referred as inner mode). This condition results in (6) and (7).

$$\frac{T_s}{12} + \Delta t + \frac{dT_s}{12} \leq \frac{T_s}{6} \tag{6}$$

$$\Delta t \leq \frac{T_s}{12} - \frac{dT_s}{12} \tag{7}$$

The phase shift δ is defined in (8). The controllable range of the phase shift δ is from -1 to 1.

$$\delta = \frac{\Delta t}{T_s/12} \tag{8}$$

The peak duty ratio of $d_1(t)$, $d_2(t)$, and $d_3(t)$ is defined in (9).

$$\hat{d} = \frac{\sqrt{3}nV_i}{V_o} \tag{9}$$

The peak duty ratio is needed to determine the range of allowable phase shift. The range of allowable phase shift is found using (6), (7), (8), and (9) and is given in (10). Similar computation can be done for negative δ as well.

$$|\delta| \leq 1 - \hat{d} \tag{10}$$

Given the definition for phase shift δ, duty ratios d_1, d_2, d_3, and the restriction on phase shift, the voltage applied by the H-bridge can be defined over the complete cycle of modulation of period T_s.

$$v_s(t)^1 = \begin{cases} 0, & 0 < t \leq t_{a1} \\ V_o, & t_{a1} < t \leq t_{b1} \\ 0, & t_{b1} < t \leq T_s/6 + t_{a1} \\ -V_o, & T_s/6 + t_{a1} < t \leq T_s/6 + t_{b1} \\ 0, & T_s/6 + t_{b1} < t \leq T_s/3 + t_{a2} \\ V_o, & T_s/3 + t_{a2} < t \leq T_s/3 + t_{b2} \\ 0, & T_s/3 + t_{b2} < t \leq T_s/2 + t_{a2} \\ -V_o, & T_s/2 + t_{a2} < t \leq T_s/2 + t_{b2} \\ 0, & T_s/2 + t_{b2} < t \leq 2T_s/3 + t_{a3} \\ V_o, & 2T_s/3 + t_{a3} < t \leq 2T_s/3 + t_{b3} \\ 0, & 2T_s/3 + t_{b3} < t \leq 5T_s/6 + t_{a3} \\ -V_o, & 5T_s/6 + t_{a3} < t \leq 5T_s/6 + t_{b3} \\ 0, & 5T_s/6 + t_{b3} < t \leq T_s \end{cases} \tag{11}$$

B. Computation of input current

In order to compute the average power and RMS of the transformer winding currents over one period of the AC voltages $\left(T_i = \frac{1}{f_i}\right)$, we need to determine the inductor current $i_L(t)$ over one modulation cycle of period T_s. As each third of the modulation cycle is identical, we will show the details of the computation of i_L over the first third of the modulation cycle when 'ab' line to line voltage is applied at the transformer primary. The voltage across the inductor is given by obtained by taking the difference between the applied reflected primary voltage $nv_p(t)$ (2) and secondary voltage $v_s(t)$ (11).

$$v_L(t) = nv_p(t) - v_s(t) \tag{12}$$

Now, (12) can be used to compute the inductor current $i_L(t)$.

$$v_L(t) = L\frac{di_L}{dt} \tag{13}$$

To compute $i_L(t)$, it is also assumed that in steady state, the DC component of the inductor current is zero. This is true for a circuit with finite resistances where the DC offset will die down to zero under steady state operation. As the applied secondary voltage pulse $v_s(t)$, in each one sixth of the modulation cycle has a duty ratio of $\frac{n|v_p(t)|}{V_o}$, the average voltage applied across the inductor is zero. So, it is possible to assume $i_L(t)$ to be zero at the beginning of the modulation cycle. Let us focus on the determination of $i_L(t)$ over the first one sixth of the modulation cycle. As shown in Fig. 3, $i_L(t)$ is a piecewise linear function of time, characterized by two peaks I_1 and I_2. The expressions for I_1 and I_2 are given in (14) and (15) respectively. $I_3 = 0$ because the average of the applied inductor voltage is zero over the period $0 < t \leq \frac{T_s}{6}$.

$$I_1 = \frac{n|v_{ab}|}{L}\frac{T_s}{12}(\delta - d + 1) \tag{14}$$

$$I_2 = \frac{n|v_{ab}|}{L}\frac{T_s}{12}(\delta + d - 1) \tag{15}$$

[1] $t_{ai} = \frac{T_s}{12}(1 + \delta - d_i)$ & $t_{bi} = \frac{T_s}{12}(1 + \delta + d_i)$ $\forall$ $i \in \{1, 2, 3\}$

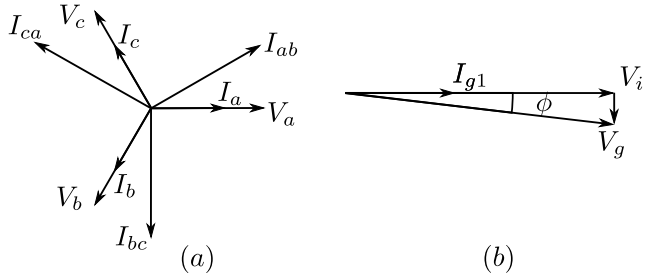

Fig. 4. Phasor Diagram showing (a) Unity DPF (b) Effect of filter on power factor correction

Following a similar procedure, it is possible to determine $i_L(t)$ over one period of the modulation cycle. Note that the line to line current $i_{ab}(t)$ is rectified in $i_L(t)$ in the first $1/3^{rd}$ of the modulation cycle and zero in rest of the period, Fig. 3. So, the average value of i_{ab} over one modulation cycle is given in

$$\bar{i}_{ab} = \frac{2}{T_s}\int_0^{\frac{T_s}{6}} n i_L(\tau)d\tau = \frac{n^2\delta}{36 f_s}\sqrt{3}V_i \sin\left(\omega_i t + \frac{\pi}{6}\right) \quad (16)$$

where $f_s = 1/T_s$. Similarly, it is possible to compute the average value of the two other line currents (17) and (18).

$$\bar{i}_{bc} = \frac{n^2\delta}{36 L f_s}\sqrt{3}V_i \sin\left(\omega_i t - \frac{\pi}{2}\right) \quad (17)$$

$$\bar{i}_{ca} = \frac{n^2\delta}{36 L f_s}\sqrt{3}V_i \sin\left(\omega_i t + \frac{5\pi}{6}\right) \quad (18)$$

It is possible to determine the line currents from the line to line currents using (19), (20) and (21).

$$\bar{i}_a = \bar{i}_{ab} - \bar{i}_{ca} \quad (19)$$

$$\bar{i}_b = \bar{i}_{bc} - \bar{i}_{ab} \quad (20)$$

$$\bar{i}_c = \bar{i}_{ca} - \bar{i}_{bc} \quad (21)$$

The resultant phase currents are given in (22), (23), and (24).

$$\bar{i}_a = \frac{n^2\delta}{12 L f_s} V_i \sin(2\pi f_i t) \quad (22)$$

$$\bar{i}_b = \frac{n^2\delta}{12 L f_s} V_i \sin\left(2\pi f_i t - \frac{2\pi}{3}\right) \quad (23)$$

$$\bar{i}_c = \frac{n^2\delta}{12 L f_s} V_i \sin\left(2\pi f_i t - \frac{4\pi}{3}\right) \quad (24)$$

The magnitude of the three phase currents is directly proportional to the control variable δ. Additionally, the modulation of the converter ensures that the fundamental component of the current is in phase with the line to neutral voltage. This ensures a displacement power factor of unity as shown in Fig.4a. However due to a finite amount of switching ripple flowing to the grid, the power factor differs from unity. The relation between displacement power factor and power factor is given in [30] as,

$$PF = \frac{1}{\sqrt{1+THD^2}} DPF \quad (25)$$

IEEE standards [31] specify the maximum amount of distortion in terms of the THD. An upper limit of 5% is put on the allowable THD. Thus, the power factor of the system is very close to unity.

Ideally, the inductor L_{ac} should appear as a short-circuit at line frequency so that the grid voltage appears at the input of the AC side converter. However, there is a finite drop across the leakage at fundamental frequency which prevents the converter from exact unity power factor operation. The modulation ensures that the voltage to the input of the converter V_i and fundamental grid current I_{g1} are in phase. However due to filter drop the current I_{g1} becomes leading with reference to the grid voltage for a power transfer from DC to AC (Fig.4b). However, this drop is very small and thus the converter operates at near unity power factor.

C. Design of transformer turns ratio and Leakage Inductance

The average power (26) is found using (22), (23), (24), and (1)

$$P = \frac{1}{T_i}\int_0^{T_i} (v_a\bar{i}_a + v_b\bar{i}_b + v_c\bar{i}_c)dt = \frac{n^2 V_i^2}{8 L f_s}\delta = \frac{\hat{d}^2 V_o^2}{24 L f_s}\delta \quad (26)$$

Note the average power is DC and linearly proportional to the control variable δ. This simple relationship simplifies the control architecture. The design of the dual active bridge converter is carried out keeping in mind the minimisation of the losses and improvement of efficiency. Thus the aim is to choose n and L such that the rms current is minimised for a given power transfer requirement. The rms current is computed using,

$$i_{rms,L}^2 = \frac{1}{T_i}\int_0^{T_i} i_L^2(t)\ dt \quad (27)$$

For evaluating the integral over line cycle, the rms current for one modulation cycle is computed first. Using the current magnitudes in (14) and (15), the rms current computed over first one third of the modulation cycle is given by

$$i_{L,rms1,Ts}^2 = \frac{T_s^2 d_1^2 V_o^2}{1296 L^2}\left(d_1^2 - 2d_1 + 3\delta^2 + 1\right) \quad (28)$$

The rms currents in the subsequent two thirds of modulation cycle ($i_{L,rms2,Ts}^2$ & $i_{L,rms3,Ts}^2$) can be similarly obtained by replacing d_1 by d_2 and d_3 respectively. The net rms current in a switching cycle is $i_{L,rms,Ts}^2 = i_{L,rms1,Ts}^2 + i_{L,rms2,Ts}^2 + i_{L,rms3,Ts}^2$. Putting the values of d_1, d_2 and d_3 and taking the average over line cycle, the rms current is given by,

$$i_{rms,L}^2 = \frac{T_s^2\hat{d}^2 V_o^2}{10368\pi L^2}\left(36\pi\delta^2 + 9\pi\hat{d}^2 - 64\hat{d} + 12\pi\right) \quad (29)$$

The average power in per unit is calculated with a power base of $V_o^2/2\pi L f_s$

$$P_{pu} = \frac{\pi\delta\hat{d}^2}{12} \quad (30)$$

Similarly, the per unit rms current using the base current $I_{base} = V_o/2\pi L f_s$ is given by,

$$i_{rmspu,L}^2 = \frac{\pi\hat{d}^2}{2592}\left(36\pi\delta^2 + 9\pi\hat{d}^2 - 64\hat{d} + 12\pi\right) \quad (31)$$

It can be seen that the per unit power and rms currents depend on the design variables $\hat{d}$ and δ. The objective is to choose $\hat{d}$

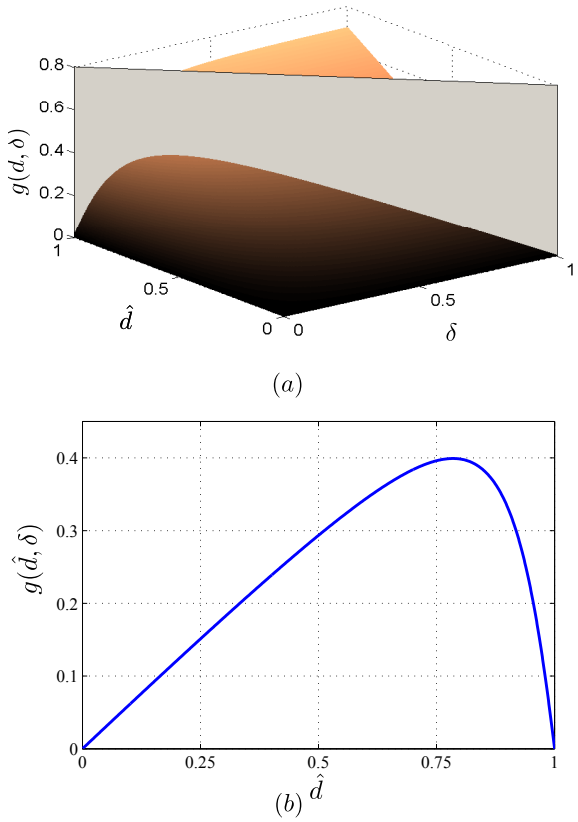

Fig. 5. (a) Plot showing variation of $g(\hat{d},\delta)$ (b) Plot of $g(\hat{d},\delta)$ for various $\hat{d}$ and $\delta = 1-\hat{d}$

and δ such that the net rms current is minimised for a given per-unit power transfer. Accordingly, the function $g(\hat{d},\delta) = P_{pu}/i_{rmspu,L}$ is plotted over the feasible range of $\hat{d}$ and δ ($0 \leq \hat{d},\delta \leq 1$) in Fig.5a and the maxima is identified. Apart from individual limits on $\hat{d}$ and δ, the values of $\hat{d}$ and δ should be chosen such that the converter operates in inner mode. For a positive δ, using (10) we have,

$$\hat{d}+\delta \leq 1 \tag{32}$$

Since $g(\hat{d},\delta)$ is a monotonically increasing function over $\hat{d}$ and δ, it is easy to conclude that the optimum operating point occurs for $\hat{d}+\delta = 1$. This is identified as the contour generated because of intersection of the two curves in Fig.5b. The optimum value of $\hat{d} = 0.76$ is obtained from the Fig.5b which gives a maximum possible phase angle as $\delta_{max} = 0.24$. The per unit maximum power under this operating condition is given by

$$P_{pumax} = \frac{\pi\delta\hat{d}^2}{12} = 0.036\ pu \tag{33}$$

Since the operating power P and the output voltage of the converter is known, the inductance can be accordingly designed so that the maximum per unit power is achieved. The inductor L should be chosen such that

$$\frac{V_o^2}{2\pi f_s L} = \frac{P}{P_{pumax}} \tag{34}$$

The transformer turns ratio n is chosen using (9) once the operating $\hat{d}$ is fixed.

D. Soft switching

1) ZCS of the AC side Bridge: To ensure that the volt seconds applied from primary is balanced with the volt seconds applied from secondary in every one-sixth of the modulation cycle, pulse width of the secondary voltage is determined using (3)-(5). Ensuring a volt second balance will result in equal currents at the beginning and end of each one-sixth of modulation cycle. Every practical circuit will have some finite resistances. For a lossy circuit, the DC offset which is governed by the complementary function of the solution will die down to zero and the steady state current will not have any DC offsets. It is possible to observe that the instants at which the AC side converter switches, i.e. at $t = 0$, $\frac{T_s}{6}$, $\frac{T_s}{3}$, $\frac{T_s}{2}$, $\frac{2T_s}{3}$, $\frac{5T_s}{6}$, the primary winding current, which is reflected inductor current, is zero, so the primary converter is zero current switched (ZCS). Note that in practical implementation, due to magnetization component of the transformer current and voltage ripple at input and output, the primary current may not be zero, but would have a small magnitude at the time of switching.

2) ZVS of the DC side Bridge: Fig.6 shows a detailed diagram of a single leg of the DC side H-bridge and the events occurring during switching. Fig.6a shows the waveforms applied during first $1/3^{rd}$ of the modulation cycle. The H-bridge is switched four times during this interval. The first switching transition is considered where the switch S_2 is turning-off and switch S_1 is turning-on after dead time (Fig.6(b)). The inductor current i_L at this instant is I_1 given by (15) and is assumed to be positive. Accordingly, the current is going into the pole terminal and switch S_2 is conducting at the instant of turn-off. Switch S_1 was blocking a voltage of V_o. After switch turn-off, the current has to flow through the capacitances. The current charges up the capacitance C_2 and discharges capacitance C_1 (Fig.6(c)). The capacitances do not allow the voltage across the switch to change instantaneously but the channel current of switch S_2 quickly goes to zero [32]. Thus, it is turned off at zero voltage (ZVS). Once, the capacitor C_1 is completely discharged to zero (Fig.6(d)), the current starts to flow through the diode D_1. If the switch S_1 is turned on when its body diode is conducting, it is soft switched.

Thus, when leg 1 of the H-Bridge (S_1 and S_2) is switching, the inductor current i_L is I_1 which should be *more than zero* to ensure soft switching. Similarly, when leg 2 of the H-Bridge (S_3 and S_4) is switching, the inductor current i_L is I_2 should be *less than zero* to ensure soft switching. The currents in the next one sixth of the modulation cycle follow the same pattern resulting in ZVS. It can be shown that the currents next two thirds of the modulation cycle follow the same pattern for a balanced operation. From (14) and (15), we have,

$$(\delta - d_1 + 1) \geq 0 \tag{35}$$

$$(\delta + d_1 - 1) \leq 0 \tag{36}$$

When $\delta > 0$, since duty is a positive number < 1 we have $\delta \geq d_1 - 1$ which gives $(\delta - d_1 + 1) \geq 0$. Also, since the converter is operating in inner mode, $\delta \leq 1 - d_1$ which gives $(\delta + d_1 - 1) \leq 0$. Same conclusions can be drawn for $\delta < 0$.

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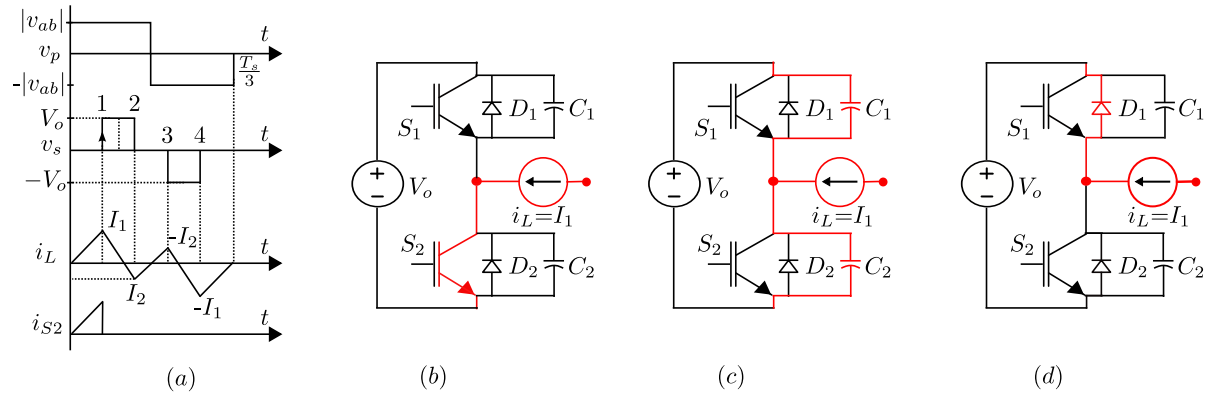

Fig. 6. Soft-Switching events (a) Waveforms for one-third of line cycle, (b) Situation prior to device S_2 turn-off, (c) Switch S_2 turned-off: capacitor assisted ZVS, (d) End of soft-turn off of S_2, diode D_1 conducting, Soft turn on of S_1

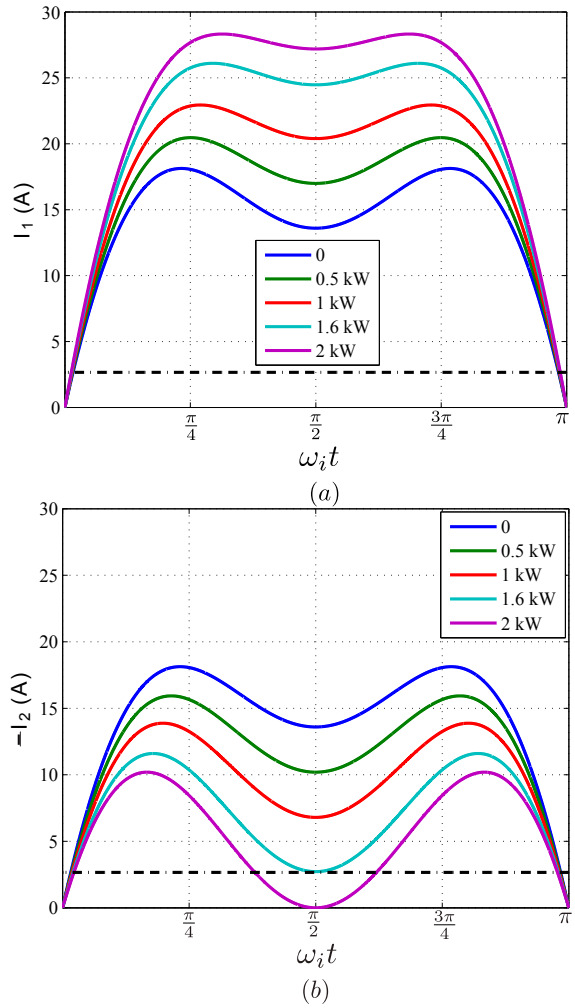

Fig. 7. Variation over line cycle: (a) I_1 for various load, (b) $-I_2$ for various load

Effect of device capacitances on soft switching: The pole current i_L should be capable of charging/discharging the capacitances C_2 and C_1 within the dead time so that the transition is fully soft switched. This imposes a minimum requirement on the pole current i_L. Assuming $C_1 = C_2 = C$ and applying KCL in the pole circuit gives,

$$i_L = 2C\frac{dv_{c2}}{dt} \tag{37}$$

Noting that the time of charging the capacitor fully should be less than the dead time of the circuit we have, $I_{Lmin} = \frac{2CV_o}{t_{dead}}$ [33]. The variations of I_1 and $-I_2$ over line cycle for various loads is plotted in Fig.7a and b respectively. The minimum current required for complete soft switching ($C = 2nF$, $t_{dead} = 600ns$) is also shown on the figures. It can be observed that for $\omega_i t$ close to 0 and π, ZVS may not happen in both the legs. This range remains relatively unchanged with loading. ZVS may not happen in one of the legs for a narrow region around $\omega_i t = \pi/2$ for heavy loading conditions. But Fig.7b reveals that this range is very small. As δ is increased, the magnitude of current I_1 increases and magnitude of current I_2 decreases as shown in Fig.7a and b respectively. This improves the soft switching range of one leg in the H-bridge but reduces the soft switching range of other leg. The converter soft-switching is unaffected under light loading conditions whereas the range reduces for high loading of the converter.

At the instant of switching, the pole current i_L is modelled as a current source. This is true only if we have enough series inductance L. This inductance is a series combination of the leakage inductance of the transformer and the external inductance added to achieve the power transfer. It is possible to show that L must satisfy the following inequality.

$$\frac{2CV_o}{i_L} < \sqrt{2LC} \tag{38}$$

E. Design of Filter

1) Design of DC side filter: The instantaneous output current is governed by the switching function of the secondary bridge and the inductor current, i_L.

$$i_{out} = (S_1 - S_3)\, i_L \tag{39}$$

The output rms current is computed using the equation

$$i^2_{rms,o} = \frac{1}{T_i}\int_0^{T_i} i^2_{out} dt \tag{40}$$

$$i^2_{rms,o} = \frac{T_s^2 \hat{d}^3 V_o^2}{25920\pi L^2}\left(240\delta^2 + 64\hat{d}^2 - 45\pi\hat{d} + 80\right) \tag{41}$$

The per unit average current i_{avpu} is computed using (30) which can be multiplied with base current to obtain the actual current. The filter needs to be designed such that the entire switching frequency ripple flows through it. The rms ripple current is given by

$$\tilde{i}_{rms} = \sqrt{i_{rms,o}^2 - i_{av}^2} \tag{42}$$

The operating point of the converter decides the value of the rms and average current. Once the ripple current rms is determined, it is assumed that the entire ripple is concentrated at the switching frequency. This results in a slight overdesign [34]. Considering an allowable voltage ripple to be a λ fraction of the DC voltage V_o, the filter admittance is given by,

$$Y_{pu} = \omega_s C_{dc} = \frac{\tilde{i}_{rms}}{\lambda V_o} \tag{43}$$

Although the capacitor C_{dc} is designed to carry the entire ripple at switching frequency, some part of it may leak into the DC source. To prevent this, an inductor L_{dc}, is put in series with the voltage source V_o. The inductor is designed such that only 5% of the total ripple flows into the source. Thus the output current $\tilde{i_o}(\omega_s)$,

$$\tilde{i_o}(\omega_s) = \frac{1}{|-L_{dc}C_{dc}\omega_s^2 + 1|} \leq 0.05\tilde{i}_{rms} \tag{44}$$

2) Design of AC side filter: The instantaneous input current is given by the primary current ni_L and the switching function of the primary bridge. The instantaneous current in phase A is given by

$$i_a = (S_{aA} - S_{aB})\, ni_L \tag{45}$$

Using (45), the rms current in phase A is given by,

$$i_{rms,a}^2 = \frac{1}{T_i}\int_0^{T_i} i_a^2 dt \tag{46}$$

$$i_{rms,a}^2 = \frac{T_s^2 \hat{d}^2 V_o^2 n^2}{15552\pi L^2}\left(36\pi\delta^2 + 9\pi\hat{d}^2 - 64\hat{d} + 12\pi\right) \tag{47}$$

The capacitive filter C_{ac} should be designed to carry the entire ripple component of the current. The ripple current rms $\tilde{i}_{rms,a}$ is found by subtracting the fundamental current rms from $i_{rms,a}$ in (47). It is assumed that the entire ripple is concentrated at the switching frequency. Considering an allowable voltage ripple to be a λ fraction of the AC voltage V_i, the filter admittance is given by,

$$Y_{pu} = \omega_s C_{ac} = \frac{\tilde{i}_{rms,a}}{\lambda V_i} \tag{48}$$

An inductor L_{ac} needs to be put after the capacitive filter to prevent any high frequency current from flowing into the grid. Following the IEEE THD requirement of 5% [31], the ripple current $\tilde{i_g}$ should be limited to 5% of fundamental.

$$\tilde{i_g}(\omega_s) = \frac{1}{|-L_{ac}C_{ac}\omega_s^2 + 1|} \leq 0.05\tilde{i}_{arms} \tag{49}$$

III. Simulation and Experimental Results

The proposed modulation strategy was simulated with MATLAB/Simulink and the results have been presented in Fig. 8. The simulation parameters are listed in Table I. Fig. 8a shows the transformer primary and secondary voltages, and the inductor current for a switching period for $\delta = 0.2$. It can be observed that the inductor current is close to zero at the transitions of v_p, demonstrating ZCS in the primary side converter, while the inductor current polarities at switching transitions in v_s show that ZVS occurs in the secondary side H-bridge. Both the AC and DC side currents have high frequency harmonics starting at switching frequency. The input AC currents for all three phases is shown in Fig.8b. The currents are sinusoidal and balanced as predicted by (22)-(24). The phase A voltage v_{an} and the current i_a are nearly in phase in Fig.8c, confirming unity power factor operation. Similar observations were found from the simulation results for negative phase shift with $\delta = -0.2$. Lastly, in order to demonstrate the accuracy of the analysis done for power transfer and RMS currents, the system was simulated for

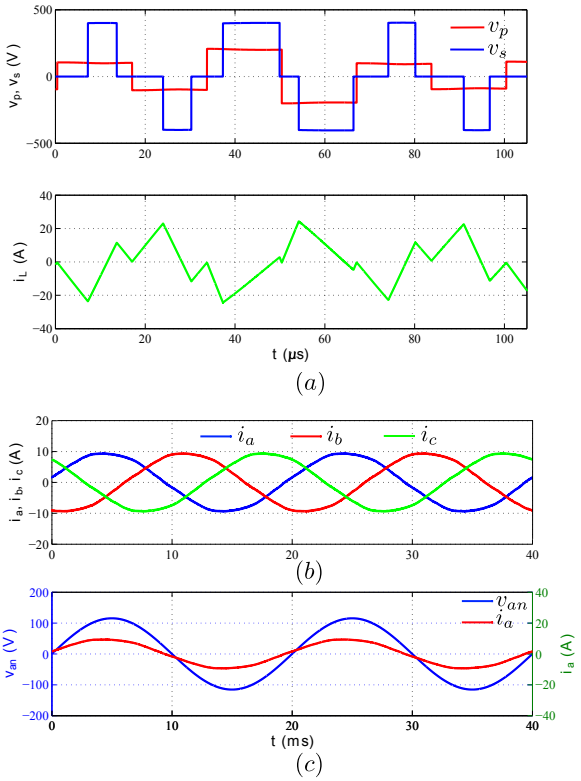

Fig. 8. Simulation results for positive phase shift $\delta = 0.2$ (a) Transformer primary and secondary voltages and inductor current (b) Currents drawn from the supply (c) v_{an} and i_a

TABLE I
Simulation and Experimental Parameters

L	n	V_i	V_o	f_i	f_s	P
47μH	1.5	115V	400V	50Hz	10kHz	1.6kW

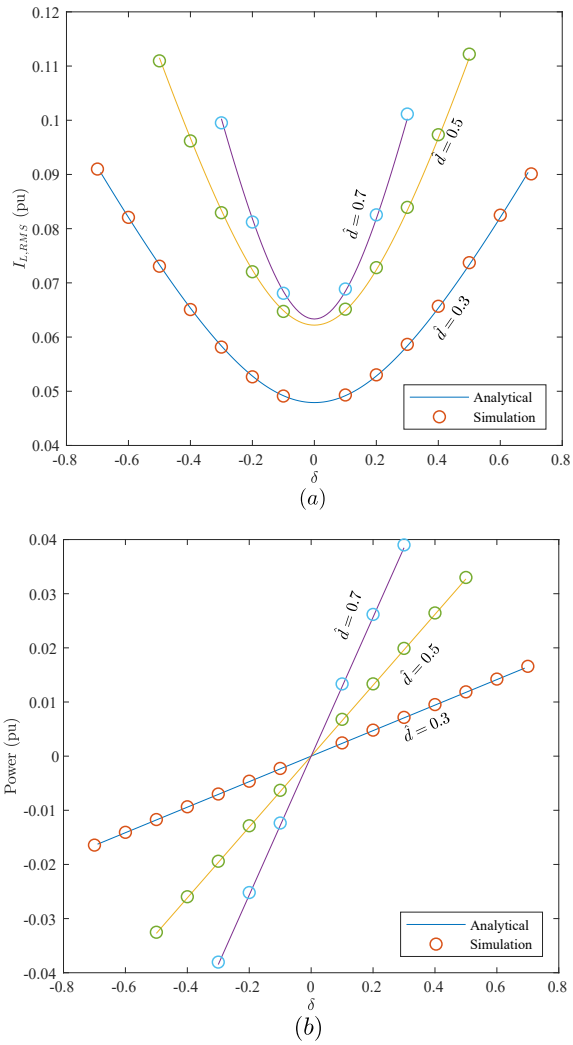

Fig. 9. Comparison for $\hat{d} = 0.3$, $\hat{d} = 0.5$ and $\hat{d} = 0.7$ (a) Comparison of analytical and simulated per unit RMS currents (b) Comparison of analytical and simulated DC per unit power

different modulation indices and phase shift values and the simulation results have been plotted together with analytical values in Fig. 9. It is observed that the simulation results follow the analytical values closely.

The setup used for the experiment is shown in Fig.10. The list of components is given in Table II. The experimental setup was run with the parameters listed in Table I with $\delta = \pm 0.2$. A positive δ signifies AC-DC power flow and vice-versa. The leakage inductance current (i_L), primary voltage (v_p) and secondary voltage (v_s) for positive δ are shown in Fig.11a. Note, that each time the primary voltage switches, the current is essentially close to zero which confirms zero current switching of the matrix converter. The sign of the inductor current at the transitions of secondary voltage v_s, ensures the soft switching of the DC side H-bridge. The switching cycle waveforms for negative δ is shown in Fig.11b. Again, it is possible to observe each time the matrix converter voltage changes, the current through the leakage inductance is essentially close to zero.

Since the H-bridge is duty cycle modulated, the pulse width

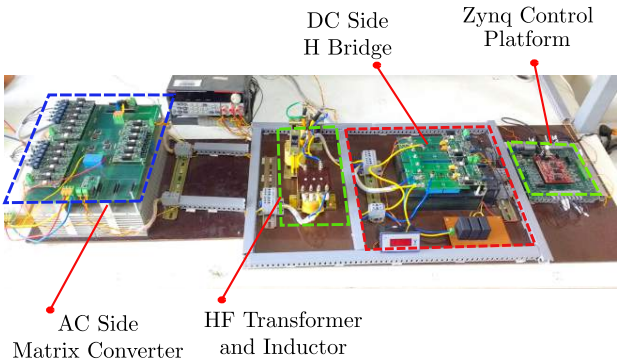

Fig. 10. Experimental Setup

TABLE II
COMPONENT LIST

Part	Part Number	Rating
IGBTs $S_{aA} - S_{cB}$	IKW40N120H3	1200V 40A
IGBTs $S_1 - S_4$	SKM100GB12T4	1200V 100A
Capacitor C_{ac}	C4ATJBW5150A3NJ	15μF $\times$ 2
Capacitor C_{dc}	MKP1848C61012JP4	10μF $\times$ 2

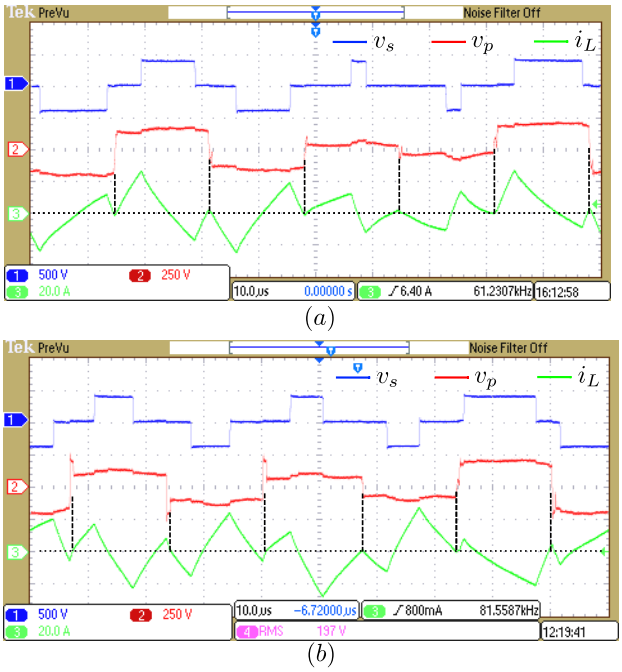

Fig. 11. Modulation Cycle waveforms for (a) $\delta = 0.2$ (b) $\delta = -0.2$

of the voltage applied at the secondary depends on phase of the input line voltage. This is demonstrated in Fig.12. For a modulation cycle where the line voltage v_{ab} is close to its peak value (Fig.12a), the pulse width of the applied secondary voltage is maximum. Similarly, a modulation cycle where the v_{ab} is close to zero (Fig.12b), the pulse width of the applied secondary voltage is small.

The three phase filtered input currents for $\delta = 0.2$ and $\delta = -0.2$ are shown in Fig.13a and Fig.13d respectively. These

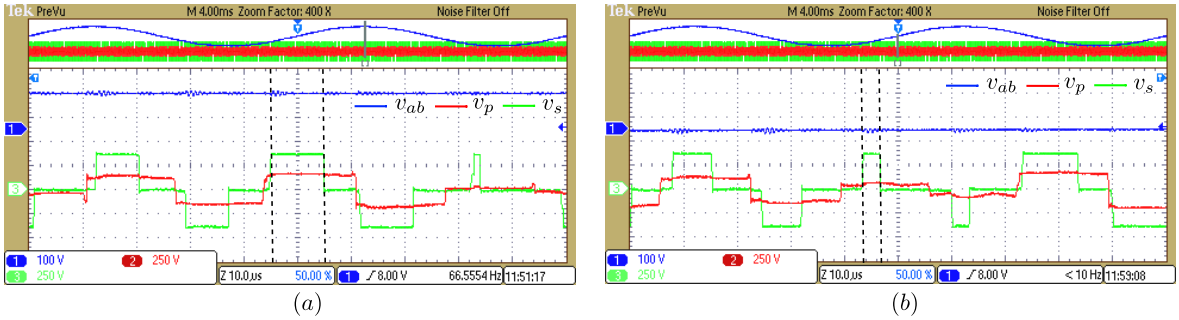

Fig. 12. Experimental Results showing duty cycle modulation (a) Line voltage v_{ab} close to peak value (b) Line voltage v_{ab} close to zero crossing

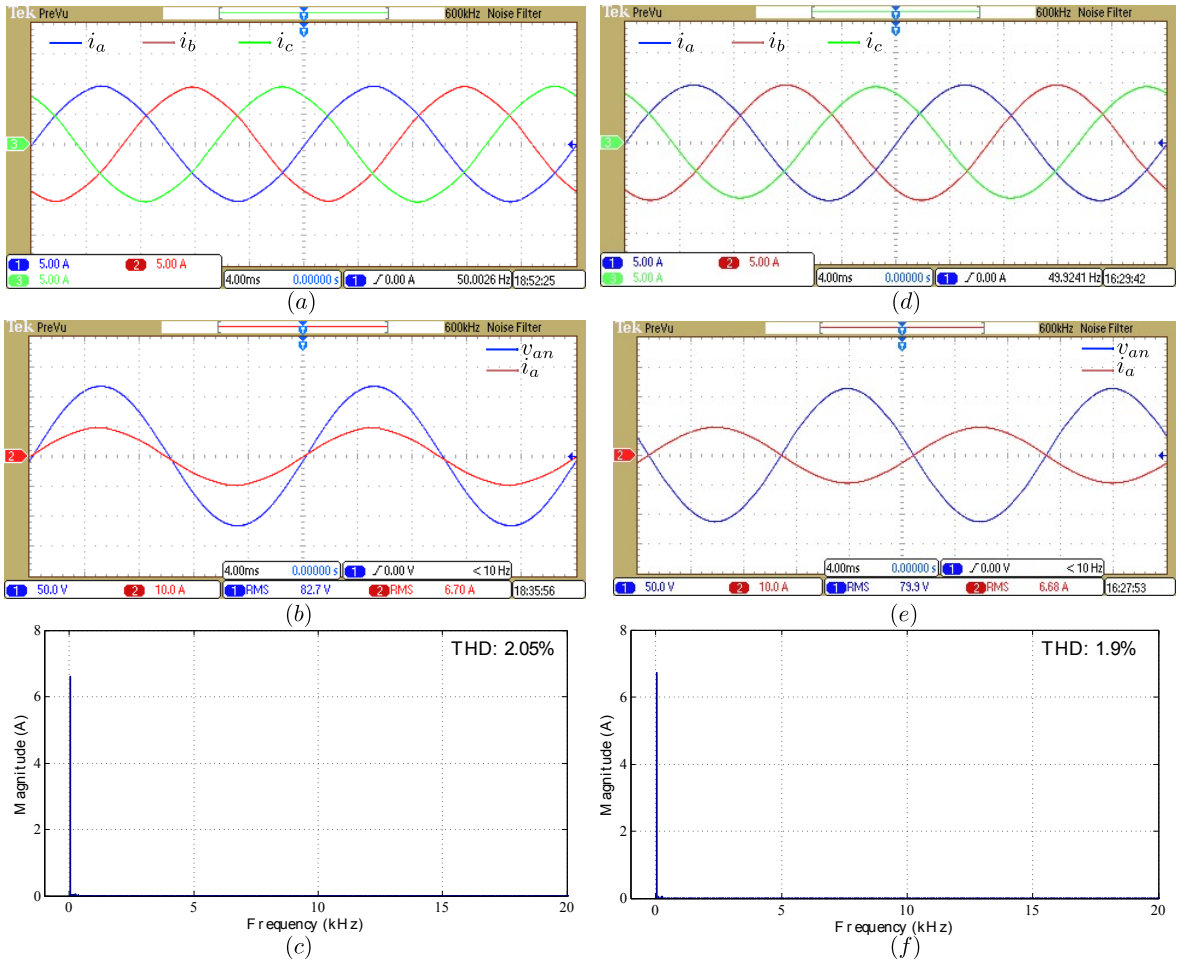

Fig. 13. Line Cycle waveforms at a Power level of 1.6 kW (a) Three phase currents ($\delta = 0.2$) (b) UPF operation ($\delta = 0.2$) (c) Experimental THD ($\delta = 0.2$) (d) Three phase currents ($\delta = -0.2$) (e) UPF operation ($\delta = -0.2$) (f) Experimental THD ($\delta = -0.2$)

waveforms confirm balanced three phase operation for both AC-DC and DC-AC operation of the converter. Fig.13b shows the line-neutral voltage v_{an} and line current i_a for AC-DC operation. The current is in phase with the voltage indicating unity power factor operation. Fig.13e shows the same result for DC-AC operation. The current i_a is $180°$ out of phase with voltage indicating negative power flow. The grid current is free from any considerable high frequency components for both the cases indicating proper filtering. The experimentally obtained harmonic spectra of the current is shown in Fig.13c and Fig.13f. The THD for both the cases is within the IEEE requirement. A comparison between the theoretical, simulation and experimental quantities is shown in Table III. A good agreement can be observed.

A. *Efficiency and Loss Estimation*

The experimentally obtained efficiency and power factor is shown in Table IV. The main reason for low efficiencies is that the hardware is not specifically designed for the operating power level but to only test the validity of the proposed modulation strategy. A theoretical and experimental loss breakdown is carried out for further insight. The conduction

TABLE III
COMPARISON AT $\delta = 0.2$

$\delta = 0.2$	Input Power (W)	AC Current (A)	PF
Theory	1631	6.66	0.99
Simulation	1625	6.71	0.98
Experiment	1662	6.70	0.99

TABLE IV
EXPERIMENTAL EFFICIENCY AND POWER FACTOR

AC Power (W)	1572	1191	825	-1639.8	-1380	-1035
Efficiency (%)	82.1	81.6	80.8	81.2	78.0	76.3
Power Factor	0.99	0.98	0.97	0.99	0.99	0.99

losses in primary and secondary bridges and the total losses in transformer and high frequency inductor is calculated. Since the current waveform in each modulation cycle has different slopes, it is difficult to arrive at a analytical closed form expression for conduction loss. The conduction loss for primary and secondary bridges have been obtained numerically. The transformer and inductor copper loss is computed using the rms current and the winding resistances.

$$P_{cu,HFT} = I^2_{rms,p} R_p + I^2_{rms,s} R_s \tag{50}$$

A comparison between the analytically and the experimentally obtained losses is given in Fig.14a. A good agreement is observed. Fig.14b shows the percentage loss distribution in each stage of the converter. It can be seen that major losses are the conduction losses in the bridges and copper loses in the transformer. For analytical demonstration of soft switching, the switching losses are calculated assuming the turn off to be completely hard-switched. The total losses obtained are **242 W**. However, the experimentally obtained losses are much less than this value (**154 W**) which provide an analytical evidence of soft switching.

B. Experimental verification of ZVS in H-Bridge

Fig.15a shows the waveforms during turn off of switch S_1 and turn on of S_2 after dead time (refer Fig. 2). The switch S_1 was carrying a current $i_L < 0$ as seen from Fig. 15a. At time t_0, the voltage input to the gate emitter circuit is reduced to -15 V. The gate emitter voltage starts to reduce. Since the sum of voltage across the switch and the diode is constant, the diode cannot start conducting unless it has become forward biased, or equivalently the voltage across the switch (and C_1) has risen to V_o. The constant pole current i_L is the sum of currents through the diode, switch and their respective capacitances. Since the pole current is no longer restricted to the switch channel, the current transfers to the capacitors C_1 and C_2. The voltage rise across switch S_1 starts at $t = t_1$ after the gate-emitter voltage goes below threshold ($v_{ge}(t_1) = 2V < V_{ge,th} = 5.8V$). The switch is in cut off region for $t > t_1$, so the channel current must be zero. Thus, the current through the switch has become zero

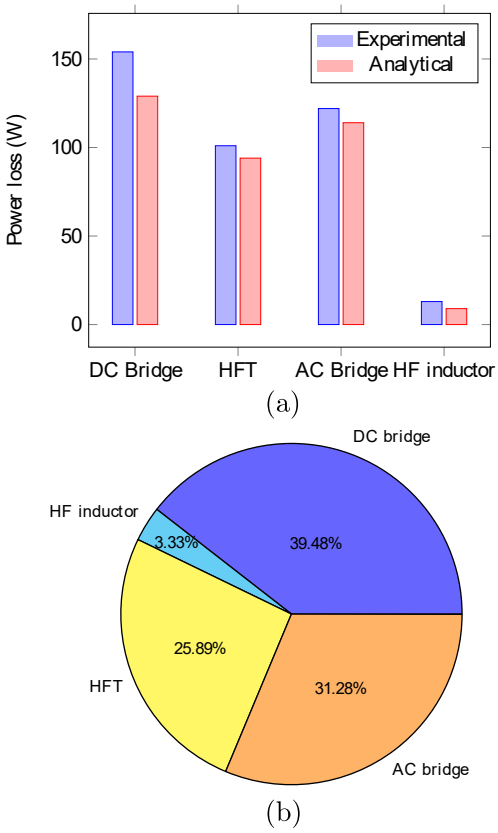

Fig. 14. (a) Power loss break-down at 1.38 kW output power obtained experimentally and analytically, (b) Percentage loss distribution shown at 1.38 kW output power obtained experimentally

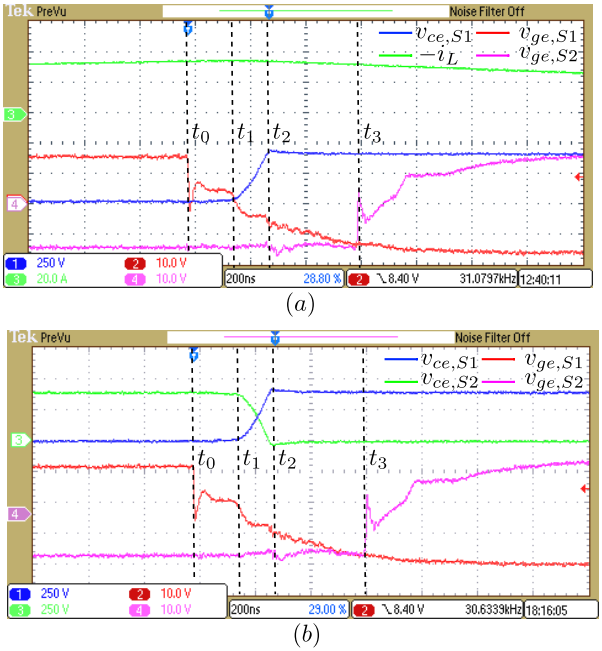

Fig. 15. Experimental waveforms demonstrating soft switching (a) Waveforms demonstrating soft turn-off (b) Waveforms demonstrating soft turn on

before voltage starts increasing implying ZVS turn off of S_1 [32]. The negative value of inductor current i_L discharges the capacitance C_2 and charges capacitor C_1. This can be seen

TABLE V
TOPOLOGY COMPARISON

		Scaling Factor	VSI+DAB (square wave)	Proposed topology
AC side converter	No. of switches	-	10	12
	Blocking voltage	V_i	$\sqrt{3}$	$\sqrt{3}$
	Switch RMS current	P/V_i	0.333 (VSI), 0.667 (DAB)	0.6373 (Switch)
DC side converter	No. of switches	-	4	4
	Blocking voltage	V_o	1	1
	Switch RMS current	P/V_o	1.155	1.0264, 2.2968
	Electrolytic capacitor	-	1	0
Transformer	Area Product	$P/(f_s J B_{max} K_w)$	0.272	0.3189
Inductor	Value	$V_o^2/(2\pi f_s)$	0.267	0.036
	RMS Current	P/V_o	1.633	2.5157

J: Current density, B_{max}: Peak flux density, K_w: Window Factor

TABLE VI
LOSS COMPARISON

		Scaling Factor	VSI+DAB (square wave)	Proposed topology
AC side converter	Conduction loss	$\left(\frac{P}{V_i}\right)^2 R_{ON,pr}$	2.447	4.8738
	Switching loss	$P f_s t_{sw,pr}$	1.104	0
DC side converter	Conduction loss	$\left(\frac{P}{V_o}\right)^2 R_{ON,sec}$	5.336	12.6575
	Switching loss	$P f_s t_{sw,sec}$	0	0
Transformer	Core & Cond.	K	0.376	0.424

Losses Proportional to $(A_c A_w)^{0.75}$, K being the constant of proportionality factor
$R_{ON,pr}$ and $R_{ON,sec}$ are device resistances. $t_{sw,sec}$: Device Switching Time

in Fig.15b. At time t_2, the capacitor C_1 is charged to V_o and the diode D_2 starts to conduct. This makes the voltage across switch S_2 zero. At t_3, the switch S_2 is turned on with zero v_{ce}. This ensures ZVS turn-on of S_2. Similar transitions can be observed for switching events in the other leg which verify the occurrence of soft switching in the bridge.

IV. CONCLUSION

In this paper, a modulation scheme for a single stage three-phase AC-DC bidirectional converter with high frequency link is presented. The main features of the modulation scheme are 1) Single stage power conversion 2) Bidirectional power flow 3) Open loop power factor correction 4) Soft switching of primary and secondary side power converters and 5) Simple linear relationship between control variable δ and transferred DC power. Presented analysis of the proposed scheme shows that all these benefits are achieved. These features are successfully demonstrated and validated through presented simulations and experimental results. The performance of the proposed topology was investigated to be at par with the conventional two stage topology. Due to lossless switching, the switching frequency of the converter may be increased leading to high power density. Moreover, due to bidirectional power flow capability, high power density and loss less switching, the proposed solution may find promising solution for V2G application.

APPENDIX

A. Comparison with conventional two stage topology

A detailed comparison of the proposed topology and the multi-stage topology shown in Fig. 1a is carried out. Same power (P), input (V_i) and output (V_o) voltage levels is assumed for both the topologies. The multi stage topology used for comparison consists of a DC-DC DAB operated with conventional phase shift modulation followed by a three-phase PWM rectifier realised with a voltage source inverter modulated using Conventional space vector PWM (CSVPWM). The DAB converter is modulated at a point where power is maximum and the VSI is modulated with maximum possible modulation index. For comparing cost and power density, the device requirement (number, voltage, current rating) and transformer size is compared in Table V. For comparing the efficiency, a loss comparison is given in Table VI. It can be seen from Table V that most of the parameters are comparable for both the topologies. However, Table VI reveals that the proposed topology is having higher conduction losses. However, the switching losses for the proposed converter are absent which

enables operation of the converter at much higher switching frequency leading to better size and power density.

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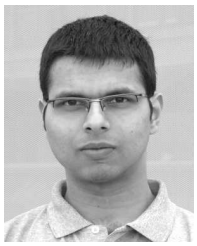
Dibakar Das received the B.Tech degree from National Institute of Technology, Durgapur, India, in 2014 and M.S degree in electrical engineering from the Indian Institute of Science, Bangalore, India, in 2017. He is currently pursuing his Ph.D. in electrical engineering from Indian Institute of Science, Bangalore, India. His research interests include dual active bridge converters.

Nathan D. Weise (M'08) received the B.S. degree in computer engineering, the M.S. degree in electrical engineering, and the Ph.D. degree in electrical engineering in 2005, 2007, and 2011, respectively, from the University of Minnesota, Minneapolis,MN, USA.

He was an Electrical Engineer at Cummins Power Generation and General Electric Global Research. He joined the University of Maine, Orono, ME, USA as an Assistant Professor in 2011. His current interests include electrification of transportation, control of renewable energy sources, wave energy converters, HVDC, and smart grid.

Kaushik Basu (S'07, M'13, SM'17) received the BE. degree from the Bengal Engineering and Science University, Shibpore, India, in 2003, the M.S. degree in electrical engineering from the Indian Institute of Science, Bangalore, India, in 2005, and the Ph.D. degree in electrical engineering from the University of Minnesota, Minneapolis, in 2012, respectively. He was a Design Engineer with Cold Watt India in 2006 and an Electronics and Control Engineer with Dynapower Corporation USA from 2013-15. Currently he is an Assistant Professor, in the Department of Electrical Engineering in Indian Institute of Science. He has been an author and coauthor of several technical papers published in peer reviewed journals and conferences. His research interests include various aspects of the general area of Power Electronics. He is the founding chair of both IEEE PELS and IES Bangalore Chapter.



Rohit Baranwal (S'12, M'16) received the B.Tech. degree in electrical engineering from the Indian Institute of Technology Roorkee, Roorkee, India, in 2008, and the M.S. and Ph.D. degrees in electrical engineering from the University of Minnesota, Minneapolis, MN, USA, in 2014 and 2015, respectively.

He is currently an Electrical Engineer with MTS Systems Corporation, Eden Prairie, MN, USA. His research interests include electric drives and grid-tied converters.

Ned Mohan (S'72, M'73, SM'91, F'96, LF'12) received the Bachelor's degree in electrical engineering from the Indian Institute of Technology Kharagpur, India, in 1967, and the Master's degree in nuclear engineering and the Ph.D. degree in electrical engineering from the University of Wisconsin Madison, USA, in 1972 and 1973, respectively.

He is currently the Oscar A. Schott Professor of power electronics with the University of Minnesota, Minneapolis,MN, USA, where he has been engaged in teaching since 1976. He has numerous patents and publications in the field of power electronics, electric drives, and power systems. He has authored or co-authored five textbooks, one of which has been translated into six languages.

Dr. Mohan received the 2008 IEEE PES Outstanding Educator Award, 2010 IEEE Undergraduate Teaching Award, 2010 UWIG Achievement Award from Utility Wind Integration Group, 2011 Distinguished Alumnus Award from IIT Kharagpur, and 2012 IEEE Power and Energy Society Ramakumar Family Renewable Energy Excellence Award. In 2013, he received the Innovative Program Award from the ECE Department Heads Association made up of over 250 universities in the United States.