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A Dual Active Bridge Based Single Phase AC to DC Power Electronic Transformer With Advanced Features

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***Abstract*—Power Electronic Transformers (PET) offer the advantage of size and weight reduction compared to line frequency transformers by operating at much higher frequencies than line frequency. In this paper, a push-pull based AC/DC PET has been proposed and analyzed. The PET offers bidirectional power flow between single phase AC and DC, using the Dual Active Bridge (DAB) principle. Such a system may find applications in interfacing plug-in hybrid and electric vehicles to the grid. The proposed PET offers advantages of (a) open loop unity power factor operation, (b) soft-switching of secondary side converter power switches for all operating points, (c) high power density owing to use of a high frequency transformer and (d) high utilization factor, compared to previous work. Analysis has been done for power transfer, utilization factor and soft-switching. Simulation and experimental results have been provided to demonstrate the operation of the PET.**

***Index Terms*—Power Electronic Transformer, AC−DC conversion, Pulse Width Modulation (PWM), Push-pull, Power factor correction, Soft-switching, Unity power factor, Dual Active Bridge**

I. Introduction

[1] Power Electronic Transformers (PET) offer the benefit of reduced size and weight over line frequency transformers, along with advanced features such as controlled power flow etc. [3]. With rapid advances in semiconductor technology [4]–[7], they are coming closer to being viable in practical applications. They can be used in a variety of applications requiring galvanic isolation and connection of systems at different voltage levels and control of power flow. One of the promising applications of PET is the integration of renewable energy sources to the grid and the AC load. Most of these renewable resources such as PV or fuel cells are available in the form of DC. Hence, an isolated single phase AC to DC inverter forms an integral part of PET. Some of the applications of an isolated single phase AC to DC inverter are integration of solar panels to the grid [8], DC distribution systems [9], charging of plug-in hybrid and electric vehicles [10], [11], propulsion systems and as a front end for isolated AC/AC converters [12]. A single phase isolated AC/DC converter can be realized either by single stage or by multi-stage topologies.

Several two stage systems have been proposed for AC/DC conversion with isolation. Typically they consist of an uncontrolled rectification stage or an active front end rectifier with power factor correction, creating a stable DC link, which is then followed by an isolated DC/DC converter. The DC/DC converter could either be a pulse width modulated (PWM) converter i.e. isolated boost [13], flyback, full bridge converter, dual active bridge (DAB) [8], [14]–[18] or it could be resonant based converter [19], [20]. Single stage conversion systems on the other hand generate a high frequency voltage directly from the AC source without a DC link in between. The benefits of single stage systems over their two stage counterparts are increased power density and lower device count etc. Single stage converters can be classified into two groups: PWM based [2], [21]–[24] and resonant based converters [25]–[28]. DAB based single stage converters offer benefits of soft switching, control of active power transfer and bidirectional power flow capability, along with galvanic isolation.

DABs were introduced in [29], where the control of power transfer was achieved through phase shift between two square waves. This is known as traditional phase shift modulation (TPS). Later, Pulse Width Modulation (PWM) was employed in the control of DABs, resulting in an improvement of the soft switching range [30]–[37]. In [38], [39], an extended phase shift modulation (EPS) is proposed where only one bridge is duty cycle modulated and results in minimization of backflow power. In [40], a dual phase shift modulation (DPS) is proposed where the outputs of both of the bridges are duty cycle modulated with same duty ratio, leading to an overall minimization of losses. Varying all three degrees of freedom, i.e. the duty cycle of both bridges and the phase shift between the voltages has also been considered for minimization of RMS of the transformer current [41]. Multi-level topologies of DABs have also been investigated [42].

A single stage DAB based isolated AC/DC unidirectional converter was proposed in [43]. Bidirectional version of this converter is considered in [2], [44], [45]. In all these works, the DC side converter is an H-bridge with four two quadrant switches (an active switch with an anti-parallel diode). In [2] and [44], an H-bridge with four quadrant switches (two active switches with two anti-parallel diodes) is used as the AC

[1]The topology proposed in this paper was first presented in [1]. The current paper proposes a new modulation scheme that results in 50% higher utilization factor (UF) than [2] and still achieves complete soft switching of the DC side converter and open loop input power factor correction. Higher UF implies smaller transformer size, lower current rating of the switches, less conduction loss and less DC ripple current, leading to higher power density. This paper also presents experimental results.

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side converter. This requires eight total active switches with a voltage rating equal to the peak value of the AC voltage (V_{pr}). In [23], a half bridge configuration is considered requiring active switches with voltage rating of V_{pr}. This paper proposes a push-pull configuration that requires only two active switches with voltage rating of $2V_{pr}$. This topology requires maximum number of diodes and two primary windings. Eight diodes are also required in [2], [44], whereas four diodes are required in [23]. A single primary winding is required in [2], [23], [44]. The proposed push-pull configuration significantly simplifies the primary converter topology requiring only two controlled switches which are switched in a complimentary fashion with a dead time.

In [2], [23], [44], [45], the AC side converter is switched with square wave modulation and the output of the DC side H-bridge is duty cycle modulated, thus giving two control parameters: duty cycle d and the phase shift between the voltages. In [44], these parameters are set using a look up table and a closed loop controller that ensures soft switching. In [23], switching frequency along with other control parameters viz. duty cycle and phase shift are set to minimize the peak of the transformer current over a switching period. Here also, a look up table (obtained from off-line optimization) along with closed loop controllers is used for the determination of control parameters. In [2], the control parameters are set to obtain soft switching (ZCS in AC side converter and ZVS in DC side converter) and open loop power factor correction. This paper extends this control technique to obtain substantial reduction in RMS transformer current and still achieves ZVS in secondary side converter and open loop power factor correction. Lower RMS transformer current implies smaller transformer size, lower current rating of switches, less conduction losses and less dc ripple current, leading to higher efficiency and power density. If instead of push-pull (two winding primary), a full bridge (single winding primary) is considered, this control strategy results in substantially smaller transformer size or area product.

The paper is organized in nine sections. The second section introduces the topology along with the modulation technique and defines the modes of operation. In the third section, the converter is analyzed for a switching period to derive power transfer and RMS currents. In the fourth section, line frequency averages have been computed for average power transfer and utilization. A transformer design method is explained in the fifth section, that also talks about some of the practical aspects of the circuit. Soft switching has been studied in section six. Section seven gives the analysis to show how low order harmonics appear in AC current and then describes a compensation technique to suppress those harmonics. The simulation and experimental results have been provided in section eight to validate all the analysis done in the paper. Finally, the last section concludes the paper.

II. Topology Description and Modulation Technique

The circuit diagram of proposed topology is shown in Fig. 1. The primary windings of the transformer are connected to the single phase AC source $v_{pr}(t)$ in a push-pull configuration with two switches S_1 and S_2. Each four quadrant switch is realized with an IGBT and a single phase diode rectifier, as seen in the figure. The turns ratio of each primary winding to the secondary winding is $1:n$. The dot at each winding of the transformer signifies the voltage polarity. The secondary side of the transformer is connected to an H-bridge through an inductor L that represents the leakage inductance of the transformer reflected on secondary side along with any additional inductance connected to the secondary winding. The H-bridge consists of four IGBTs S_{X_1}, S'_{X_1}, S_{X_2} and S'_{X_2}. It is connected to a DC link with voltage V_{dc}.

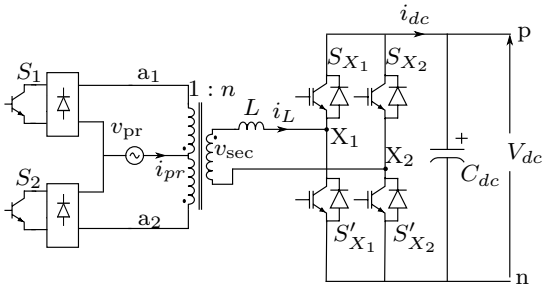

Fig. 1. Circuit diagram of the high frequency link converter

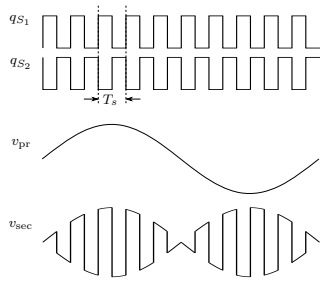

Fig. 2. Primary side switch pulses and voltage waveforms

The input (utility) voltage $v_{pr}(t)$ is assumed to be purely sinusoidal with amplitude V_{pr} and angular frequency $\omega = 2\pi f = \dfrac{2\pi}{T}$, where f is the line frequency of 60 Hz or 50 Hz. Switches S_1 and S_2 are switched at a frequency $f_s = \dfrac{1}{T_s}$ with 50% duty ratio in a complimentary fashion and $f_s >> f$, as illustrated in Fig. 2. The waveforms q_{S_1} and q_{S_2} represent the control pulses of IGBTs S_1 and S_2 respectively. The push-pull action of the transformer produces a high frequency square wave $v_{sec}(t)$ with a sinusoidal envelope across the secondary winding of the transformer, as defined in (2). Since $f_s >> f$, voltage v_{sec} can be approximated as a true square wave in one switching period.

$$v_{pr} = V_{pr}\sin(\omega t) = V_{pr}\sin\theta \tag{1}$$

$$v_{sec} = \pm V_{sec} = \pm n V_{pr}\sin(\omega t)$$
$$(+ \text{ when } S_1 \text{ ON}, - \text{ when } S_2 \text{ ON}) \tag{2}$$

The secondary side H-bridge is pulse width modulated at the same switching frequency f_s to generate a quasi-square voltage $v_{X_1X_2}$, with duty ratio d and amplitude V_{dc}, as shown in Fig. 3(a) with $QR = d\dfrac{T_s}{2}$. The duty cycle is computed as

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the ratio $\frac{|v_{\rm sec}|}{V_{dc}}$ (3), with the turns ratio chosen such that the modulation index $m = \frac{nV_{pr}}{V_{dc}}$, is a proper positive fraction. The duty ratio is chosen as the ratio between secondary side voltage and DC voltage (3).

$$d = \frac{|v_{\rm sec}|}{V_{dc}} = m|\sin\theta| \tag{3}$$

Both voltage waveforms $v_{\rm sec}$ and $v_{X_1X_2}$ have quarter wave symmetry over a switching cycle T_s . The points N and M in Fig. 3(a) are the mid-points of $v_{\rm sec}$ and $v_{X_1X_2}$ respectively for one half of switching period T_s. The distance between these points is defined as δT_s. It is the time delay of $v_{X_1X_2}$ with respect to $v_{\rm sec}$. The delay is defined as positive if $v_{X_1X_2}$ lags $v_{\rm sec}$, as shown in Fig. 3(a). If the voltage $v_{X_1X_2}$ leads $v_{\rm sec}$, then δ is said to be negative, as shown in Fig. 3(b), where the distance between points M and N is $-\delta T_s$. It will be shown in the next section, that the power flow between the two voltage sources through the series inductor L, is a function of δ. No time delay ($\delta = 0$) results in zero power flow. Power flow from primary to secondary side is defined as positive.

Considering a symmetric bipolar range of δ, from -0.5 to +0.5, it is possible to show a positive δ results in positive power flow, while the negative δ results in negative power flow. Again, due to quarter wave symmetry of the voltage waveforms, its possible to show that both the ranges $0.25 < |\delta| < 0.5$ and $0 < |\delta| < 0.25$, result in same power flow, so we keep δ, between -0.25 to 0.25.

As mentioned earlier, the power flow depends on δ, but the functional dependence of power flow on δ changes based on the condition whether the positive voltage pulse of $v_{X_1X_2}$, is completely contained in the positive half of $v_{\rm sec}$ or not. In other words, the time segment QR in Fig. 3(a), is completely contained in segment OP. For positive δ as shown in Fig. 3(a), this implies OR $<$ OP = $\frac{T_s}{2}$. Note, in Fig. 3(a), the voltage $v_{X_1X_2}$ lags the voltage v_{sec} and ON = $\frac{T_s}{4}$, NM = δT_s and MR = $\frac{\rm QR}{2}$= $d\frac{T_s}{4}$. For negative δ, the waveform $v_{X_1X_2}$ leads v_{sec}, as shown in Fig. 3(b) and MN = $-\delta T_s$. Now in Fig. 3(a), given that OR = ON + NM + MR, this condition implies, $d < 1-4\delta$. Similarly, a condition for negative δ can be derived. When the condition given in (4) is satisfied, the PET is said to be operating in MODE I. When the condition in (4) is not satisfied, the PET is said to be operating in MODE II. The waveforms $v_{X_1X_2}$ and $v_{\rm sec}$ with positive δ for MODE II are shown in Fig. 3(c). The waveforms $v_{X_1X_2}$ and $v_{\rm sec}$ with negative δ for MODE II are shown in Fig. 3(d).

$$d < 1 - 4|\delta| \tag{4}$$

From, (3) and Fig. 4, it is possible to show that, if $m < 1-4|\delta|$, the PET will always be in MODE I, as shown by the horizontal line for δ_1. Otherwise, there will be mixed mode operation where the PET is in MODE II when $\phi < \omega t < \pi-\phi$, with ϕ defined in (5) and is in MODE I elsewhere, as shown by the horizontal line for δ_2 in Fig. 4. Note that maximum

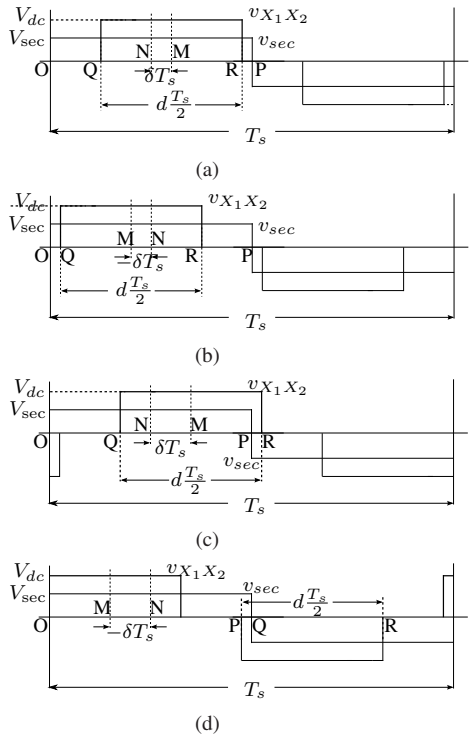

Fig. 3. Modes of operation of single phase PET (a) Mode I, positive δ (b) MODE I, negative δ (c) MODE II, positive δ (d) MODE II, negative δ

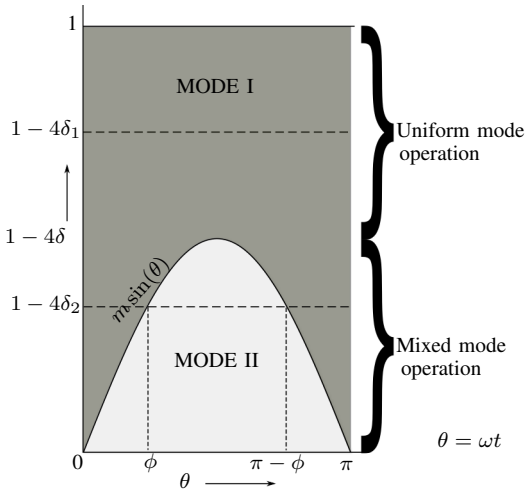

Fig. 4. Single phase PET operating modes: δ_1 shows Uniform Mode operation while δ_2 shows Mixed Mode operation

value of m and $1-4|\delta|$, both are equal to one.

$$\phi = \sin^{-1}\left(\frac{1-4|\delta|}{m}\right) \tag{5}$$

The conditions for the single phase PET to operate in various modes and regions are summarized in Table I.

III. Computation over one switching period

In this section, the average power transferred and the RMS value of the ripple current through the output capacitor over one switching cycle are computed as a function of $d = m|\sin\theta|$ and δ. The functional relation will depend on

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TABLE I
MODES OF OPERATION OF SINGLE PHASE PET

	Condition on δ	Mode		Mode transition θ expression
		MODE I	MODE II	
Uniform	$0 < \lvert\delta\rvert \leq \frac{1-m}{4}$	$0 < \theta \leq \pi$	N/A	N/A
Mixed	$\frac{1-m}{4} < \lvert\delta\rvert \leq \frac{1}{4}$	$0 < \theta \leq \phi$ $\pi - \phi < \theta \leq \pi$	$\phi < \theta \leq \pi - \phi$	$\phi = \sin^{-1}\left(\frac{1-4\lvert\delta\rvert}{m}\right)$

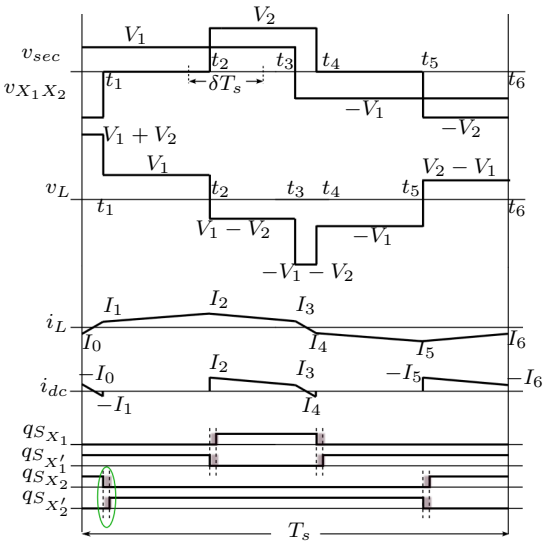

Fig. 5. MODE II operation (positive δ): Transformer secondary and H-bridge voltages, inductor voltage, inductor current, DC link current and H-bridge gate pulses

the mode of operation. The computation of these quantities for MODE I can be found in [1]. Hence, details of the computation are provided only for MODE II. However, the results of MODE I have been included in this section for completion and its application in finding the line frequency quantities in the next section.

The first step is the determination of the inductor current i_L over one switching cycle in MODE II in steady state. Fig 5 shows the typical voltage and current waveforms across the inductor. The voltage waveform can be obtained as a difference between v_{sec} and $v_{X_1X_2}$. For simplicity, the waveforms have been relabeled here as $V_1 = mV_{dc}\sin\theta$ and $V_2 = V_{dc}$. The slopes of the piece wise linear inductor current waveform i_L are directly related to the voltage across it, v_L as $L\frac{di_L}{dt} = v_L$. Computation of currents I_0 to I_6 completely determines i_L . The inductor current during all the six time segments in one switching period is now described.

- Time t_0 to t_1: The primary side switch S_1 is ON. The secondary side voltage v_{sec} therefore equals the primary side voltage multiplied by the turns ratio n, i.e. $nV_{pr}\sin\theta$. The H-bridge switches $S_{X'_1}$ and S_{X_2} are turned ON during this period. The converter circuit looks like that in Fig. 6(a). The output voltage of the H-bridge $v_{X_1X_2}$ is therefore equal to $-V_{dc}$. Hence, the inductor current is given by the relation below.

$$i_L = I_0 + \frac{v_L}{L}(t - t_0) = I_0 + \frac{nV_{pr}\sin\theta + V_{dc}}{L}(t - t_0)$$

The dc link current i_{dc} equals the inductor current. The primary side current i_{pr} equals the inductor current multiplied by turns ratio n.

- Time t_1 to t_2: The primary side switch S_1 is ON, making secondary side voltage $v_{sec} = nV_{pr}\sin\theta$. The switches $S_{X'_1}$ and $S_{X'_2}$ of the H-bridge are ON, leading to zero voltage at H-bridge output. The converter circuit looks like that in Fig. 6(b). The dc link current is zero in this period. The inductor current is given as follows.

$$i_L = I_1 + \frac{v_L}{L}(t - t_1) = I_1 + \frac{nV_{pr}\sin\theta}{L}(t - t_1)$$

The primary side current i_{pr} equals the inductor current multiplied by turns ratio n.

- Time t_2 to t_3: The primary side switch S_1 is ON, making secondary side voltage $v_{sec} = nV_{pr}\sin\theta$. The switches S_{X_1} and $S_{X'_2}$ are ON, making the H-bridge output voltage V_{dc}. The converter circuit looks like that in Fig. 6(c). The dc link current equals the inductor current and the primary current equals the inductor current multiplied by turns ratio n. The inductor current is described by the following equation.

$$i_L = I_2 + \frac{v_L}{L}(t - t_2) = I_2 + \frac{nV_{pr}\sin\theta - V_{dc}}{L}(t - t_2)$$

- Time t_3 to t_4: The primary side switch S_2 is ON, making secondary side voltage $v_{sec} = -nV_{pr}\sin\theta$. The switches S_{X_1} and $S_{X'_2}$ are ON, making the H-bridge output voltage V_{dc}. The converter circuit looks like that in Fig. 6(d). The dc link current equals the inductor current. The primary current $i_{pr} = -ni_L$. The inductor current is described by the following equation.

$$i_L = I_3 + \frac{v_L}{L}(t - t_3) = I_3 + \frac{-nV_{pr}\sin\theta - V_{dc}}{L}(t - t_3)$$

- Time t_4 to t_5: The primary side switch S_2 is ON, making secondary side voltage $v_{sec} = -nV_{pr}\sin\theta$. The switches $S_{X'_1}$ and $S_{X'_2}$ are ON, making the H-bridge output voltage zero. The converter circuit looks like that in Fig. 6(e). The dc link current is zero. The primary current $i_{pr} = -ni_L$. The inductor current is described by the following equation.

$$i_L = I_4 + \frac{v_L}{L}(t - t_4) = I_4 + \frac{-nV_{pr}\sin\theta}{L}(t - t_4)$$

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- Time t_5 to t_6: The primary side switch S_2 is ON, making secondary side voltage $v_{sec} = -nV_{pr}\sin\theta$. The switches $S_{X_1'}$ and S_{X_2} are ON, making the H-bridge output voltage $-V_{dc}$. The converter circuit looks like that in Fig. 6(f). The dc link current is equal to the inductor current. The primary current $i_{pr} = -ni_L$. The inductor current is described by the following equation.

$$i_L = I_5 + \frac{v_L}{L}(t - t_5) = I_5 + \frac{-nV_{pr}\sin\theta + V_{dc}}{L}(t - t_5)$$

The time instants $t_1 - t_6$ are given as follows, wrt to t_0.

$$\begin{aligned}
t_1 &= \left(\delta + \frac{d-1}{4}\right) T_s \\
t_2 &= \left(\delta + \frac{1-d}{4}\right) T_s \\
t_3 &= \frac{T_s}{2} \\
t_4 &= \frac{T_s}{2} + t_1 \\
t_5 &= \frac{T_s}{2} + t_2 \\
t_6 &= T_s
\end{aligned}$$

The currents I_1 through I_6 are first computed by assuming I_0 as an unknown variable. Once computed, the expression for I_0 is determined using the assumption that the average value of i_L over a switching period T_s is zero. Upon doing these calculations, following values are obtained.

$$\begin{aligned}
I_0 &= -\frac{T_s V_{dc}}{4L}(-1 + 4\delta + m\sin\theta) \\
I_1 &= \frac{T_s V_{dc}}{4L} m\sin\theta(-1 + 4\delta + m\sin\theta) \\
I_2 &= -\frac{T_s V_{dc}}{4L} m\sin\theta(-1 - 4\delta + m\sin\theta) \\
I_3 &= -I_0 \\
I_4 &= -I_1 \\
I_5 &= -I_2 \\
I_6 &= I_0
\end{aligned} \tag{6}$$

The average power that has been transferred from the AC to the DC side over a switching cycle in MODE II is given in (7) as a function of m, θ and δ, while the expression for MODE I is given in (8) [1]. The RMS of the inductor current over a switching cycle in different modes is given in (10), (9). The RMS ripple current that goes into the DC link capacitor, can be obtained from the RMS of the DC link current i_{dc} as given in (11). They are given in (12) and (13).

IV. Computation over one line cycle

In this section, the average and RMS values of different quantities over one cycle of the input AC voltage will be computed from the switching cycle average obtained in the last section. Assuming the general case of mixed mode of operation $(1 - 4|\delta| < m)$, the per unit average power as a function of m and δ, transferred from the AC to the DC side can be computed using (14). The voltage base and the impedance base for computing the per unit quantities are V_{dc} and $2\pi f_s L$ respectively. Similarly the RMS per unit ripple current through the DC link capacitor can be computed as a function of m and δ, as given in (15). The inductor RMS current $< i_L >_T$, also the transformer secondary current $I_{s,RMS}$, is given in (16). The utilization factor (UF) of this converter can be defined as the ratio of the active power transferred to the RMS of the current through the inductor, $UF = \dfrac{< P >_T}{< i_L >_T}$. UF is an indication of the amount of RMS current needed to transfer a particular amount of active power. The RMS of the inductor current in this converter is a measure of conduction loss, the current rating of the semi-conductor switches and the size of the high frequency transformer. A better utilization factor also implies lower ripple current in the DC link capacitor.

Based on above discussion, it is now determined that for $1 - 4|\delta| > m$, the converter always operates in MODE I (uniform mode). Expressions for per unit power and the ripple current in this case are derived in [1] and given in the appendix. Fig 7(a) shows a plot of per unit power as a function of δ and m. A black curve in the plot denotes the boundary of uniform mode and mixed mode operation. For a given m, for $\delta < \dfrac{1-m}{4}$, the plot follows the power expression given in the appendix (only in MODE I), i.e. till it touches the black curve. Beyond this point, it follows the expression for mixed mode of operation given in (14). Fig. 7(b) and Fig. 7(c) show plots for RMS per unit inductor current and RMS per unit ripple current through the capacitor respectively. Fig. 7(d) shows the plot of utilization factor. In all these plots, the black curve marks the boundary between uniform mode and mixed mode of operation. From Fig. 7(a), it is immediately visible that the maximum power transfer in mixed mode is nearly four times that of maximum power transfer in uniform mode of operation, provided the primary side AC, secondary side DC voltage levels, the inductance L and switching frequency f_s are kept same. In addition, it is observed from Fig. 7(d) that the maximum utilization factor is 0.613 at $m = 1$ and $\delta = 0.09$, an improvement of over 50% in the mixed mode of operation compared to 0.399 at $m = 0.78$ and $\delta = 0.055$ in the uniform mode of operation.

Based on the analysis done so far, the procedure to generate control pules for the converter is presented as a flowchart in Fig. 8.

V. Design procedure

A design method for the proposed converter is given in this section. In order to start the design, the given specifications are

1) Peak AC voltage V_{pr}
2) DC voltage V_{dc}
3) Rated power P
4) Switching frequency $f_s = \dfrac{1}{T_s}$

The choice of m and δ decides the amount of active power $< P >_T$ transferred over a line frequency cycle and also the RMS of the inductor current $< i_L >_T$. The RMS inductor current is a measure of current stress in the switching

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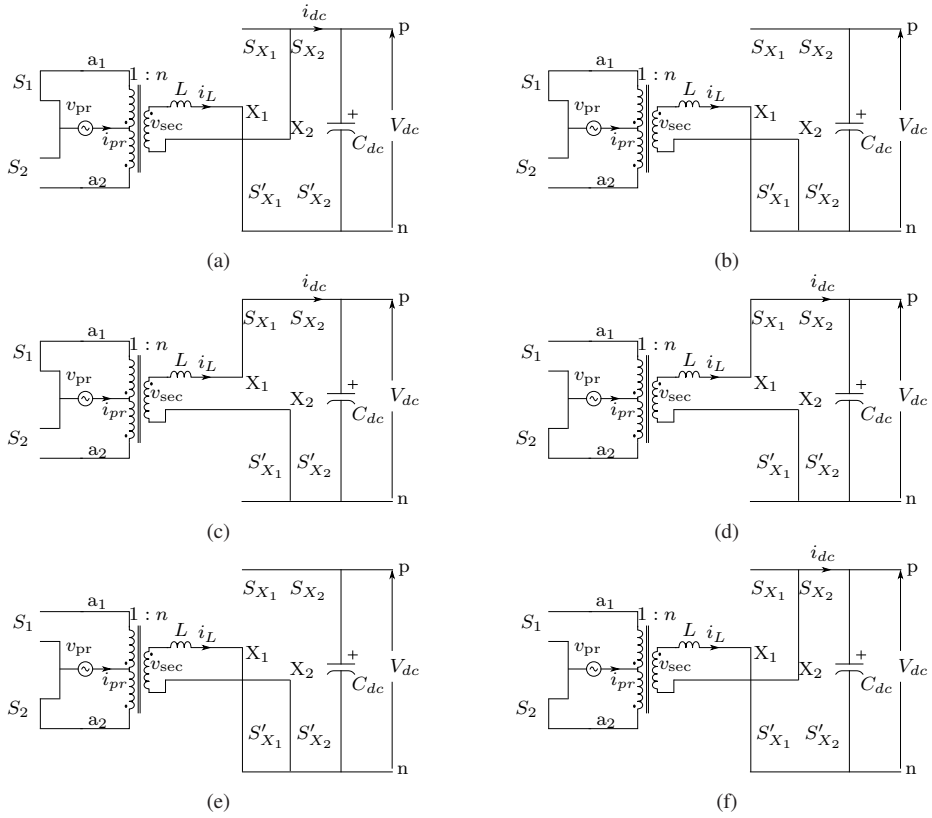

Fig. 6. Converter circuit in different time segments in MODE II (a) Time t_0 to t_1 (b) Time t_1 to t_2 (c) Time t_2 to t_3 (d) Time t_3 to t_4 (e) Time t_4 to t_5 (f) Time t_5 to t_6

$$< P_{II} >_{T_s} (d = m|\sin\theta|, \delta) = \frac{1}{T_s}\int_0^{T_s} v_L i_L dt = \frac{V_{\text{sec}} V_{dc} T_s}{L}\left(\delta(1-2\delta) - \frac{(1-d)^2}{8}\right)$$
$$= \frac{m V_{dc}^2 \sin\theta T_s}{L}\left(\delta(1-2\delta) - \frac{(1-m\sin\theta)^2}{8}\right) \quad (7)$$

$$< P_I >_{T_s} (d = m|\sin\theta|, \delta) = \frac{\delta d V_{\text{sec}} V_{dc} T_s}{L} = \frac{\delta(m V_{dc}\sin\theta T_s)^2}{L} \quad (8)$$

$$< i_{L_{II}} >_{T_s} (d = m|\sin\theta|, \delta) = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_L^2 dt} = \frac{T_s V_{dc}}{4\sqrt{6}L}[m\sin\theta(2 - 24\delta + 96\delta^2 - 128\delta^3 + m^2$$
$$- 12\delta m^2 + (-1 + 12\delta)m^2\cos(2\theta) + 4(-1 + 12\delta)m\sin\theta)]^{\frac{1}{2}} \quad (9)$$

$$< i_{L_I} >_{T_s} (d = m|\sin\theta|, \delta) = \frac{T_s V_{dc} m\sin\theta}{4\sqrt{6}L}\sqrt{2 + 96\delta^2 + m^2 - m^2\cos(2\theta) - 4m\sin\theta} \quad (10)$$

$$< \tilde{i}_{C_{II}} >_{T_s} (d = m|\sin\theta|, \delta) = \sqrt{(< i_{dc_{II}} >_{T_s})^2 - \left(\frac{< P_{II} >_{T_s}}{V_{dc}}\right)^2} \quad (11)$$

devices, winding losses in the transformer and the size of the transformer. Given the amount of active power that needs to be transferred, the values of m and δ are to be selected to get highest utilization factor $UF = \dfrac{< P >_T}{< i_L >_T}$, plotted in Fig. 7(d). The highest utilization factor occurs at $m = 1$ and $\delta = 0.09$. Therefore, the turns ratio of the transformer should be $n = \dfrac{V_{dc}}{V_{pr}}$. At $m = 1$ and $\delta = 0.09$, the per unit power is $< P >_T (m = 1, \delta = 0.09) = 0.255$. Thus, the required

$$< \tilde{i}_{C_{II}} >_{T_s} (d = m|\sin\theta|, \delta) = \frac{T_s V_{dc}}{16\sqrt{3}L}[m\sin\theta(-3m\sin\theta(2 - 16\delta + 32\delta^2 + m^2 - m^2\cos(2\theta) - 4m\sin\theta)^2 + 16(-(-1+4\delta)^3 - 3(1-4\delta)^2 m\sin\theta + 4(1 - 3\delta + 12\delta^2)m^2\sin\theta^2 - 3m^3\sin\theta^3 + m^4\sin\theta^4))]^{\frac{1}{2}} \quad (12)$$

$$< \tilde{i}_{C_I} >_{T_s} (d = m|\sin\theta|, \delta) = \frac{T_s V_{dc}}{4\sqrt{3}L}\sqrt{m^3\sin\theta^3(-1 + m\sin\theta)(-1 - 48\delta^2 + m\sin\theta)} \quad (13)$$

$$< P >_T (m, \delta) = \frac{2\pi f_s L}{V_{dc}^2}\frac{1}{\pi}\left(\int_0^{\phi} < P_I >_{T_s} (d = m|\sin\theta|, \delta)d\theta + \int_{\phi}^{\pi-\phi} < P_{II} >_{T_s} (d = m|\sin\theta|, \delta)d\theta + \int_{\pi-\phi}^{\pi} < P_I >_{T_s} (d = m|\sin\theta|, \delta)d\theta\right)$$
$$= \frac{m}{24}\left[-3(4(1-4\delta)^2 + 3m^2)\sqrt{1 - \frac{(1-4\delta)^2}{m^2}} + m\left(m\cos\left(3\sin^{-1}\left(\frac{1-4\delta}{m}\right)\right) + 6\left(\pi - 2(1-4\delta)\sin^{-1}\left(\frac{1-4\delta}{m}\right) + (1-4\delta)\sin\left(2\sin^{-1}\left(\frac{1-4\delta}{m}\right)\right)\right)\right)\right] \quad (14)$$

$$< \tilde{i}_C >_T (m, \delta) = \frac{\sqrt{\pi}}{48\sqrt{10}}\left[m\left(12(8(-1+4\delta)^3(-9 + 8\delta(-3 + 10\delta)) + 2(1-4\delta)(413 + 8\delta(-109 + 130\delta))m^2 + (437 + 300\delta)m^4)\sqrt{1 - \frac{(1-4\delta)^2}{m^2}} + 4m\left(8m(80 + 64m^2 - 45m\pi + 120\delta^2(32 - 9m\pi)) - 45(8(1-4\delta)^2(5 + 8\delta(-1+2\delta)) - 4(-11 + 24\delta(1+2\delta))m^2 + 5m^4)\cos^{-1}\left(\frac{1-4\delta}{m}\right)\right)\right)\right]^{\frac{1}{2}} \quad (15)$$

$$< i_L >_T (m, \delta) = \frac{m}{24\pi}\left[-3(4(1-4\delta)^2 + 3m^2)\sqrt{1 - \frac{(1-4\delta)^2}{m^2}} + m\left(m\cos\left(3\sin^{-1}\left(\frac{1-4\delta}{m}\right)\right) + 6\left(\pi - 2(1-4\delta)\sin^{-1}\left(\frac{1-4\delta}{m}\right) + (1-4\delta)\sin\left(2\sin^{-1}\left(\frac{1-4\delta}{m}\right)\right)\right)\right)\right] \quad (16)$$

inductance L is computed as

$$0.255 = \frac{P}{\frac{V_{dc}^2}{2\pi f_s L}}$$
$$\implies L = \frac{0.255}{P} \times \frac{V_{dc}^2}{2\pi f_s} \quad (17)$$

The blocking voltage of the primary side devices is $2V_{pr}$ and that of the devices on the secondary side is V_{dc}. The inductor RMS current is computed as follows.

$$I_{2,RMS} = \frac{V_{dc}}{2\pi f_s L} < i_L >_T (m = 1, \delta = 0.09)$$
$$= \frac{V_{dc}}{2\pi f_s L}\frac{< P >_T}{UF} = V_{dc}\frac{P}{UF} = \frac{1.63P}{V_{dc}} \quad (18)$$

The primary side RMS current is given as follows.

$$I_{1,RMS} = n\frac{I_{2,RMS}}{\sqrt{2}} = \frac{V_{dc}}{V_{pr}}\frac{1.63P}{V_{dc}}\frac{1}{\sqrt{2}} = \frac{1.153P}{V_{pr}} \quad (19)$$

Now, a basic design method for designing the transformer is discussed. Fig. 9 shows a two winding transformer is presented and is used to estimate the flux in the three winding transformer used in the proposed topology. Voltage waveforms v_1 and v_2 as presented in Fig. 10(a) are $V_1 = V_{pr}\sin\theta$ and $V_2 = V_{dc}$. Assuming that the transformer shown in Fig. 9 is ideal, following equations hold. From Fig. 9, following equations are written.

$$v_1 = L_1\frac{di_1}{dt} + e_1$$
$$e_2 = L_2\frac{di_2}{dt} + v_2$$
$$e_2 = \frac{N_2}{N_1}e_1$$
$$I_1 = \frac{N_2}{N_1}I_2 \quad (20)$$

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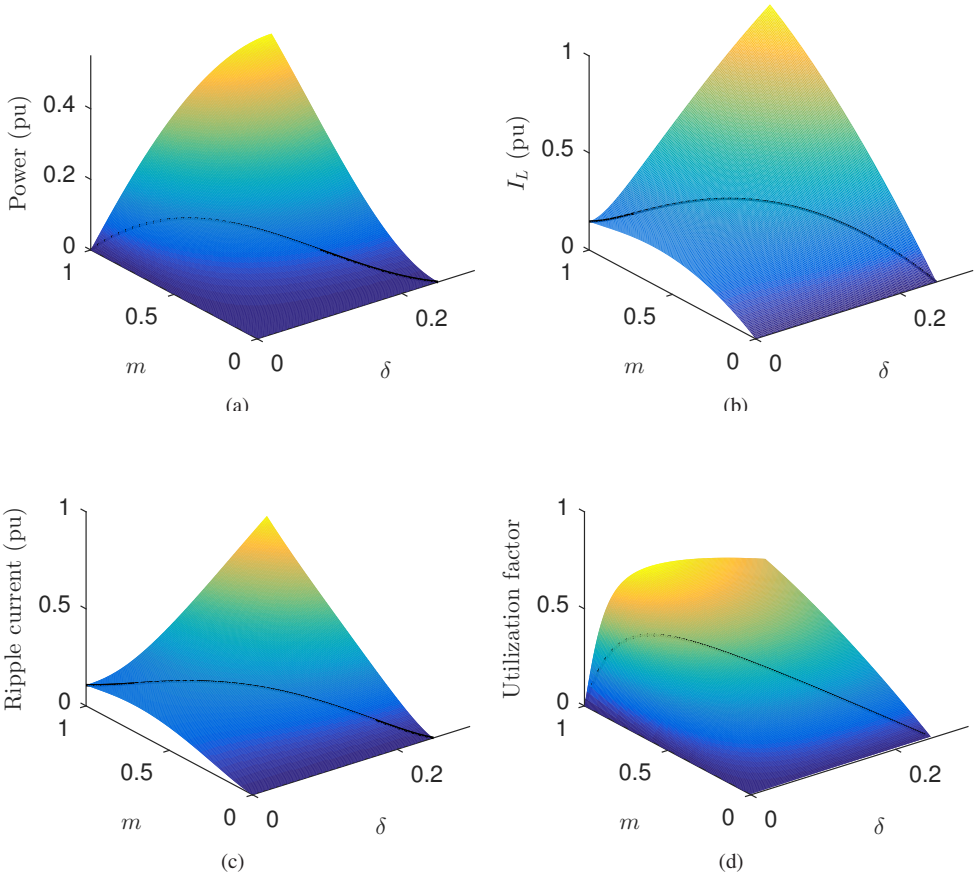

Fig. 7. Single phase PET characteristics for complete range of operation (black curves on plots indicate uniform mode boundary) (a) Average power vs δ and m (b) Transformer secondary RMS current vs δ and m (c) DC ripple current vs δ and m (d) Utilization factor vs δ and m

The equations can be solved to obtain e_1.

$$e_1 = \frac{1}{2}\left(v_1 + \frac{N_1}{N_2}v_2\right) + \left(\left(\frac{N_1}{N_2}\right)^2 L_2 - L_1\right)\frac{di_1}{dt} \tag{21}$$

If it is assumed that the series inductance L is equally distributed on the primary and secondary side, then $\left(\frac{N_1}{N_2}\right)^2 L_2 - L_1 = 0$. This gives

$$e_1 = \frac{1}{2}\left(v_1 + \frac{N_1}{N_2}v_2\right) = \left(\frac{v_1 + \frac{1}{n}v_2}{2}\right) \tag{22}$$

This waveform has been shown in the Fig. 10(a) and Fig. 10(b) for MODE I and MODE II respectively. The peak to peak flux variation is given as follows.

$$\begin{aligned}\Phi_{pk-pk_I} &= \frac{1}{N_1}\int_0^{t_3} e_1 dt = \frac{T_s}{2N_1}(V_1 + d\frac{N_1}{N_2}V_2) \\ &= \frac{T_s}{N_1}V_{pr}\sin\theta \end{aligned} \tag{23}$$

$$\begin{aligned}\Phi_{pk-pk_{II}} &= \frac{1}{N_1}\int_{t_1}^{t_4} e_1 dt = \frac{T_s}{2N_1}\left((2-d-4\delta)V_1 + d\frac{N_1}{N_2}V_2\right) \\ &= \frac{T_s}{2N_1}(3-d-4\delta)V_1 \\ &= \frac{T_s}{2N_1}\left(3 - m\sin\theta - 4\delta\right)V_{pr}\sin\theta \end{aligned} \tag{24}$$

The expression given in (23) maximizes when $\theta = \frac{\pi}{2}$, with a maximum value equal to $\frac{T_s}{N_1}V_{pr}$.

The expression in (24) has two maxima i.e. $\theta = \frac{\pi}{2}$ and $\theta = \sin^{-1}\left(\frac{3-4\delta}{2m}\right)$. It should however be noted, that the quantity $\left(\frac{3-4\delta}{2m}\right) \geq 1$ for $m\epsilon[0,1]$ and $\delta\epsilon[0,0.25]$. Thus, this second maximum is a valid solution only when $\delta = 0.25$ and $m = 1$ and then, it equals the first maximum of $\theta = \frac{\pi}{2}$. Thus, the expression in (24) is going to be maximum at $\theta = \frac{\pi}{2}$, with a maximum value of $\frac{T_s}{2N_1}\left(3 - m - 4\delta\right)V_{pr}$. For a design range of $m = 1$ and $\delta\epsilon[0, 0.09]$, the maximum value occurs at $\delta = 0$ and is equal to $\frac{T_s}{N_1}V_{pr}$. Therefore, the maximum peak-peak flux is given as follows.

$$\Phi_{pk-pk,max} = \frac{T_s}{N_1}V_{pr} \tag{25}$$

The peak flux density B_{max} is related to the peak-peak flux through the transformer core area A_c.

$$A_c B_{max} = \frac{1}{2}\Phi_{pk-pk,max} \tag{26}$$

The window area A_w, along with the window fill factor K_w is related to the primary and secondary currents through the current density J. This is shown in equation (27) for the three

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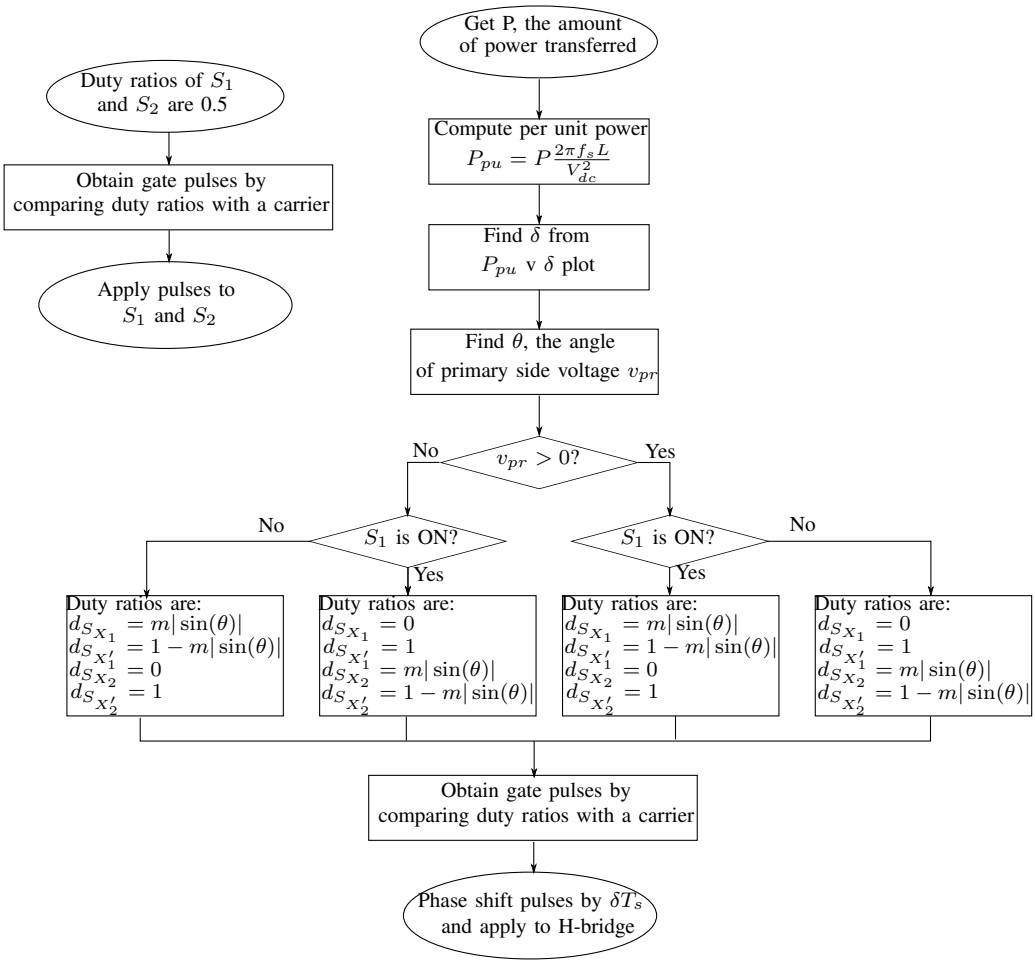

Fig. 8. Flowchart of proposed modulation technique

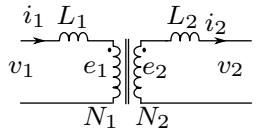

Fig. 9. Transformer circuit

winding transformer.

$$A_w K_w = 2\frac{N_1 I_{1,RMS}}{J} + \frac{N_2 I_{2,RMS}}{J} = (1+\sqrt{2})\frac{N_2 I_{2,RMS}}{J} \tag{27}$$

Using (18) and (25)-(27), the product of core and window areas is then computed as follows.

$$A_c A_w = \frac{1}{2}\frac{\Phi_{pk-pk,max}}{B_{max}} \times \frac{1}{K_w}(1+\sqrt{2})\frac{N_2 I_{2,RMS}}{J}$$
$$\implies A_c A_w = \frac{1.968P}{B_{max} K_w J f_s} \tag{28}$$

The core area product allows the selection of a core for the transformer. Also, the RMS currents $I_{1,RMS}$ and $I_{2,RMS}$, determined earlier, is used to select the transformer windings.

Based on the design procedure defined above, for same specifications of P, V_{pr}, V_{dc} and f_s, the RMS currents and the transformer core area product is obtained for the solution proposed in [2]. Note in this case, maximum utilization happens $m = 0.78$ and $\delta = 0.055$, with a UF of 0.399. The proposed strategy results in significant reduction in the RMS of the winding currents. Table II presents a comparison between the solution proposed in [2] with the control method proposed in this paper, both for full bridge and push-pull structures for the AC side converter. Note that [2] uses a full birdge structure. In comparison with [2], there is a significant reduction in the area product for the full bridge implementation. The area product remains similar in case of the push-pull topology due to the inclusion of an additional winding on the transformer primary side.

It should be noted that in actual implementation, the transformer core may saturate due to multiple reasons which include device drops, mismatched gate pulses etc. Following methods can be used to avoid core saturation.

1) An air gap can be introduced in the transformer core to reduce the peak flux density, after taking into account the maximum flux that can occur in the given operating range. This ensures that there is enough margin in flux density, to prevent core saturation [46].
2) A capacitor can be placed in series in the winding, to block the dc voltage [47].
3) Actively nullify the dc component of the flux using a

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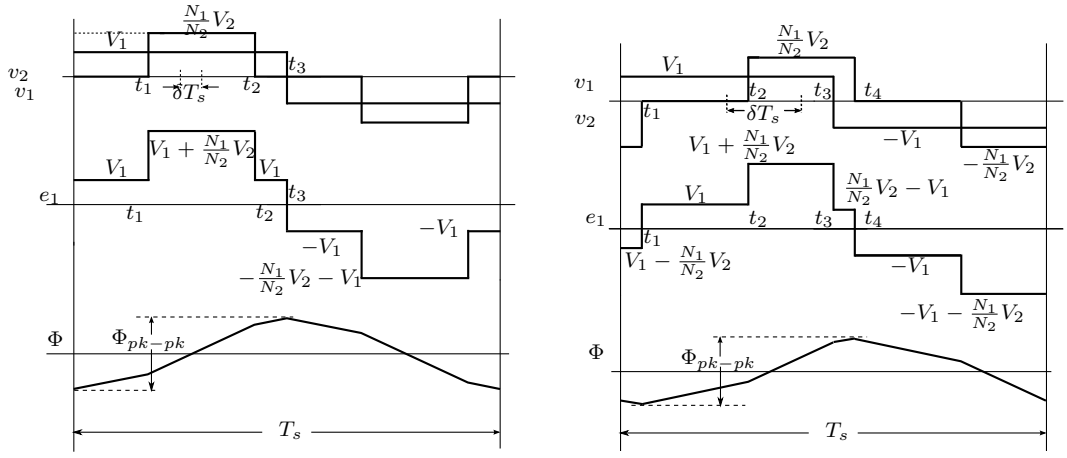

Fig. 10. Transformer voltages and flux (a) MODE I (b) MODE II

TABLE II
TRANSFORMER SIZE AND RMS CURRENT COMPARISON WITH [2]

	[2]	Proposed control method	
		Push-pull	Full bridge
$I_{1,RMS}$	$\frac{1.955P}{V_{pr}}$	$\frac{1.153P}{V_{pr}}$	$\frac{1.630P}{V_{pr}}$
$I_{2,RMS}$	$\frac{2.506P}{V_{dc}}$	$\frac{1.630P}{V_{dc}}$	$\frac{1.630P}{V_{dc}}$
A_cA_w	$\frac{1.955P}{B_{max}K_wJf_s}$	$\frac{1.968P}{B_{max}K_wJf_s}$	$\frac{1.630P}{B_{max}K_wJf_s}$

controller [48], [49].

Also, if the device is a MOSFET, as current increases, the temperature will rise leading to increasing $R_{ds,on}$ and eventually correcting for the transformer current.

Another practical consideration to take care of is voltage clamping on the primary side. In MODE II, the inductor current i_L has a non-zero value nI_3 when primary side switches S_1 and S_2 switch. The primary current jumps from nI_3 to $-nI_3$ instantly, when the primary side switches S_1 and S_2 undergo a switching transition. In a practical transformer however, due to leakage inductance L_{p1} and L_{p2} in the two primary windings of the transformer, transfer of current from one winding to the other requires a clamp circuit consisting of a capacitor and four diodes, as shown in Fig. 11(a). Consider a state when S_1 is ON and primary side current is positive, say I, as shown in Fig. 11(a).Hence, $i_{pr} = I$, $I_{p1} = I$ and $I_{p2} = 0$. Now, if S_1 is switched OFF (S_2 is still OFF), the current in L_{p1} starts to decay and that in L_{p2} starts to rise. This process ends when $i_{pr} = 0$, $i_{p1} = \frac{I}{2}$ and $i_{p2} = -\frac{I}{2}$, as shown in Fig. 11(b). Now after a dead time, when S_2 is turned ON, current through L_{p1} decays to zero and currents i_{pr} and i_{p2} both become equal to $-I$. Then the clamp is no longer in conduction, as shown in Fig. 11(c). In Fig. 12, the change in i_{pr} and the switching signals for S_1 and S_2 are displayed.

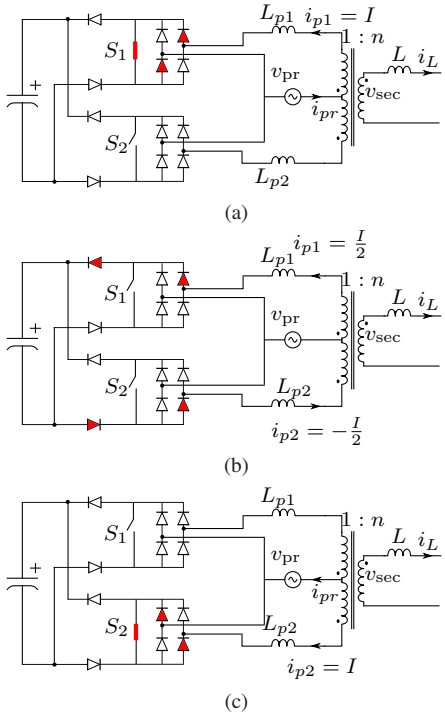

Fig. 11. Primary side commutation from S_1 to S_2 (a)S_1 ON (b) Clamp conducting (c) S_2 ON

The shaded area in the q_{S_1} and q_{S_2} denotes the dead time between the switches. The dead time between S_1 and S_2 in the experimental implementation for this paper is $1\mu s$.

VI. SOFT SWITCHING

The switches in the secondary side H-bridge, S_{X_1} and S'_{X_1}, are turned on to apply a positive voltage pulse, $v_{X_1X_2} = V_{dc}$. Switches S_{X_2} and S'_{X_2}, are turned on to apply negative voltage pulse, $v_{X_1X_2} = -V_{dc}$. The zero voltage is applied by turning on the two bottom switches, S'_{X_1} and S'_{X_2}, simultaneously. It has been shown in [1], that in MODE I, the switches in the ac side converter are soft switched with zero current (ZCS). The switches in the secondary side bridge, are soft switched with

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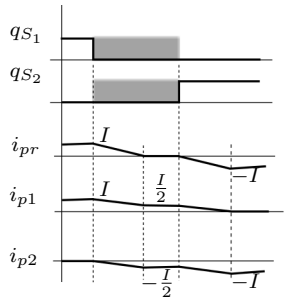

Fig. 12. Waveforms for clamp commutation

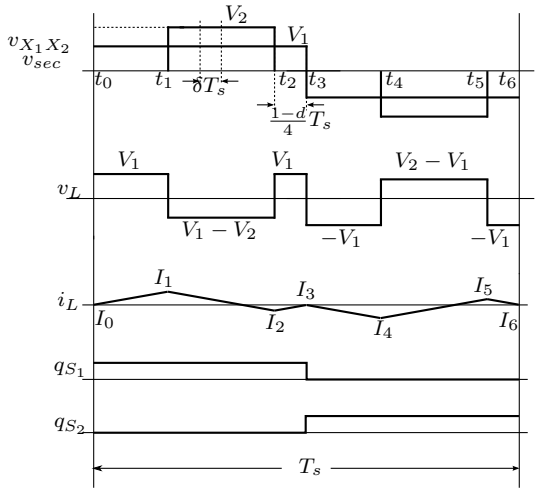

Fig. 13. Voltage and current waveforms in MODE I for positive δ

zero voltage (ZVS), considering the presence of capacitances across the terminals of the switch (drain source for MOSFET and collector emitter for IGBT).

A brief discussion of ZCS or zero current switching of the AC side switches S_1 and S_2 is being given here. More details can be found in [1] and [2]. Fig. 13 shows the relevant waveforms when δ is positive and the converter is operating in MODE I. The duration of the $v_{X_1X_2}$ pulse is $\frac{dT_s}{2} = \frac{V_1}{V_2}\frac{T_s}{2}$ and in MODE I, the entire pulse is contained within the half switching period, as shown in Fig. 13. This implies that the average of the inductor voltage is zero over the half switching cycle, i.e. $\int_0^{\frac{T_s}{2}} v_L dt = 0$. This means that if the inductor current starts at zero at $t = t_0$, then it will be zero again at the end of the half cycle i.e., $t = t_3 = \frac{T_s}{2}$. Hence, the primary winding current is zero, when the primary side switches are switching, resulting in ZCS for these two devices.

Let us first consider the case when $\delta > 0$ and the converter is operating in MODE II. The switches in each leg (S_{X_1}, $S_{X_1'}$ and S_{X_2}, $S_{X_2'}$) of the DC side H-bridge are switched in a complimentary fashion, with a dead time, shown with the shaded areas in Fig. 5. Let us consider the transition in secondary side converter at time instant t_1 in Fig. 5. Prior to instant t_1, switches $S_{X_1'}$ and S_{X_2} are ON. The current i_L is positive and both of these switches are conducting, as shown in Fig. 15(a). As a first step at time instant t_1, switch S_{X_2} is

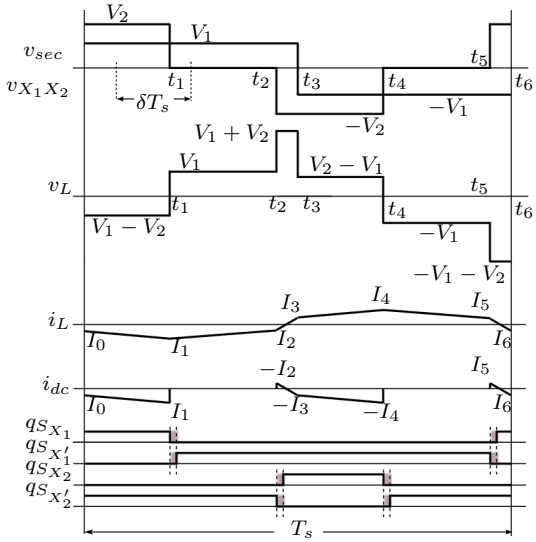

Fig. 14. MODE II operation for negative δ

turned OFF. Since both S_{X_2} and $S_{X_2'}$ are in the OFF state, the leg current flows through the capacitors C_{X_2} and $C_{X_2'}$. Initially at t_1, capacitor C_{X_2} is at zero voltage since S_{X_2} was conducting prior to t_1, while the voltage across $C_{X_2'}$ is V_{dc}. The inductor current discharges the capacitor $C_{X_2'}$ and charges the capacitor C_{X_2}, as seen in Fig. 15(c). Since it takes some time to charge the capacitor C_{X_2}, the turning OFF of S_{X_2} happens practically at zero voltage (ZVS). This process ends when C_{X_2} is charged to V_{dc} and $C_{X_2'}$ is discharged to zero and then the anti-parallel diode of $S_{X_2'}$ gets forward biased and starts conducting, as shown in Fig. 15(c). If $S_{X_2'}$ is turned ON after voltage across $C_{X_2'}$ reaches zero, then the turn ON of $S_{X_2'}$ also happens with ZVS. The time to discharge $C_{X_2'}$ from V_{dc} to zero depends on the magnitude of current I_1 and it takes longer if I_1 is less. If I_1 is so small that the discharge time of $C_{X_2'}$ is longer than the dead time, then turn ON of $S_{X_2'}$ may not happen with ZVS. Thus, the soft switching of S_{X_2} and $S_{X_2'}$ at time instant t_1 happens if $i_L = I_1$ is positive, but it also depends on its magnitude even when the current is positive. Fig. 16(a) shows the value of I_1 in per unit for various value of $0 < \delta \leq 0.09$ for $m = 1$, which is the operating point about which the system would typically be designed.

It is possible to show that at time instant t_2, both the turning OFF of $S_{X_1'}$ and turning ON of S_{X_1} with a dead time are ZVS if the current I_2 in Fig. 5 is positive. Plots of I_2 as a function of θ for $m = 1$ and $0 < \delta \leq 0.09$ are shown in Fig. 16(b).

Similarly, it is possible to show that switching of the secondary side H-bridge is lossless at time instants t_4 and t_5 if I_4 and I_5 are negative. Due to symmetry, $I_4 = -I_1$ and $I_5 = -I_2$. Thus, soft switching conditions at time instants t_1 and t_2 also guarantee soft switching at instants t_4 and t_5.

Fig. 14 shows the relevant waveforms when the converter is operating in MODE II with a negative δ. By doing analysis similar to that done for positive δ above, it can be shown that soft switching happens when $I_1 = -I_4$ and $I_2 = -I_5$ are negative. Fig. 17(a) and Fig. 17(b) show the per unit values of I_1 and I_2 vs θ at $m = 1$, for various negative values of δ.

The zero voltage switching (ZVS) of the secondary side

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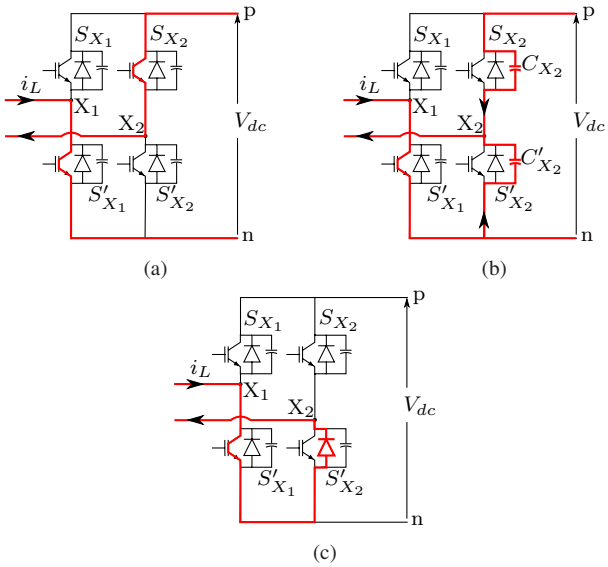

Fig. 15. Circuit diagrams to illustrate ZVS (a) $S_{X_1'}$ and S_{X_2} conducting (b) S_{X_2} and $S_{X_2'}$ capacitor charge discharge (c) $S_{X_1'}$ and anti-parallel diode of $S_{X_2'}$ conducting

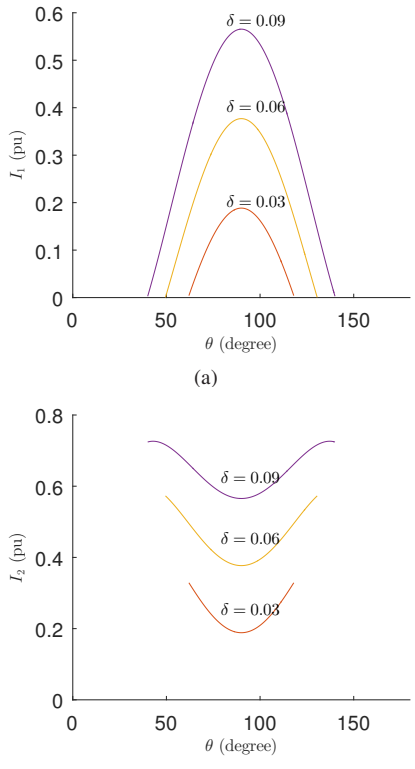

Fig. 16. Inductor current vs θ plots for $m = 1$ (a) I_1 for positive δ (refer Fig. 5) (b) I_2 for positive δ (refer Fig. 5)

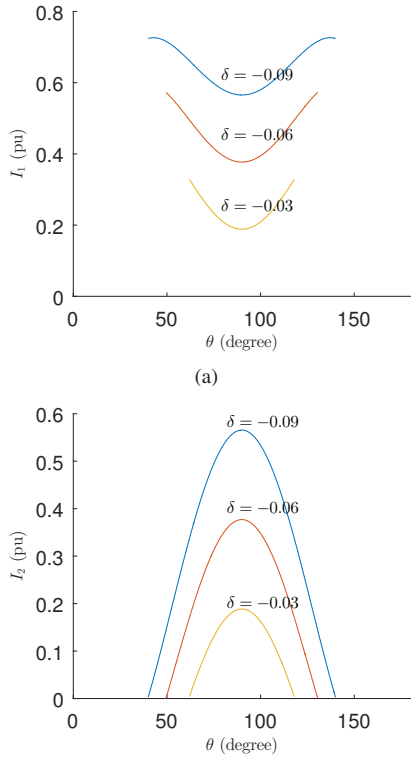

Fig. 17. Inductor current vs θ plots for $m = 1$ (a) I_1 for negative δ (refer Fig. 14) (b) I_2 for positive δ (refer Fig. 14)

converter is conditional on the relative amplitude of the inductor current at the time of switching. Depending on the value of the device capacitances, the DC bus voltage V_{dc} and device turn OFF time, soft switching may not happen below certain magnitude of the current.

VII. Harmonic Compensation

The input current drawn from the AC source is periodic over one half of a switching period T_s, as shown in Fig. 5. The average of the input current over one half of the switching cycle is given in (29), where $0 < \theta \leq \pi$.

$$< i_{in_I} >_{T_s} = \frac{\delta T_s V_{dc}}{L} m \sin\theta \quad \text{(MODE I)}$$
$$< i_{in_II} >_{T_s} = -\frac{T_s V_{dc}}{8L}[(1-4\delta)^2 + m\sin\theta(-2 + m\sin\theta)] \quad \text{(MODE II)} \tag{29}$$

For θ varying between π to 2π, the current waveform attains same average value but is opposite in sign. It is clear from equation (29), that in MODE I, the average current is sinusoidal, whereas in MODE II, the waveform deviates from sinusoidal shape. In uniform mode operation, where PET operates only in MODE I, the average current is sinusoidal and in phase with the input AC voltage. For operation in mixed mode, the average current deviates from the sinusoidal shape as it enters MODE II. This means that low order harmonics are present in the average input current, although the fundamental component of the current is in phase with the voltage, thus having unity displacement power factor (DPF). This implies that

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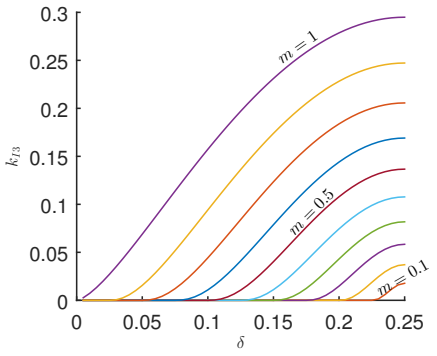

Fig. 18. Third harmonic factor k_{I3} plots

both in MODE I and MODE II, the fundamental component of the current is in phase with the voltage, as long as the duty cycle is chosen as in (3), i.e. $d = m|sin(\theta)|$. It is possible to show if d is set as $m|\sin(\theta+\psi)|$, then the displacement power factor (DPF) becomes $\cos\psi$, which may become important in case of VAR support and low voltage ride through (LVRT). In mixed mode, the amplitude of the third harmonic component of the input current is found by doing Fourier analysis, given in (30).

$$I_{3h} = \frac{m^2 T_s V_{dc}}{15L\pi}\left(1 - \left(\frac{1-4\delta}{m}\right)^2\right)^{\frac{5}{2}} \tag{30}$$

Other harmonic coefficients can also be obtained in a similar fashion. Harmonic factor k_{I3} has been defined as the ratio of third harmonic component to the fundamental component $k_{I3} = \dfrac{I_{3h}}{I_{1h}}$. This factor has been plotted for various values of δ and m in Fig. 18. In order to reduce this third harmonic current component, a third harmonic component is injected in the modulation signal of the secondary side H-bridge, as seen in the equation below.

$$MI_{\text{comp},3} = m\sin\theta + k_3 m\sin(3\theta) \tag{31}$$

It is however observed that upon introducing this third harmonic component in the modulation signal, a fifth harmonic component starts to show up in the current. To suppress the fifth harmonic in current, a fifth harmonic component is introduced in the modulation signal of the secondary side H-bridge. The modulation signal then takes the following form.

$$MI_{\text{comp},3,5} = m\sin\theta + k_3 m\sin 3\theta + k_5 m\sin 5\theta \tag{32}$$

The optimum values of k_3 and k_5 at various values of m and δ for reducing current harmonics were estimated from multiple simulations of the system. These values of $k_3 m$ and $k_5 m$ have been plotted in Fig. 19. It is observed from these graphs that the compensation is needed only for the mixed mode operation, since the values of k_3 and k_5 are zero in uniform mode of operation. In addition, the plots in Fig. 19(a) appear similar to those in Fig. 18 although opposite in sign, which indicates that there is a relation between the harmonic current amplitude and the compensation voltage to suppress the harmonic.

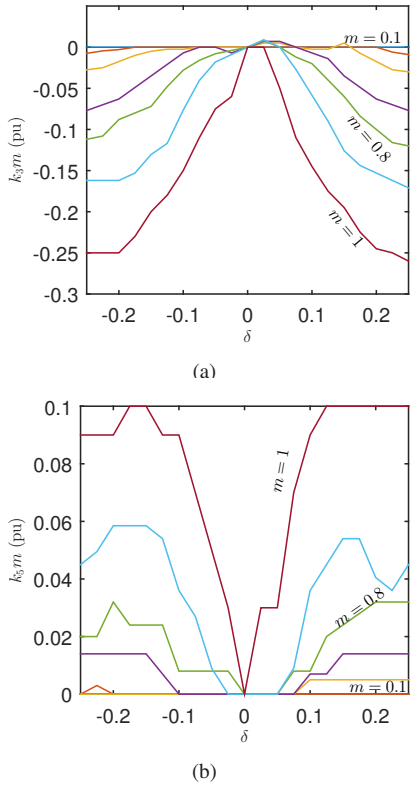

Fig. 19. Harmonic compensation coefficients (multiplied by the modulation index) plots (a) $k_3 m$ (b) $k_5 m$

VIII. Simulation and Experimental Results

The single phase PET with proposed modulation technique is simulated using MATLAB Simulink and PLECS blockset to study its operation. In addition, a laboratory hardware prototype was also built to experimentally verify the analysis and operation. The parameters of the setup are given in Table III. A picture of the lab prototype of the proposed topology is given in Fig. 20. The primary side switches S_1 and S_2 are Ixys IXGH30N120B3D1 IGBTs and the diodes are CREE C4D10120A. The secondary side inverter uses a Microsemi APTGF50TA120PG module. The gate drivers on the primary side are Concept 2SD106AI and those on the secondary side are Concept 6SD106EI. The nominal power is 100W. The dSPACE DS1103 controller is used to issue the duty ratio and δ commands to a Xilinx Spartan 3 XC3S500E FPGA, which then generates appropriate gate pulses for the primary side and secondary side switches.

Simulation results for power flow through the PET from AC to DC side (positive δ) are given in Fig. 21. These waveforms are taken for $m = 0.9$ and $\delta = 0.225$ ($m > 1 - 4\delta$, mixed mode of operation). It is immediately observed that the filtered (average) input current is nearly in phase (some phase difference present due to filter) with the AC voltage, demonstrating unity power factor operation. The current waveforms in Fig. 21(a) are without any harmonic compensation. Upon applying harmonic compensation, the current waveforms obtained are shown in Fig. 21(b), in which the AC current appears more sinusoidal in nature compared to that without compensation. To further illustrate this, frequency spectra of average input

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TABLE III
CIRCUIT PARAMETERS FOR SINGLE PHASE PET SIMULATION AND EXPERIMENTS

Parameter	Value
DC link voltage (V_{dc})	80V
Modulation index (m)	0.5, 0.7, 0.8, 0.9
AC voltage frequency (f)	60 Hz
Switching frequency (f_s)	5 kHz
δ	[-0.25,0.25] (steps of 0.05)
Transformer turns ratio (n)	1:1
Secondary side inductance (L)	480 μH
DC side capacitor (C_{dc})	1.3mF
Filter capacitor (C_{fltr})	20μF
Filter inductor (L_{fltr})	820μH

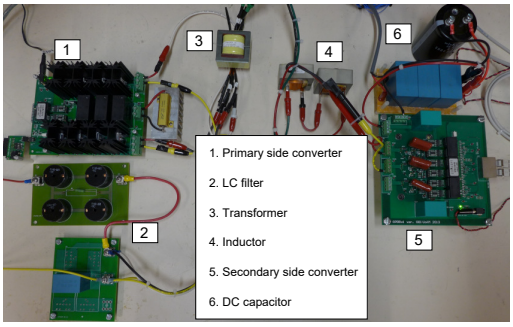

Fig. 20. Experimental setup

current with and without harmonic compensation are shown in Fig. 21(c), where the third harmonic is not present in AC current when compensation is used. It is also seen that the fundamental component of the current reduces, which is indicative of the lower power transfer for the same value of δ and m. Fig. 22 shows similar waveforms for DC to AC power flow.

The experimental results for AC and DC currents with the same settings ($m = 0.9$, $\delta = 0.225$) are shown in Fig. 23, for power flow from AC to DC side. The experimental results are similar to the simulation results with regards to unity power factor operation and AC current harmonic content reduction due to harmonic compensation. It should be noted that due to leakage energy commutation losses on the primary side of the transformer, device drops and winding resistances, the current in experimental results does not match exactly the magnitude of that in simulation results. Finally, the experimental results for AC and DC currents for power flow from DC to AC side are shown in Fig. 24. The results demonstrate unity power factor operation and also show harmonic content reduction when harmonic compensation is used. The THD of AC current for the results discussed in Fig. 21-Fig. 24 are given in table IV. Also, the efficiency of the experimental prototype is given in table V at an AC voltage of 51.6V RMS and DC voltage of 80 V with various values of power transfer.

In order to demonstrate that the power flow analysis in section IV translates to the actual system, simulations and experiments were performed for the single phase PET at several values of m and δ, as given in table III. The plots are

TABLE IV
INPUT CURRENT THD ($m = 0.9$, $|\delta| = 0.225$)

	$\delta > 0$		$\delta < 0$	
Harmonic compensation	No	Yes	No	Yes
Simulation THD	10.36	4.21	10.78	4.52
Experimental THD	10.28	4.58	11.41	6.79

given in Fig. 25, with each plot showing analytical, simulated and experimental results for one value of modulation index m for various values of δ. It is observed that the various curves in each figure show a similar trend, which shows that the analytical expressions translate to actual system within some margin of error. There are a few differences to be noted however. The first difference is that the simulation values themselves do not exactly match the analytical values at higher values of δ, which is accredited to the harmonic compensation. Then, the AC and DC power values obtained through experiments do not match each other and the simulation results exactly, due to system losses caused by non-idealities such as device drops, leakage commutation on primary side of transformer and winding losses. It should be noted that for positive values of δ, where power is transferred from AC to DC side, the AC power input is more than the DC power output (barring for very low values of δ where power transfer is not measurable accurately). The reverse is true for negative values of δ.

In Fig. 26(a), experimental waveforms of primary side voltage v_{pr}, H-bridge voltage $v_{X_1X_2}$ and inductor current i_L are shown for line frequency period. The converter is operated at $m = 0.9$, $\delta = 0.225$. Fig. 26(b) shows a zoom of the waveforms at an angle $\theta \approx 44°$ (around the shaded area in Fig. 26(a)), when the converter is operating in MODE II, since $\phi < \theta \leq \pi - \phi$, where $\phi = \sin^{-1}\left(\frac{1-4\delta}{m}\right) = 6.4°$. Fig. 26(b) also shows the gate emitter voltages of switches S_{X_2} and $S_{X_2'}$. A similarity can be observed between these experimental waveforms and the theoretical waveforms given in Fig. 5. In Fig. 26(b), $I_1 = 3A > 0$, when S_{X_2} is turned OFF and $S_{X_2'}$ is turned ON after a dead time, confirming soft switching of S_{X_2} and $S_{X_2'}$ at this instant. From Fig. 26(b), it has been experimentally observed that $I_1 = 3A > 0$, $I_2 = 7A > 0$, $I_4 = -3A < 0$ and $I_5 = -7A < 0$. As discussed in section VI, this confirms soft switching of the DC side H-bridge in MODE II for positive δ. Similar waveforms can be obtained for negative δ.

In order to demonstrate ZCS in primary side switches, the Fig. 27(a) and Fig. 27(b) give transformer secondary voltage v_{sec} and inductor current i_L over a line frequency and switching frequency period respectively. The operating condition is $m = 0.9$ and $\delta = 0.1$. The shaded area in Fig. 27(a) is $\theta \approx 20.3°$, where the converter is operating in MODE I. This is where Fig. 27(b) zooms in. Fig. 27(b) also shows the gate emitter voltage waveforms for switches S_1 and S_2. It is observed that the current I_3 is nearly zero (some error due to device drop), where the transition between S_1 and S_2 happens, confirming ZCS in MODE I. Similar waveforms can be obtained for negative δ as well for showing ZCS in MODE

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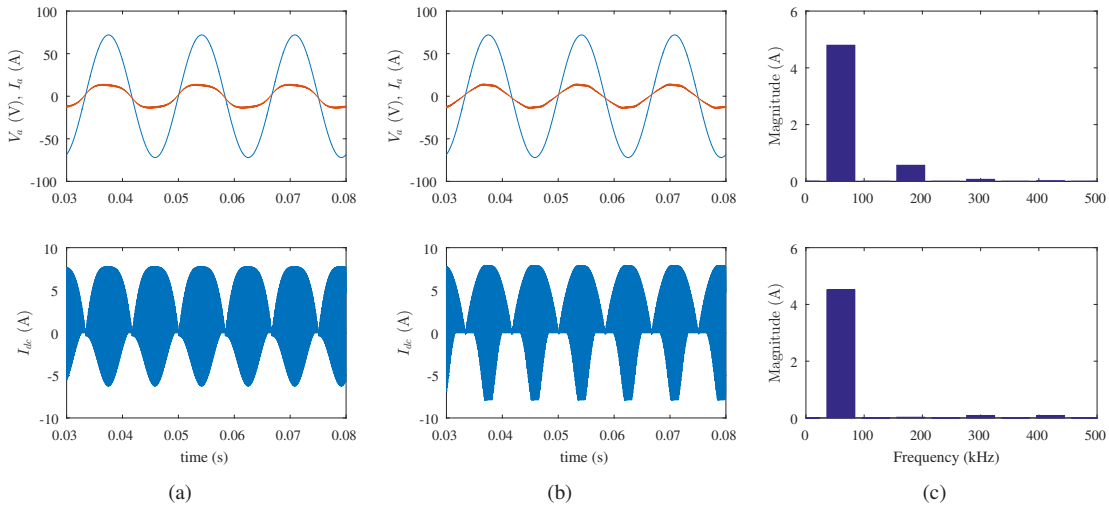

Fig. 21. Simulation results for power flow from AC to DC side, for single phase PET (a) Without harmonic compensation (AC voltage and filtered AC current(zoomed by factor of 3) (top), DC link current(bottom)) (b) With harmonic compensation (AC voltage and filtered AC current(zoomed by factor of 3) (top), DC link current(bottom)) (c) AC current Frequency spectra, without compensation (top) and with compensation (bottom)

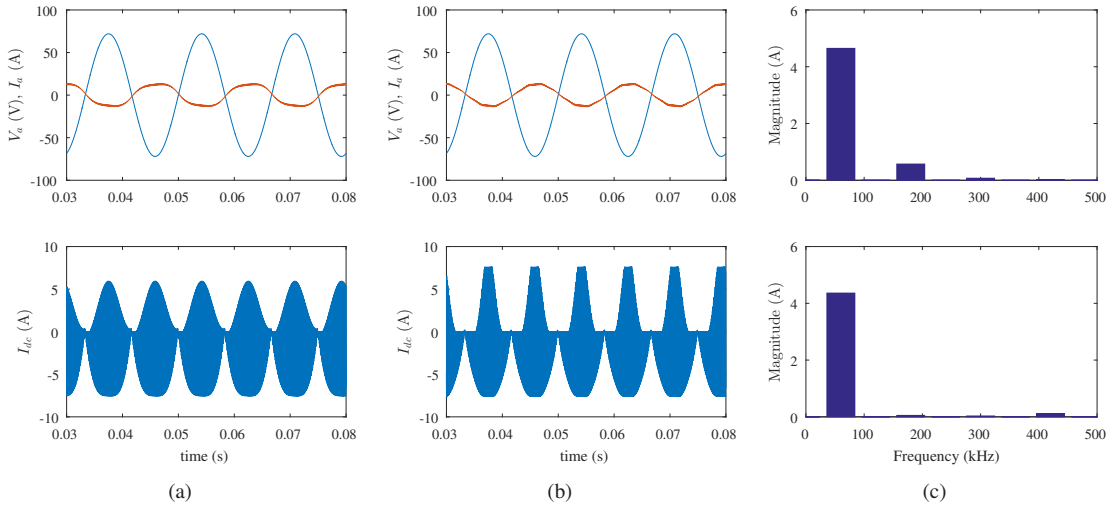

Fig. 22. Simulation results for power flow from DC to AC side, for single phase PET (a) Without harmonic compensation (AC voltage and filtered AC current(zoomed by factor of 3) (top), DC link current(bottom)) (b) With harmonic compensation (AC voltage and filtered AC current(zoomed by factor of 3) (top), DC link current(bottom)) (c) AC current Frequency spectra, without compensation (top) and with compensation (bottom)

TABLE V
EXPERIMENTAL EFFICIENCY

AC Power (W)	174	156	124	80	-59	-104	-125
Efficiency (%)	79.1	83.3	84	86	88	85.6	79.2

I.

IX. CONCLUSION

In this paper, a novel power electronic transformer topology was analyzed in accordance with proposed modulation scheme for bidirectional power conversion between single phase AC and DC power sources. The transferred active power, RMS of the current though the inductor, ripple current through the DC link capacitor and the utilization factor were analytically determined. The analysis for soft switching shows lossless switching of the DC side converter for all operating conditions.

The proposed scheme results in excellent utilization factor along with open loop power factor correction. Additionally, a compensation technique has been proposed that significantly reduces low frequency third harmonic in the AC current. Using simulation and experimental results, the analytical power transfer curves, harmonic compensation and soft switching were validated within limits of experimental error.

APPENDIX

The expressions for the proposed PET system in the uniform mode of operation (where only MODE I occurs) are given

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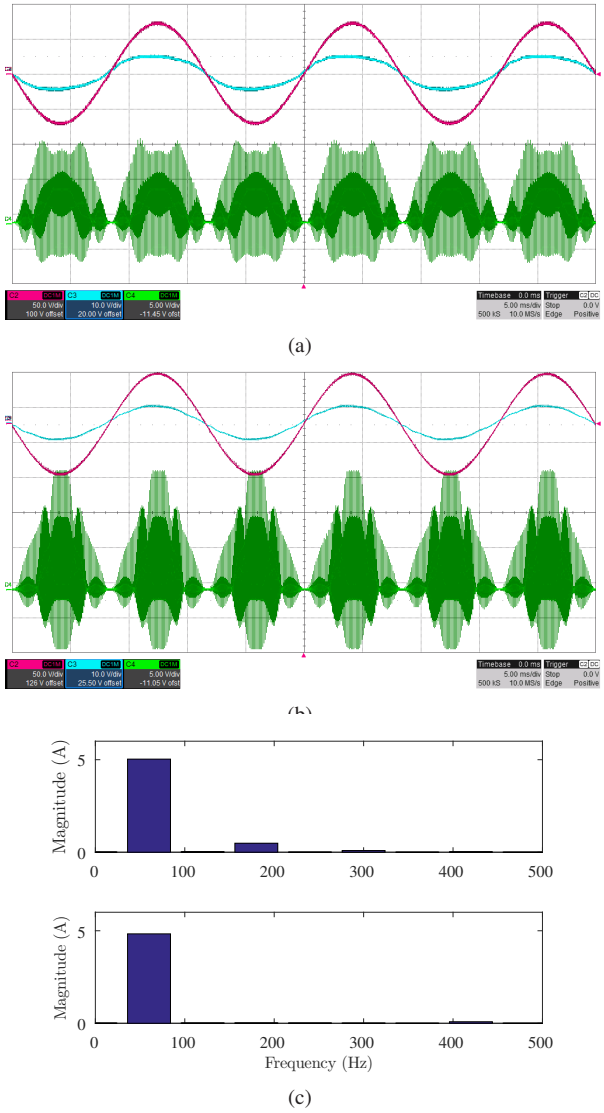

Fig. 23. Experimental results for power flow from AC to DC side, for single phase PET (a) Without harmonic compensation: AC voltage and filtered AC current (top) [50 V/div, 10 A/div], DC link current(bottom) [5 A/div] (b) With harmonic compensation: AC voltage and filtered AC current (top) [50 V/div, 10 A/div], DC link current(bottom) [5 A/div] (c) AC current Frequency spectra, without compensation (top) and with compensation (bottom)

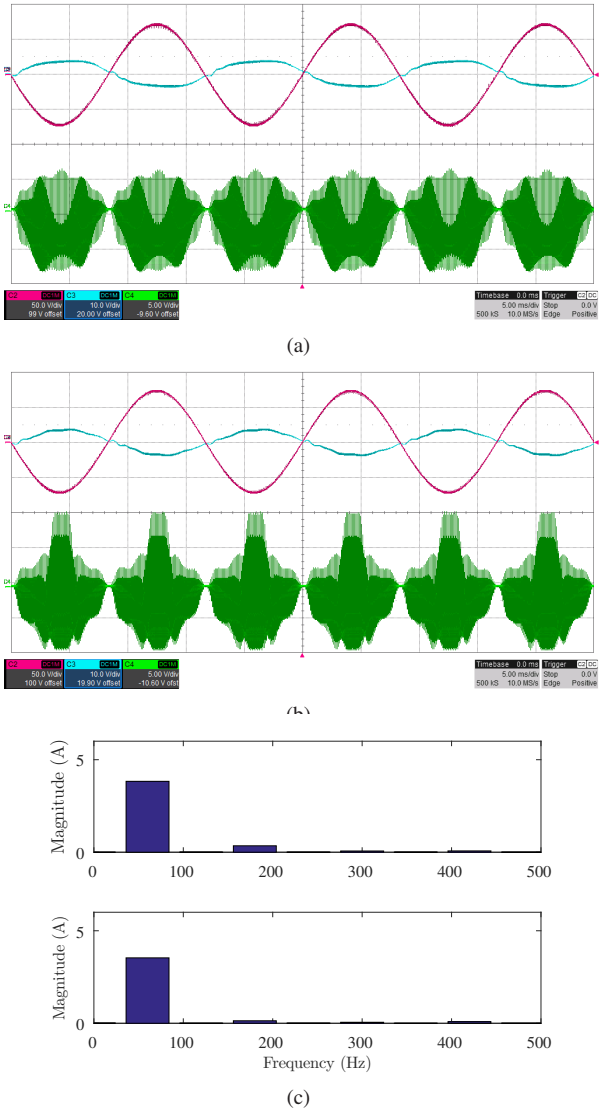

Fig. 24. Experimental results for power flow from DC to AC side, for single phase PET (a) Without harmonic compensation: AC voltage and filtered AC current (top) [50 V/div, 10 A/div], DC link current(bottom) [5 A/div] (b) With harmonic compensation: AC voltage and filtered AC current(top) [50 V/div, 10 A/div], DC link current(bottom) [5 A/div] (c) AC current Frequency spectra, without compensation (top) and with compensation (bottom)

in this appendix. The expression for per unit average power transfer over a fundamental cycle in the uniform mode is given below.

$$< P >_T (m, \delta) = m^2 \delta \pi \quad \text{(Uniform mode)} \qquad (33)$$

The expression for pu RMS ripple current through the DC link capacitor in the uniform mode of operation is given below.

$$< \tilde{i}_C >_T (m, \delta) = \frac{\sqrt{\pi}}{12\sqrt{5}} [m^3(80 + 64m^2 - 45m\pi - 120\delta^2(-32 + 9m\pi))]^{\frac{1}{2}} \quad \text{(Uniform mode)} \qquad (34)$$

The expression for pu RMS current through the inductor L in uniform mode of operation is given below.

$$< i_L >_T (m, \delta) = \frac{m\sqrt{\pi}}{12\sqrt{2}} \sqrt{-64m + 9m^2\pi + 12(\pi + 48\delta^2\pi)} \quad \text{(Uniform mode)} \qquad (35)$$

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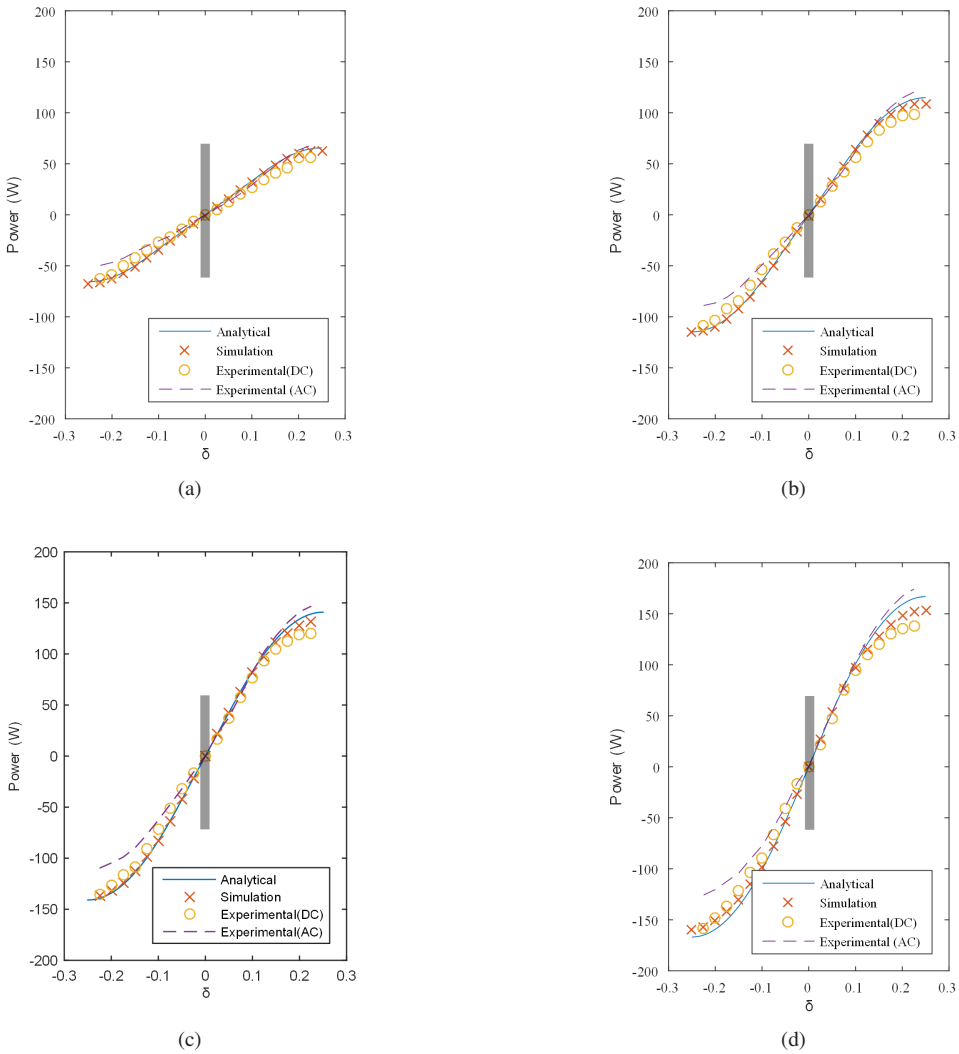

Fig. 25. Comparison of analytical, simulation and experimental results for power transfer in single phase PET. Shaded region represents dead zone for power transfer due to losses and dead time (a) $m = 0.5$ (b) $m = 0.7$ (c) $m = 0.8$ (d) $m = 0.9$

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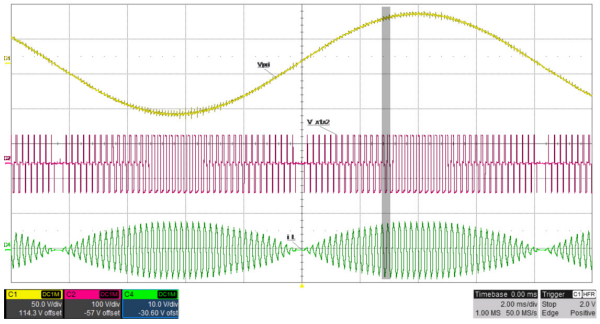
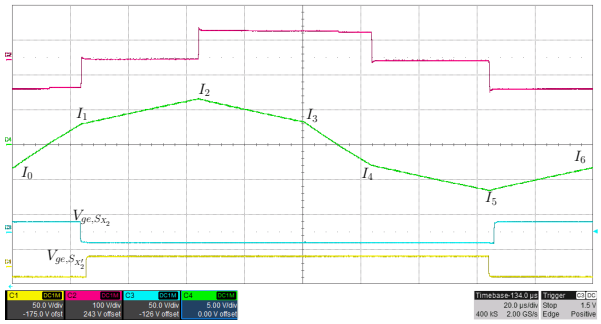
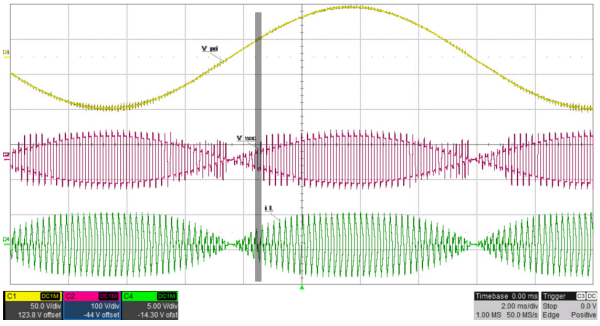


(a)

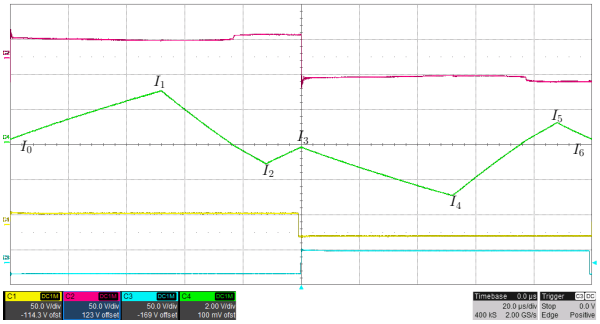


(b)

Fig. 26. Experimental results to demonstrate ZVS (a) Primary side voltage v_{pr}, H-bridge voltage $V_{X_1X_2}$ and inductor current i_L (b) H-bridge voltage $V_{X_1X_2}$, inductor current i_L, gate emitter voltages of S_{X_2} and $S_{X_2'}$



(a)



(b)

Fig. 27. Experimental results to demonstrate ZCS (a) Primary side voltage v_{pr}, secondary voltage V_{sec} and inductor current i_L (b) Secondary voltage V_{sec}, inductor current i_L, gate emitter voltages of S_1 and S_2

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