


A Unidirectional Single-Stage Three-Phase Soft-Switched Isolated DC–AC Converter

Anirban Pal , *Student Member, IEEE*, and Kaushik Basu, *Senior Member, IEEE*

Abstract—This paper presents a novel single-stage soft-switched high-frequency-link three-phase dc–ac converter topology. The topology supports unidirectional dc to ac power flow and is targeted for applications like grid integration of photovoltaic sources, fuel cell, etc. The high frequency magnetic isolation results in reduction of system volume, weight, and cost. Sine-wave pulswidth modulation is implemented in dc-side converter. Though high-frequency switched, dc-side converter is soft switched for most part of the line cycle. The ac-side converter active switches are line frequency switched incurring negligible switching loss. The line frequency switching of ac-side converter facilitates use of high voltage blocking inherently slow semiconductor devices to generate high voltage ac output. In addition, a cascaded multilevel structure is presented in this paper for direct medium-voltage ac grid integration. A detailed circuit analysis considering nonidealities like transformer leakage and switch capacitances, is presented in this paper. A 6-kW three-phase laboratory prototype is built. The presented simulation and experimental results verify the operation of the proposed topologies.

Index Terms—Cascaded multilevel inverter, dc–ac converter, high-frequency transformer (HFT), pulswidth modulation (PWM), rectifier-type HFL, single stage, zero-voltage switching (ZVS).

I. INTRODUCTION

DEPLETION of conventional fossil-fuel-based resources and present global warming scenario are providing fresh impetus to power generation from renewable energy sources. Research on grid integration of renewable energy sources like solar and fuel cell are gaining attention in both academia and industry [1]–[6]. The grid integration of photovoltaic system using nonisolated converter topologies have problems associated with high ground leakage current [7], [8]. In isolated topologies, the galvanic isolation between dc source and ac grid provides required voltage magnification, reduces circulation of leakage or common mode current, and ensures safety. Conventionally, a three-phase inverter along with a line-frequency (50/60 Hz) transformer (LFT) is used. In comparison, high frequency link

(HFL) dc–ac solutions have some attractive features such as, lower weight, volume, and cost.

In the literature, the HFL dc–ac converter topologies are broadly classified as multistage HFL and single-stage HFL topology. In multistage HFL topology [see Fig. 1(a)], an isolated dc–dc converter is connected to an H-bridge inverter through a dc-link capacitor [9], [10]. The converter has bidirectional power conduction capability. The capacitor makes the dc link as stiff voltage port for the next stage H-bridge inverter. But the capacitor has long term reliability issues [11]. In single-stage converter topology, this capacitor is eliminated. Two known single-stage topologies are rectifier-type HFL (RHFL) [12]–[14] and cycloconverter-type HFL (CHFL) [15]–[18]. The structure of RHFL [see Fig. 1(b)] is similar as multistage topology without the dc link filter capacitor. Here, the dc link is pulsating. In the CHFL topology, dc-side H bridge generates high frequency ac from the input dc source. In the secondary of HFT, a cycloconverter directly converts the high frequency ac to line-frequency ac. In the literature, two cycloconverter configurations are widely discussed for 1ϕ topologies full bridge [see Fig. 1(c)] [6], [19]–[21] and push–pull [see Fig. 1(b)] [22]–[25], based on the ac-side converter configuration. Both the RHFL and CHFL topologies can operate in all four quadrants of $\bar{v}_o - i_o$ plane where \bar{v}_o is the average output voltage of the converter and i_o is the output current. The CHFL push–pull converter [see Fig. 1(d)] when operates only in *I* and *III* quadrant of $\bar{v}_o - i_o$ plane (supporting only positive active power ($P > 0$) whereas reactive power ($Q = 0$)), the ac switches can be line frequency switched based on the direction of i_o and modulation can be implemented in the dc-side H bridge. This paper presents a novel topology, as shown in Fig. 1(e), which has a three winding HFT as the CHFL topology but supports only positive active power flow ($P > 0$ and $Q = 0$). A dc–ac converter with capability to support only $P > 0$ and $Q = 0$ is useful in the grid integration of solar or fuel cell, etc., where power flow is unidirectional and any nonzero Q support implies increase in the rating of the converter. The secondary has only two-quadrant switches in a modular half-bridge configuration, instead of four such switches in two ac switch configuration, which is not commonly available and difficult to drive in comparison with half-bridge modular structure. Both of this active switches are line frequency switched incurring negligible switching loss. Another single-phase topology can be developed from the bidirectional RHFL topology [see Fig. 1(b)] by replacing one of the ac-side H bridge with a diode bridge rectifier. This topology is shown in Fig. 1(f) [26]. It supports only $P > 0$ and $Q = 0$ with

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The authors are with the Department of Electrical Engineering, Indian Institute of Science, Bengaluru 560012, India (e-mail: anirbanp@iisc.ac.in; kbasu@iisc.ac.in).

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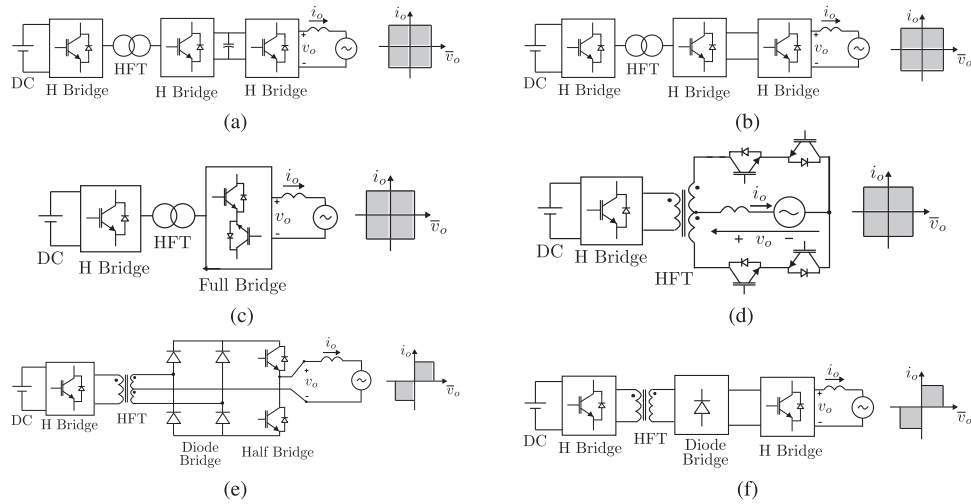


Fig. 1. (a) Multistage 1 ϕ HFL topology. (b) Single-stage 1 ϕ RHFL topology. (c) Single-stage 1 ϕ CHFL full bridge topology. (d) 1 ϕ CHFL push-pull configuration. (e) Novel 1 ϕ unidirectional HFL topology. (f) Novel unidirectional 1 ϕ RHFL topology.

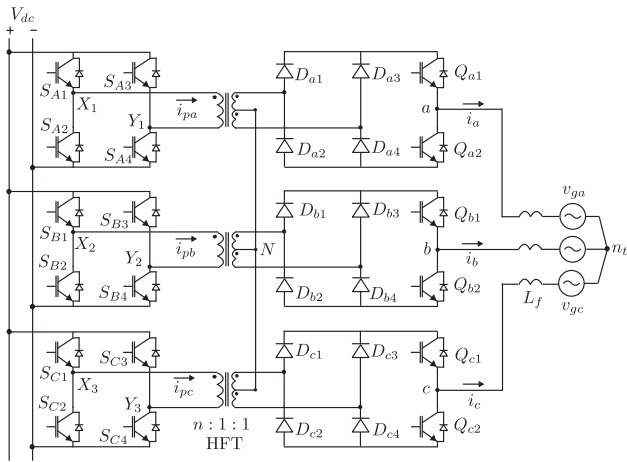


Fig. 2. Proposed 3 ϕ single-stage HFL topology.

line-frequency switching of the ac-side switches. When compared with the topology in Fig. 1(e), it has two more switches and one less winding in the secondary. Also blocking voltage rating of the secondary switches are half of that in Fig. 1(e). In [18], a 3 ϕ three wire configuration is obtained from the 1 ϕ CHFL push-pull topology. The center taps of the HFT of each of the three phases are connected together to form a floating star point. Similar idea is used here to derive the 3 ϕ three wire version of the novel 1 ϕ HFL topology [see Fig. 1(e)]. The resultant 3 ϕ topology is shown in Fig. 2. This 3 ϕ HFL inverter topology is unidirectional and does not support reactive power transfer. Again here, all ac-side switches are line frequency switched. A novel three phase version of the single-phase configuration given in Fig. 1(f) is shown in Fig. 3 (when the secondary module number per phase $p = 1$).

A number of unidirectional 3 ϕ HFL topologies are presented in the literature based on variations of number of legs in dc-side bridge and the ac-side diode bridge and number of HFTs [see Fig. 1(f)]. In [27], three high-frequency transformers (HFT) are

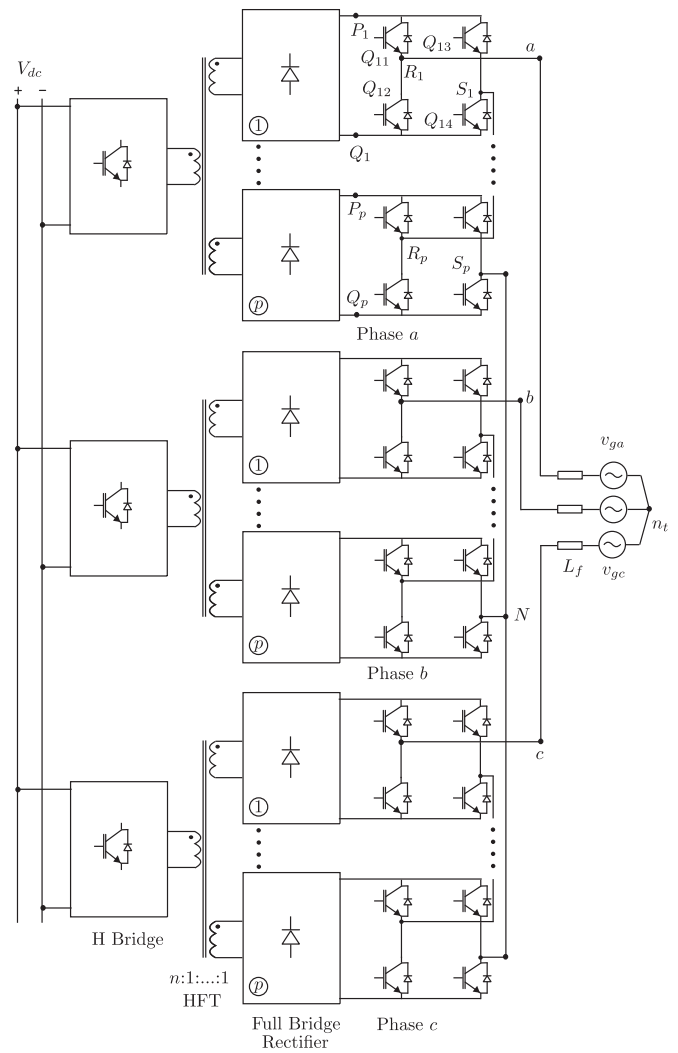


Fig. 3. Proposed 3 ϕ cascaded multilevel HFL topology.

connected to three legs of the dc-side HF inverter and the ac-side has 3ϕ diode bridge rectifier connected to a 3ϕ voltage source inverter (VSI). Here, hybrid modulation (HM) strategy is used resulting in reduction of HF switching of the ac-side VSI. The ac-side VSI is HF switched for one-third of the line cycle but the switching frequency is twice of the dc-side HF inverter. The converter is hard-switched and circuit nonidealities are not considered. The topology in [28] is a variation of [27] where the dc-side converter has six legs. The HM strategy implemented here ensures soft switching of the dc-side converter without using additional snubber. The ac-side VSI is hard switched for one-third of the line cycle and has same switching frequency as of the dc-side converter. In switching analysis, role of device capacitances are not considered. The dc-side HF inverter is asymmetrically switched resulting in uneven conduction loss in the active switches. In [29], another variation of the topology with four leg dc-side converter along with two HFTs are shown. This paper uses a modified HM scheme to ensure zero-voltage switching (ZVS) of the ac-side VSI but the dc-side converter is hard switched. In [30], the topology has an H bridge in the dc-side and a diode bridge rectifier along with 3ϕ VSI in ac side of the HFT. HM strategy reduces HF switching of the ac-side VSI, but is hard switched for one-third of the line cycle.

The proposed converter topology can be integrated to a medium-voltage (MV) grid using a step up LFT. A direct integration scheme replacing the LFT will have the following advantages: first, conduction losses in the secondary converter will reduce and, second, size of line filter as well as filter copper loss will reduce with decreased current rating. Due to limitation of voltage blocking capability of commercially available semiconductor devices, a direct integration with a medium-voltage (11/33 kV) grid is not possible with the proposed structure, as shown in Fig. 2. A cascaded multilevel approach is considered to modify the converter configuration. The HFL MV cascaded multilevel converter topologies are broadly classified as multistage and single stage. The multistage converter topologies have an interstage dc-link capacitors. The multistage topology can either be multiwinding HFT type [31] or multiple HFT type [32]. In multiple HFT type in each phase, the multistage single-phase topology of Fig. 1(a) is series connected on the ac side to connect to the MV grid. A unidirectional multi-stage multiple HFT topology is shown in [33] where the secondary H bridges connected to HFTs are replaced with diode bridge rectifiers. In multiwinding HFT type, a single HFT with multiple secondary is used. The primary is identical to Fig. 1(a). Multiple secondary-side converters connected to different secondary windings are cascaded on the grid side to form a multilevel configuration. A multiwinding-type single-stage topology is proposed in [3] and [5] based on the single-phase topology given in Fig. 1(c). In this paper, a multiwinding-type single-stage multilevel topology is proposed that supports unidirectional power flow with no var support with line frequency switching of ac-side switches, as shown in Fig. 3. This topology is based on the configuration given in Fig. 1(f).

In this paper, the modulation strategy along with converter switching process considering the circuit nonidealities are discussed in detail for both the proposed 3ϕ topologies in Figs. 2

and 3. The dc-side converter is soft switched (ZVS) for most part of the line cycle without additional snubber circuit. All active switches in the ac-side converter are line frequency switched resulting in negligible switching loss. Power is transmitted at unity power factor (UPF) to the grid. A part of this work is presented in [34].

The rest of this paper is organized as follows. In Section II, modulation strategy of the proposed converters are discussed. Detailed circuit operation and soft-switching process are presented in Section III. Design and implementation aspects of a laboratory prototype is first discussed followed by key simulation and experimental results are presented in Section IV. The converter power loss is obtained analytically and experimentally and is presented in Section V.

II. MODULATION STRATEGY

In this section, modulation strategies for the generation of balanced adjustable magnitude 3ϕ ac at grid frequency at the output from the dc source are discussed in details.

The reference signals for the generation of output voltages are given in (1) where m is the modulation index and $\omega_o = \frac{2\pi}{T_o}$ is the angular line frequency, $j \in \{a, b, c\}$, and $K_a = 0, K_b = -1, K_c = +1$. Due to unidirectional nature of the instantaneous power flow, the reference signals are in phase with the average line currents $i_{a,b,c}$

$$v_{\text{ref},j} = m \sin \left(\omega_o t + K_j \frac{2\pi}{3} \right). \quad (1)$$

Intermediate reference signals $\delta_{a,b,c}$ are obtained from the reference signals, where $\delta_j = |v_{\text{ref},j}|$. The dc-side H bridges generate pulsewidth modulated (PWM) HF ac across the transformer terminals. A control signal F is considered with 50% duty ratio and time period T_s , as shown in Fig. 4. In the positive half of the line cycle when F is high, upper half of the secondary-side windings are in conduction. When F is zero, lower half of the secondary winding of HFTs take part in power transfer. F is aligned with the carrier signal C , which is a periodic ramp with unity peak and time period $\frac{T_s}{2}$. The control signals of switches S_{A1} , S_{B1} , and S_{C1} (see Fig. 2) are same as F . The gating signals of S_{A3} , S_{B3} , and S_{C3} are derived as follows:

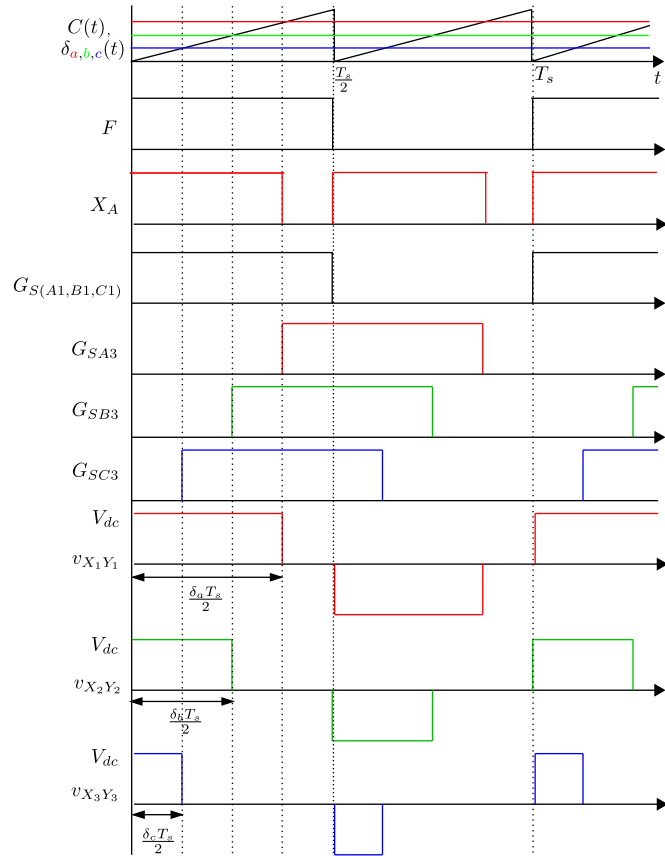
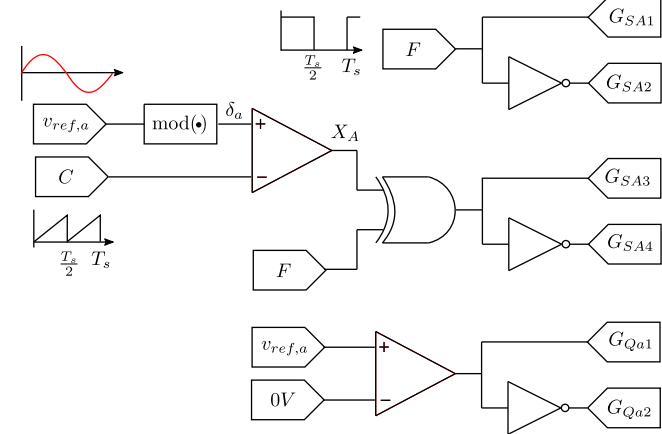
$$G_{S_{i3}} = X_i \oplus F \quad (2)$$

where

$$X_i(t) = \begin{cases} 1, & \delta_j(t) \geq C(t) \\ 0, & \text{Otherwise} \end{cases} \quad (3)$$

where $i \in \{A, B, C\}$.

The intermediate reference signals $\delta_j(t)$ are slowly varying compared to signal C and can be assumed to be constant over a switching period (T_s) (see Fig. 4). The switch pairs $S_{i1} - S_{i2}$ and $S_{i3} - S_{i4}$, $i \in \{A, B, C\}$ are complementary switched with a dead time to avoid short circuit of the dc source. Fig. 5 shows the gating signal generation scheme of the active switches corresponding to phase a . This modulation results in three-level voltages ($\pm V_{dc}$ and 0) being applied across HFT terminals,


 Fig. 4. Switching strategy of dc-side H bridges of 3ϕ topology.

 Fig. 5. Gating signal generation scheme for phase a .

as shown in Fig. 4. From these applied transformer primary voltages ($v_{X_i Y_i}$), it is possible to see that transformer fluxes are balanced over a switching cycle. The voltages applied across the HFTs are step up/down and then rectified by the ac-side diode bridges. The ac-side active switch pairs $Q_{a1,a2}$, $Q_{b1,b2}$, and $Q_{c1,c2}$ are complementary switched at line frequency ($f_o = \frac{1}{T_o}$). The line frequency switching (see Fig. 6) is based on reference voltage polarity, e.g., if $v_{ref,a} > 0$, Q_{a1} is ON. The switching scheme results line frequency inversion of the rectified output of the diode bridges. Applied 3ϕ pole voltages v_{aN} , v_{bN} , and

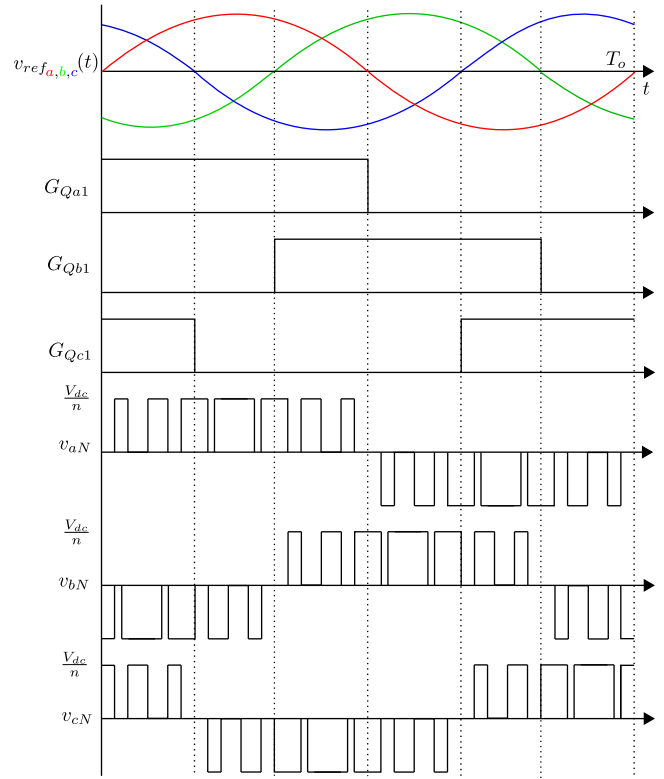


Fig. 6. Switching strategy of grid or ac-side active switches.

v_{cN} with respect to transformer neutral N are shown in Fig. 6. Average pole voltages are given as

$$\bar{v}_{jN} = \frac{m}{n} V_{dc} \sin\left(\omega_o t + K_j \frac{2\pi}{3}\right) \quad (4)$$

where modulation index $m = \frac{nV_{pk}}{V_{dc}}$ and V_{pk} is the desired peak value of average pole voltage. n is HFT primary to secondary turns ratio. As the ac port is connected to a balanced three-phase system and the sum of the switching cycle average of the pole voltages ($\sum_{j=a,b,c} \bar{v}_{jN} = 0$) are zero, the average line to neutral voltages are same as the pole voltages, $\bar{v}_{jn_t} = \bar{v}_{jN}$.

It is possible to have a 3ϕ topology with two winding HFTs where in the ac side the diode rectifier stage is connected to line frequency switched full bridge inverter (see Fig. 3 with $p = 1$). Similar modulation strategy can be implemented to generate balanced 3ϕ output voltage. In this case, the blocking voltage rating of the ac-side switches and diodes is half of the original topology (see Fig. 2).

What follows is a discussion of the modulation strategy of 3ϕ cascaded multilevel HFL topology shown in Fig. 3. The gating signal generation scheme for the three dc-side H bridges are same as discussed above. The generation of the output voltage v_{aN} of phase a is discussed in detail. Phases b and c have similar switching scheme. The output of the multiwinding HFTs are fed to diode bridge rectifiers. Output voltage of k th rectifier module averaged over a switching cycle is expressed as

$$\bar{v}_{PQ(k)} = \frac{m}{n} V_{dc} |\sin(\omega_o t)| \quad (5)$$

where $k \in (1, 2, \dots, p)$ and p is the total number of secondary modules in phase a (see Fig. 3). Output of these rectifiers are fed to line frequency inverters to obtain bipolar output voltage. The gating signals of k th line frequency inverter are given as

$$G_{Qk1} = G_{Qk4} = \begin{cases} 1, & v_{\text{ref},a} \geq 0 \\ 0, & \text{Otherwise} \end{cases} \quad (6)$$

$$G_{Qk2} = G_{Qk3} = \overline{G_{Qk1}}. \quad (7)$$

Due to cascade connection, output of these line frequency inverters is summed up to build total output phase voltage. The average output voltage of phase a is given \bar{v}_{aN} , which is shown as follows:

$$\bar{v}_{aN} = \begin{cases} + \sum_{k=1}^p \bar{v}_{PQ(k)}, & 0 < \omega_o t < \pi \\ - \sum_{k=1}^p \bar{v}_{PQ(k)}, & \pi \leq \omega_o t \leq 2\pi. \end{cases} \quad (8)$$

Using (8), the average output voltage can be expressed as

$$\bar{v}_{aN} = \frac{pm}{n} V_{\text{dc}} \sin(\omega_o t). \quad (9)$$

A brief description for design of the three winding HFT, based on the described modulation strategy is presented here. Note that the primary voltage is duty cycle modulated square wave with amplitude V_{dc} . The duty cycle is maximum when $\omega_o t = \frac{\pi}{2}$. So given maximum flux density B_{pk} , the core area $A_c = \frac{mV_{\text{dc}}T_s}{4B_{\text{pk}}N_1}$, where N_1 is the number of primary turns. Assuming good filtering, the output currents can be assumed to be sinusoidal at the output frequency with amplitude I_{pk} . The primary winding current is a square wave with a time-varying amplitude. The amplitude is a rectified sine with peak $\frac{I_{\text{pk}}}{n}$. Each of the secondary windings conduct only half the time. Using this information, it is possible to show that window area $(1 + 1/\sqrt{2})N_1 I_{\text{pk}} / (nK_w J)$, where K_w is the window fill factor and J is the current density. The area product is given in (10), the three-phase power $P_{3\phi} = 1.5V_{\text{pk}}I_{\text{pk}}$

$$A_c A_w = \frac{(1 + \sqrt{2})P_{3\phi}T_s}{6\sqrt{2}K_w J B_{\text{pk}}}. \quad (10)$$

III. CIRCUIT OPERATION

This section presents detailed circuit operation over a switching cycle (T_s) describing the soft-switching process of the dc-side H bridges of the proposed topologies. As the switching strategy is similar for all the three phases, a detailed discussion on the circuit operation of phase a is presented here.

The high-frequency switched dc-side converters are partially soft switched. Soft switching is achieved using device parasitic capacitance (C_s) and transformer leakage and additional series inductance (L_{lk}). For the ease of analysis, the output filter inductor (L_f) is considered large enough to treat the slowly varying line frequency output current (i_a) as a constant current (I_a) sink for the analysis of switching transitions. The circuit is shown in Fig. 7. The switching process is described for negative half cycle of the line current i_a . The switching transitions of the dc-side converter are broadly classified as *active to zero state* transition and *zero to active state* transition. Where the *active*

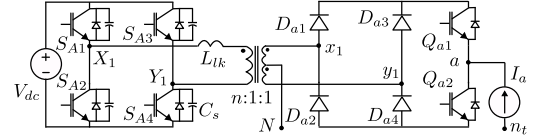


Fig. 7. Simplified circuit diagram for switching analysis of phase a .

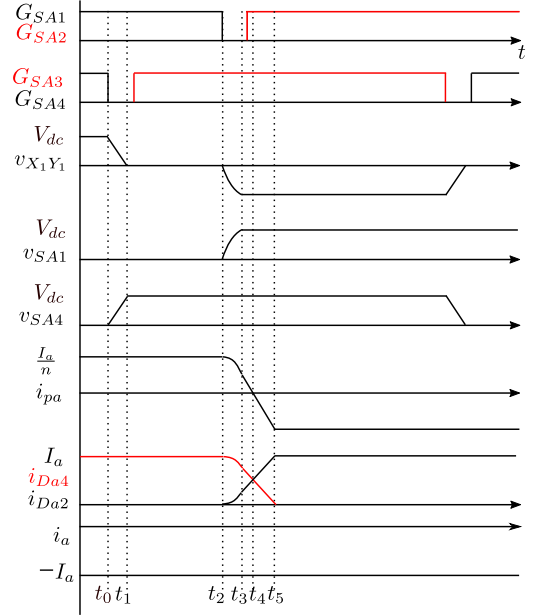


Fig. 8. Switching waveforms showing zero to active and active to zero state transitions.

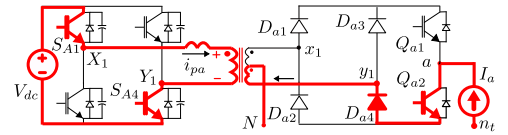


Fig. 9. Simplified circuit diagram during active state.

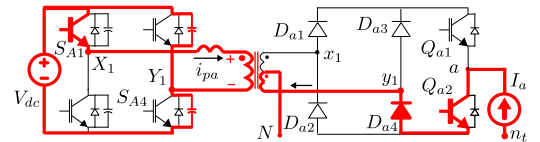


Fig. 10. Circuit diagram during active to zero state transition.

state is referred to the converter switching state when the applied voltage across the transformer terminals X_1Y_1 is V_{dc} or $-V_{\text{dc}}$. *Zero state* is the switching state when $v_{X_1Y_1} = 0$. Switching transition waveforms are shown in Fig. 8.

A. Active State ($t < t_0$: Fig. 8)

In this state, switches S_{A1} and S_{A4} are ON (see Fig. 9) and are conducting a current, $i_{pa} = \frac{I_a}{n}$. The switches S_{A2} and S_{A3} are blocking the dc voltage V_{dc} . A positive voltage V_{dc} is applied across the transformer terminals X_1Y_1 . In ac side, the diode D_{a4} and the switch Q_{a2} are conducting the load current I_a , whereas

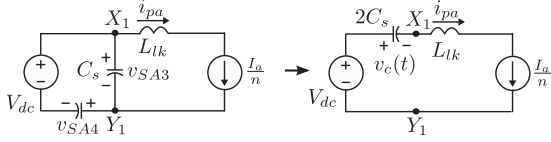


Fig. 11. Equivalent circuit during active to zero state transition.

D_{a2} is blocking a voltage $2V_{dc}/n$. The polarities of transformer voltage and current indicate the active power flow from dc to ac side.

B. Active State \Rightarrow Zero State ($t_0 < t < t_1$: Fig. 8)

At the beginning of this transition, the switch S_{A4} is turned OFF. Due to the presence of switch capacitance C_s , voltage across the device cannot change immediately. Channel current through the device falls first and then the device drain to source voltage starts rising. So, turn OFF of S_{A4} is a *zero voltage transition*. The current i_{pa} starts charging the device capacitance of S_{A4} and discharging the capacitance of S_{A3} (see Fig. 10). This causes the transformer voltage $v_{X_1 Y_1}$ to fall linearly from V_{dc} . In the ac side, D_{a4} and Q_{a2} are conducting. The equivalent circuit in this mode is shown in Fig. 11. The initial conditions are given as: $v_{X_1 Y_1}(t_0) = V_{dc}$, $i_{pa}(t_0) = \frac{I_a}{n}$. Relevant circuit equations are

$$\begin{aligned} V_{dc} &= v_{SA3}(t) + v_{SA4}(t) \\ i_{pa}(t) &= \frac{I_a}{n} \\ i_{pa}(t) &= C_s \left(\frac{dv_{SA4}}{dt} - \frac{dv_{SA3}}{dt} \right) \\ v_{X_1 Y_1}(t) &= v_{SA3}(t) \end{aligned} \quad (11)$$

where v_{SA3} and v_{SA4} are the voltages across the devices S_{A3} and S_{A4} , respectively. C_s is the device capacitance across S_{A3} and S_{A4} . L_{lk} is the transformer leakage and additional series inductance. Solving (11)

$$v_{X_1 Y_1}(t) = V_{dc} - \left(\frac{I_a}{nC_T} \right) t \quad (12)$$

where $C_T = 2C_s$.

The transition ends at t_1 when $v_{X_1 Y_1}$ reaches 0, i.e., the device capacitance across S_{A3} is completely discharged and the body diode of S_{A3} is forward biased and starts conducting. After t_1 , S_{A4} is blocking V_{dc} . The time interval, $t_{az} = (t_1 - t_0)$, is estimated as solving (12)

$$t_{az} = \frac{nC_T V_{dc}}{I_a}. \quad (13)$$

C. Zero State ($t_1 < t < t_2$: Fig. 8)

After t_1 , the transformer terminals $X_1 Y_1$ are shorted through switch S_{A1} and the body diode of S_{A3} . To ensure *zero voltage turn ON* of S_{A3} , the gating signal is applied after t_1 when the

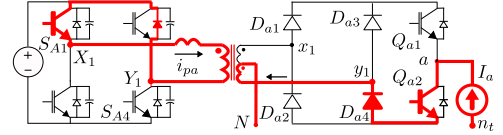


Fig. 12. Simplified circuit in zero state.

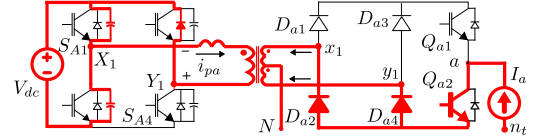


Fig. 13. Simplified circuit in zero to active state transition in submode I.

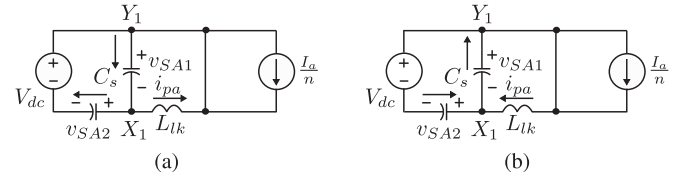


Fig. 14. Equivalent circuit of zero to active state transition. (a) In submode I. (b) During resonant oscillation in submode I.

body diode of S_{A3} is conducting. A simplified circuit diagram is shown in Fig. 12. No active power is transferred from dc to ac side in this state.

D. Zero State \Rightarrow Active State

The transition starts at t_2 , when the switch S_{A1} is turned OFF. This transition is divided into three submodes.

1) *Submode I* ($t_2 < t < t_3$: Fig. 8): A simplified circuit diagram is shown in Fig. 13. Turn OFF of S_{A1} is capacitor assisted ZVS as explained in the case of S_{A4} in active to zero state transition. The current i_{pa} starts charging the device capacitance of S_{A1} and discharging the device capacitance of S_{A2} . A negative voltage is applied across $X_1 Y_1$, which forward biases D_{a2} and D_{a2} starts conducting. The HFT secondary winding is shorted through D_{a2} and D_{a4} . The equivalent circuit is shown in Fig. 14. Initial conditions are given as: $v_{SA1}(t_2) = 0$, $v_{SA2}(t_2) = V_{dc}$, and $i_{pa}(t_2) = \frac{I_a}{n}$. Relevant circuit equations are

$$\begin{aligned} C_s \frac{dv_{SA1}(t)}{dt} &= C_s \frac{dv_{SA2}(t)}{dt} + i_{pa}(t) \\ L_{lk} \frac{di_{pa}(t)}{dt} &= -v_{SA1}(t) \\ V_{dc} &= v_{SA1}(t) + v_{SA2}(t). \end{aligned} \quad (14)$$

Solving (14), the following expressions are obtained

$$\begin{aligned} i_{pa}(t) &= \frac{I_a}{n} \cos \omega_p t + \frac{i'_{pa}(t_2)}{\omega_p} \sin \omega_p t \\ v_{SA1}(t) &= \frac{\omega_p L_{lk} I_a}{n} \sin \omega_p t - L_{lk} i'_{pa}(t_2) \cos \omega_p t \end{aligned} \quad (15)$$

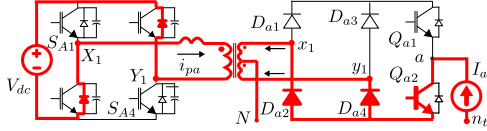


Fig. 15. Simplified circuit in zero to active state transition in submode II.

where $\omega_p = \frac{1}{\sqrt{L_{lk}C_T}}$ and $i'_{pa}(t_2) = \frac{di_{pa}(t)}{dt}|_{t_2}$.

Here, $i'_{pa}(t_2) = 0$ as $v_{SA1}(t_2) = 0$. At t_3 , $v_{SA1}(t)$ reaches V_{dc} . The capacitor across S_{A2} is completely discharged and the body diode is forward biased. The time interval, $t_{za1} = (t_3 - t_2)$, is estimated as

$$t_{za1} = \frac{1}{\omega_p} \sin^{-1} \left(\frac{nV_{dc}}{\omega_p L_{lk} I_a} \right). \quad (16)$$

The capacitor across S_{A2} will be completely discharged and the circuit will move to next submode only if

$$\omega_p L_{lk} I_a \geq nV_{dc}. \quad (17)$$

Else the circuit will experience resonant oscillation with angular frequency ω_p , i.e., before v_{SA2} becomes zero, i_{pa} will be negative and will start charging and discharging the capacitances across S_{A2} and S_{A1} , respectively. The circuit moves back and forth between Fig. 14(a) and (b) till next switching transition, i.e., till the gating pulse of S_{A2} is applied. And this turn ON of S_{A2} will be hard switching, as capacitance across the device is not completely discharged. If (17) is satisfied, at t_3 , $i_{pa}(t)$ is given as

$$i_{pa}(t_3) = \frac{\sqrt{(\omega_p L_{lk} i_{pa}(t_2))^2 - (V_{dc})^2}}{\omega_p L_{lk}}. \quad (18)$$

2) *Submode II* ($t_3 < t < t_4$: Fig. 8): In this submode, body diodes of S_{A2} and S_{A3} conduct $i_{pa}(t)$. A simplified circuit diagram is shown in Fig. 15. As $-V_{dc}$ is applied across L_{lk} [see Fig. 16(a)], i_{pa} falls linearly

$$i_{pa}(t) = i_{pa}(t_3) - \frac{V_{dc}}{L_{lk}} t \quad (19)$$

This mode ends when i_{pa} reaches zero at t_4 . The time interval, $t_{za2} = (t_4 - t_3)$, is given as

$$t_{za2} = i_{pa}(t_3) \frac{L_{lk}}{V_{dc}}. \quad (20)$$

To ensure ZVS turn ON of S_{A2} , gating signal is applied during this interval. Dead time (DT) between the gating signals of S_{A1} and S_{A2} must be

$$t_{za1} \leq DT \leq (t_{za1} + t_{za2}). \quad (21)$$

From (16) and (20), due to dependence on the initial conditions of $i_{pa}(t)$, t_{za1} and t_{za2} varies over a line cycle. With fixed DT switching signals and for a given load, (21) will not be satisfied in some part of the line cycle, which will result in hard switching of S_{A2} . It is seen that near zero-crossing of the line current when I_a is small, (21) is not satisfied. But as the current magnitude is small, resulting switching loss is less.

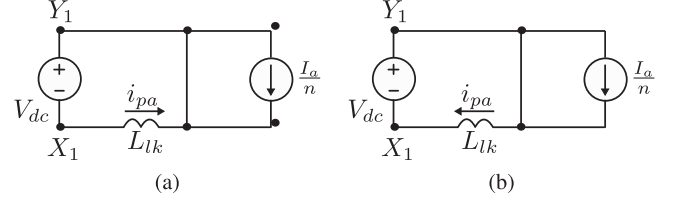


Fig. 16. Equivalent circuit of zero to active state transition. (a) In submode II. (b) In submode III.

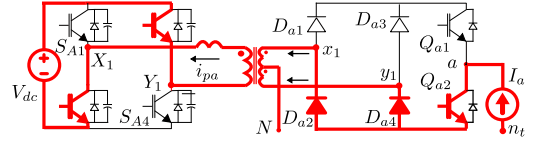


Fig. 17. Simplified circuit in zero to active state transition in submode III.

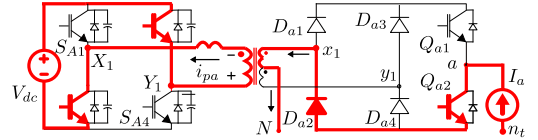


Fig. 18. Simplified circuit in next active state.

3) *Submode III* ($t_4 < t < t_5$: Fig. 8): A simplified circuit diagram in this submode is shown in Fig. 17. After t_4 , i_{pa} starts flowing in the opposite direction as the switches S_{A2} and S_{A3} are ON and $-V_{dc}$ is still applied across L_{lk} [see equivalent circuit in Fig. 16(b)]. i_{pa} can be expressed as

$$i_{pa}(t) = -\frac{V_{dc}}{L_{lk}} t. \quad (22)$$

This mode ends at t_5 when $i_{pa} = -\frac{I_a}{n}$.

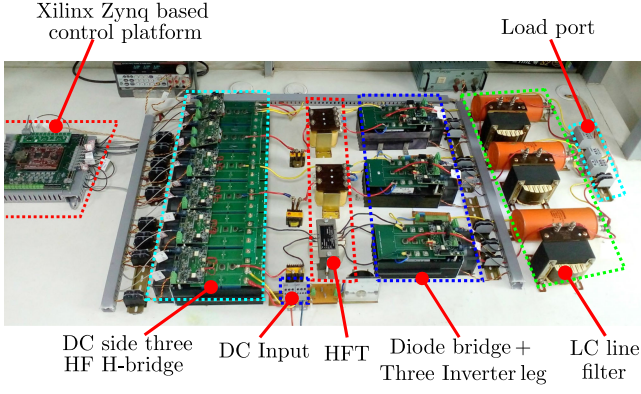
E. Active state ($t > t_5$: Fig. 8)

At t_5 , current through D_{a4} becomes zero. The applied voltage polarity across the transformer terminal $X_1 Y_1$ reverse biases the diode D_{a4} . Simplified circuit schematic is shown in Fig. 18. The circuit is in the next active state.

The above discussion shows the polarity reversal of transformer primary voltage and current in one half of the switching cycle. In remaining half of the switching cycle, another two state transitions take place—*active to zero state transition* (S_{A3} is turned OFF and S_{A4} is turned ON) followed by *zero to active state transition* (S_{A2} is turned OFF and S_{A1} is turned ON). Similar switching process and circuit analysis are followed in these switching state transitions. In positive half-cycle of the line current i_a , the diodes D_{a1} , D_{a3} and the switch Q_{a1} take part in conduction and switching process. The operation of the primary H bridge remains same.

IV. SIMULATION AND EXPERIMENTAL RESULTS

The modulation strategy and switching techniques of the proposed topologies discussed so far are simulated in

Fig. 19. 3 ϕ Hardware prototype.TABLE I
COMPONENT USED

Component	Particulars
Active switches	SKM75GB123D (1200V,75A)
Diode	MEE 75-12 DA (1200V,75A)
HFT	Turns ratio ($N_1:N_2:N_2$)- 51:34:34, Enamelled copper wire-21 SWG, Core material- ferrite E80/38/20, $L_m = 23mH$, $L_{lkT} = 6 - 8\mu H$
Series inductor with HFT	$36\mu H$
Filter inductor	$L_f = 2.3mH$
Filter capacitor	$10\mu F$
Controller	Xilinx Zynq-7000 based SoC platform

MATLAB/Simulink and experimentally verified on the laboratory prototype (see Fig. 19). Table I shows the details of the hardware prototype. The switching frequency of the dc-side converter is 20 kHz, whereas ac-side active switches are switched at 50 Hz. A DSP-FPGA-based system on chip (SoC) controller platform (Xilinx Zynq-7000) is used to generate required PWM signals of the converter. Optically isolated intelligent gate driver ICs (ACPL-339J) with 15- Ω gate resistance are used to drive the insulated gate bipolar transistor (IGBT) devices. An effective dead time of 600 ns is provided between the gating signals of top and bottom IGBT devices of an IGBT module. For three-winding high-frequency transformers ferrite E core (E80/38/20) from the EPCOS are used. The converter is modulated in open loop at the operating conditions given in Table II. As described in the modulation section, in order to generate the ac output voltage, one requires reference signals $v_{ref(a,b,c)}(t)$. These reference voltages are generated from three-phase balanced internal sinusoidal signals at frequency f_o . In order to compute the amplitude m , given the turns ratio n and V_{dc} , we need to find the value of V_{pk} .

The converter can support only instantaneous unidirectional power flow. So, \bar{v}_{jm_i} and line currents $i_{a,b,c}$ must be in phase. Fig. 20 shows per phase equivalent circuit (here for phase a) of the converter connected to the grid along with the phasor

TABLE II
OPERATING CONDITION OF THE 3 ϕ TOPOLOGY

Parameter	Values
Output Power, $P_{3\phi}$ (kW)	6.2
DC input, V_{dc} (V)	440
Grid voltage peak, V_{gpk} (V)	252
Output frequency, f_o (Hz)	50

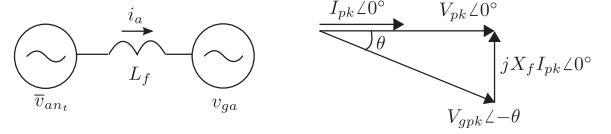
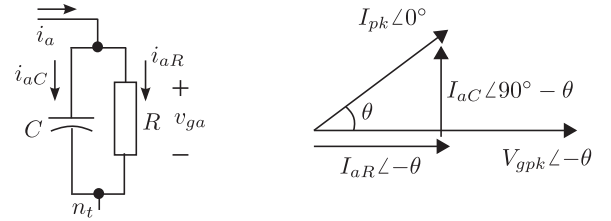
Fig. 20. Equivalent circuit showing grid connection of the converter and phasor diagram corresponding to phase a .Fig. 21. Grid is modeled as parallel RC branch for a particular operating point.

diagram for the line frequency (f_o) components. Equation (23) represents the phasor diagram and can be solved along with the fact that $P_{3\phi} = 1.5V_{pk}I_{pk}$, to find V_{pk} in terms of the parameters given in Tables I and II, (24). Once, V_{pk} is known one can determine I_{pk} from $P_{3\phi}$

$$V_{pk}\angle 0^\circ = V_{gpk}\angle -\theta + jX_f I_{pk}\angle 0^\circ \quad (23)$$

$$V_{pk} = \left(\frac{V_{gpk}^2}{2} + \sqrt{\frac{V_{gpk}^4}{4} - \left(\frac{X_f P_{3\phi}}{3} \right)^2} \right)^{1/2} \quad (24)$$

where $X_f = \omega_o L_f$. The line current leads the grid voltage by $\theta = \cos^{-1} \left(\frac{V_{pk}}{V_{gpk}} \right)$. The line current has an in phase ($I_{aR} = I_{pk} \cos \theta$) and a leading quadrature ($I_{aC} = I_{pk} \sin \theta$) component with respect to the grid voltage (see Fig. 21). Because the power is unidirectional, the grid can be modeled as parallel RC network for a particular operating point, V_{gpk} and $P_{3\phi}$ (see Fig. 21), where the value of $R = \frac{V_{gpk}}{I_{aR}}$ and $C = \frac{I_{aC}}{\omega_o V_{gpk}}$.

A. Experimental Validation of Modulation Strategy

This section presents key simulation and experimental results to validate the modulation strategy of the proposed 3 ϕ converter (see Fig. 2).

Fig. 22(a) and (b) shows the grid voltage waveforms $v_{g-a,b,c}$ obtained from the simulation and the experiment, respectively. The experimental result have a peak of approximately 250 V, whereas the simulation result peak is 253 V. The high-frequency

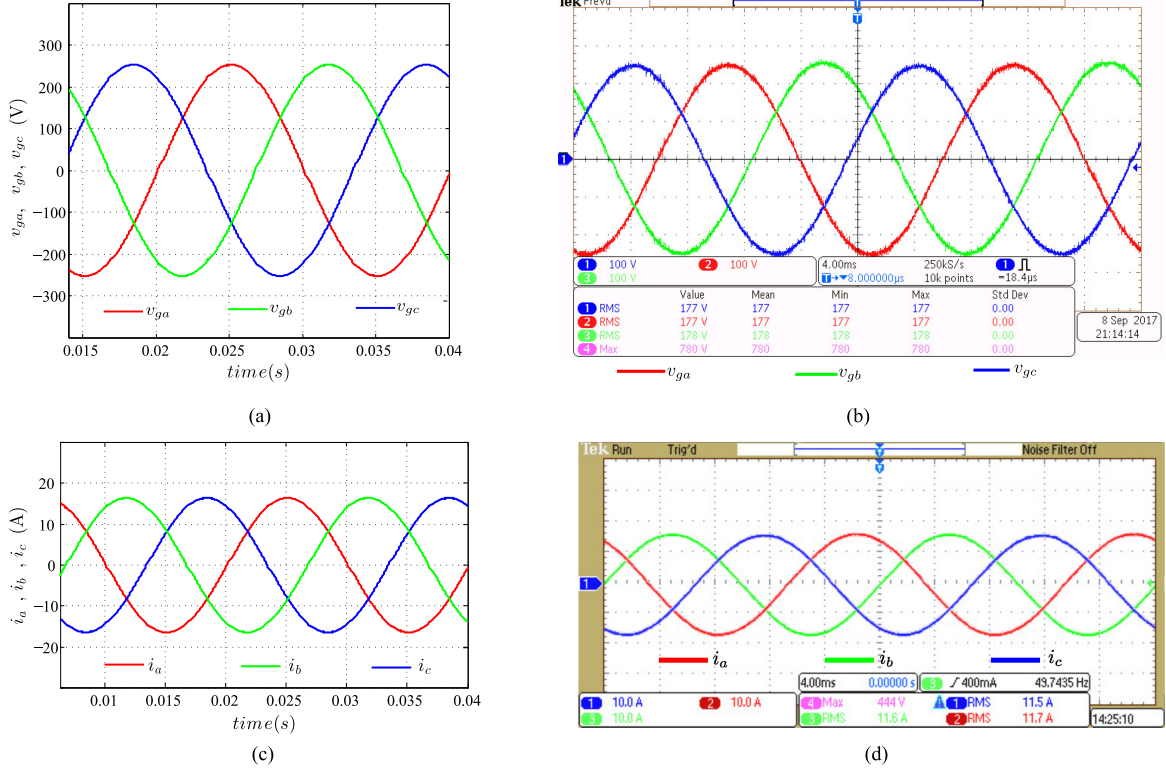


Fig. 22. Output phase voltages ([CH1] c phase voltage (100 V/div.), [CH2] a phase voltage (100 V/div.), and [CH3] b phase voltage (100 V/div.). Time scale 4 ms/div.). (a) Simulation. (b) Experimental. Output current waveforms ([CH1] c phase current (10 A/div.), [CH2] a phase current (10 A/div.), and [CH3] b phase current (10 A/div.). Time scale 4 ms/div.). (c) Simulation. (d) Experimental.

switching ripple in the pole voltages is filtered by the low pass filter formed by L_f and $R-C$. Both simulation and experimental results of the line currents have a peak 16.4 A [see Fig. 22(c) and (d)]. Fig. 23(a) and (b) shows the grid voltage, line current, and pole voltage with respect to load neutral (n_t) and pole voltage with respect to the transformer neutral point (N) of phase a . The line current i_a leads the load voltage v_{ga} by an angle 2.77° . Due to the presence of switching frequency common-mode voltage, the instantaneous waveforms of v_{aN} and v_{an_t} are not same. Fig. 23(c) and (d) presents the gate-emitter voltages of Q_{a1} and Q_{a2} along with the pole voltages w.r.t N and line current of phase a . These figures show that Q_{a1} and Q_{a2} are complementary switched at line frequency and Q_{a1} is conducting when the line current i_a is positive. The primary voltage of the transformer along with the primary current corresponding to phase a is shown in Fig. 24(b) over a line cycle. An expanded view of Fig. 24(b) over two switching cycles ($2T_s$) is shown in Fig. 24(d). The figure shows the applied volt-second across the transformer primary over a switching cycle (T_s) is zero. The primary current in the experimental result has high-frequency oscillation due to the parasitic capacitance of the diode bridge which is not included in the simulation. The input voltage and the magnetizing current waveform of the HFT of phase a are presented in Fig. 24(e) and (f). The magnetizing current is obtained by exciting the system at no load. The experimental result of the magnetizing current contains high-frequency oscillation at switching transitions. This oscillation

appears mainly due to the leakage inductance and interturn and interwinding parasitic capacitances of the transformer. These parasitic capacitances are neglected in the simulation. High frequency flux balance is clearly observed from the experimental result. Fig. 25(a) and (b) presents the input dc bus voltage and input dc current. The current has high frequency switching ripple. Fig. 25(d) shows the simulation and experimental results of the pole voltages with respect to HFT neutral, i.e., $v_{(a,b,c)N}$ and v_{Nn_t} . The high frequency v_{Nn_t} causes the common mode current to circulate in the secondary of the converter, which can be limited by using common mode choke.

To verify the modulation strategy of the multilevel converter in Fig. 3, a prototype is used with two cascaded modules ($p = 2$) in the ac side per phase. Simulation and experimental results are presented corresponding to phase a . Experiments are done with $V_{dc} = 600$ V, $V_{gpk} = 650$ V and per phase output power $P_\phi = 3.5$ kW. Fig. 26(b) shows the output voltage of module-1 ($v_{R_1S_1}$), module-2 ($v_{R_2S_2}$) and the resultant output voltage ($v_{R_1S_2}$). The grid phase voltage and line current waveforms are shown in Fig. 26(d). The observed line current peak is 11 A.

B. Experimental Verification of Soft Switching

In this section, results corresponding to switching transitions of dc-side H bridges are shown to validate soft switching of the converter. Switching transitions of the dc-side H bridge corresponding to phase a is considered for discussion. Fig. 27 shows

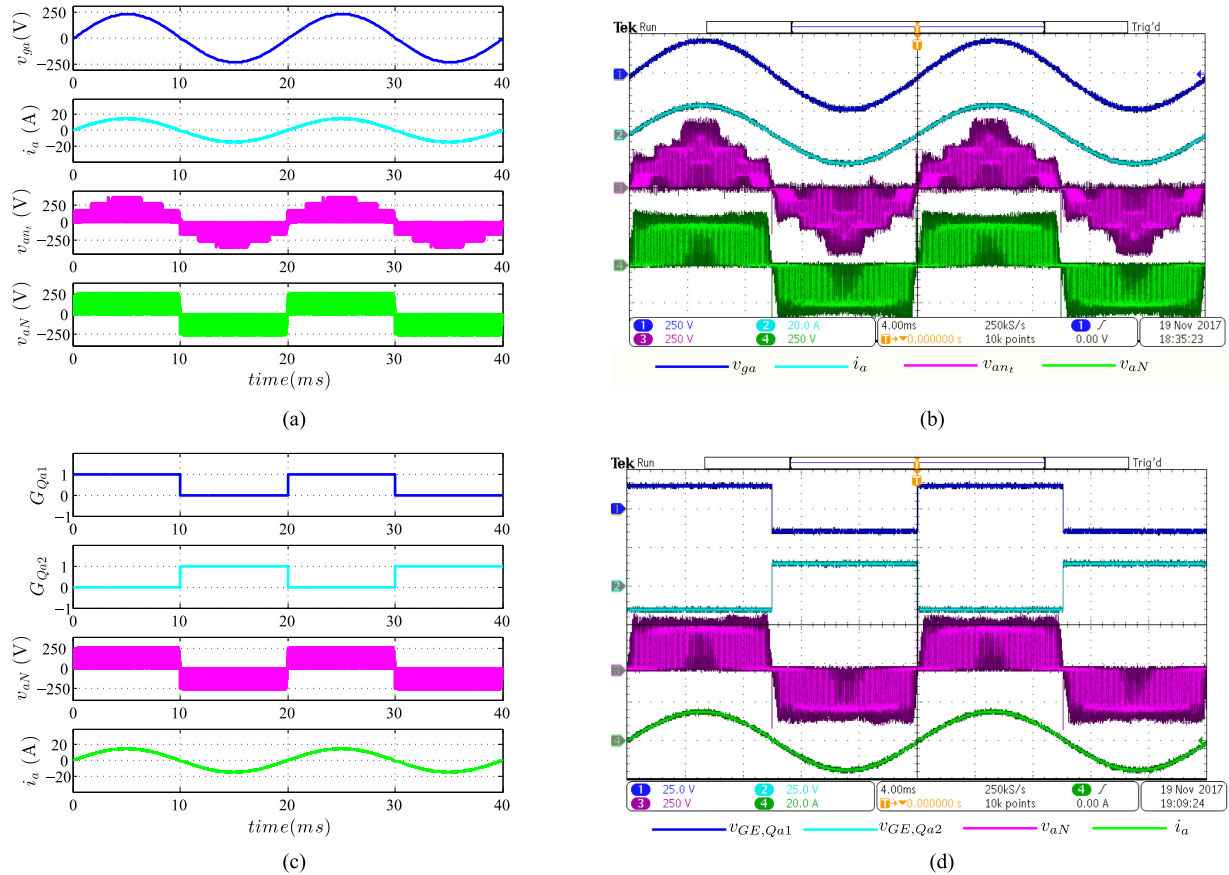


Fig. 23. Pole voltage waveforms ([CH1] Load voltage (250 V/div.), [CH2] line current (20 A/div.), [CH3] pole voltage w.r.t load neutral (250 V/div.), and [CH4] pole voltage w.r.t transformer neutral (250 V/div.) of phase a . Time scale 4 ms/div.). (a) Simulation. (b) Experimental. Line frequency switching ([CH1] Gate-emitter voltage of Q_{a1} (25V/div.), [CH2] gate-emitter voltage of Q_{a2} (25V/div.), [CH3] pole voltage w.r.t transformer neutral (250V/div.), and [CH4] line current (20A/div.) of phase a . Time scale 4ms/div.). (c) Simulation. (d) Experimental.

the gating signals of one leg of the dc-side H bridge ($S_{A1,2}$) along with primary voltage and current waveforms over two switching cycles.

Fig. 28 shows the zero to active state transition. In Fig. 27, the transition is marked using red-dotted circle. Before the transition, S_{A1} and body diode of S_{A3} are conducting (see Fig. 12). A zero voltage is applied across the transformer terminals X_1Y_1 . The experimental result shows the switching transition from S_{A1} to S_{A2} . At the end of this transition, -600 V is applied across X_1Y_1 . At t_2 , the gating signal of S_{A1} is removed. After sometime at t_2 , when gate-emitter voltage of S_{A1} , $v_{GE,S_{A1}}$ is almost zero, the voltage across S_{A1} starts rising resulting change in voltage $v_{X_1Y_1}$, as shown in Fig. 28, which implies the channel current of S_{A1} is zero before the voltage across the device starts to rise. The delay in voltage rise is caused by the device capacitance across the collector-emitter terminals of S_{A1} . This results in ZVS turn OFF of S_{A1} . In between t_2 and t_3 (see Fig. 28), the transformer current i_{pa} charges the capacitance across S_{A1} and discharges capacitor across S_{A2} . The LC dynamics given by (15) are clearly visible from the nonlinear change of i_{pa} and $v_{X_1Y_1}$ in Fig. 28. At t_3 , when $v_{X_1Y_1}$ is -600 V, the capacitor across S_{A2} is completely discharged and the body diode of S_{A2}

comes into conduction. Between t_3 to t_4 (see Fig. 28), a linear fall i_{pa} verifies (19). To achieve ZVS turn ON of S_{A2} , gating pulse is applied in between t_3 and t_4 (when the body diode is conducting), as seen from $v_{GE,S_{A2}}$ in Fig. 28. At t_4 , the primary current i_{pa} becomes zero. After t_4 , linear fall of i_{pa} continues as per (22) and is shown in Fig. 28, i_{pa} becomes negative. Switches S_{A2} and S_{A3} start conducting i_{pa} .

Using experimentally obtained datasets with the dynamic circuit equations obtained in Section III, transformer series inductance and device capacitances can be estimated. The estimated results are validated against actual measured quantity. Using (18), $\omega_p L_{lk}$ can be expressed as

$$\omega_p L_{lk} = \frac{V_{dc}}{\sqrt{i_{pa}^2(t_2) - i_{pa}^2(t_3)}}. \quad (25)$$

Again, from (20)

$$L_{lk} = \frac{V_{dc}}{i_{pa}(t_3)}(t_4 - t_3). \quad (26)$$

For different V_{dc} and load current i_a , the following parameters are experimentally obtained: $i_{pa}(t_2)$, $i_{pa}(t_3)$, $(t_3 - t_2)$, and

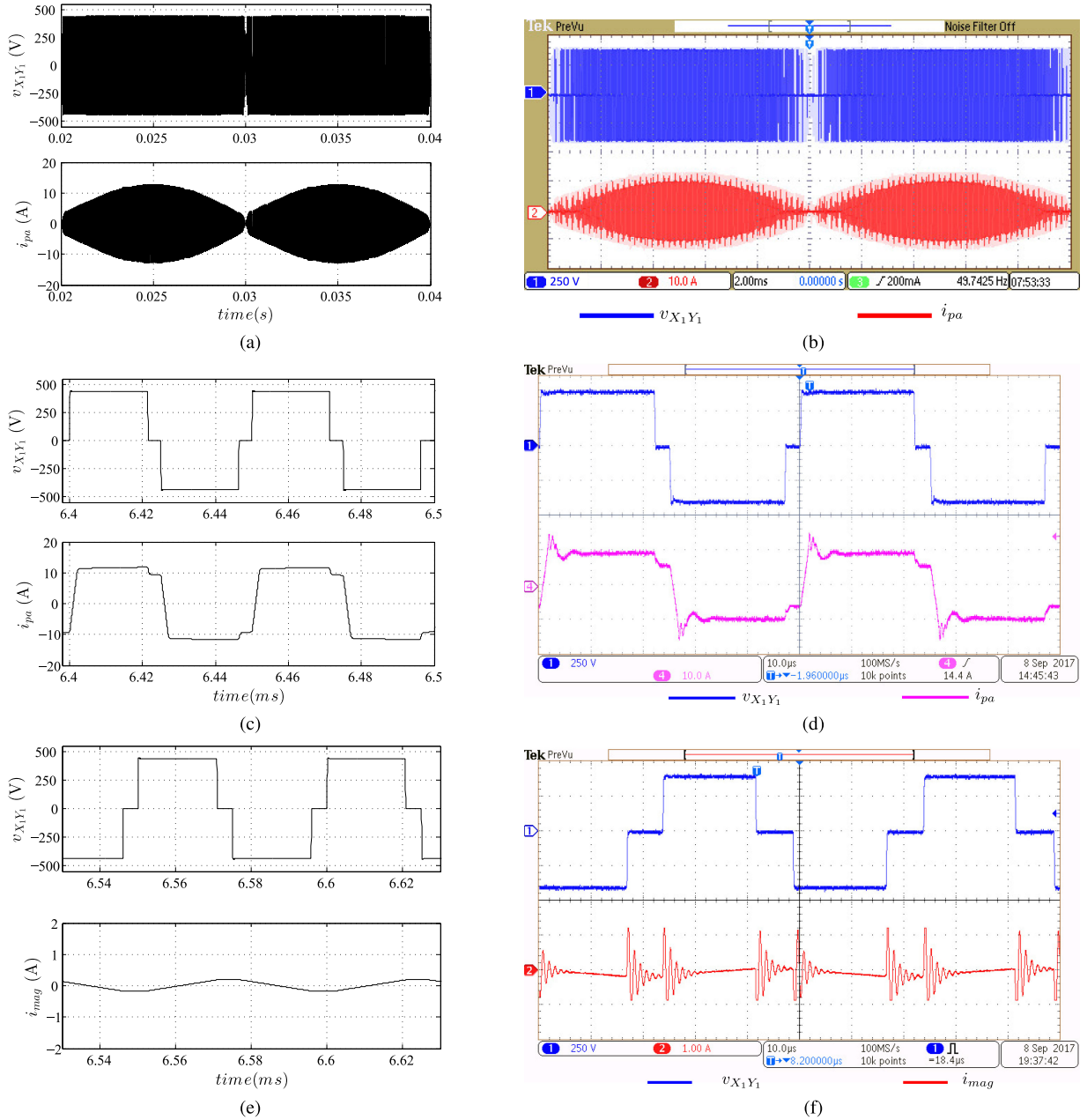


Fig. 24. Over a line cycle (HFT [CH1] input voltage (250 V/div.) and [CH2] input current (10 A/div.). Time scale 2 ms/div.). (a) Simulation. (b) Experimental. Over a switching cycle (HFT [CH1] input voltage (250 V/div.) and [CH4] input current (10 A/div.). Time scale 10 μ s/div.). (c) Simulation. (d) Experimental. HFT ([CH1] input voltage (250 V/div.) and [CH2] magnetizing current (1 A/div.). Time scale 10 μ s/div.). (e) Simulation. (f) Experimental.

$(t_4 - t_3)$. Using these values with (25) and 26, L_{lk} , ω_p , and C_T are estimated and tabulated in Table III. The measured value of L_{lk} and C_T are given in Table IV. The measured and estimated values are close. This verifies the theoretical analysis presented in Section III for zero to active state transition.

At the end of zero to active state transition ($t > t_5$), a high frequency ringing is observed in transformer current i_{pa} (see Fig. 27). Diode parasitic capacitance and transformer series inductance forms the resonating circuit resulting this high frequency ringing.

Fig. 29 shows the active to zero state transition. In Fig. 27, the transition is marked in blue-dotted circle. Before this transition, S_{A1} and S_{A4} were conducting and V_{dc} was applied across the transformer terminal X_1Y_1 (see Fig. 9). At t_0^- , gating signal of S_{A4} is withdrawn. After some time when gate-emitter voltage of S_{A4} , $v_{GE,S_{A4}}$ is almost zero (below device threshold voltage 5.5 V), the voltage across S_{A4} starts to rise (which is indicated by the fall in $v_{X_1Y_1}$). So, by the time device voltage starts rising, channel current through the device is zero. This indicates a ZVS turn OFF of S_{A4} . The delay in voltage rise across S_{A4} is due

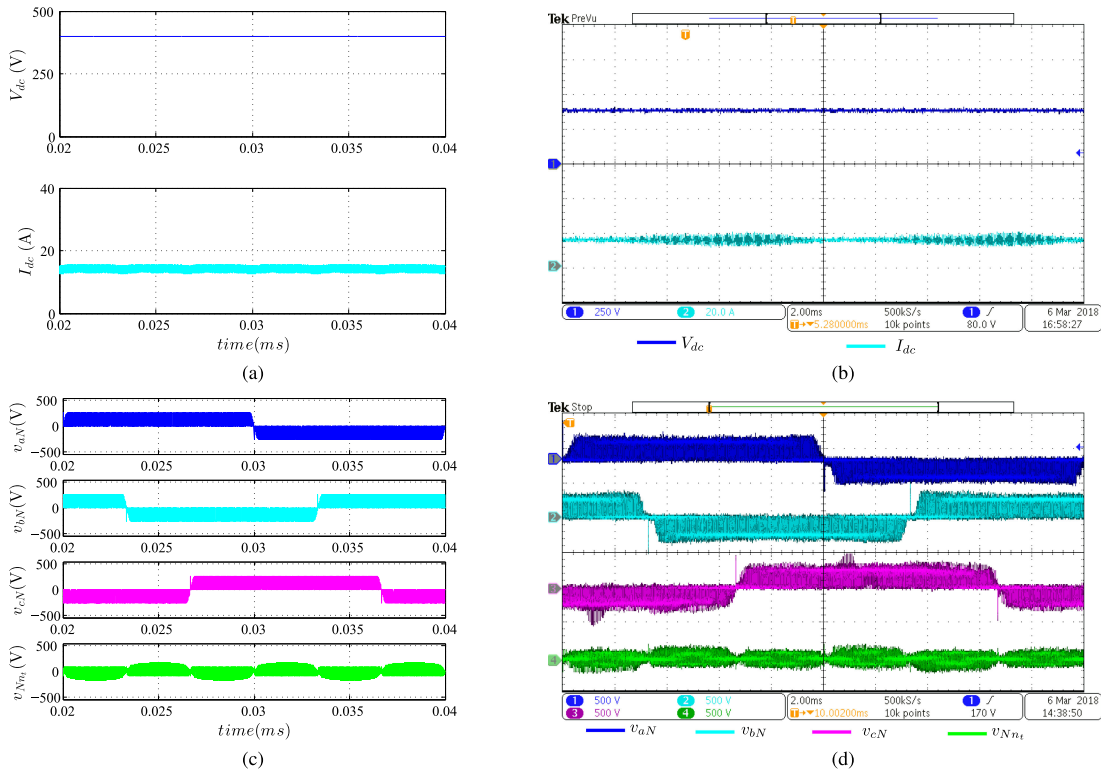


Fig. 25. DC input ([CH1] Input dc voltage (250 V/div.) and [CH2] Input dc current (20 A/div.). Time scale 2 ms/div.). (a) Simulation. (b) Experimental. Common mode voltage ([CH1] v_{aN} (500 V/div.), [CH2] v_{bN} (500 V/div.), [CH3] v_{cN} (500 V/div.), and [CH4] v_{Nn_t} (500 V/div.). Time scale 2 ms/div.). (c) Simulation. (d) Experimental.

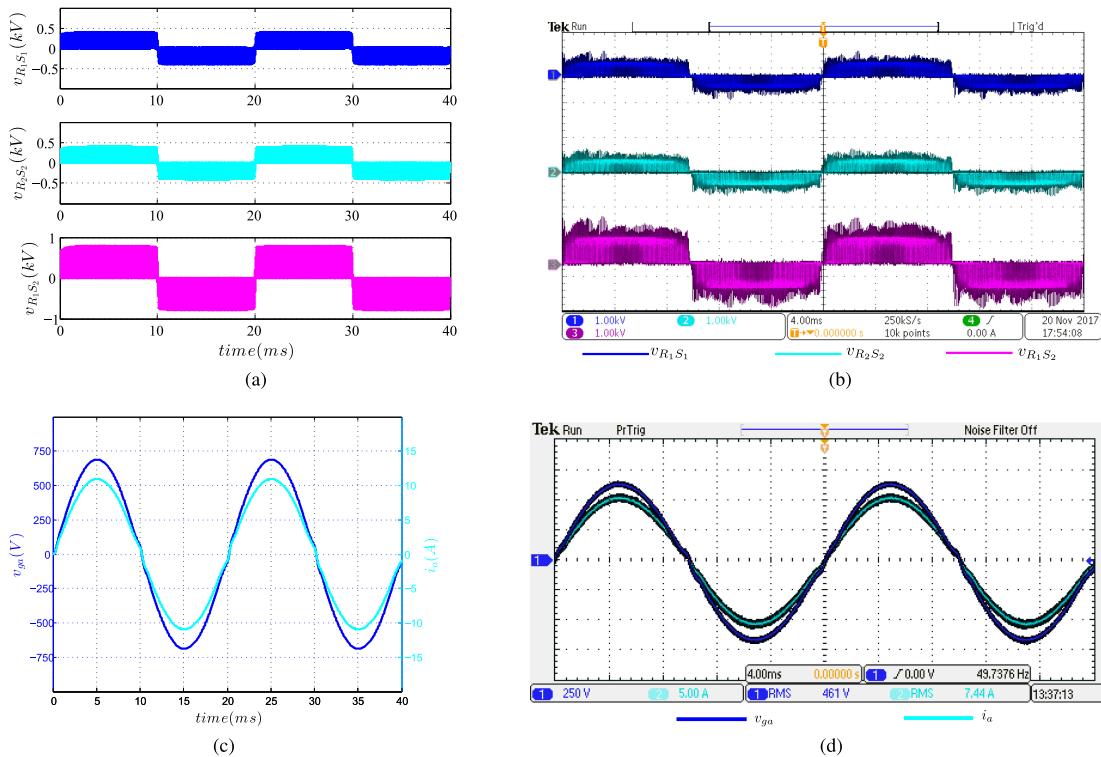


Fig. 26. Pole voltages of multilevel topology (see Fig. 3) ([CH1] pole voltage of module-1 (250V/div.), [CH2] pole voltage of module-2 (250V/div.), and [CH3] combined pole voltage of two modules (500V/div.). Time scale 4 ms/div.). (a) Simulation. (b) Experimental. Load voltage and current waveform of the multilevel topology corresponding to phase a . ([CH1] load voltage (250V/div.) and [CH3] load current (5A/div.). Time scale 4 ms/div.). (c) Simulation. (d) Experimental.

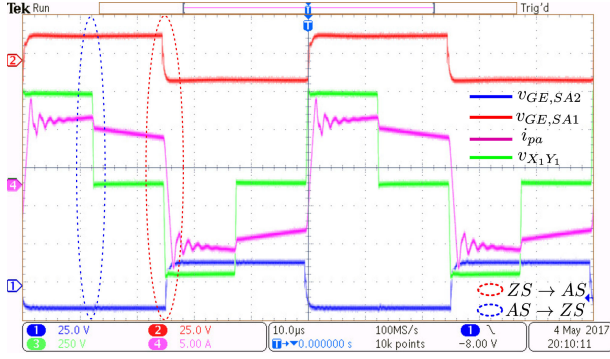


Fig. 27. [CH1] Gate-emitter voltage of S_{A2} (25 V/div.), [CH2] gate-emitter voltage of S_{A1} (25 V/div.), [CH3] HFT input voltage (250 V/div.), and [CH4] HFT input current (5 A/div). Time 10 μ s/div.

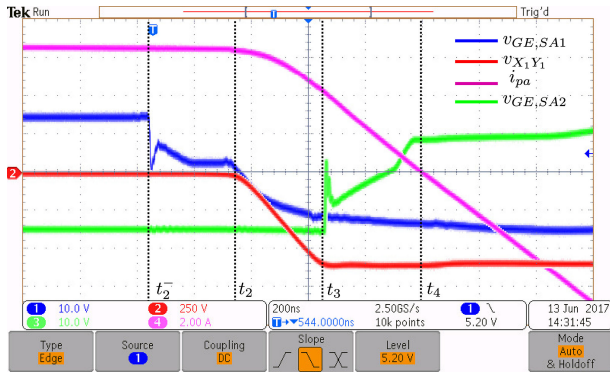


Fig. 28. Zero to active state transition: [CH1] gate-emitter voltage of S_{A1} (10 V/div.), [CH2] HFT input voltage (250 V/div.), [CH3] gate-emitter voltage of S_{A2} (10 V/div.), and [CH4] HFT input current (2 A/div). Time 200 ns/div.

to parasitic capacitance across the device as the voltage cannot change instantaneously across a capacitance. At t_1 , when the voltage across S_{A4} reaches 600 V, the voltage across S_{A3} is zero and the body diode of S_{A3} is forward biased. The transformer terminal X_1Y_1 is shorted through S_{A1} and body diode of S_{A3} . After some time of this instant, at t_1^+ , gating signal of S_{A3} is applied to turn it ON. As the body diode is in conduction, this ensures ZVS turn ON of S_{A3} .

V. LOSS ESTIMATION AND TARGET DESIGN

A. Analytical Estimation of Converter Power Loss

Fig. 30(a) shows the different stages of the converter module corresponding to phase a . Closed form expressions of power losses in active switches and diodes are given in this section. Phase b and phase c switches have similar loss expressions. Over a switching cycle in the dc bridge, S_{A1} – S_{A4} and the antiparallel diodes of S_{A3} and S_{A4} take part in conduction. The conduction losses of these switches and the antiparallel diodes are given in the following equations:

$$P_{C_{S_{A1}}} = P_{C_{S_{A2}}} = \frac{V_{CE_p} I_{pk}}{n\pi} + \frac{R_{CE_p} I_{pk}^2}{4n^2} \quad (27)$$

$$P_{C_{S_{A3}}} = P_{C_{S_{A4}}} = \frac{mV_{CE_p} I_{pk}}{4n} + \frac{mR_{CE_p} I_{pk}^2}{1.5\pi n^2} \quad (28)$$

$$P_{C_{D,S_{A3}}} = P_{C_{D,S_{A4}}} = \frac{V_{D_p} I_{pk}}{\pi n} + \frac{R_{D_p} I_{pk}^2}{4n^2} - \frac{mV_{D_p} I_{pk}}{4n} - \frac{mR_{D_p} I_{pk}^2}{1.5\pi n^2} \quad (29)$$

where V_{CE_p} and R_{CE_p} are ON state collector–emitter voltage drop and ON state resistance, respectively, of the IGBT. V_{D_p} and R_{D_p} are forward voltage drop and ON state resistance, respectively, of the antiparallel diodes of S_{A3} and S_{A4} .

The range of soft turn ON of S_{A1} – S_{A4} in one half of line cycle is indicated as $(\theta_1, \pi - \theta_1)$, as shown in Fig. 30(b). The shaded region indicates hard turn ON zone of the dc bridge over a line cycle for a given load. For a given dead time DT, the range of soft turn ON is estimated as follows. θ_1 of switch pair S_{A1} – S_{A2} can be obtained by solving the following equations simultaneously when $\omega_p L_{lk} I_s \geq nV_{dc}$:

$$\theta_{1_{S_{A1,2}}} = \frac{\pi I_s}{2I_{pk}}$$

$$I_s = \frac{nV_{dc}}{\omega_p L_{lk}} \sqrt{1 + (\omega_p t_{za2})^2}$$

$$t_{za2} = DT - \frac{1}{\omega_p} \sin^{-1} \left(\frac{nV_{dc}}{\omega_p L_{lk} I_s} \right). \quad (30)$$

θ_1 of switch pair S_{A3} – S_{A4} is expressed in as follows:

$$\theta_{1_{S_{A3,4}}} = \frac{n\pi}{I_{pk}} \left(\frac{V_{dc} C_s}{DT} \right). \quad (31)$$

The turn OFF of S_{A1} – S_{A4} are capacitor assisted soft transition. In this paper, the range of soft turn OFF is not derived. In loss calculation, the zone of soft turn ON is also considered as zone of soft turn OFF of the dc bridge. The switching loss of the dc bridge switches is expressed in the following equation:

$$P_{S_{S_{A_i}}} = \frac{2V_{dc} I_{pk}}{n\pi T_s} \left(\frac{E_{ON,R} + E_{OFF,R}}{V_{CC} I_C} \right) (1 - \cos \theta_{1_{S_{A_i}}}) \quad (32)$$

where $i \in 1, 2, 3, 4$. $E_{ON,R}$ and $E_{OFF,R}$ are the turn ON and turn OFF energy losses of the IGBT at rated condition— V_{CC} , I_C , respectively. Conduction losses of Q_{a1} – Q_{a2} and D_{a1} – D_{a4} are given in the following equation:

$$P_{C_{Q_{a1}}} = P_{C_{Q_{a2}}} = \frac{V_{CE_s} I_{pk}}{\pi} + \frac{R_{CE_s} I_{pk}^2}{4} \quad (33)$$

$$P_{C_{D_{a_i}}} = \frac{V_{D_s} I_{pk}}{2\pi} + \frac{R_{D_s} I_{pk}^2}{8} \quad (34)$$

where V_{CE_s} and R_{CE_s} are ON state collector–emitter voltage drop and ON state resistance, respectively, of the IGBT. V_{D_s} and R_{D_s} are forward voltage drop and ON state resistance of the diode, respectively. Copper loss of the HFT is given as

$$P_{Cu,HFT} = R_{AC,p} I_{ap}^2 + (R_{AC,s_1} + R_{AC,s_2}) I_{as}^2. \quad (35)$$

$I_{ap} = \frac{I_{pk}}{n\sqrt{2}}$ and $I_{as} = \frac{I_{pk}}{2}$ are the RMS currents of primary and secondary windings of the HFT, respectively. $R_{AC,p}$ and R_{AC,s_1} and R_{AC,s_2} are the primary and secondary winding resistances of the HFT at the operating frequency.

TABLE III
ESTIMATED L_{lk} , ω_p , AND C_T FROM EXPERIMENTAL DATA

Experimentally observed					Estimated				
V_{dc} (V)	$i_{pa}(t_2)$ (A)	$i_{pa}(t_3)$ (A)	$(t_3 - t_2)$ (ns)	$(t_4 - t_3)$ (ns)	$\omega_p L_{lk}(\Omega)$	$\omega_p(\text{rad/s})$	$L_{lk}(\mu\text{H})$	$C_T(\text{nF})$	
200	1.85	1.05	330	250	131	2757435	47.6	2.76	
300	3.2	2.3	280	360	134	2871592	46.9	2.58	
400	4	2.5	320	330	128	2426184	52.8	3.2	
500	6.1	4.5	280	440	121	2483401	48.9	3.3	
600	6.4	4.4	300	360	129	2629803	49	2.94	

TABLE IV
MEASURED L_{lk} AND C_T

$L_{lk}(\mu\text{H})$	$C_T(\text{nF})$
53	3.06

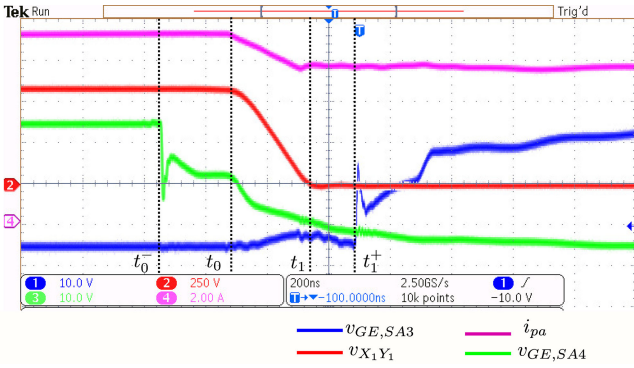


Fig. 29. Active to zero state switching transition: [CH1] gate-emitter voltage of S_{A3} (10 V/div.), [CH2] HFT input voltage (250 V/div.), [CH3] gate-emitter voltage of S_{A4} (10 V/div.), and [CH4] HFT input current (2 A/div.). Time 200 ns/div.

B. Experimentally Measured Converter Power Loss

In Fig. 31(a), experimentally obtained converter efficiency is plotted against the variation of output power from 1 to 5.3 kW. The dc voltage is kept fixed at 420 V. The maximum efficiency of 90.6% is observed at 3 kW. Fig. 31(b) presents the variation of power losses of different stages of the converter with output power variation and these losses are obtained experimentally. The dc bridge has maximum power loss throughout the entire output power range. With increase in output power level, a significant reduction (2.5%) of dc bridge power loss is observed. The switching loss contributes major portion of the dc bridge power loss. With the increase of output power level, the line current peak I_{pk} increases. As shown in (30) and (31), θ_1 decreases with the increase of I_{pk} , results in increase of soft turn ON range ($\theta_1, \pi - \theta_1$) over one half of the line cycle. The ac bridge has low (1.51%) and flat loss profile throughout the output power range. The flat loss profile indicates that major loss in the ac bridge is dominated by conduction loss of the diodes and active switches. The line frequency switching of the ac-side active switches incurring negligible switching loss results in low loss in the ac bridge. In Fig. 32(a), power

loss distribution of the converter is shown as bar diagram at 4.64-kW output power. The analytically estimated power losses at the different stages of the converter are matched with the experimentally obtained losses. The dc bridge contributes around 260 W out of 500 W of total loss. In Fig. 32(b), a pie chart is presented showing percentage loss contribution of the different stages of the converter at 4.64-kW output power. The dc bridge incurs more than 50% of total power loss, whereas line frequency switched ac bridge contributes only 17%. The benefit of the proposed modulation strategy with line frequency switched ac side compared to conventional high frequency hard switching based ac-side modulation strategy is clearly seen. Fig. 33 presents the dc bridge losses over a variation of output power 3–5 kW. The figure shows that the analytically estimated dc bridge losses are closely matched with the experimentally obtained values. The figure also presents the losses corresponding to completely hard-switched dc-side converter. Soft switching results in 1.5 times reduction of the losses in the dc bridge of the proposed 3ϕ HFL inverter and thus improving the overall converter efficiency.

C. Converter Design for Target Application

The proposed topology is targeted for grid integration of utility scale photovoltaic systems with hundreds of kW to few MW power level. A sample design of 200-kW system with 800-V dc input and 415-V, 50-Hz line output is discussed. The switching frequency of the dc bridge converter is 20 kHz. In the design, the following parameters are considered as base quantities: $V_{base} = 415$, $P_{base} = 200$ kW, $I_{base} = \frac{P_{base}}{\sqrt{3}V_{base}} = 278$ A, and $Z_{base} = \frac{V_{base}}{\sqrt{3}I_{base}} = 0.86 \Omega$. The line choke is designed as 5% of the base impedance. Using (24), peak value (V_{pk}) of the fundamental component of the converter phase voltage output is estimated to be 338.4 V. The peak converter output current I_{pk} is estimated as 394 A. Considering the maximum modulation index (m_{max}) 0.85, the transformer primary to secondary turns ratio $n = \frac{m_{max} V_{dc}}{V_{pk}} = 2$. Due to center tap winding structure of HFT, the blocking voltage of the ac-side devices and diodes is $\frac{2V_{dc}}{n} = 800$ V and the current rating should be 394 A. SEMIKRON IGBT module SKM450GB12T4 with voltage and current ratings of 1200 V and 450 A, respectively, is selected for ac-side converter active switches. IXYS 1200-V, 450-A fast

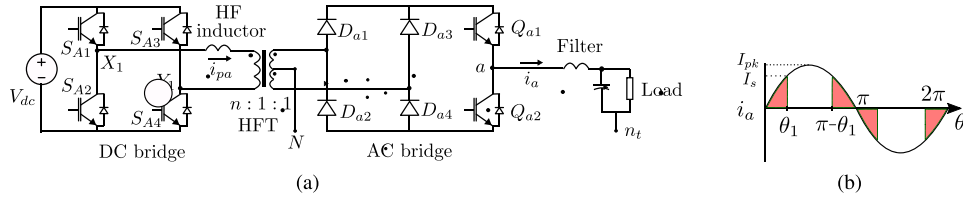


Fig. 30. (a) Module corresponding to phase a of the 3ϕ HFL topology. (b) Shaded area showing hard-switching region of dc-side switches over a line cycle.

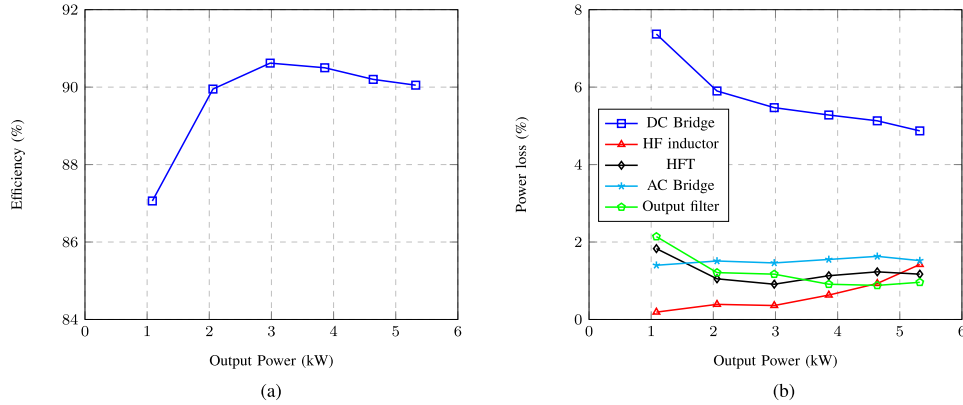


Fig. 31. (a) Efficiency of the proposed 3ϕ HFL inverter. (b) Power loss at different stages of 3ϕ HFL inverter.

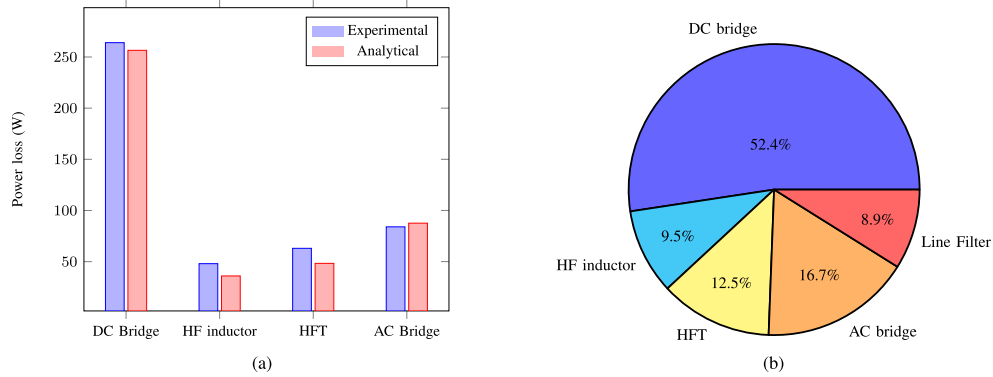


Fig. 32. (a) Power loss break down at 4.64-kW output power obtained experimentally and analytically. (b) Percentage loss distribution shown at 4.64-kW output power obtained experimentally.

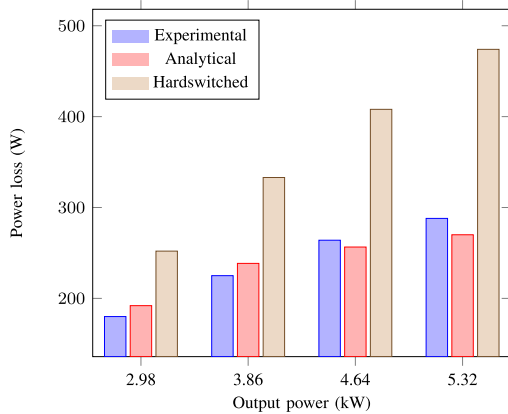


Fig. 33. DC-side HF H bridge power loss: experimental, analytical, and complete hard switched.

recovery diode module MEO 450-12 DA is considered for the ac-side diode bridge. The three winding HFT primary current rating $\frac{I_{pk}}{\sqrt{2n}} = 138.6$ A and the secondary winding current rating is $\frac{I_{pk}}{2} = 197$ A. The base impedance in HFT primary is given by $Z_{base,p} = n^2 Z_{base} = 3.48 \Omega$. A high-frequency inductor with impedance 30% of $Z_{base,p}$ is designed and connected in series with the HFT primary to increase the ZVS turn ON range of the dc-side bridge devices. Required voltage blocking and current-carrying capabilities are 800 V and 196 A, respectively. SEMIKRON IGBT half bridge module SKM400GB125D with voltage rating 1200 V and current rating 300 A is selected for dc-side active switches. Table V summarizes the target design of 200-kW converter. The analytically estimated converter efficiency at the operating point is 95.6%.

TABLE V
200-kW TARGET DESIGN PARAMETER

Parameter	Values
Output Power, $P_{3\phi}$ (kW)	200
DC input, V_{dc} (V)	800
Grid line voltage (V)	415
Grid frequency (Hz)	50
Switching frequency (kHz)	20
Modulation index (m)	0.85
HFT primary peak current (A)	196
DC side device blocking voltage (V)	800
DC side IGBT	SKM400GB125D
Series inductor with HFT (μH)	8.3
HFT turns ratio (n)	2
AC side device blocking voltage (V)	800
AC side peak current (A)	394
Diode of bridge rectifier	MEO 450-12 DA
AC side IGBT	SKM450GB12T4
Line filter (μH)	137

VI. CONCLUSION

In this paper, a single-stage unidirectional 3ϕ high-frequency link inverter topology along with its multilevel configuration is proposed. The proposed topologies have the following features.

- 1) The dc-side converter is soft switched (ZVS) for most part of the line cycle without additional snubber circuit.
- 2) High-frequency magnetic isolation improves the system power density and reduces weight and cost.
- 3) The ac-side active switches are line frequency switched incurring negligible switching loss.
- 4) High voltage blocking slow switches can be used in line frequency switched ac-side converter to generate high-voltage ac output.
- 5) The cascaded structure proposed in this paper is targeted for direct medium-voltage grid integration.
- 6) In this scheme, the grid end line filter will have high voltage and low current rating resulting in smaller size with reduced conduction loss.

The circuit operation of the proposed converters are discussed in detail considering nonidealities, such as transformer leakage inductance and device capacitances. The presented simulation and experimental results verify the operation principle and advantages of the proposed converter topologies. The proposed topologies support unidirectional dc to ac power flow and primarily targeted for grid integration of utility scale photovoltaic sources.

APPENDIX

REACTIVE COMPENSATION OF LINE FILTER DROP

The proposed converter in Fig. 2 supports only instantaneous unidirectional power flow from dc to ac side due to presence of diode bridge rectifier.

In the proposed solution, due to line filter reactor, grid side power factor will not be unity. For UPF operation, a solu-

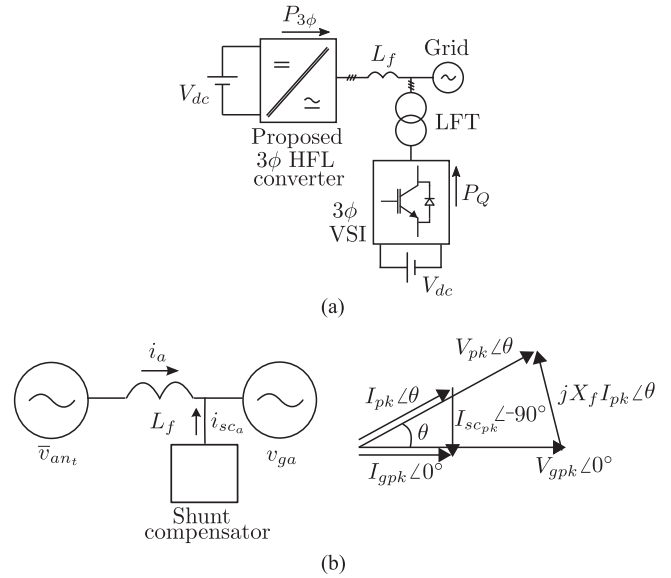


Fig. 34. (a) Scheme to support reactive power. (b) Equivalent circuit and phasor diagram.

tion is shown in Fig. 34(a) to compensate the reactive drop. A 3ϕ VSI is connected to the common coupling point through a small line frequency transformer. This 3ϕ VSI supports the reactive power compensating the line filter drop. The reactive power supplied by shunt compensator is estimated as follows. The equivalent circuit and the phasor diagram are shown in Fig. 34(b). The active power supplied to the grid at UPF is given as

$$P_{3\phi} = 1.5V_{gpk}I_{gpk} = 1.5V_{pk}I_{pk}. \quad (36)$$

From the phasor diagram

$$\begin{aligned} V_{pk} \angle \theta &= V_{gpk} \angle 0^\circ + j(2\pi f L_f) I_{gpk} \angle 0^\circ \\ I_{pk} \angle \theta &= I_{gpk} \angle 0^\circ - I_{scpk} \angle 90^\circ \end{aligned} \quad (37)$$

where L_f is the combined line and filter inductance and I_{shpk} is the peak current supplied by the shunt compensator. Considering $V_{gpk} = 1$ p.u. and $I_{gpk} = 1$ p.u. and line inductive reactance 0.05 p.u. using (36) and (37), the power rating of the 3ϕ shunt compensator can be shown as 4.5% of $P_{3\phi}$.

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Anirban Pal (S'17) received the B.E. degree from the Indian Institute of Engineering Science and Technology, Howrah, India, in 2010, and the M.E. degree from the Indian Institute of Science, Bengaluru, India, in 2015, both in electrical engineering. He is currently working toward the Ph.D. degree at the Department of Electrical Engineering, Indian Institute of Science.

From 2010 to 2013, he worked as an Assistant Manager with the National Thermal Power Corporation, Ltd. His research interests include high-frequency-link single-stage converters, dual active bridge based converters, resonant converters, soft-switching techniques, and design of high-frequency magnetics.



Kaushik Basu (S'07–M'13–SM'17) received the B.E. degree from the Bengal Engineering and Science University, Shibpur, India, in 2003, the M.S. degree in electrical engineering from the Indian Institute of Science, Bengaluru, India, in 2005, and the Ph.D. degree in electrical engineering from the University of Minnesota, Minneapolis, MN, USA, in 2012.

He was a Design Engineer with the Cold Watt India in 2006 and an Electronics and Control Engineer with the Dynapower Corporation, South Burlington, VT, USA, from 2013 to 2015. He is currently an Assistant Professor with the Department of Electrical Engineering, Indian Institute of Science. He has been an author and coauthor of several technical papers published in peer-reviewed journals and conferences. His research interests include various aspects of the general area of power electronics.

Dr. Basu is the Founding Chair of the IEEE Power Electronics Society and IEEE Industrial Electronics Society Bangalore Chapter.