This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2889795, IEEE Transactions on Power Electronics

A Soft-switched High Frequency link Single-Stage Three-Phase Inverter for Grid Integration of Utility Scale Renewables

Anirban Pal, *Student Member, IEEE,* Kaushik Basu, *Senior Member, IEEE*

***Abstract*—A novel single-stage high frequency link three-phase (3ϕ) inverter along with a modulation strategy is presented in this paper. The topology is targeted for grid integration of utility scale renewable and alternative energy sources like solar, fuel cell and wind, where the power flow is unidirectional (from DC to AC). The primary side converter has 3ϕ voltage source inverter (VSI) structure along with an additional half-bridge leg. Sinusoidal pulse width modulation is implemented in the primary side converter. The three legs of the primary side VSI are zero voltage switched (ZVS) for most part of the line cycle. The additional half bridge leg is zero voltage switched (ZVS) over the complete line cycle. The active switches in secondary side converter are line frequency switched and thus results in negligible switching loss. The converter switching process is described in detail to show the soft-switching of the primary side converter using the device capacitances and leakage inductances of the high frequency transformers. The high frequency transformer galvanic isolation results in high power density. A 4 kW laboratory scale hardware prototype is built and tested with the proposed modulation strategy. The experimental results are presented to verify the converter operation.**

***Index Terms*—Single-stage, high frequency link, DC-AC converter, pulse-width modulation, zero-voltage-switching, line frequency unfolding.**

I. Introduction

WITH the depletion of fossil fuel reserve and the present global warming scenario, power utilities all over the world are focusing on renewable and alternative energy source based power generation. In 2016 globally, total installed renewable power capacity is 921 GW out of which 303 GW is solar capacity and wind power is 487 GW [1]. Commercially available power electronic converters to integrate utility scale (few hundreds of kW to few MW) renewable energy systems to AC transmission grid (Fig. 1a and Fig. 1b) use a three-phase (3ϕ) voltage source inverter (VSI) in case of PV [2], [3] or back to back connected 3ϕ VSIs in case of wind [4], [5]. The VSI output is connected to the LVAC (440-480V) grid through line filters and a 3ϕ line frequency transformer (LFT). Beside the voltage matching the LFT ensures safety by providing galvanic isolation [6], avoiding DC current injection into the grid [7] and also helps to reduce leakage current to conform with the PV system standards such as VDE 0126-1-1 [8]. The LFTs are heavy, bulky and expensive.

High frequency link (HFL) based isolated converter topologies as an alternative solution to LFT based state of the art converters have been studied extensively in recent years. The high frequency transformer (HFT) based solution comes with some attractive features like high power density, small and compact footprint, low system cost. Most popular HFL based solutions are the two-stage HFL DC-AC converter topologies [9]–[13]. In these topologies, an isolated DC-DC stage is connected to a VSI through a DC bus capacitor (Fig. 1c). The intermediate DC bus is voltage stiff. The VSI is high frequency hard-switched and the DC electrolytic capacitor has long term reliability issue [14]. The VSI can be soft-switched by employing additional switches and resonating inductors and capacitors in the DC link. The resonant DC link concept is first introduced in [15] where a LC network is used to produce oscillatory DC link voltage and the inverter is switched when the DC link voltage becomes zero. The inverter switches suffer from high voltage stress (2-3 times input DC voltage) and discrete pulse modulation (sigma-delta) strategy produces significant undesirable sub-harmonics at the output, [15], [16]. In quasi-resonant DC link inverter (QRDCLI), the resonating circuit comes in operation only during the switching transitions of the inverter to make the link voltage zero. The first QRDCLI topology was proposed in [17], where the resonating circuit has four active switches. Subsequent works [18]–[22], tried to address the problem of high voltage and current stress experienced by the additional switches in the resonant cell and to reduce the number of the active devices. [19], [20], [23] reduced the frequency of the operations of the resonant cell, by reducing the number of switching transitions through modification of the PWM strategies of the inverter. This approach usually results in low quality output voltage waveform when compared with standard conventional space vector PWM. In general, the QRDCLI uses at least one active switch in series with the DC voltage source to disconnect the supply during resonant operation. The RMS and peak current rating of this switch is significantly high compared to the inverter switches. Though soft-switched, this switch contributes significantly to the conduction loss. This restricts the use of QRDCLI in high power application. Additionally, control complexity and high current stress of resonant circuit

Manuscript received June 5, 2018; revised August 20, 2018; revised October 15, 2018; revised November 23, 2018; accepted December 17, 2018. This work was supported by the Central Power research Institute (CPRI), Ministry of Power, Government of India under the project titled "Power conversion, control, and protection technologies for microgrid". This work was also supported by Department of Science and Technology, Government of India under the project titled "Development of an advanced System-On-Chip (SoC) based embedded controller for power electronic converters". (*Corresponding author : Anirban Pal*).

The authors are with the Department of Electrical Engineering, Indian Institute of Science, Bangalore 560012, India. (e-mail: anirbanp@iisc.ac.in; kbasu@iisc.ac.in).

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2889795, IEEE Transactions on Power Electronics

are two major limitations of QRDCLI.

In literature single-stage rectifier type HFL DC-AC converters (RHFL) are widely discussed where inter-stage DC capacitor is removed (Fig. 1d) and the DC bus is pulsating [24]–[27].

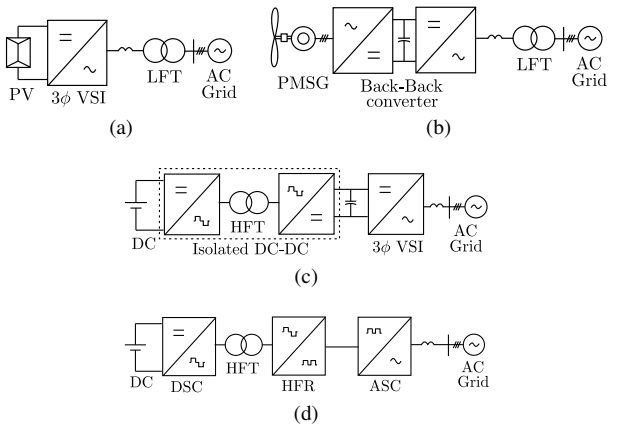


Fig. 1. State of the art grid integration of (a) PV system and (b) wind energy. (c) Multi-stage HFL DC-AC topology, (d) Single-stage RHFL topology

In applications like grid integration of PV, fuel cell and PMSG based wind generation, the power flow is unidirectional (from source to grid) [28]. Several unidirectional RHFL topologies have been proposed in literature [14], [29]–[32]. In these topologies, uncontrolled diodes are used in the high frequency rectifier (HFR in Fig. 1d). In [14], [29]–[31] hybrid modulation (HM) strategy is used which results in high frequency switching of the AC side converter (ASC) over only one third of the line cycle, results in significant reduction of switching loss in ASC. In [32], the ASC is completely line frequency switched. The DSC with six half-bridge legs are soft-switched only for some part of the line cycle. The converter supports only UPF operation.

In this paper a novel topology is proposed where the DSC has a 3ϕ VSI structure connected to the DC source V_{dc} along with one additional half bridge leg as shown in Fig. 2a. The HFR has three diode bridges and the ASC has three half-bridge legs. The proposed topology with suggested modulation scheme has following features.

- Sinusoidal PWM is implemented in DC side converter.
- The modulation strategy results in high quality output waveform along with active power transfer at UPF.
- The DSC leg S_1-S_2 is zero voltage switched (ZVS) over a complete line cycle where as other three legs are zero voltage (ZVS) switched for most part of a line cycle.
- The ASC half-bridge legs are line frequency switched resulting in negligible switching losses.
- The high frequency galvanic isolation provides a compact high power density converter solution.

A part of this work was presented in [33].

The paper is organised as follows. Section II describes the modulation strategy of the converter. In section III, the converter switching process is described in detail. Experimental results are presented in section IV to validate the theoretical analysis. The converter power loss and efficiency are presented in section V.

II. Circuit Configuration and Modulation Technique

The proposed topology is shown in Fig. 2a. The primary side of the converter has a two level three-phase (3ϕ) voltage source inverter (VSI) structure connected to the DC source V_{dc} along with one additional half-bridge leg ($S_1 - S_2$). For each phase, a three winding high frequency transformer (HFT) with turns ratio ($n:1:1$) is employed. The primary windings of the 3ϕ HFTs are star connected and the neutral point (N) is connected to the pole of leg S_1-S_2. In each phase, the staring end of one secondary winding is connected to the finishing end of the other identical secondary winding. All these points are connected to form a common point (n_t). In the secondary side, each phase of the converter has a diode bridge along with a half-bridge leg. The converter is connected to a balanced 3ϕ voltage source ($v_{a'n_g}$, $v_{b'n_g}$, $v_{c'n_g}$) with angular frequency $\omega_o = \dfrac{2\pi}{T_0}$ and peak V_{gpk} through filter inductors (L_f). All the active switches can be realized with IGBT or MOSFET with a body diode. In the following discussion, IGBTs are considered for implementation. The directions of the currents shown in Fig. 2a are considered to be positive in rest of the paper.

To generate balanced adjustable magnitude 3ϕ AC from the input DC, the modulation signals ($m^*_{r_j}$) are given in (1). Where, m is the modulation index and is a positive fraction. $j \in \{a, b, c\}$ and $M_a = 0$, $M_b = +1$ and $M_c = -1$.

$$m^*_{r_j} = m\left|\sin\left(\omega_o t + M_j\frac{2\pi}{3}\right)\right| \tag{1}$$

Due to presence of diode bridge, the instantaneous power flow is unidirectional (from DC to AC). The carrier frequency average of the synthesized pole voltages ($\overline{v}_{jn_t}$) should be in phase with the fundamental component of line currents ($i_{a,b,c}$) (Fig. 2a). So, the reference signals ($m^*_{r_j}$) are in phase with fundamental component of the line currents, i_j. The modulation is implemented in the primary-side converter. The eight switches in the DC side converter are modulated following the principle of phase-shifted full-bridge (PSFB) DC-DC converter. A high frequency square wave signal F with time period T_s and duty ratio 0.5 is considered, Fig. 2b. T_s is also the period of the HFT flux balance cycle. A unipolar saw-tooth carrier with unity peak and period of $\frac{T_s}{2}$ is considered and is aligned with F. Each half-bridge leg in the primary is complementary switched with 50% duty ratio. F is used as the gating pulse (G_{S_1}) of S_1. The gating pulses ($G_{S_{X1}}$) of the top switches of each VSI leg, S_{X1} ($X \in \{A, B, C\}$) are time shifted with respect to S_1. For example, $G_{S_{A1}}$ is time delayed by $\dfrac{m^*_{r_a}T_s}{2}$ with respect to G_{S_1} or F, Fig. 2b. So, a sine pulse width modulated (PWM) quasi square wave with levels $\pm V_{dc}$ and zero and period T_s is applied across the transformer primary (v_{AN} in Fig. 2b). The high frequency quasi-square wave is rectified by the secondary diode bridges D_{j1-4}. When $i_j > 0$, Q_{j1} is turned ON and the high frequency rectification happens with the top diodes D_{j1}, D_{j3}. Q_{j2}, $D_{j2,4}$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2889795, IEEE Transactions on Power Electronics

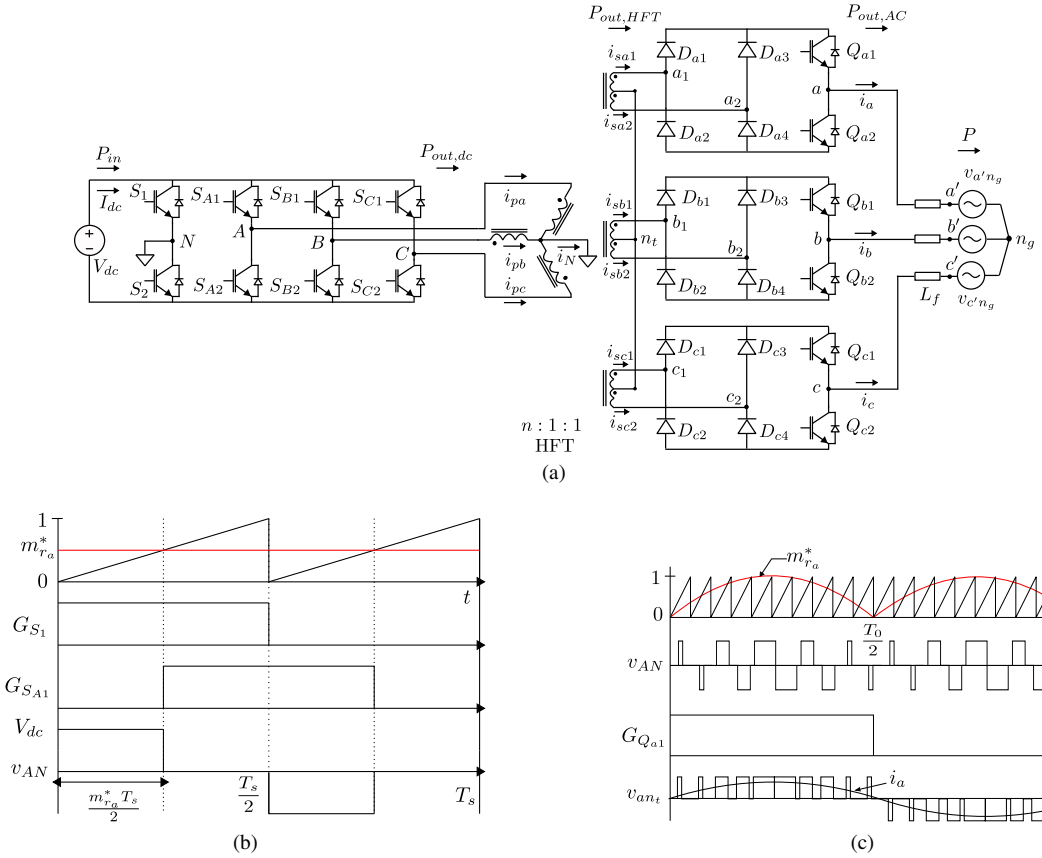


Fig. 2. (a) Proposed 3ϕ HFL DC-AC converter. Modulation strategy of the converter shown- (b) over a switching cycle, (c) over a line cycle.

take part in conduction when $i_j < 0$. So, Q_{j1} and Q_{j2} are switched at line frequency $\left(\frac{1}{T_0}\right)$ in complementary fashion, Fig.2c. This results in generation of unipolar sine PWM pole voltages v_{jn_t} with voltage levels 0 and $\pm\left(\frac{V_{dc}}{n}\right)$ with respect to n_t (see v_{an_t} in Fig. 2c). The average 3ϕ pole voltages with respect to HFT secondary neutral n_t are given in (2).

$$\overline{v}_{jn_t} = \frac{mV_{dc}}{n}\sin\left(\omega_o t + M_j\frac{2\pi}{3}\right) \tag{2}$$

For a desired average pole voltage peak, V_{pk}, the modulation index $m = \left(\frac{nV_{pk}}{V_{dc}}\right)$. As the AC ports are connected to a balanced 3ϕ system with floating neutral (n_g), the average pole voltages $\overline{v}_{jn_t}$ are equal to output voltages $\overline{v}_{jn_g}$.

III. Converter Switching Process

In this section, the circuit operation of the converter is discussed in detail over one switching cycle (T_s). The presented analysis shows that the half-bridge leg $S_1 - S_2$ is completely soft-switched and each of the legs of the VSI, $S_{X1} - S_{X2}$ ($X \in \{A, B, C\}$), are soft-switched for most part of the line cycle with the help of device parasitic capacitances (C_s) and transformer leakage and additional series inductance (L_{lk}). The secondary side active switch pairs $Q_{j1} - Q_{j2}$ are line frequency switched incurring negligible switching loss. For ease of analysis, slowly varying line currents $i_{a,b,c}$ are considered as constant current sources with magnitude $I_{a,b,c}$ over a switching cycle T_s. The switching process of the converter is described when $i_a = I_a$ and $i_b = I_b$ but $i_c = -I_c$ and $I_c > I_a > I_b$. In other regions similar switching process will be followed. Switching waveforms over T_s are shown in Fig. 3. The circuit dynamics in one half of the switching cycle (T_s) is divided into ten modes (1-10), other half evolves in an identical fashion.

A. Mode 1 ($t_0 < t < t_1$)

In this mode in the primary side converter, S_1 and S_{X2} ($X \in \{A, B, C\}$) are conducting (Fig. 4). The equivalent circuit is shown in Fig. 5a. Negative voltage $-V_{dc}$ is applied across HFT primary terminals AN, BN and CN. The HFT primary currents, $i_{pj} = -\frac{I_j}{n}$ where ($j \in \{a, b, c\}$) as shown in Fig. 3. The voltage polarity and direction of currents indicate active power flow from DC to AC side in all three phases (all three phases are in active state). In secondary D_{a3}, Q_{a1}; D_{b3}, Q_{b1} and D_{c2}, Q_{c2} are conducting.

B. Mode 2 ($t_1 < t < t_2$)

At t_1, S_{B2} is turned OFF (Fig. 6). Active to zero state transition of phase b starts at t_1. Due to device capacitance (C_s), the voltage across S_{B2} can not rise immediately. Voltage starts rising after channel current falls below zero resulting zero voltage turn OFF (ZVS) of S_{B2}. b phase primary current $-\frac{I_b}{n}$ starts charging the capacitance across S_{B2} and discharging the capacitance across S_{B1}. Equivalent circuit in this mode

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2889795, IEEE Transactions on Power Electronics

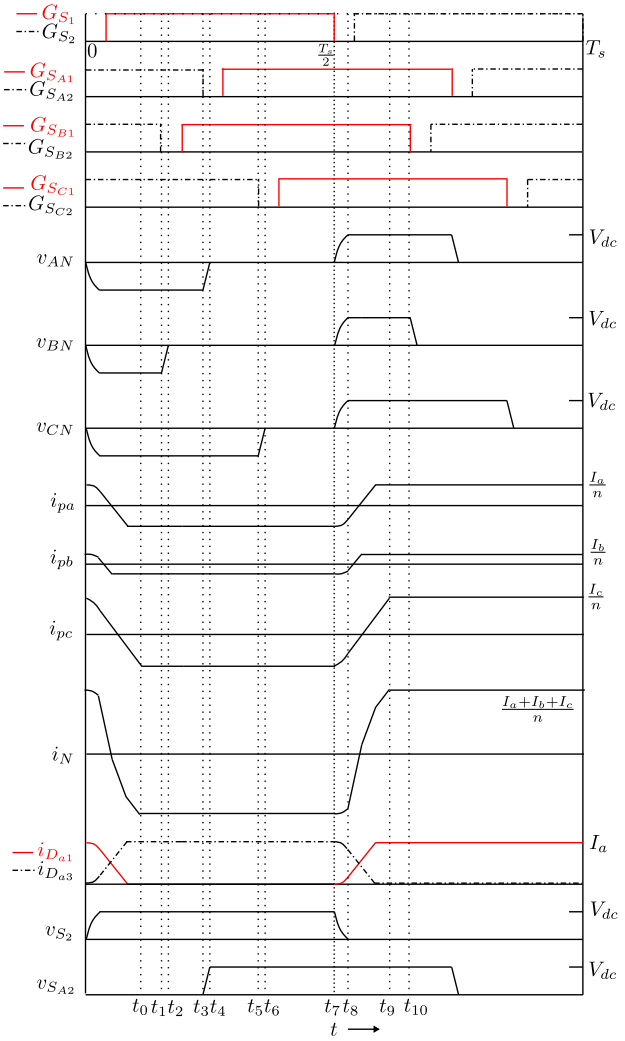


Fig. 3. Switching waveforms over T_s

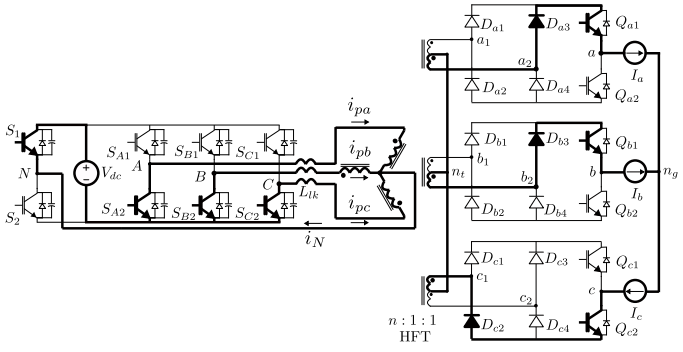


Fig. 4. Simplified circuit diagram in *Mode 1* ($t_0 < t < t_1$ in Fig. 3)

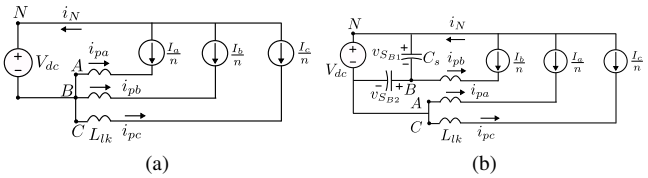


Fig. 5. (a) Equivalent circuit diagram in *Mode 1*, (b) Equivalent circuit diagram in *Mode 2*.

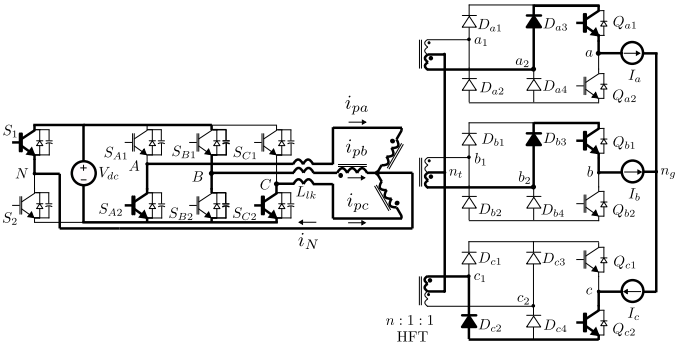


Fig. 6. Simplified circuit diagram in *Mode 2* ($t_1 < t < t_2$ in Fig. 3)

is shown in Fig. 5b. From the equivalent circuit it can be shown that the voltages across S_{B1}, $v_{S_{B1}}$ falls as per (3).

$$v_{S_{B1}}(t) = V_{dc} - \frac{I_b}{2nC_s}(t - t_1) \tag{3}$$

Phase a and c remain in active state during this duration.

C. Mode 3 ($t_2 < t < t_3$)

At t_2, the capacitor across S_{B1} is completely discharged. The anti-parallel diode of S_{B1} starts conducting (Fig. 7). After t_2, S_{B2} blocks V_{dc}. The duration $t_{az_b} = (t_2 - t_1)$ is given in (4).

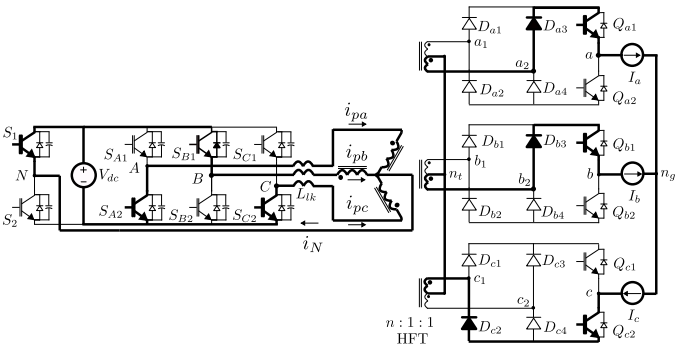


Fig. 7. Simplified circuit diagram in *Mode 3* ($t_2 < t < t_3$ in Fig. 3)

$$t_{az_b} = \frac{2nC_sV_{dc}}{I_b} \tag{4}$$

The primary of b phase HFT is shorted through S_1 and anti-parallel diode of S_{B1}. To achieve ZVS transition, S_{B1} is turned ON in this mode (dead time between S_{B2} and S_{B1} must be greater than t_{az_b}). Equivalent circuit in this mode is shown in Fig. 8a. Phase b is in zero state i.e no active power is transferred from DC to AC side in phase b.

D. Mode 4-6

Similar active to zero state transitions occur in phase a in *Mode 4* ($t_3 < t < t_4$) with ZVS turn OFF of S_{A2} and in phase c in *Mode 6* ($t_5 < t < t_6$) with ZVS turn OFF of S_{C2}. In *Mode 5* ($t_4 < t < t_5$), phase a, b are in zero states and phase c is in active state. S_{A1} is turned ON to ensure ZVS when its anti-parallel diode is conducting.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2889795, IEEE Transactions on Power Electronics

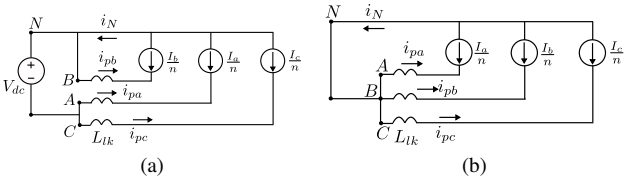


Fig. 8. (a) Equivalent circuit diagram in *Mode 3*, (b) Equivalent circuit diagram in *Mode 7*.

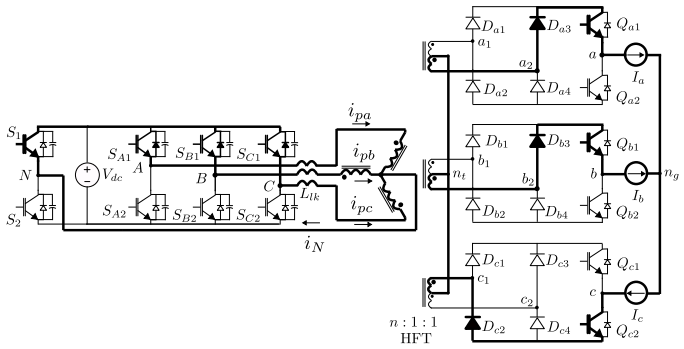


Fig. 9. Simplified circuit diagram in *Mode 7* ($t_6 < t < t_7$ in Fig. 3)

E. Mode 7 ($t_6 < t < t_7$)

In this mode, all three phases are in zero state. HFT primary terminals AN, BN and CN are shorted through S_1 and the anti-parallel diodes of S_{X1} (Fig. 9). ZVS turn ON of S_{C1} is achieved in this interval. No active power is transferred from DC to AC side. Equivalent circuit is shown in Fig. 8b.

F. Mode 8 ($t_7 < t < t_8$)

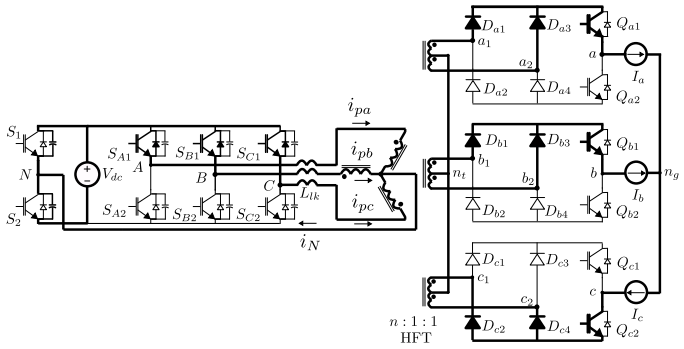


Fig. 10. Simplified circuit diagram in *Mode 8* ($t_7 < t < t_8$ in Fig. 3)

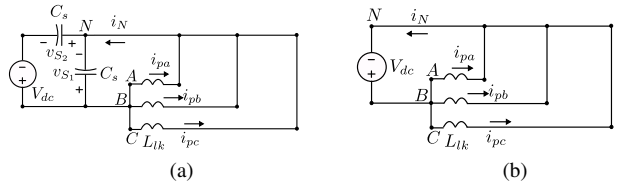


Fig. 11. (a) Equivalent circuit diagram in *Mode 8*, (b) Equivalent circuit diagram in *Sub-mode 1* of *Mode 9*

At t_7, S_1 is turned OFF. Due to device capacitance C_s, voltage across S_1, v_{S_1} can not rise immediately, resulting in ZVS turn OFF of S_1. The neutral current i_N starts charging the capacitor (C_s) across S_1 and discharging the capacitor across S_2 (Fig. 10). Equivalent circuit in this mode is shown in Fig. 11a. A positive voltage appears across the HFT primaries (AN, BN and CN). Secondary diodes D_{a1}, D_{b1} and D_{c4} are forward biased and start conducting. This results in shorting of HFT secondary windings (Fig. 11a) and the primary circuit dynamics become independent of secondary line currents. In primary, the voltage polarity is against the direction of currents through L_{lk} resulting in reduction of magnitudes of primary currents (i_{pa}, i_{pb} and i_{pc}). Circuit equations are given in (5).

$$\begin{aligned} i_N &= i_{pa} + i_{pb} + i_{pc} \\ V_{dc} &= v_{S_1} + v_{S_2} \\ i_N(t) &= C_s \left(\frac{dv_{S_1}}{dt} - \frac{dv_{S_2}}{dt} \right) \\ \frac{di_{pa}}{dt} &= \frac{di_{pb}}{dt} = \frac{di_{pc}}{dt} = -\frac{v_{S_1}}{L_{lk}} \end{aligned} \tag{5}$$

Where v_{S_1} and v_{S_2} are the voltages across S_1 and S_2. Solving (5) following expressions of voltage and currents are obtained.

$$\begin{aligned} i_N(t) &= i_N(t_7) \cos \omega_r (t - t_7) \\ i_{pj}(t) &= i_{pj}(t_7) - \frac{i_N(t_7)}{3} \left(1 - \cos \omega_r (t - t_7)\right) \\ v_{S_1}(t) &= \frac{\omega_r L_{lk} i_N(t_7)}{3} \sin \omega_r (t - t_7) \end{aligned} \tag{6}$$

Where $j \in \{a, b, c\}$ and $\omega_r = \sqrt{\dfrac{3}{2L_{lk}C_s}}$. At t_8, v_{S_1} reaches V_{dc} and $v_{S_2} = 0$. The anti-parallel diode of S_2 is forward biased and starts conducting. The duration of *Mode 8*, $t_{za_1} = (t_8 - t_7)$ is expressed as

$$t_{za_1} = \frac{1}{\omega_r} \sin^{-1} \left(\frac{3V_{dc}}{\omega_r L_{lk} i_N(t_7)} \right) \tag{7}$$

For the capacitor across S_2 to be completely discharged following condition must be satisfied

$$\omega_r L_{lk} i_N(t_7) \geq 3V_{dc} \tag{8}$$

Else the circuit will enter into resonant oscillation mode with angular frequency ω_r and will remain in this mode till the gating pulse of S_2 is being applied.

G. Mode 9 ($t_8 < t < t_9$)

From (6), $|i_{pj}(t_7) - i_{pj}(t_8)|$ have same values for $j = a, b, c$. So, $|i_{pc}(t_8)| > |i_{pa}(t_8)| > |i_{pb}(t_8)|$ as $I_c > I_a > I_b$. In this mode, the primary currents i_{pj} change the direction linearly and whenever i_{pj} reach $\dfrac{I_j}{n}$ the circuit dynamics of the corresponding phase is complete. Based on the magnitude at t_8, first b phase primary current reaches $\dfrac{I_b}{n}$ and then a and then c phase primary currents reach $\dfrac{I_a}{n}$ and $\dfrac{I_c}{n}$ respectively (see Fig. 12). *Mode 9* is divided into three sub-modes. As the primary side 3ϕ VSI switches $S_{A1,B1,C1}$ are already ON (ZVS) before entering into this mode, in the sub-modes initially the anti-parallel diodes and then active switches ($S_{A1,B1,C1}$) take part in conduction based on the direction of i_{pj}.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2889795, IEEE Transactions on Power Electronics

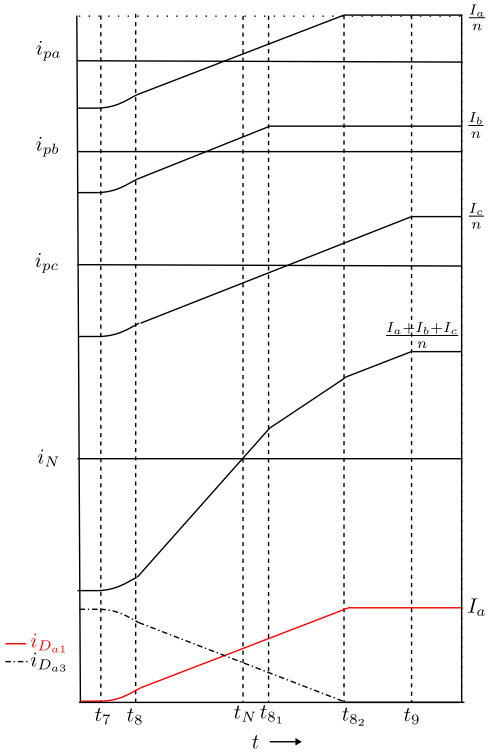


Fig. 12. Enlarged current wave forms in *Mode 9*

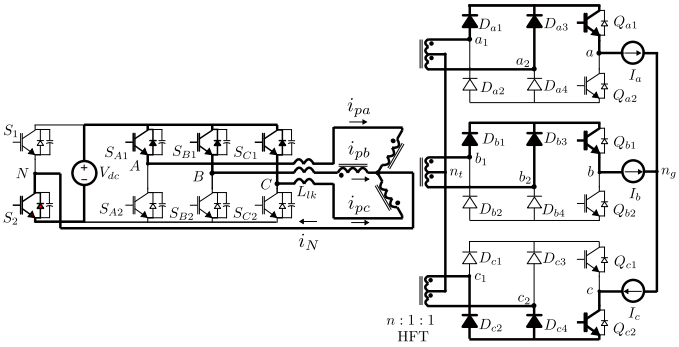


Fig. 13. Simplified circuit diagram in *Sub-mode 1* ($t_8 < t < t_{8_1}$ in Fig. 12)

1) Sub-mode 1 ($t_8 < t < t_{8_1}$): Simplified circuit in this sub-mode is shown in Fig. 13 and the equivalent circuit is shown in Fig. 11b. As the voltage polarity applied across the HFT primaries is against the direction of currents through L_{lk}, primary currents and i_N fall linearly as in (9).

$$\begin{aligned} i_N(t) &= i_N(t_8) - \frac{3V_{dc}}{L_{lk}}(t-t_8) \\ i_{pj}(t) &= i_{pj}(t_8) - \frac{V_{dc}}{L_{lk}}(t-t_8) \end{aligned} \tag{9}$$

In secondary, line currents are transferred linearly from D_{a3}, D_{b3} and D_{c2} to D_{a1}, D_{b1} and D_{c4} respectively. In Fig. 12, currents through D_{a1} and D_{a3} are shown. In this interval i_{pb} changes its direction.

2) Sub-mode 2 ($t_{8_1} < t < t_{8_2}$): At t_{8_1}, i_{pb} reaches the active state value $\frac{I_b}{n}$. In secondary, I_b is completely transferred from D_{b3} to D_{b1} and D_{b3} is reverse biased (Fig. 15).

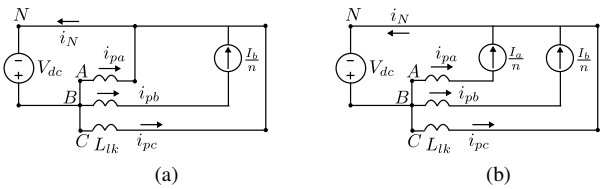


Fig. 14. (a) Equivalent circuit diagram in *Sub-mode 2* of *Mode 9*, (b) Equivalent circuit diagram in *Sub-mode 3* of *Mode 9*

Equivalent circuit is shown in Fig. 14a. As i_{pb} is clamped to $\frac{I_b}{n}$, the slope of i_N changes from $\frac{3V_{dc}}{L_{lk}}$ to $\frac{2V_{dc}}{L_{lk}}$ in this interval. Phase b has completed its zero to active state transition. Other two primary phase currents changes with same slope as in *Sub-mode 1*.

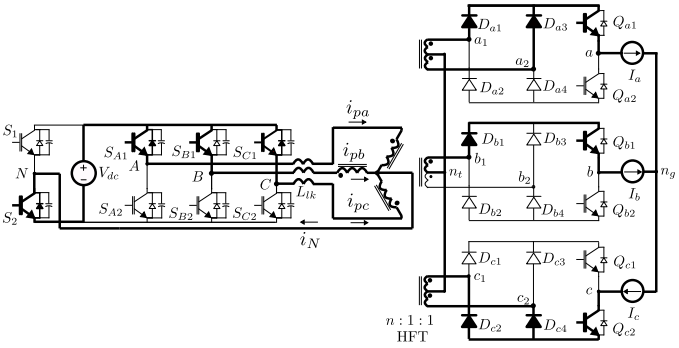


Fig. 15. Simplified circuit diagram in *Sub-mode 2* ($t_{8_1} < t < t_{8_2}$ in Fig. 12)

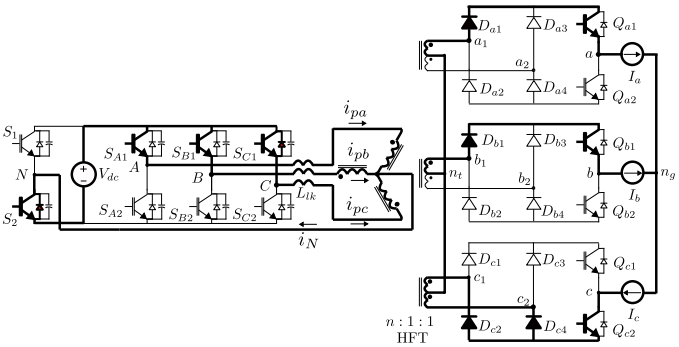


Fig. 16. Simplified circuit diagram in *Sub-mode 3* ($t_{8_2} < t < t_9$ in Fig. 12)

3) Sub-mode 3 ($t_{8_2} < t < t_9$): At t_{8_2}, i_{pa} reaches the active state value $\frac{I_a}{n}$. In secondary, I_a is transferred completely from D_{a3} to D_{a1} and D_{a3} is reverse biased (Fig. 16). Equivalent circuit is shown in Fig. 14b. As, i_{pb} and i_{pa} are clamped to $\frac{I_b}{n}$ and $\frac{I_a}{n}$ respectively, the slope of i_N changes from $\frac{2V_{dc}}{L_{lk}}$ to $\frac{V_{dc}}{L_{lk}}$ in this interval. Phase a has completed its zero to active state transition. Phase c current changes with same slope as in *Sub-mode 2*.

In *mode 9*, the slope of i_N is $3m_s$ in *Sub-mode 1*, $2m_s$ in *Sub-mode 2* and m_s in *Sub-mode 3*, where $m_s = \frac{V_{dc}}{L_{lk}}$. In

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2889795, IEEE Transactions on Power Electronics

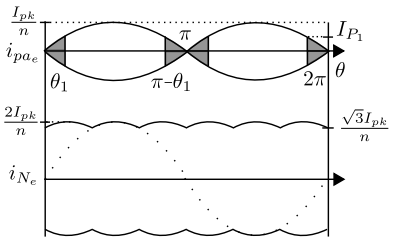


Fig. 17. Figure showing envelopes of HFT primary and neutral currents

mode 8-9, i_N is changed from $-\frac{I_a+I_b+I_c}{n}$ to $\frac{I_a+I_b+I_c}{n}$. i_N reaches zero at t_N (see Fig. 12). To achieve ZVS turn ON of S_2, it must be turned ON in some time between t_8 and t_N when the anti-parallel diode of S_2 is in conduction. So, it is important to find minimum of $(t_N - t_7) = (t_N - t_8) + (t_8 - t_7)$. $(t_8 - t_7)$ is given in (7). $\triangle t_N$ is defined as $\triangle t_N = (t_N - t_8)$. The objective of the following analysis is to find $\triangle t_{N,min}$. In this analysis, $(t_8 - t_7)$ and the change in current magnitude, $|i_{pj}(t_7) - i_{pj}(t_8)|$ are considered to be negligible. So, $\triangle t_N$ depends on m_s, I_a, I_b and I_c. Assuming negligible current ripple, the line currents are given as- $i_j = I_{pk}\sin\left(\omega_o t + M_j\frac{2\pi}{3}\right)$ (from (1)). So, $\triangle t_N$ depends on I_{pk} and α where $\alpha = (\omega_o t - 90^\circ)$. Let, i_{max} is maximum of I_a, I_b and I_c. Similarly, i_{mid} and i_{min} can be defined. As $i_a + i_b + i_c = 0$, $i_{max} = i_{min} + i_{mid}$. The waveforms of i_{pa} and i_N are square waves at switching frequency T_s and have envelopes as i_{pa_e} and i_{N_e} respectively over a line cycle ($\theta = \omega_o t$) as shown in Fig. 17. i_{max} has similar envelope as the positive half of i_{N_e}. Due to symmetry, the analysis of $\triangle t_{N,min}$ is carried out for $0^\circ < \alpha < 30^\circ$. From above assumption, $i_N(t_8) \simeq -\frac{2i_{max}}{n}$. The time interval of *Sub-mode 1* can be expressed as- $(t_{8_1} - t_8) = \frac{2i_{min}}{nm_s}$. At t_{8_1}, $i_N(t)$ can be expressed as in (10).

$$\begin{aligned} i_N(t_{8_1}) &= -\frac{2(i_{max})}{n} + 3m_s\left(\frac{2i_{min}}{nm_s}\right) \\ &= \frac{I_{pk}}{n}(3\sqrt{3}\sin\alpha - \cos\alpha) \end{aligned} \tag{10}$$

$i_N(t_{8_1})$ is monotonic in α and reaches zero at $\alpha^* = 10.89^\circ$. So, for $\alpha < \alpha^*$, $\triangle t_N$ is given in (11).

$$\begin{aligned} \triangle t_N &= \left(\frac{2i_{max}}{n}\right)\left(\frac{1}{3m_s}\right) \\ &= \frac{2I_{pk}}{3nm_s}\cos\alpha \qquad 0^\circ < \alpha < \alpha^* \end{aligned} \tag{11}$$

For $\alpha > \alpha^*$, it is possible to show i_N will reach zero in *Sub-mode 2*. i_N will take $\frac{i_N(t_{8_1})}{2m_s}$ amount of time to become zero in *Sub-mode 2*. $\triangle t_N$ is given in (12).

$$\begin{aligned} \triangle t_N &= \left(\frac{2i_{min}}{nm_s}\right) + \left(\frac{i_N(t_{8_1})}{2m_s}\right) \\ &= \frac{I_{pk}}{nm_s}\sin(\alpha + 30^\circ) \qquad \alpha^* < \alpha < 30^\circ \end{aligned} \tag{12}$$

From (11) and (12), $\triangle t_{N,min}$ occurs at $\alpha = \alpha^*$ and $\triangle t_{N,min} = 0.655\frac{I_{pk}}{nm_s}$. To achieve ZVS turn ON of the primary half-bridge leg $S_1 - S_2$ over the complete line cycle, the dead-time, DT should be less than $\triangle t_{N,min}$. Using (7), complete soft-switching condition of $S_1 - S_2$ is given in (13).

$$\frac{1}{\omega_r}\sin^{-1}\left(\frac{\sqrt{3}nV_{dc}}{\omega_r L_{lk} I_{pk}}\right) \le DT \le 0.655\frac{I_{pk}L_{lk}}{nV_{dc}} \tag{13}$$

H. Mode 10 ($t_9 < t < t_{10}$)

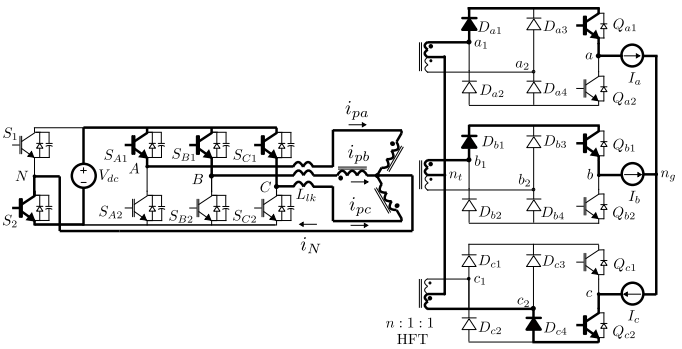


Fig. 18. Simplified circuit diagram in *Mode 10* ($t_9 < t < t_{10}$ in Fig. 3)

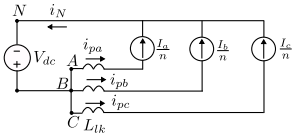


Fig. 19. Equivalent circuit diagram in *Mode 10*

At t_9, i_{pc} reaches the active state value $\frac{I_c}{n}$. In secondary, I_c is transferred completely from D_{c2} to D_{c4} and D_{c2} is reverse biased (Fig. 18). Equivalent circuit is shown in Fig. 19. All the phases are in active state and transferring power. The circuit configuration is similar as in *Mode 1*.

In above discussion, polarity reversal of HFT primary voltages and currents are shown in one half of the switching cycle. Similar switching sequence will be followed in rest half of the switching cycle with other symmetrical switches. It is seen that during active to zero state transitions 3ϕ VSI legs are switched. And the half-bridge leg $(S_1 - S_2)$ is switched during zero to active state transition. The above discussion shows, all switches in the 3ϕ VSI are zero voltage switched (ZVS) for most part of the line cycle whereas the ZVS of the half-bridge leg $(S_1 - S_2)$ can be ensured over complete line cycle.

IV. Experimental Validation

A. Setup and operating condition

The modulation strategy and switching process of the proposed topology (Fig. 2a) are experimentally verified in a laboratory scale hardware prototype (Fig. 20). Four primary HF legs and three secondary line frequency switched legs are implemented using 1200 V, 75 A SEMIKRON IGBT modules SKM75GB123D. 1200 V, 75 A IXYS fast recovery diode modules MEE 75-12 DA are used to implement secondary

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2889795, IEEE Transactions on Power Electronics

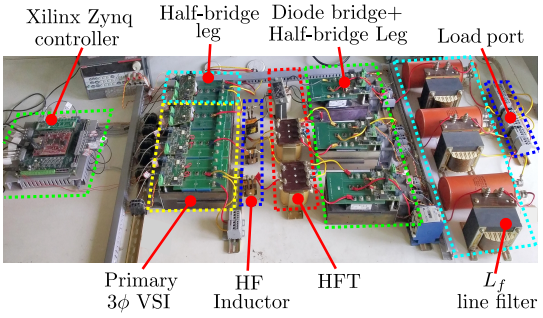


Fig. 20. Laboratory prototype

TABLE I
OPERATING CONDITION OF THE 3ϕ TOPOLOGY

Parameter	Values
Output Power, P	4 kW
DC input, V_{dc}	350 V
output voltage peak , V_{gpk}	200 V
Output frequency, f_o	50 Hz
Switching frequency, f_s	20 kHz

diode bridges. The IGBT modules are driven with optically isolated gate driver IC, ACPL 339J with driving voltage level ± 15 V. The primary modules are switched at 20 kHz where as secondary modules are switched at 50 Hz. A 600 ns dead time (DT) is provided between the gating pulses of the top and the bottom IGBTs of an IGBT module. EPCOS ferrite E cores (E 80/38/20) are used for three winding HFTs. The turns ratio is selected as 51:34:34. The leakage inductance of HFTs are in the range of 6-8μH. A series inductance of 48μH is connected to each primary of the HFTs. To implement the modulation strategy and generate the gating signals a ARM-FPGA based System on Chip (SoC) controller platform (Xilinx Zynq-7000) is used. The operating condition of the converter is given in Table I.

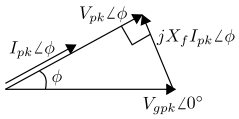


Fig. 21. Phasor diagram of the converter connected to the AC source

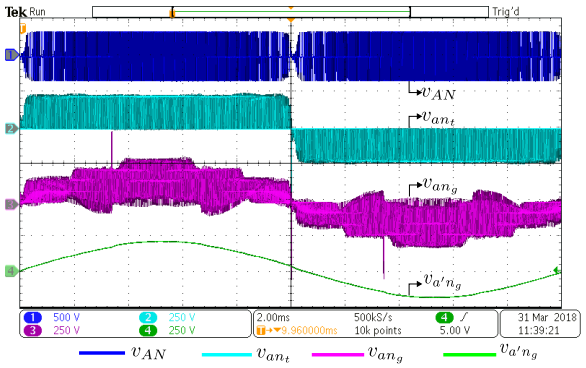
Phasor diagram is shown in Fig. 21 where V_{pk} and I_{pk} are the peak of $\overline{v}_{an_g}$ and i_a, respectively. V_{gpk} is the AC source peak value and $X_f = 2\pi f L_f$ is the line reactance and ϕ is the phase angle. From the phasor diagram (Fig. 21) following equations can be written.

$$V_{pk}\angle\phi = V_{gpk}\angle 0° + j(2\pi f L_f) I_{pk}\angle\phi$$
$$P = 1.5 V_{gpk} I_{pk} \cos\phi = 1.5 V_{pk} I_{pk} \quad (14)$$

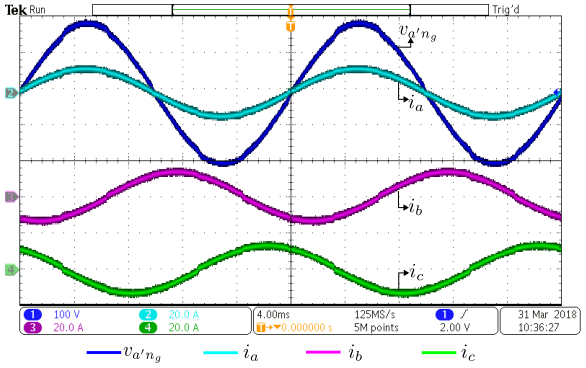
Solving (14),

$$V_{pk} = \left(\frac{V_{gpk}^2}{2} + \sqrt{\frac{V_{gpk}^4}{4} - \left(\frac{X_f P}{1.5}\right)^2} \right)^{1/2}$$
$$\phi = \sin^{-1}\left(\frac{2\pi f L_f I_{pk}}{V_{gpk}}\right) \quad (15)$$

The voltage at point a', b', c' are sensed and modulation index (m) and the phase angle (ϕ) are adjusted for a given power flow (P) to synthesized converter output voltage $\overline{v}_{(a,b,c)n_g}$. For the operating condition given in Table I, modulation index and phase angle are calculated as $\phi = 3°$, $m = 0.86$. So, power factor $\cos\phi = 0.998 \approx 1$.



(a)



(b)

Fig. 22. (a) Converter pole voltages- [CH1] v_{AN} (500V/div.), [CH2] v_{an_t} (250V/div.), [CH3] v_{an_g} (250V/div.), [CH4] $v_{a'n_g}$ (250V/div.). Time scale 2ms/div., (b) Converter output voltage and line currents- [CH1] $v_{a'n_g}$ (100V/div.), [CH2] i_a (20A/div.), [CH3] i_b (20A/div.), [CH4] i_c (20A/div.). Time scale 4ms/div.

B. Verification of modulation strategy

The output of the converter is connected to a balanced 3ϕ voltage source ($v_{a'n_g}$, $v_{b'n_g}$ and $v_{c'n_g}$) with phase peak (V_{gpk}) 200 V and frequency 50 Hz. The converter is modulated to generate balanced 3ϕ average output voltages ($\overline{v}_{an_g}$, $\overline{v}_{bn_g}$ and $\overline{v}_{cn_g}$) at 50 Hz following the strategy described in section II so that it supplies active power of 4 kW at unity power factor. $\overline{v}_{an_g}$ leads $v_{a'n_g}$. As the impedance of $L_f = 2.5$mH at 50 Hz is relatively small, $\overline{v}_{an_g}$ approximately follows $v_{a'n_g}$.

In Fig. 22a, the pulse width modulated HF AC across HFT primary of phase a (v_{AN}) is shown. v_{AN} has voltage levels of

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2889795, IEEE Transactions on Power Electronics

± 350 V and zero. The unipolar PWM pole voltage (v_{an_t}) with respect to HFT secondary neutral n_t is also shown in CH2. v_{an_t} has voltage levels of ± 233 V and zero. The experimental waveforms of v_{AN} and v_{an_t} have matched with the analytical waveforms shown in Fig. 2c. The pole voltage (v_{an_g}) with respect to load neutral n_g is presented in CH3. Due to presence of HF common mode voltage, the waveforms of v_{an_t} and v_{an_g} are different though they have same average component. The load voltage waveform ($v_{a'n_g}$) after line filter L_f is shown in CH4. As in table I, $v_{a'n_g}$ has a peak value (V_{gpk}) of 200 V.

Fig. 22b shows load voltage of phase a, $v_{a'n_g}$ and balanced 3ϕ line currents $i_{a,b,c}$ over two line cycles. $v_{a'n_g}$ is almost in phase with i_a and the line currents contain very low high frequency ripple due to filtering action of L_f. The line currents have an estimated peak of $I_{pk} = \dfrac{P}{1.5V_{gpk}\cos\phi} = 13.33$A. Experimentally measured peak is 13.4 A. These set of results confirm the three phase operation of the proposed converter.

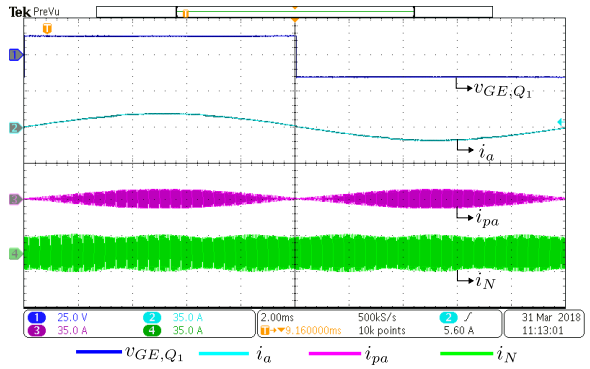
Line frequency switching of secondary switches are shown in Fig. 23a. The gate emitter voltage of Q_{a1} ($v_{GE,Q_{a1}}$) is high (+15V) when the line current $i_a > 0$. This experimental result validates line frequency switching described in the modulation strategy and shown in Fig. 2c. Fig. 23a also presents the primary current corresponding to phase a (i_{pa}) and the HFT neutral current i_N over a line cycle. The waveform of i_{pa} is high frequency square wave with magnitude sinusoidally varying over line cycle. The envelope of i_{pa} has a peak of $i_{pa,pk} = \dfrac{I_{pk}}{n} = 8.9$ A. Unlike i_{pa}, the envelope of i_N never becomes zero. The envelope of i_N has a periodicity of $\dfrac{T_0}{6}$ with peak value $i_{N,pk} = 2i_{pa,pk} = 17.8$ A and minimum value $\dfrac{\sqrt{3}i_{N,pk}}{2} = 15.4$ A. Such envelope of i_N helps to achieve complete soft-switching of leg S_1-S_2 over a line cycle.

Fig. 23b presents HFT primary voltage (v_{AN}) and current (i_{pa}) waveforms over two switching cycle ($2T_s$). HFT primary current polarity changes when applied voltage changes from zero to $\pm V_{dc}$ (zero to active state) as discussed in section III and shown in Fig. 3. Fig. 23b confirms that HFT flux balance is achieved in one switching cycle.

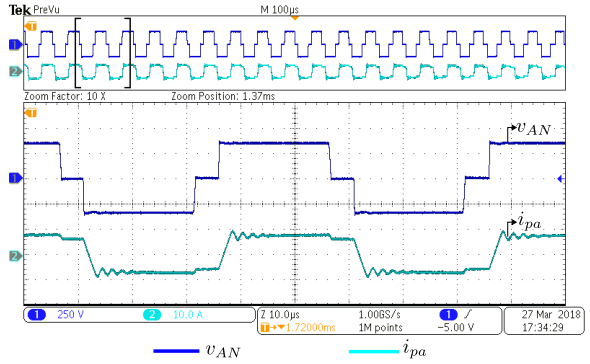
Fig. 24a shows 3ϕ primary voltages ($v_{A,B,C-N}$) of HFTs along with neutral current i_N over two switching cycles. The experimental waveforms are matched with the analytical waveforms shown in Fig. 3. From the figure, the zero to active state transition occurs simultaneously in all the three phases and during this time i_N also changes its direction. The leg $S_1 - S_2$ are switched at this instant. Active to zero transitions are not synchronised.

C. Verification of converter switching process

The switching strategy of phase legs S_{A1-A2}, S_{B1-B2} and S_{C1-C2} are similar. Hence phase A leg S_{A1-A2} are considered for discussion. In a high frequency switching cycle (T_s), S_{A1-A2} are switched twice during active to zero state transitions of phase A. During one transition S_{A2} is turned ON and S_{A1} is turned OFF and in the next transition S_{A2} is turned OFF and S_{A1} is ON. The switching process in both the transitions are same. Similarly, in a switching cycle (T_s) there

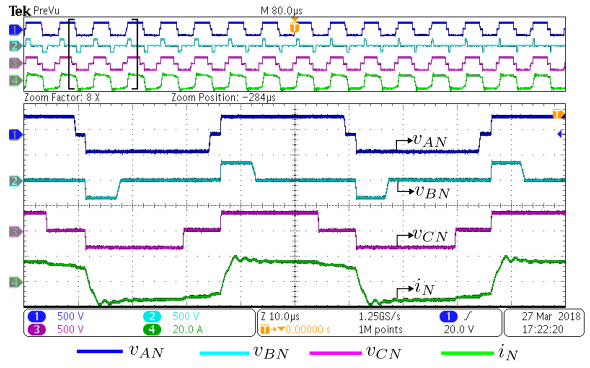


(a)

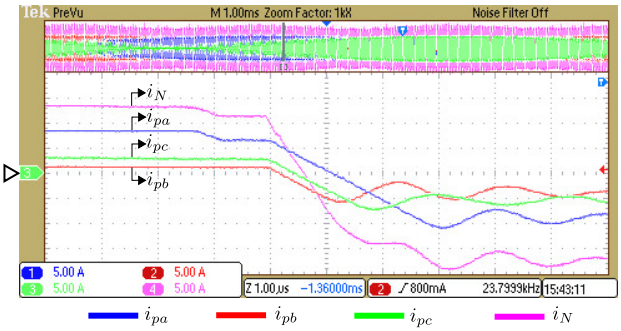


(b)

Fig. 23. (a) Line frequency switching of secondary switch- [CH1] $v_{GE,Q_{a1}}$ (25V/div.), [CH2] i_a (35A/div.), [CH3] i_{pa} (35A/div.), [CH4] i_N (35A/div.). Time scale 2ms/div. (b) HFT primary voltage and current- [CH1] v_{AN} (250V/div.), [CH2] i_{pa} (10A/div.). Time scale 10μs/div.



(a)

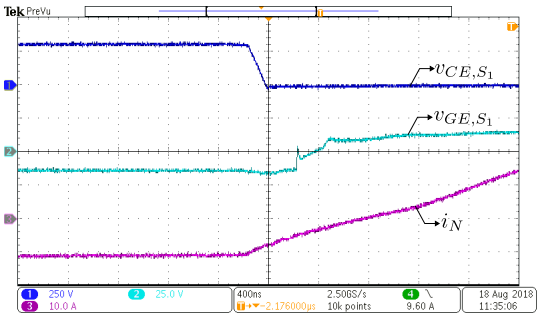


(b)

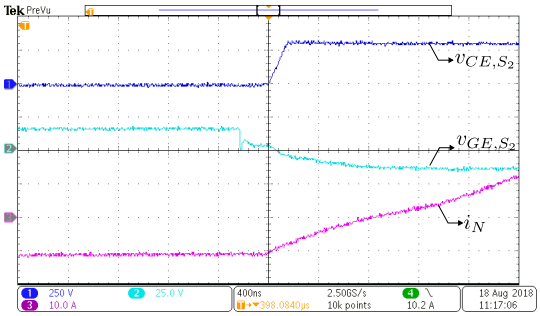
Fig. 24. (a) HFTs input voltages and neutral current- [CH1] v_{AN} (500V/div.), [CH2] v_{BN} (500V/div.), [CH3] v_{CN} (500V/div.), [CH4] i_N (20A/div.). Time scale 10μs/div., (b) Converter primary currents- [CH1] i_{pa} (5A/div.), [CH2] i_{pb} (5A/div.), [CH3] i_{pc} (5A/div.), [CH4] i_N (5A/div.). Time scale 1μs/div.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2889795, IEEE Transactions on Power Electronics

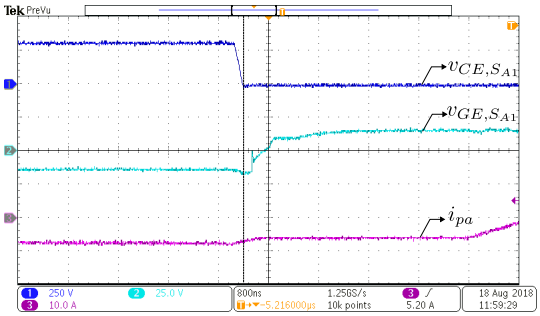
are two zero to active state transition during which leg $S_1 - S_2$ are switched. And here also, the switching process wise both the transition of $S_1 - S_2$ is similar. So, it is sufficient to check any one transition in legs S_{A1-A2} and $S_1 - S_2$ to verify the soft-switching process.



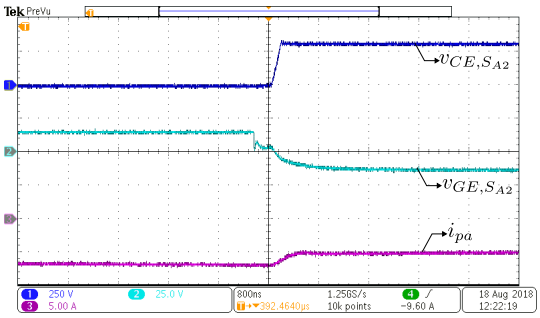
(a)



(b)



(c)



(d)

Fig. 25. Switching transition waveforms of leg $S_1 - S_2$-(a) turn ON of S_1, (b) turn OFF of S_2. Switching transition waveforms of leg $S_{A1} - S_{A2}$-(c) turn ON of S_{A1}, (d) turn OFF of S_{A2}

In Fig. 25a shows the turn ON transition of S_1. It is seen from the figure that the collector emitter voltage v_{CE,S_1} first falls to zero and the pole current i_N is negative which indicates the anti parallel diode of S_1 is in conduction. Before the direction of i_N is changed, the gate-emitter voltage v_{GE,S_1} is applied to achieve zero-voltage turn ON of S_1. Fig. 25b shows the turn OFF transition of S_2. It is seen that the voltage across S_2, v_{CE,S_2} starts rising some time after the removal of the gating pulse, v_{GE,S_2} (when v_{GE,S_2} is approximately zero or is negative). The v_{GE,S_2} represents the channel current of S_2. Below threshold voltage the channel current is zero. Due to presence of capacitance across S_2 the channel current falls first and then the voltage across S_2 starts rising which results in zero voltage turn OFF of S_2. These results show the ZVS operation of $S_1 - S_2$.

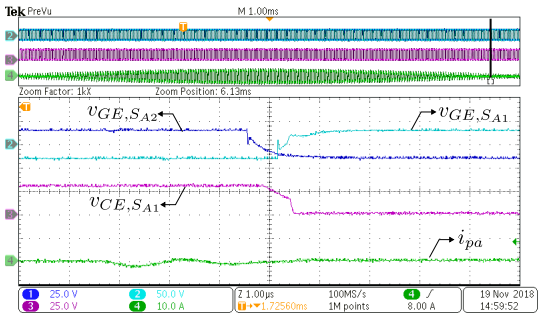


Fig. 26. Hard-switching transition of $S_{A1} - S_{A2}$

Fig. 25c shows the turn ON transition of S_{A1}. From the figure it is seen that the gating pulse $v_{GE,S_{A1}}$ is applied after the collector emitter voltage $v_{CE,S_{A1}}$ becomes zero. As the pole current (i_{pa}) direction does not change during the transition, the anti-parallel diode of S_{A1} is in conduction. So the turn ON of S_{A1} is a zero voltage transition. In Fig. 25d the turn OFF transition of S_{A2} is shown. The collector emitter voltage ($v_{CE,S_{A2}}$) starts rising some time after the gating pulse $v_{GE,S_{A2}}$ is removed and when $v_{GE,S_{A2}}$ is approximately zero or negative. This indicates the channel current through S_{A2} is zero when $v_{CE,S_{A2}}$ starts rising, results in zero voltage turn OFF transition. The delay in rise of $v_{CE,S_{A2}}$ is caused by the capacitance presents across S_{A2}. These results show the ZVS operation of S_{A1-A2}.

The $S_{A1} - S_{A2}$ are hard switched in the shaded zone shown in Fig. 17. Fig. 26 presents the hard turn ON of S_{A1}. The magnitude of i_{pa} is very low. After the gating pulse of S_{A2}, $v_{GE,S_{A_2}}$ is removed, the voltage across S_{A1}, $v_{CE,S_{A1}}$ starts falling linearly. A sharp fall in $v_{CE,S_{A1}}$ is observed when the S_{A1} is turned ON before the device capacitance C_s is completely discharged. This results in hard turn ON of S_{A1}.

V. Converter Power Loss and Efficiency

In this section, power loss of different stages of the converter is estimated and also obtained experimentally for a variation of load power in the range of 1kW-4kW.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2889795, IEEE Transactions on Power Electronics

A. Analytical loss estimation of the converter

The conduction loss in switch pair $S_1 - S_2$ is given as-

$$P_{C_{S_1}} = P_{C_{S_2}} = \frac{3V_{CE,S_{1,2}}I_{pk}}{n\pi} + 1.827\frac{R_{CE,S_{1,2}}I_{pk}^2}{n^2} \quad (16)$$

Where $V_{CE,S_{1,2}}$ and $R_{CE,S_{1,2}}$ are constant voltage drop (1.4V) and on state resistance (22mΩ) respectively of the IGBT module. The conduction loss of switches $S_{A1} - S_{C2}$ are given as-

$$P_{C_{S_{X1}}} = P_{C_{S_{X2}}} = \frac{mV_{CE,S_{X1,2}}I_{pk}}{4n} + \frac{2m}{3\pi n^2}R_{CE,S_{X1,2}}I_{pk}^2 \quad (17)$$

Where $X \in \{A, B, C\}$ and $V_{CE,S_{X1,2}}$ and $R_{CE,S_{X1,2}}$ are constant voltage drop (1.4V) and on state resistance (22mΩ) of IGBT modules used for $S_{X1} - S_{X2}$. The conduction loss expression of anti-parallel diodes of switch pairs $S_{X1} - S_{X2}$ is given in (18).

$$P_{C_{D,SX1}} = P_{C_{D,SX2}} = \frac{V_{D,X1,2}I_{pk}}{\pi n} + \frac{R_{D,X1,2}I_{pk}^2}{4n^2} - \frac{mV_{D,X1,2}I_{pk}}{4n} - \frac{mR_{D,X1,2}I_{pk}^2}{1.5\pi n^2} \quad (18)$$

The anti-parallel diodes have a voltage drop $V_{D,X1,2}$ (1.1V) and on state resistance $R_{D,X1,2}$ (18mΩ).
The conduction losses in a secondary diode of $D_{a1} - D_{c4}$ and a IGBT switch of $Q_{a1} - Q_{c2}$ are given in (19).

$$P_{C_{D_{a1}}} = \frac{V_{D_{a1}}I_{pk}}{2\pi} + \frac{R_{D_{a1}}I_{pk}^2}{8}$$
$$P_{C_{Q_{a1}}} = \frac{V_{CE_{a1}}I_{pk}}{\pi} + \frac{R_{CE_{a1}}I_{pk}^2}{4} \quad (19)$$

$V_{D_{a1}}$ (1.16V), $V_{CE_{a1}}$ (1.48V) and $R_{D_{a1}}$ (4mΩ), $R_{CE_{a1}}$ (2.3mΩ) are the constant voltage drop and on state resistance of the secondary diode D_{a1} and IGBT Q_{a1} respectively.
In Fig. 17, the pole current envelopes of $S_{A1} - S_{A2}$ (i_{pa_e}) and $S_1 - S_2$ (i_{N_e}) are shown. $S_1 - S_2$ is completely soft-switched. In Fig. 17, the shaded portions in i_{pa_e} indicate hard-switching zones of $S_{A_1} - S_{A_2}$. The range of soft turn ON of $S_{A1} - S_{A2}$ is given as $(\theta_1, \pi - \theta_1)$, as shown in Fig. 17. θ_1 is given in (20).

$$\theta_1 = \sin^{-1}\left(\frac{2nC_sV_{dc}}{I_{pk}DT_a}\right) \quad (20)$$

DT_a is the dead time between the gating pulses of $S_{A_1} - S_{A_2}$. Switching loss of S_{A1} is given in (21).

$$P_{S_{SA1}} = \frac{2V_{dc}I_{pk}}{n\pi T_s}\left(\frac{E_{ON_R} + E_{OFF_R}}{V_{CC}I_C}\right)(1 - \cos\theta_1) \quad (21)$$

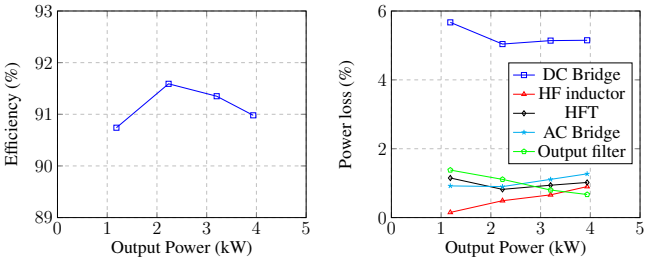
E_{ON_R} and E_{OFF_R} are the turn ON and OFF energy losses at rated condition (V_{CC}, I_C) given in device datasheet.

B. Power loss in HFTs

Copper loss of a HFT can be given as- $P_{cu,HFT} = \frac{I_{pk}^2}{2}\left(\frac{R_{AC,p}}{n^2} + R_{AC,s}\right)$, where $R_{AC,p}$ and $R_{AC,s}$ are primary and secondary winding AC resistances of the HFT. The core loss of the HFT is estimated at peak operating flux density using core loss per unit volume versus operating frequency plot provided in the core datasheet.

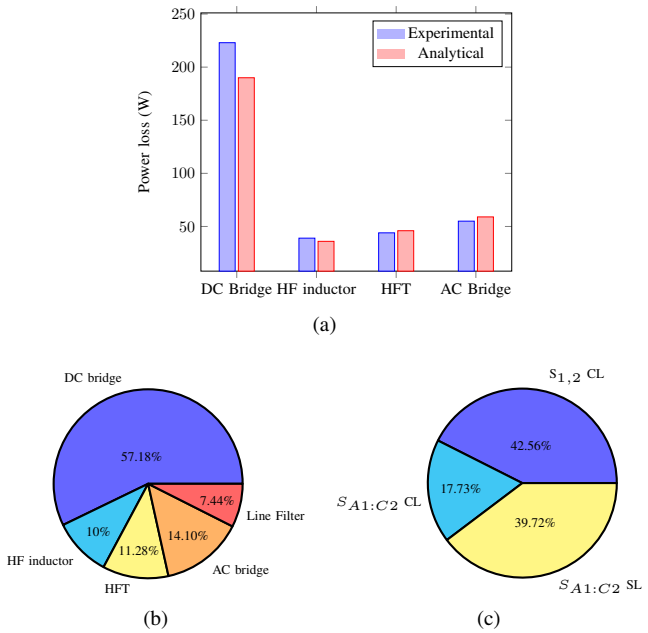
C. Experimentally measured loss

The converter power loss is measured experimentally using Vitrek precision multi-channel harmonic power analyser PA300 by taking the difference of measured power between input and output of each stage. Table II summarises the input quantities (voltages and currents) to the VA300 to measure power at different stages of the proposed inverter. In Fig. 2a, measured voltages, currents and powers in different stages are indicated. The DC side converter loss is measured as $(P_{in} - P_{out,dc})$. In similar way, the loss in each stage of the converter is measured experimentally.



(a) (b)

Fig. 27. (a) Efficiency of the proposed HFL inverter, (b) Power loss at different stages of 3ϕ HFL inverter



(a) (b) (c)

Fig. 28. (a) Power loss break down at 3.94kW output power obtained experimentally and analytically, (b) Percentage loss distribution shown at 3.94kW output power obtained experimentally, (c) Percentage loss distribution in the DC side converter shown at 4kW output power obtained analytically (SL-switching loss, CL- conduction loss)

Fig. 27a presents the converter efficiency for a variation of load from 1kW to 4kW with input DC supply 350V. The converter has a peak efficiency of 91.6% at 2.2kW load.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2889795, IEEE Transactions on Power Electronics

TABLE II
DIFFERENT STAGE POWER MEASUREMENT USING PA300 POWER ANALYSER

Inputs to PA300	V_{dc}, I_{dc}	$v_{(A,B,C)N}$, $i_{p(a,b,c)}$	$v_{(a_1,a_2)n_t}$,$i_{s(a1,a2)}$	$v_{(a,b,c)n_t}$,$i_{(a,b,c)}$	$v_{(a',b',c')n_g}$,$i_{(a,b,c)}$
Measured power	P_{in}	$P_{out,dc}$	$P_{out,HFT}$	$P_{out,AC}$	P

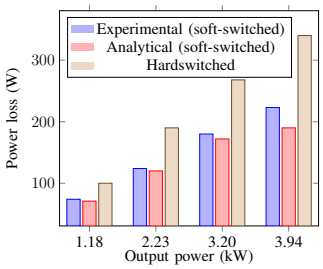


Fig. 29. DC side HF H bridge power loss: experimental, analytical and complete hard-switched

In Fig. 27b the variation of power losses in different stages of the converter are plotted against the load variation. Among different stages the high frequency switched primary bridge incurs maximum loss. The loss is reduced with the increase of load as the soft-switching zone is increased. Loss contributed by the line frequency switched secondary converter is relatively less (around 1%). This result shows the effectiveness of the line frequency switching based modulation strategy.

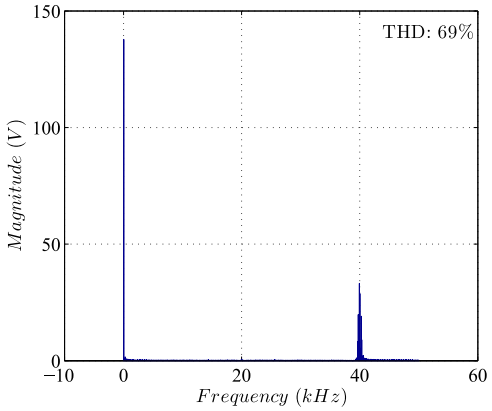
Fig. 28a shows power loss distribution for 3.94kW load obtained experimentally and analytically. The analytically estimated losses are closely matching with the experimentally obtained values other than the DC bridge. A 15% difference is observed in experimental and analytical obtained loss of the DC bridge. This difference is mainly the due to variation of device on state resistance with temperature and inaccuracy in estimation of hard-switching zone of $S_{A1} - S_{C2}$.

Fig. 28b presents a pie chart showing experimentally obtained losses at 3.94kW output power. The primary bridge incurs 57% loss compared with 14% of the secondary converter.

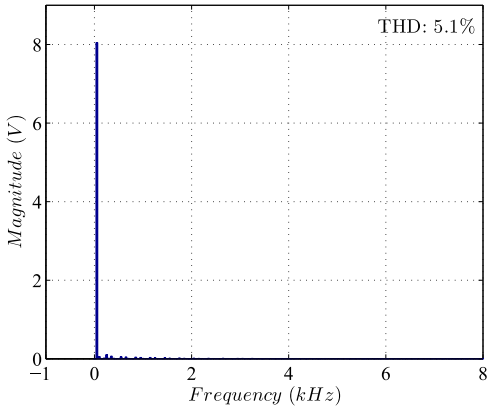
In Fig. 28c, the pie chart shows analytically obtained DC side converter loss distribution at 3.94kW output power. The conduction loss (CL) in $S_1 - S_2$ dominates the loss. As S_{A1}-S_{C1} are partially soft-switched, they also have switching loss (SL).

Fig. 29 presents the primary bridge loss variation over the load range. Experimental and analytical loss of the soft-switched primary bridge is presented along with complete hard-switched loss of the primary bridge. The soft-switching of the primary bridge significantly reduces the converter loss at high output power (as θ_1 is reduced in Fig. 17).

In Fig. 30, experimentally measured THD of output pole voltage (v_{ang}) and line current are shown. The pole voltage has a THD of 69% with an effective modulation index 0.8. As seen from Fig. 30a, after fundamental most dominant frequency components are at $40kHz$ which is twice of the DC bridge switching frequency. The line current THD is 5.1%.



(a)



(b)

Fig. 30. (a) Experimentally measured pole voltage (v_{ang}) THD. (b) Line current THD.

VI. COMPARISON WITH OTHER TOPOLOGIES

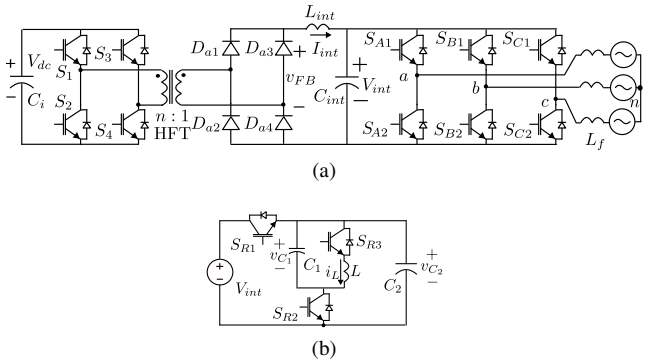
In this section a detailed comparison of the proposed solution is presented with a) topology 1- a ZVS phase-shifted full-bridge (PSFB) DC-DC converter followed by a 3ϕ voltage source inverter (in Fig 31a) and b) topology 2- a ZVS PSFB DC-DC converter followed by a quasi-resonant DC link inverter (QRDCL). In the second topology a resonating cell with three active switches (Fig. 31b) is connected between the PSFB and 3ϕ VSI (Fig 31a) to achieve ZVS of the 3ϕ VSI. The QRDCL circuit is shown in Fig. 31b [17]. The comparison is shown for a target application of grid integration of utility scale photovoltaic system with the specification given in Table III.

The proposed inverter is modulated at a modulation index $m = 0.85 = \frac{nV_{pk}}{V_{dc}}$. Thus the high frequency transformer (HFT) primary to secondary turns ratio, $n = 2$. IGBT SKM450GB12T4 (1200V,450A) are considered for the DC side switches $S_1 - S_2$ and the AC side switches $Q_{a1} - Q_{c2}$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2889795, IEEE Transactions on Power Electronics

TABLE III
TARGET DESIGN SPECIFICATION

Parameter	Value
Output power (P)	200 kW
Input DC (V_{dc})	800V
Output phase AC peak (V_{pk})	339V (415V L-L RMS)
Switching frequency (f_s)	20kHz
Line frequency (f_o)	50Hz



(a)

(b)

Fig. 31. (a) Topology 1: PSFB+3ϕ VSI, (b) Circuit diagram of QRDCL [17]

(Fig. 2a). The switches $S_{A1}-S_{C2}$ are implemented with IGBT SKM400GB125D (1200V,300A) whereas MEO 450-12DA (1200V,450A) is considered for secondary diodes $D_{a1}-D_{c4}$.

To be consistent, the DC-DC and the three-phase inverter in both topology 1 and 2 are modulated near the 85% of their respective maximum voltage transfer ratio. The DC-DC converter is modulated as PSFB [34] with duty ratio $D = 0.85 = \frac{nV_{int}}{V_{dc}}$ whereas the inverter is modulated with conventional space vector PWM with modulation index $M = 0.864 = \frac{\sqrt{3}V_{pk}}{V_{int}}$. This implies $V_{int} = 680V$, (see Fig. 31a) and HFT turns ratio $n = 1$. In topology 1, all active switches in PSFB and 3ϕ VSI are implemented using IGBT SKM450GB12T4. MEO 450-12DA is considered for the PSFB diode bridge.

The PSFB and the 3ϕ VSI in topology 2 are same as in topology 1. The QRDCL is designed based on the procedure given in [17]. S_{R1} is implemented with IGBT FZ1200R12HP4 (1200V, 1200A). IGBT FZ600R17KE3 (1700V, 840A) is used for S_{R2}. 1200V, 900A IGBT SKM900GA12E4 are used for $S_{R(3,4)}$.

Table IV summarises the comparison in terms of number of passive and active semiconductors, their blocking voltage (V_b), peak (I_P) and RMS (I_{RMS}) current. S.F is the scaling factor. The proposed topology uses 8 active switches in the DC side converter where the RMS current of 6 switches are 2.3-2.5 times less than the 4 DC side switches of the topology 1 and 2. The RMS current of the remaining two switches are slightly more. Blocking voltage of the devices are same as input DC bus voltage V_{dc} in all three topologies.

In the AC side, the proposed topology and the topology 1 have 6 active switches with similar RMS current and blocking voltage. The topology 2 needs 3 additional switches with high voltage and current stress to implement QRDCL. The blocking voltage of S_{R2} is 4.4 times the peak output voltage (V_{pk}). The current stress of all three switches are high and is maximum for S_{R1}, approximately 2.9 times the 3ϕ VSI switches. The RMS current rating of S_{R1} is approximately 1.7 times higher than the 3ϕ VSI switches. This results in significant additional conduction loss added to the AC side of the converter causing further decrease in converter efficiency. Now the 3ϕ VSI is soft-switched at the expense of additional active switches with very high voltage and current stresses. The proposed topology uses 12 diodes with same blocking voltage and 60% RMS current of the topology 1 and 2 that use 4 diodes in the AC side.

Loss and efficiency of the three topologies are presented in Table V where P_{CL} and P_{SL} are the conduction and switching loss respectively. The efficiency does not include the losses in HFTs and filters. The conduction loss in DC side converter of the proposed topology is slightly higher than the topology 1 and 2. The switching loss in DC side converter is negligible due to zero voltage switching (ZVS) in all three solutions. In the AC side, the topology 2 has higher conduction loss than other two topologies. The topology 1 has high switching loss due to hard-switching of the AC side 3ϕ VSI. As the

TABLE IV
TOPOLOGY COMPARISON

		S.F	Topology 1	Topology 2	Proposed Topology
DC side	Switch count	—	4	4	8
	$V_{b,sw}$	V_{dc}	1	1	1
	$I_{RMS,sw}$	$\frac{P}{V_{dc}}$	0.83($S_{1,2}$), 0.77($S_{3,4}$)	0.83($S_{1,2}$), 0.77($S_{3,4}$)	1.06($S_{1,2}$), 0.33 (S_{A1-C2})
	$I_{P,sw}$	$\frac{P}{V_{dc}}$	1.2	1.2	1.57($S_{1,2}$), 0.79 (S_{A1-C2})
AC side	switch count	—	6	9	6
	Diode count	—	4	4	12
	$V_{b,sw}$	V_{pk}	2.0	4.4(S_{R2}), 2.0 ($S_{R(1,3)}$), (S_{A1-C2})	2.35
	$V_{b,D}$	V_{pk}	2.35	2.35	2.35
	$I_{RMS,sw}$	$\frac{P}{V_{pk}}$	0.327	0.55(S_{R1}), 0.327 (S_{A1-C2})	0.334
	$I_{P,sw}$	$\frac{P}{V_{pk}}$	0.667	1.96(S_{R1}), 1.4 ($S_{R(2,3)}$), 0.667 (S_{A1-C2})	0.667
	$I_{RMS,D}$	$\frac{P}{V_{pk}}$	0.35	0.35	0.236
	$I_{P,D}$	$\frac{P}{V_{pk}}$	0.5	0.5	0.667

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2889795, IEEE Transactions on Power Electronics

AC side switches in the proposed solution and topology 2 incur negligible switching loss, they achieve similar efficiency. But in topology 2, this improved efficiency comes at the cost of using higher rated active devices in QRDCL cell. The decoupling of switching frequency with the losses in the proposed solution, provides an opportunity to push for higher switching frequency and hence smaller size of the filters and cost.

TABLE V
LOSS COMPARISON (SCALING FACTOR $\frac{P}{100}$)

		Topology 1	Topology 2	Proposed topology
DC side	P_{CL}	0.445	0.445	0.7
	P_{SL}	0	0	0
AC side	P_{CL}	1.03	1.23	1.138
	P_{SL}	2.353	0	0
Total Loss	P_{TL}	3.83	1.675	1.84
Efficiency	$\eta(\%)$	96.3	98.35	98.2

The proposed topology employs three HFTs where the secondary has two identical windings. The topology 1 and 2 use a single two-winding transformer. As the power flow in the proposed topology gets divided into three high frequency transformers, the RMS winding currents and individual area product are significantly small when compare with the topology 1 and 2 (see Table VI) . But due to push-pull winding structure of the secondary windings, the total area product for the proposed solution is 1.7 times, that of the conventional one.

TABLE VI
HIGH FREQUENCY TRANSFORMER COMPARISON

	S.F	Topology 1&2	Proposed topology
$I_{RMS,pri}$	$\frac{P}{V_{dc}}$	1.33	0.557
$I_{RMS,sec}$	$\frac{P}{V_{pk}}$	0.565	0.334
Area product	$\frac{P}{f_s J B_m K_w}$	0.425	0.242
HFT count	–	1	3

TABLE VII
FILTER SIZE COMPARISON USING THD

	Topology 1&2	Proposed topology
DC Side	0.42 (THD_I)	0.55 (THD_I)
AC Side	0.69 (THD_V)	0.6 (THD_V)
Intermediate DC Link	0.42 (THD_V, PSFB), 0.48 (THD_I, 3ϕVSI)	–

Filter requirement comparison

The filtering requirement can be expressed in terms of voltage and current THD [35]. In Table VII, the filtering requirements are compared between the proposed topology and topology 1 and 2 for the target specification. The topology 1 and 2 require additional filter after the DC-DC stage. For which both the capacitive and inductive filter requirement in topology 1 and 2 are 1.5-2 times when compared with the proposed solution. Hence, from the filter requirement perspective, the proposed solution is cost effective and will result in higher power density. Moreover, in any multi-stage solution, some additional capacitance (over and above than what is required for filtering) are used in the DC link to support load transient. Hence, an electrolytic capacitor is mostly employed and which is considered to be the most unreliable component. One of the major objective of proposed single stage configuration is the elimination of this capacitance.

VII. CONCLUSION

This paper presents a single-stage high frequency link converter topology that supports active power transfer from DC to AC at near UPF condition. A 4kW laboratory scale hardware prototype is built and tested. The suggested sine PWM based modulation strategy results in high quality output, evident from the AC side line currents obtained experimentally. This technique also ensures line frequency switching of the AC side converter incurring negligible switching loss. The converter loss is analytically estimated and the estimation is experimentally verified. The experimentally obtained loss breakdown verifies high efficiency of the secondary converter. Zero voltage switching (ZVS) of all active devices in the DC side converter with the help of circuit parasitics has been analysed and experimentally verified. The soft-switching of the primary side converter significantly reduces the converter loss at high power. The proposed converter with high frequency galvanic isolation provides a compact, cost effective and efficient solution for the utility scale grid integration of renewables.

REFERENCES

[1] "*Renewables 2017 global status report*," [online] Available at: http://www.ren21.net, 2017, [Accessed 20 Apr. 2018].

[2] "*LV5 Series Solar Inverter*," [online] Available at: http://www.gepowerconversion.com, [Accessed 20 Apr. 2018].

[3] S. Kouro, J. I. Leon, D. Vinnikov, and L. G. Franquelo, "Grid-connected photovoltaic systems: An overview of recent research and emerging pv converter technology," *IEEE Industrial Electronics Magazine*, vol. 9, no. 1, pp. 47–61, 2015.

[4] "*PCS6000 wind turbine converter brochure*," [online] Available at: https://library.e.abb.com, [Accessed 20 Apr. 2018].

[5] V. Yaramasu, B. Wu, P. C. Sen, S. Kouro, and M. Narimani, "High-power wind energy conversion systems: State-of-the-art and emerging technologies," *Proceedings of the IEEE*, vol. 103, no. 5, pp. 740–788, 2015.

[6] "*PV inverter designs and operation*," [online] Available at: http://www.iaeisj.org, February 2011, [Accessed 20 Apr. 2018].

[7] T. K. S. Freddy, N. A. Rahim, W.-P. Hew, and H. S. Che, "Comparison and analysis of single-phase transformerless grid-connected pv inverters," *IEEE Transactions on Power Electronics*, vol. 29, no. 10, pp. 5358–5369, 2014.

[8] T. Kerekes, R. Teodorescu, and U. Borup, "Transformerless photovoltaic inverters connected to the grid," in *Applied Power Electronics Conference, APEC 2007-Twenty Second Annual IEEE*. IEEE, 2007, pp. 1733–1737.

[9] S. Inoue and H. Akagi, "A bidirectional dc–dc converter for an energy storage system with galvanic isolation," *IEEE Transactions on Power Electronics*, vol. 22, no. 6, pp. 2299–2306, 2007.

[10] R. Gurunathan, A. Ballatine, C. Cottuli, and A. Doronzo, "Fuel cell power generation system with isolated and non-isolated buses," Dec. 27 2012, uS Patent App. 13/533,331.
[11] M. R. Islam, Y. Guo, and J. Zhu, "A high-frequency link multilevel cascaded medium-voltage converter for direct grid integration of renewable energy systems," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4167–4182, 2014.
[12] Y. Shi, R. Li, Y. Xue, and H. Li, "High-frequency-link-based grid-tied pv system with small dc-link capacitor and low-frequency ripple-free maximum power point tracking," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 328–339, 2016.
[13] R. Gao, X. She, I. Husain, and A. Q. Huang, "Solid-state-transformer-interfaced permanent magnet wind turbine distributed generation system with power management functions," *IEEE Transactions on Industry Applications*, vol. 53, no. 4, pp. 3849–3861, 2017.
[14] U. R. Prasanna and A. K. Rathore, "A novel single-reference six-pulse-modulation (srspm) technique-based interleaved high-frequency three-phase inverter for fuel cell vehicles," *IEEE Transactions on Power Electronics*, vol. 28, no. 12, pp. 5547–5556, 2013.
[15] Divan, Deepakraj M, "The resonant DC link converter-a new concept in static power conversion," *IEEE Transactions on Industry Applications*, vol. 25, no. 2, pp. 317–325, 1989.
[16] Divan, Deepakraj M and Skibinski, Gary, "Zero-switching-loss inverters for high-power applications," *IEEE Transactions on industry applications*, vol. 25, no. 4, pp. 634–643, 1989.
[17] He, Jin and Mohan, Ned, "Parallel resonant DC link circuit-a novel zero switching loss topology with minimum voltage stresses," *IEEE Transactions on Power Electronics*, vol. 6, no. 4, pp. 687–694, 1991.
[18] De Doncker, RW and Lyons, JP, "The auxiliary quasi-resonant dc link inverter," in *Power Electronics Specialists Conference, 1991. PESC'91 Record., 22nd Annual IEEE*. IEEE, 1991, pp. 248–253.
[19] Cho, Jung G and Kim, Hack S and Cho, Gyu H, "Novel soft switching PWM converter using a new parallel resonant DC-link," in *Power Electronics Specialists Conference, 1991. PESC'91 Record., 22nd Annual IEEE*. IEEE, 1991, pp. 241–247.
[20] Malesani, Luigi and Tenti, Paolo and Tomasin, Paolo and Toigo, Vanni, "High efficiency quasi-resonant DC link three-phase power inverter for full-range PWM," *IEEE Transactions on Industry Applications*, vol. 31, no. 1, pp. 141–148, 1995.
[21] Jung, YC and Liu, Hyo L and Cho, Guk C and Cho, Gyu H, "Soft switching space vector PWM inverter using a new quasi-parallel resonant DC link," *IEEE Transactions on power electronics*, vol. 11, no. 3, pp. 503–511, 1996.
[22] Mandrek, Slawomir and Chrzan, Piotr J, "Quasi-resonant dc-link inverter with a reduced number of active elements," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 4, pp. 2088–2094, 2007.
[23] Kedarisetti, Jayalakshmi and Mutschler, Peter, "A motor-friendly quasi-resonant DC-link inverter with lossless variable zero-voltage duration," *IEEE transactions on power electronics*, vol. 27, no. 5, pp. 2613–2622, 2012.
[24] R. Huang and S. K. Mazumder, "A soft-switching scheme for an isolated dc/dc converter with pulsating dc output for a three-phase high-frequency-link pwm converter," *IEEE Transactions on Power Electronics*, vol. 24, no. 10, pp. 2276–2288, 2009.
[25] D. De and V. Ramanarayanan, "A proportional multiresonant controller for three-phase four-wire high-frequency link inverter," *IEEE Transactions on Power Electronics*, vol. 25, no. 4, pp. 899–906, 2010.
[26] L. Jia and S. K. Mazumder, "A loss-mitigating scheme for dc/pulsating-dc converter of a high-frequency-link system," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 12, pp. 4537–4544, 2012.
[27] A. Kulkarni and V. John, "High performance modulation of high-frequency ac link inverter," in *Transportation Electrification Conference (ITEC), 2015 IEEE International*. IEEE, 2015, pp. 1–6.
[28] "Manufacturing cost analysis of 100 and 250 kw fuel cell systems for primary power and combined heat and power applications," [online] Available at: https://www.energy.gov, U.S. Department of Energy, Tech. Rep., January 2016.
[29] S. K. Mazumder, "Hybrid modulation scheme for a high-frequency ac-link inverter," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 861–870, 2016.
[30] R. Mazumder, Sudip K sand Huang, "A soft switching scheme for multiphase dc-pulsating dc converter for three-phase high-frequency-link pulsewidth modulation (pwm) inverter," *IEEE Transactions on Power Electronics*, vol. 25, no. 7, pp. 1761–1774, 2010.
[31] A. Rahnamaee and S. K. Mazumder, "A soft-switched hybrid-modulation scheme for a capacitor-less three-phase pulsating-dc-link inverter," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 3893–3906, 2014.
[32] A. Pal and K. Basu, "A unidirectional single-stage three-phase soft-switched isolated dc-ac converter," *IEEE Transactions on Power Electronics*, vol. PP, p. DOI 10.1109/TPEL.2018.2833747, 2018.
[33] ——, "A unidirectional snubber less fully soft-switched single stage three phase high frequency link dc/ac converter," in *Future Energy Electronics Conference and ECCE Asia (IFEEC 2017-ECCE Asia), 2017 IEEE 3rd International*. IEEE, 2017, pp. 1777–1784.
[34] R. W. Erickson and D. Maksimovic, *Fundamentals of power electronics*. Springer Science & Business Media, 2007.
[35] R. Baranwal, K. Iyer, K. Basu, G. Castelino, and M. Ned, "A reduced switch count single stage three-phase bidirectional rectifier with high frequency isolation," *IEEE Transactions on Power Electronics*, 2018.

Anirban Pal (S'17) received the B.E. degree from the Indian Institute of Engineering Science and Technology, Shibpore, India in 2010 and the M.E. degree from the Indian Institute of Science, Bangalore, India in 2015, both in electrical engineering. He is currently pursuing the Ph.D. degree at the Electrical Engineering Department, Indian Institute of Science, Bangalore, India. From 2010 to 2013, he worked as an Assistant Manager in National Thermal Power Corporation Limited. His research interests include high-frequency-link single stage converters, dual active bridge based converters, resonant converters, soft-switching techniques, design of high-frequency magnetics.

Kaushik Basu (S'07, M'13, SM'17) received the BE. degree from the Bengal Engineering and Science University, Shibpore, India, in 2003, the M.S. degree in electrical engineering from the Indian Institute of Science, Bangalore, India, in 2005, and the Ph.D. degree in electrical engineering from the University of Minnesota, Minneapolis, in 2012, respectively. He was a Design Engineer with Cold Watt India in 2006 and an Electronics and Control Engineer with Dynapower Corporation USA from 2013-15. Currently he is an Assistant Professor, in the Department of Electrical Engineering in Indian Institute of Science. He has been an author and coauthor of several technical papers published in peer reviewed journals and conferences. His research interests include various aspects of the general area of Power Electronics. He is the founding chair of both IEEE PELS and IES Bangalore Chapter.