A Single-Stage Solid-State Transformer for PWM AC Drive With Source-Based Commutation of Leakage Energy

Kaushik Basu, *Member, IEEE*, Arushi Shahani, Ashish Kumar Sahoo, *Student Member, IEEE*, and Ned Mohan, *Life Fellow, IEEE*

***Abstract*—A solid-state transformer is a three-phase ac/ac converter with a high-frequency transformer. Due to advanced features like high power density, on demand var support and frequency regulation, solid-state transformer is an enabling technology for the modern power distribution system. It can also find application in high-power-density motor drives. The single-stage solid-state transformer considered in this paper is capable of bidirectional power flow and open loop power factor correction. This topology uses a minimum amount of copper and has relatively few semiconductor switches. One major problem in this converter is the commutation of leakage energy which results in power loss, reduction in switching frequency, loss of output voltage, and additional common-mode voltage switching. This paper presents a source-based commutation strategy along with a novel modulation technique resulting in 1) elimination of additional snubber circuits, 2) minimization of the frequency of leakage inductance commutation, 3) recovery of the leakage energy, and 4) soft switching of the output converter. The topology and its proposed control have been analyzed. Simulation and experimental results confirm the operation.**

***Index Terms*—High-frequency transformer (HFT), indirect modulation, leakage commutation, matrix converter, PWM AC drive, solid-state transformer.**

I. Introduction

POWER transformers are an integral part of the electric power system. Increasing the frequency of operation of a power transformer above the grid frequency results in considerable reduction in the size, weight, and cost. Due to the availability of advanced magnetic material (nanocrystalline) with very low loss density and high saturation flux density, it is possible to design high-frequency transformers (HFT) with comparable efficiency [1], [2]. The recent advancements in power semiconductor technology have resulted in the development of high-voltage and high-current devices capable of switching at a high frequency and have relatively low conduction loss [3]. These developments have enabled the possible realization of HFT link ac/ac power converters, known as power electronic transformers (PET) or solid-state transformers (SST) [4]. SSTs can be employed in modern power distribution systems due to advanced features like voltage and frequency control, reactive power support, etc. [5]–[7]. Another major area of application is high-power-density electric motor drives, for example, in 1) electric traction [8]–[10], 2) wind power [11], [12], and 3) medium voltage ASDs [13].

Extensive classification of different types of SSTs can be found in [14] and [15]. Two-stage SSTs (ac–dc–ac) are of two kinds: high-voltage dc link (HVDC) [16] and low-voltage dc link (LVDC) [8]–[10]. A three-stage SST (ac–dc–dc–ac) has a high-frequency link dc/dc converter [17]–[19]. Multistage SSTs have the advantage of interfacing with renewable energy sources or storage systems with the available dc link [20]. Due to their multistage configuration, these topologies usually experience reduction in efficiency, reliability, and power density.

Single-stage single-phase ac/ac SSTs (based on full-bridge [21]–[23] or fly-back converters [24]) are fixed frequency and do not provide power factor correction [14], [25]. Single-stage resonant-based three-phase SST can be found in [26] and [27]. Qin and Kimball [28] and Shah *et al.* [29] present dual active bridge (DAB) converter-based SSTs. Resonant and DAB-based converters have the limitations of higher conduction loss and limited soft-switching range. DAB suffers larger turn-off loss compared to a resonant-based topology due to larger current at the time of switching.

Three-phase single-stage SSTs are primarily based on matrix converters [30] and provide an all silicon solution with grid power factor control and adjustable magnitude and frequency PWM voltage generation.

These types of SSTs can be broadly classified into three groups. Fig. 1 shows the topology of the first type of SST. It has a bank of three HFTs. The grid or the primary side of the HFTs has two windings connected in a push–pull structure, achieved by two three-phase diode bridges and two IGBTs S_1 and S_2. S_1 and S_2 operate in a complementary fashion with 50% duty cycle to chop the input ac grid voltage to a high-frequency ac. The load-side converter operates as a matrix converter to generate three-phase PWM ac at the load end. Reduced switch count (20 IGBTs, but uses a relatively large number of diodes) and soft switching of the grid-side converter are important advantages of this topology [31].

Fig. 2 presents the circuit diagram of the second type of SST. The primary or grid-side converter turns the input ac to an

Manuscript received November 22, 2013; revised March 7, 2014; accepted April 14, 2014. Date of publication April 30, 2014; date of current version October 15, 2014. Recommended for publication by Associate Editor P.-T. Cheng.

K. Basu is with Dynapower Company LLC, South Burlington, VT 05403 USA (e-mail: basux017@umn.edu).

A. Shahani was with the Department of Electrical Engineering, University of Minnesota, Minneapolis, MN 55455 USA. She is now with IBM, USA (e-mail: shah0379@umn.edu).

A. K. Sahoo and N. Mohan are with the Department of Electrical Engineering, University of Minnesota, Minneapolis, MN 55455 USA (e-mail: saho0007@umn.edu; mohan@umn.edu).

Digital Object Identifier 10.1109/TPEL.2014.2320996

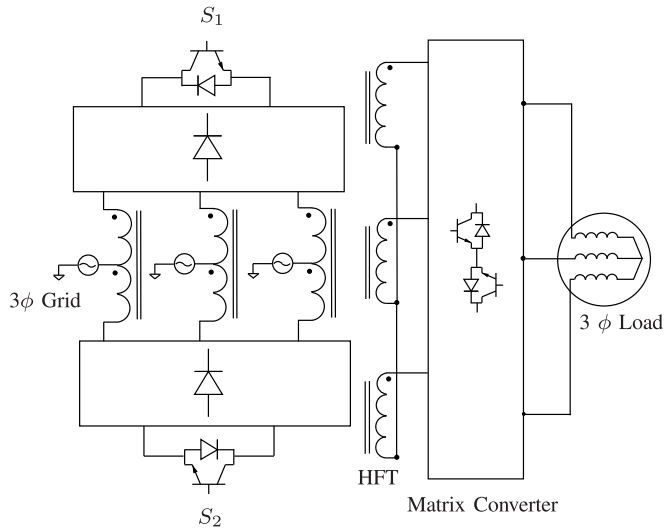


Fig. 1. Circuit diagram of type-1 SST.

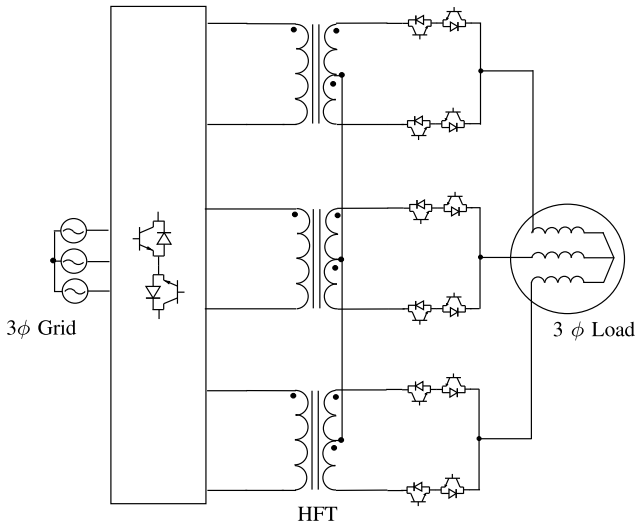


Fig. 2. Circuit diagram of type-2 SST.

adjustable magnitude and frequency PWM ac and then inverts it to generate a 50% duty cycle modulated virtual high-frequency ac. The secondary side of the HFTs is connected to the load in a full-bridge structure that rectifies the high-frequency ac to apply the PWM ac generated by the primary-side converter to the load. The modulation is done in the primary side in order to minimize the effect of the commutation of leakage energy along with suppression of the switching common-mode voltage. A major disadvantage of this topology is its large switch count (48 IGBTs), [32].

The third type of SST has been proposed in [33]. A variation of this topology can be found in [34]. This particular type of SST is shown in Fig. 3 and is the focus of this paper. This paper identifies a connection of this topology with indirect matrix converter [35], [36]. In this type of SST, the virtual dc link of an indirect matrix converter is chopped with a 50% duty-cycle by the grid-side converter and passed through a single-phase HFT. The load-side converter first rectifies the high-frequency ac to get back the virtual dc and then inverts it to generate adjustable frequency and magnitude PWM ac at the load end. First, two types of SSTs use a bank of three single-phase three-winding transformers, where two of the windings are used only 50% of time (see Figs. 1 and 2). Due to the use of only one two-winding transformer the SST based on indirect modulation requires least amount of copper. It also has a fairly low switch count of 24 IGBTs. Unlike the second type of SST suppression of switching common-mode voltage is not possible in this type of SST.

The windings of the HFT have leakage inductance. Due to the inductive nature of the three-phase load, any switching transition of the load-side converter needs commutation of leakage energy resulting in output voltage loss, common-mode voltage switching, and ultimately reduction in switching frequency. In this paper, a novel PWM technique has been developed to minimize the frequency of leakage commutation by minimizing the switching of the load-side converter. The proposed switching strategy reduces the switching of the load-side converter by one-third in comparison with the conventional method, [37], [38].

Commutation of leakage energy by additional snubber circuits leads to loss of the leakage energy and reduction in reliability and power density. Source-based commutation of leakage energy has been implemented for high-frequency link dc/ac [39], single-phase ac/ac [40], bidirectional rectifier [41], and the second type of three-phase ac/ac SST [32]. Source-based commutation is not possible in the first type of SST due to push–pull structure in the primary side [31]. In this paper, a source-based commutation technique of leakage energy has been developed. It results in the elimination of additional snubber circuits, soft switching of the load-side converter, and recovery of the leakage energy.

The content of this paper was first appeared in [42]. In this paper: 1) section I is rewritten to include the recent literature; 2) modulation strategy (see Section II) has been improved for further reduction in the number of switching of the grid-side converter; 3) section III on commutation has been expanded to include further analysis; and 4) section IV presents the key simulation and experimental results confirming the proposed advantages.

II. Modulation

This section presents a detailed description of the generation of adjustable frequency and amplitude three-phase PWM ac voltage at the load end. The modulation strategy presented here results in 1) flux balance in the HFT, and 2) minimization of the frequency of leakage inductance commutation.

The operation of this converter is controlled by two signals S and C as shown in Fig. 4. Flux balance is achieved over one complete cycle of signal S in $2T_s$ period of time. C is related to the commutation of leakage energy and will be discussed in the next section. The grid-side converter is modulated to rectify the input three-phase voltage given in (1) to a virtual dc and then invert the rectified dc to a high-frequency ac over one period of signal S. V_i is the peak and ω_i is the angular frequency of the input voltage. (2) gives the corresponding voltage vector. In the first half of signal S (when it is high or 1), a positive average

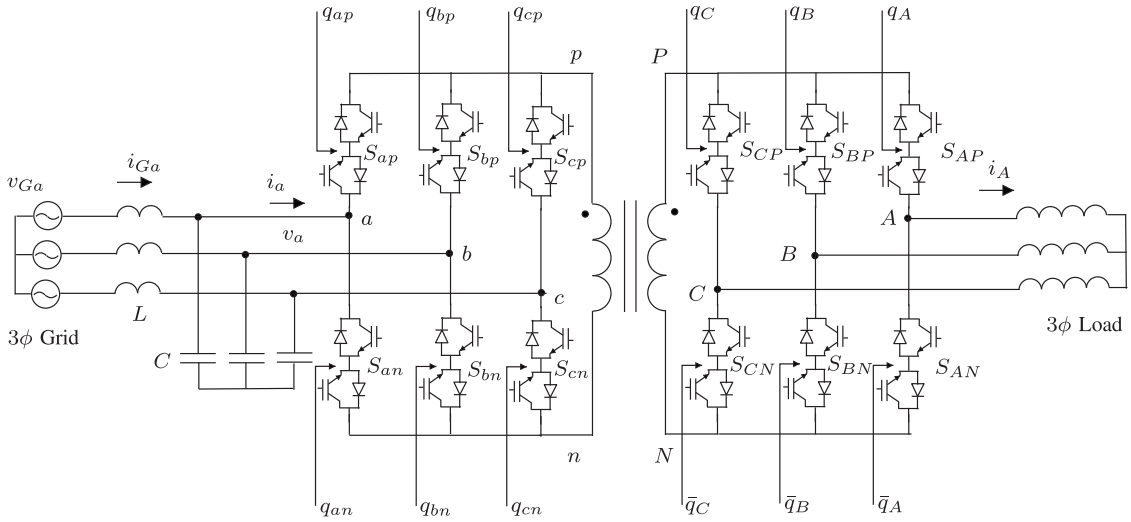


Fig. 3. Circuit diagram of the type-3 SST along with the input filter.

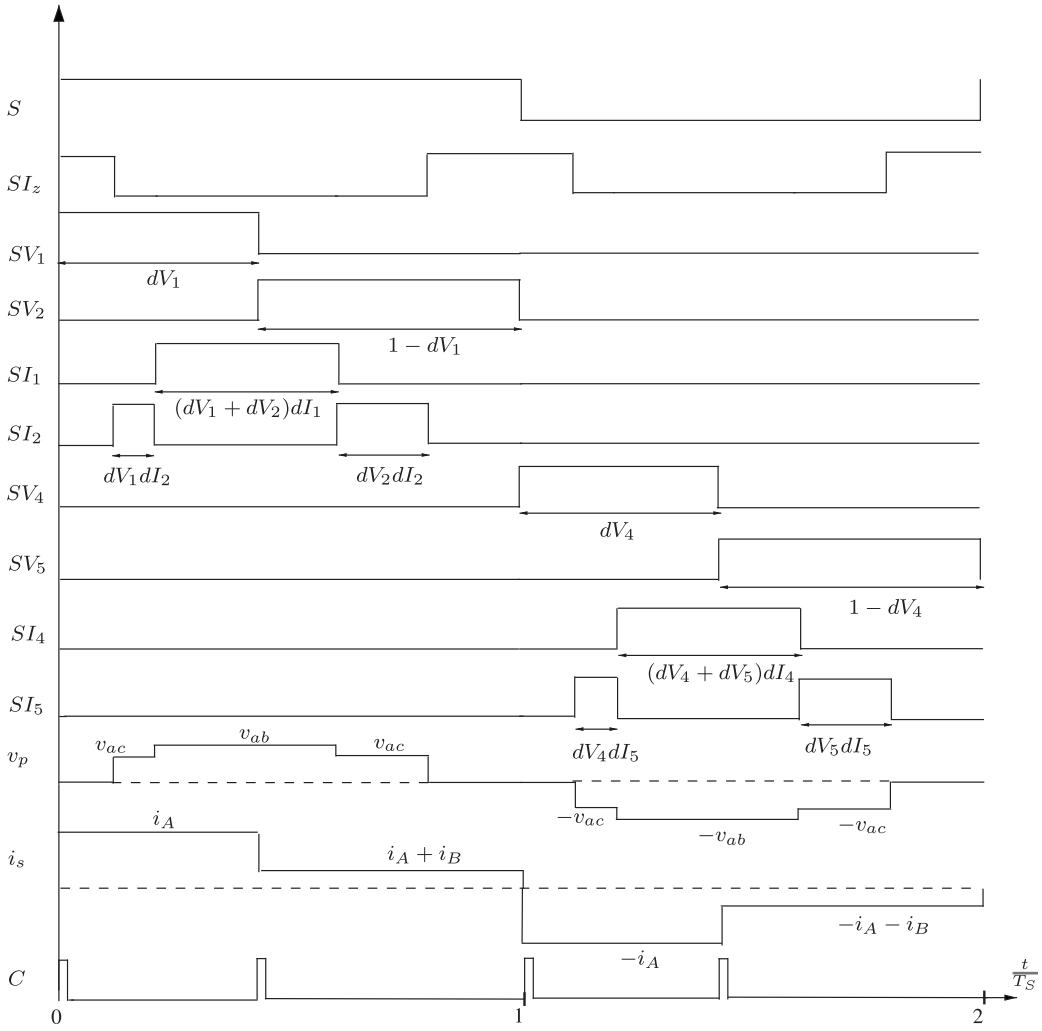


Fig. 4. Control signals.

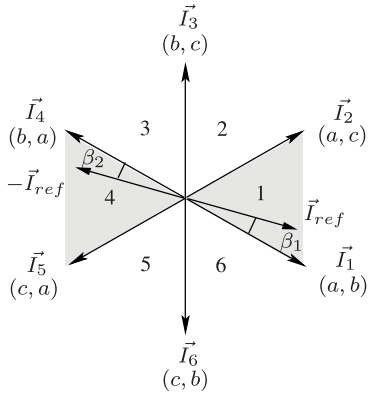


Fig. 5. Space vector modulation of the grid-side converter.

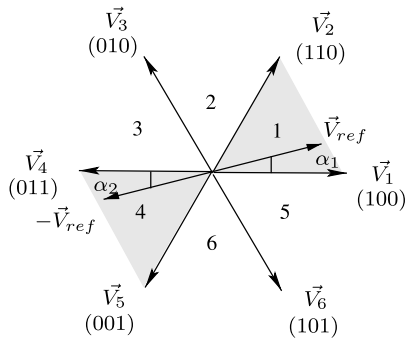


Fig. 6. Space vector modulation of the load-side converter.

voltage is applied across the transformer primary $\bar{v_p} > 0$. $\bar{v_p}$ is the average of the primary winding voltage over a period T_s. In the second half, when signal S is low $\bar{v_p}$ is negative. When S is 1, for a positive power flow (grid to load), the average primary winding current $\bar{i_p}$ is positive. For a positive power flow (grid to load), when S is 0, $\bar{i_p}$ is negative

$$\begin{aligned} v_a &= V_i \cos \omega_i t \\ v_b &= V_i \cos\left(\omega_i t - \frac{2\pi}{3}\right) \\ v_c &= V_i \cos\left(\omega_i t + \frac{2\pi}{3}\right) \end{aligned} \tag{1}$$

$$\vec{V} = v_a + v_b e^{j\frac{2\pi}{3}} + v_c e^{-j\frac{2\pi}{3}} = \frac{3}{2} V_i e^{j\omega_i t} \tag{2}$$

$$\vec{I}_{\rm ref} = \bar{i}_a + \bar{i}_b e^{j\frac{2\pi}{3}} + \bar{i}_c e^{-j\frac{2\pi}{3}} \tag{3}$$

$$\vec{I}_{\rm ref} = \frac{3}{2} I_i e^{j\omega_i t} = \begin{cases} dI_1 \vec{I}_1 + dI_2 \vec{I}_2 & S = 1 \\ dI_4 \vec{I}_4 + dI_5 \vec{I}_5 & S = 0 \end{cases} \tag{4}$$

$$\begin{aligned} dI_1 &= m_I \sin\left(\frac{\pi}{3} - \beta_1\right) \quad dI_4 = m_I \sin\left(\frac{\pi}{3} - \beta_2\right) \\ dI_2 &= m_I \sin\beta_1 \quad dI_5 = m_I \sin\beta_2 \end{aligned} \tag{5}$$

Let us discuss the case when $S = 1$ and power flow is positive. The input current space vector is defined as $\vec{I} = i_a + i_b e^{j\frac{2\pi}{3}} + i_c e^{-j\frac{2\pi}{3}}$. When $\bar{i_p}$ is positive, the input converter, modulated as rectifier, produces six active current vectors ($\vec{I_1}$ to $\vec{I_6}$) and three zero vectors (see Fig. 5). A switching combination (a, b) implies that the switches S_{ap} and S_{bn} are ON in Fig. 3. This switching state produces a current vector $\vec{I}_1 = \sqrt{3}\bar{i}_p e^{-j\frac{\pi}{6}}$. The reference input current vector $\vec{I}_{\rm ref}$ as shown in (3) is aligned along the input voltage vector $\vec{V}$ to get power factor correction [see (4)]. The angle between these two vectors can be adjusted to achieve grid power factor control. If $\vec{I}_{\rm ref}$ is in sector 1, as shown in Fig. 5, two nearest active vectors, in this case $\vec{I}_1$ and $\vec{I}_2$, are used to synthesize $\vec{I}_{\rm ref}$ [see (4)]. The corresponding duty cycles dI_1 and dI_2 are given in (5). Modulation index m_I is defined as the ratio of the peak of the fundamental component of the input current I_i to $|\bar{i}_p|$. Considering positive power flow when $S = 0$, $\bar{i}_p$ is negative, the current vectors for a particular switching combination reverse its direction. This implies in this stage $\vec{I}_1 = -\sqrt{3}\bar{i}_p e^{-j\frac{\pi}{6}}$. To produce the same reference input current vector, we can still use the current space vector diagram of Fig. 5 and synthesize $-\vec{I}_{\rm ref}$ by applying $\vec{I}_4$ and $\vec{I}_5$, [see (4) and (5)]. When power flow is negative, $\bar{i}_p < 0$ for $S = 1$ and $\bar{i}_p > 0$ for $S = 0$. So if we follow the modulation just described for positive power flow we will synthesize an input current vector opposite to $\vec{I}_{\rm ref}$. In case of negative power flow with unity power factor, the input current vector must be opposite in direction with respect to the input voltage vector. So for negative power flow, if we align $\vec{I}_{\rm ref}$ still in the direction of $\vec{V}$ and follow the modulation strategy as described for positive power flow we will get power factor correction.

The load-side converter is modulated to rectify the high-frequency secondary voltage to a virtual dc and then invert it to generate balanced three-phase ac voltage of magnitude V_o and angular frequency ω_o. The reference output voltage space vector is given in (6). When $S = 1$, the average secondary voltage $\bar{v}_s$ is positive and the allowable eight switching states of the output converter produce six active ($\vec{V}_1$ to $\vec{V}_6$) and two zero output voltage vectors, as shown in Fig. 6. A switching state (1 1 0) indicates switches $S_{\rm AP}$, $S_{\rm BP}$, $S_{\rm CN}$ are ON (see Fig. 3) and vector $\vec{V}_2 = \bar{v}_s e^{j\frac{\pi}{3}}$ is applied. If the reference output voltage vector $\vec{V}_{\rm ref}$ is in sector 1, as in Fig. 6, the two adjacent active vectors $\vec{V}_1$ and $\vec{V}_2$ are used [see (7) and (8)]. Modulation index m_V is defined as the ratio of the peak of the fundamental component of the output voltage V_o to $|\bar{v}_s|$. When $S = 0$, $\bar{v}_s < 0$ and each voltage vector for a particular switching state of the load-side converter is reversed. In order to generate same output voltage vector, we need to synthesize $-\vec{V}_{\rm ref}$ by applying vector $\vec{V}_4$ and $\vec{V}_5$ in Fig. 6 [see (7) and (8)]

$$\vec{V}_{\rm ref} = \bar{v}_A + \bar{v}_B e^{j\frac{2\pi}{3}} + \bar{v}_C e^{-j\frac{2\pi}{3}} \tag{6}$$

$$\vec{V}_{\rm ref} = \frac{3}{2} V_o e^{j\omega_o t} = \begin{cases} dV_1 \vec{V}_1 + dV_2 \vec{V}_2, & S = 1 \\ dV_4 \vec{V}_4 + dV_5 \vec{V}_5, & S = 0 \end{cases} \tag{7}$$

$$\begin{aligned} dV_1 &= \sqrt{3} m_V \sin\left(\frac{\pi}{3} - \alpha_1\right), \quad dV_4 = \sqrt{3} m_V \sin\left(\frac{\pi}{3} - \alpha_2\right) \\ dV_2 &= \sqrt{3} m_V \sin\alpha_1, \quad dV_5 = \sqrt{3} m_V \sin\alpha_2 \end{aligned} \tag{8}$$

N_1 and N_2 are the number of turns of the primary and secondary windings, respectively. This implies transformer

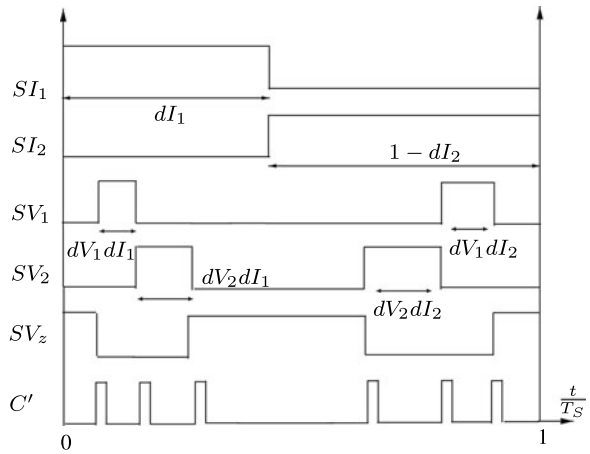


Fig. 7. Switching sequence for conventional modulation.

relations $\frac{\bar{v}_p}{N_1} = \frac{\bar{v}_s}{N_2}$ and $\bar{i}_p N_1 = \bar{i}_s N_2$ hold. Assuming no power loss in the transformer and in both input and output converters, we get $\frac{3}{2} V_i I_i = \bar{v}_p \bar{i}_p = \bar{v}_s \bar{i}_s = \frac{3}{2} V_o I_o \cos\theta$, where I_o is the peak of the fundamental component of the load current and θ_o is the load power factor angle. Using these relations and definitions of the m_I and m_V, it is possible to obtain

$$V_o = \left(\frac{N_2}{N_1}\right) \frac{3}{2} m_I m_V V_i \tag{9}$$

$$I_i = \left(\frac{N_2}{N_1}\right) \frac{3}{2} m_I m_V \cos\theta_o I_o \tag{10}$$

Each switching transition in the load-side converter requires commutation of leakage energy. Commutation results in power loss, loss of output voltage, and increased common-mode voltage switching. This also implies reduction in the operating frequency. The modulation of this converter is related to indirect modulation of matrix converter. Consider modulation when $S = 1$, the switching signal corresponding to different active voltage and current vectors over a period T_s for conventional indirect modulation is shown in Fig. 7, [37], [38]. SI_1 goes high when vector I_1 is applied in the grid-side converter. SV_z corresponds to the application of zero voltage vector by the load-side converter. The signal C' goes high each time the load-side converter switches. Each switching transition of the load-side converter in Fig. 7 results in switching of one leg. The output-side converter has three legs, corresponding to three output phases. For example, switches $S_{\rm AP}$ and $S_{\rm AN}$ forms the leg corresponding to phase A (see Fig. 3). From modulation, $S_{\rm AP}$ and $S_{\rm AN}$ are switched in a complementary fashion. From Fig. 7, C' goes high six times over one sampling cycle of period T_s. So with conventional indirect modulation, there will be 12 switching over one complete cycle of signal S.

This paper proposes an alternative sequence for the application of these vectors as described in Fig. 4 leading to minimum switching of the output-side converter. Fig. 4 presents the switching signals corresponding to each applied active vectors over one complete cycle of signal S, when both $\vec{I}_{\rm ref}$ and $\vec{V}_{\rm ref}$ are in their respective sector 1 as discussed before. The signal C goes high when the load-side converter is switched. From Fig. 4, it can be observed that the load-side converter is switched only once in one sampling cycle T_s. For example, when switching from $\vec{V}_1$ to $\vec{V}_2$ with $S = 1$. This results in switching in one leg (leg B in this case) as compared to six switchings in the conventional method. In the conventional method, (see Fig. 7) for a particular input current vector say $\vec{I}_1$, the output converter is switched to apply $\vec{V}_1$ and $\vec{V}_2$ for $dI_1 dV_1$ and $dI_1 dV_2$ fractions of time, respectively. In the proposed method for a particular voltage vector in the load-side converter, say $\vec{V}_1$, the grid-side converter is switched to apply $\vec{I}_1$ and $\vec{I}_2$ for $dV_1 dI_1$ and $dV_1 dI_2$ fractions of time, respectively. The zero vector in the proposed method is applied using the input converter (SI_z, Fig. 4) in comparison with the conventional method that applies the zero state using the output converter (SV_z, Fig. 7). In the proposed scheme, the load-side converter switches at the transitions of signal S. For example, in Fig. 4, when S goes from high to low, the load-side converter switches from $\vec{V}_2$ to $\vec{V}_4$ resulting in the switching of two legs of the load-side converter (phase A and C). Over one complete cycle of signal S, in comparison with 12 switchings in the conventional scheme, the proposed method results in only four switchings. The applied primary voltage waveform v_p shows how flux is balanced over one cycle of signal S. This figure also shows typical secondary current waveform. Signal C is related to commutation and described in detail in the next section.

Given the switching sequence of the output-side converter, the proposed switching sequence results in minimum number of switching of the source-side converter. This is an improvement over the scheme described in [42].

In Fig. 3, q_{ap} is the control signal for switch S_{ap}. Tables I and II show how these signals can be derived from the signals controlling the application of active and zero vectors during

TABLE I
SWITCHING SIGNALS FOR THE PRIMARY-SIDE CONVERTER DURING MODULATION

	Sector					
	1	2	3	4	5	6
q_{ap}	1	SI_2	0	SI_z	0	SI_1
q_{bp}	0	SI_3	1	SI_4	0	SI_z
q_{cp}	0	SI_z	0	SI_5	1	SI_6
q_{an}	SI_z	0	SI_4	1	SI_5	0
q_{bn}	SI_1	0	SI_z	0	SI_6	1
q_{cn}	SI_2	1	SI_3	0	SI_z	0

TABLE II
SWITCHING SIGNALS FOR THE SECONDARY-SIDE CONVERTER DURING MODULATION

	Sector					
	1	2	3	4	5	6
q_A	1	SV_2	0	0	SV_6	1
q_B	SV_2	1	1	SV_4	0	0
q_C	0	0	SV_4	1	1	SV_6

modulation. In these tables, sector is determined by the position of $\vec{I}_{\rm ref}$ (for Table I) and of $\vec{V}_{\rm ref}$ (for Table II) when $S = 1$. Negative of these vectors are used when $S = 0$. For example, when $S = 1$, $\vec{I}_{\rm ref}$ is in the first sector and q_{bn} is assigned to SI_1, Table I. In this particular case, SI_1 is shown in Fig. 4. When $S = 0$, $-\vec{I}_{\rm ref}$ is in Sector 4 and q_{bn} is assigned to 0.

III. Commutation

Windings of the high-frequency transformer have leakage inductance. The three-phase load is essentially inductive in nature. So any switching transition in the load-side converter requires the current through the leakage inductance to change by the application of suitable voltage across it. This process is referred as commutation of leakage energy. Commutation by passive means, using a snubber or clamp circuit, results in power loss. The modulation method proposed in the previous section minimizes the frequency of commutation but does not eliminate it (one needs to switch the load-side converter). This paper presents a source-based commutation technique that results in complete recovery of the leakage energy without the use of additional snubber circuits. The source-side converter is switched to apply the necessary voltage required for commutation. This process also results in complete soft switching of the load-side converter.

Over one-half cycle of the signal S, the load-side converter is switched only once. For example, in Fig. 4, consider the switching transition from $\vec{V}_1$ to $\vec{V}_2$ when $S = 1$ and $\vec{V}_4$ to $\vec{V}_5$ when $S = 0$. In this type of transition, the first active vector is switched to the next active vector in a given sector (sector 1, $\vec{V}_1$ to $\vec{V}_2$). This transition results in switching of only one leg of the load-side converter. In a switching transition from $\vec{V}_1$ to $\vec{V}_2$, the leg connected to output phase B is switched. The load-side converter is also switched at the transition of the signal S (see Fig. 4). In this transition, the load-side converter is switched from $\vec{V}_2$ to $\vec{V}_4$ when S goes from 1 to 0 and from $\vec{V}_5$ to $\vec{V}_1$ when S goes from 0 to 1. This type of transition require switching of two legs of the load-side converter. For example, $\vec{V}_2$ to $\vec{V}_4$ require switching of legs corresponding to phase A and C. In this type of transition when two legs switch, we delay the switching signal of one of the legs, so that we can implement the commutation due to each leg sequentially one after another. So, commutation in this paper essentially refers to the process of changing the current through the leakage inductance when one leg of the load-side converter switches. Two switches in a particular leg in the load-side converter are switched in a complementary fashion. Let us define S_X be the switching signal for a leg connected to the output phase X, where $X = A, B, C$. $S_X = 1$ implies $S_{\rm XP}$ is ON and $S_{\rm XN}$ is OFF and $S_X = 0$ implies $S_{\rm XP}$ is OFF and $S_{\rm XN}$ is ON. Depending on the nature of the transition of signal S_X ($1 \rightarrow 0$ or $0 \rightarrow 1$) and the direction of the load current i_X, four cases are possible. Each of the switches in the load-side converter $S_{\rm XP}$ and $S_{\rm XN}$ is realized by the common-emitter connection of two IGBTs with antiparallel diodes. These IGBTS and corresponding diodes are referred as $Q_{1X}, Q_{2X}, Q_{3X}, Q_{4X}$ and $D_{1X}, D_{2X}, D_{3X}, D_{4X}$ as shown in Fig. 8 for phase B. The switching signal for these IGBTs for all of these four cases of commutation is shown in Fig. 9. Let us discuss the case when $i_X > 0$ and S_X is making a transition from 0 to 1. For example, consider the case when $S = 1$ and the load-side converter is switching from $\vec{V}_1$ to $\vec{V}_2$ (S_B is going from 0 to 1) and assume $i_B > 0$ at that instant of time (see Fig. 8).

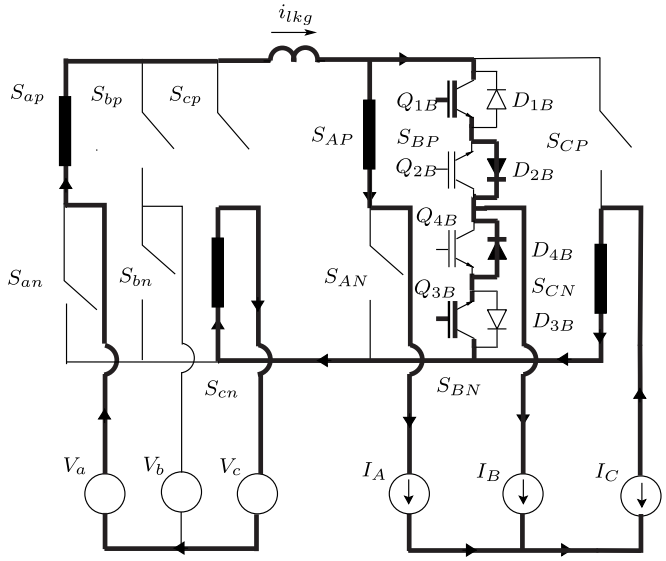


Fig. 8. Commutation of leakage energy.

In this analysis, the magnetizing current is neglected and the transformer is represented as a series combination of reflected primary $L_p(\frac{N_2}{N_1})^2$ and secondary leakage inductance L_s. The commutation period is much smaller in comparison with that of the input voltage and output current waveforms. So the output inductive load currents and input source voltages can be modeled as dc sources during commutation, as shown in Fig. 8. The commutation process can be divided into three distinct steps.

Step 1: As a first step when S_B goes from 0 to 1, the non-conducting IGBT Q_{4B} of the switch $S_{\rm BN}$ that is going out of conduction is turned OFF. This is a zero voltage switching (ZVS). Now, the input-side converter is switched to apply the maximum positive line-to-line voltage available at that time to the transformer primary. The direction of the applied voltage in all four cases of commutation is given in Table III. Without any loss of generality, let us assume this voltage is V_{ac}. We wait in this state for time t_{d1}, for the primary converter to apply the required voltage.

Step 2: After a delay of time t_{d1}, the IGBT Q_{1B} which will be conducting in the upcoming switching state is turned ON. As the applied primary voltage is positive and the current through the leakage inductance cannot change instantaneously, the diode D_{2B} is forward biased and Q_{1B} is turned ON with ZCS. D_{2B} starts conducting (see Fig. 8). By KCL, (11) and (12) hold. Neglecting the effect of magnetizing current and voltage drop across the switches Q_{1B}, Q_{3B} and diodes D_{2B}, D_{4B}, it is possible to obtain (13). Using (11) to (13) and noting $v_s = V_{ac}(\frac{N_2}{N_1})$, we get (14). As the diodes conduct only in one direction this process comes to a natural end when i_{D2} becomes I_B, i_{D4} goes to zero, and the leakage current i_{lkg} becomes $I_A + I_B$. This

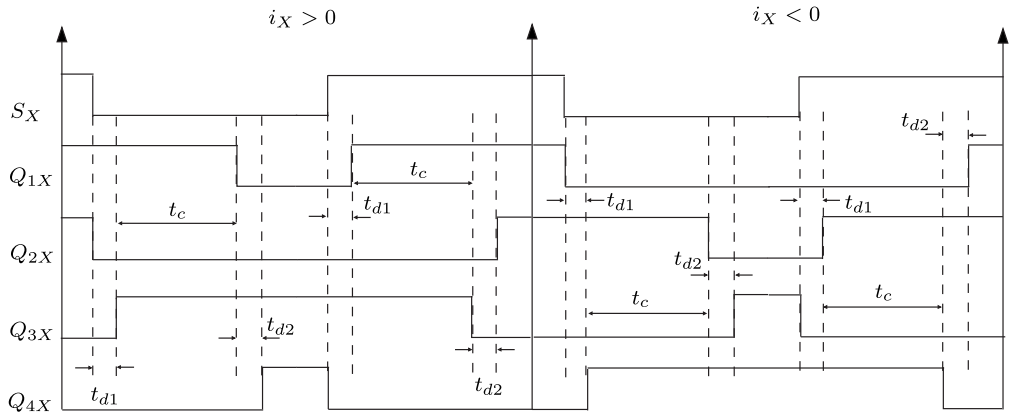


Fig. 9. Switching signals of the load-side converter for all four cases of commutation $X = A, B, C$.

TABLE III
SIGN OF THE PRIMARY WINDING VOLTAGE APPLIED BY THE PRIMARY CONVERTER DURING COMMUTATION, $X = A, B, C$

S_X	$i_X > 0$	$i_X < 0$
1→0	−	+
0→1	+	−

process takes maximum time, t_c as in (15), when maximum available line-to-line voltage is at its minimum ($V_i\sqrt{3}\frac{\sqrt{3}}{2}$) and the load current is at its peak I_o. At the end of this step, Q_{3B} is turned OFF with zero current.

$$i_{D_{2B}} + i_{D_{4B}} = I_B \tag{11}$$

$$i_{D_{2B}} + I_A = i_{lkg} \tag{12}$$

$$v_s = \left[L_p\left(\frac{N_2}{N_1}\right)^2 + L_s\right]\frac{d}{dt}i_{lkg} \tag{13}$$

$$\frac{d}{dt}i_{lkg} = \frac{d}{dt}i_{D_{2B}} = -\frac{d}{dt}i_{D_{4B}} = \frac{V_{ac}\left(\frac{N_2}{N_1}\right)}{\left[L_p\left(\frac{N_2}{N_1}\right)^2 + L_s\right]} \tag{14}$$

$$t_c = \frac{\left[L_p\left(\frac{N_2}{N_1}\right)^2 + L_s\right]I_o}{1.5V_i\left(\frac{N_2}{N_1}\right)} \tag{15}$$

Step 3: As a last step after a delay t_{d2}, the nonconducting IGBT Q_{2B} is turned ON with ZVS.

In conclusion, leakage commutation is the process of changing the current through the leakage inductance at a switching transition of any one leg of the load-side converter. It is achieved by the application of suitable voltage by the primary-side converter and controlling the switching of individual IGBTs of the transitioning leg. This process results in complete recovery of the leakage energy along with soft switching of the load-side converter.

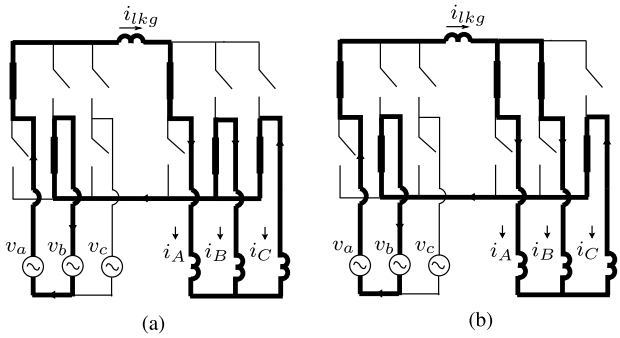


Fig. 10. Circuit configuration (a) before commutation and (b) after commutation.

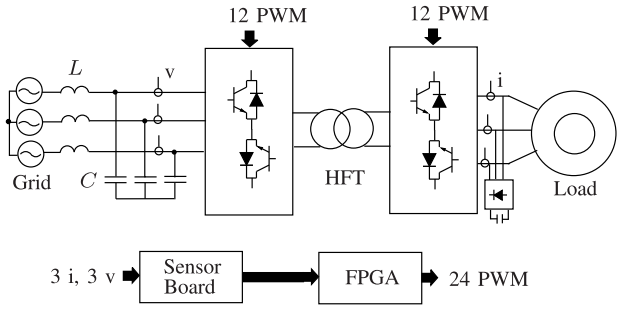


Fig. 11. Experimental setup.

Just before the transition of the load-side converter from $\vec{V}_1$ to $\vec{V}_2$, the grid-side converter was applying $\vec{I}_1$, switches S_{ap} and S_{bn} are ON in Fig. 3. Fig. 10(a) shows the corresponding circuit configuration. Fig. 10(b) shows the same configuration after commutation process is over. During modulation, the leakage inductance of the transformer comes in series with inductive load. For example, in Fig. 10(a), it comes in series with load phase A and in Fig. 10(b) it comes in series with load phase C. As the leakage inductance is small in comparison with the load inductance, it can be neglected in the analysis of the circuit during modulation. In case of an *R–L* load with load resistance R and load inductance L, (16) holds, where $\vec{I}_o = \bar{i}_A + \bar{i}_B e^{\frac{j2\pi}{3}} +$

TABLE IV
PARAMETERS

L_{load}	R_{load}	L_p, L_s	R_{lkg}	$\frac{N_2}{N_1}$	V_{in}	f_i	$f_s = \frac{1}{T_s}$	f_o	m_I	m_V	L_F	C_F
$27mH$	7Ω	$42\mu H$	0.1Ω	1	85V	60 Hz	5kHz	42 Hz	0.8	0.46	$0.5mH$	$13.2\mu F$

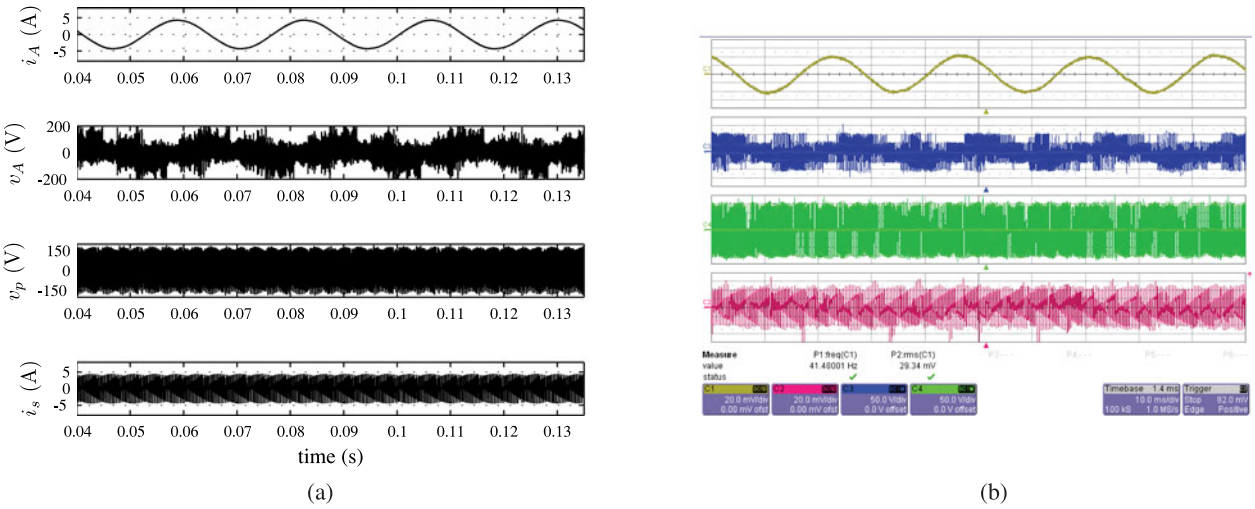


Fig. 12. (Top to bottom) Output line current of phase A (CH1) (2 A/div), output line to neutral voltage of phase A (CH3) (50 V/div), primary winding voltage (CH4) (50 V/div), secondary winding current (CH2) (2 A/div), time 5 ms/div. (a) Simulation. (b) Experimental.

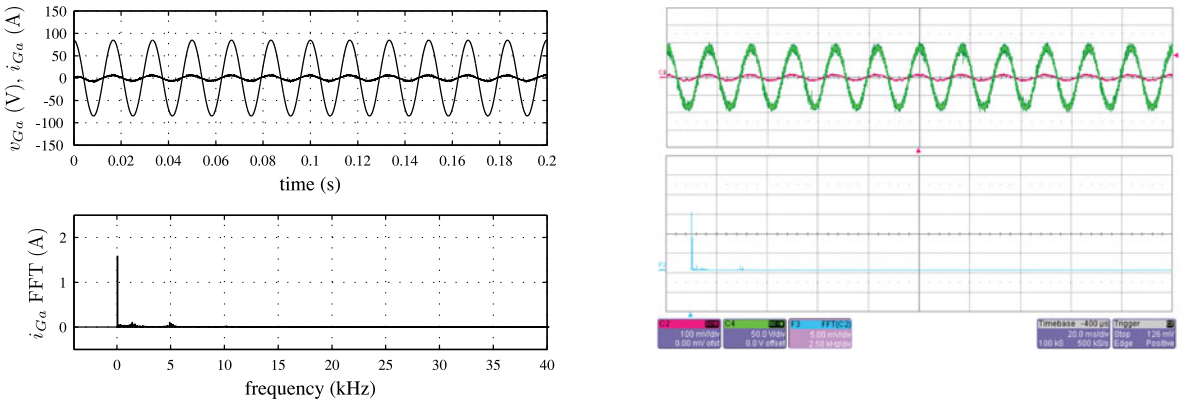


Fig. 13. (Top to bottom) grid line to neutral voltage (CH4) (50 V/div), filtered grid current (CH2) (10 A/div) and time 20 ms/div, FFT of grid current (vertical axis 0.5 A/div and horizontal axis 2.5 kHz/div). (a) Simulation (b) Experimental.

$\bar{i}_C e^{-\frac{j2\pi}{3}}$ is the average output current vector

$$\vec{V}_{\text{ref}} = R\vec{I}_o + L\frac{d}{dt}\vec{I}_o \tag{16}$$

IV. RESULTS

The topology in Fig. 3 along with the proposed control has been simulated in MATLAB/Simulink with ideal switches and experimentally verified on a laboratory prototype. The parameters for the simulation and experiments are chosen to be the same for a direct comparison. This section presents the key simulation and experimental results.

Fig. 11 shows the experimental setup. Integrated power module (IPM) APTGT75DU120TG from Microsemi is used to implement the semiconductor switches. A FPGA-based control platform (Xilinx XC3S500E) has been used to generate PWM signals. A high-frequency transformer has been designed with area product method and fabricated with a Ferrite core. The key design equations for core and window areas are given by (17) and (18), respectively. Equation (19) gives an expression for the rms of the secondary winding current $I_{s\text{RMS}}$. Turns ratio is

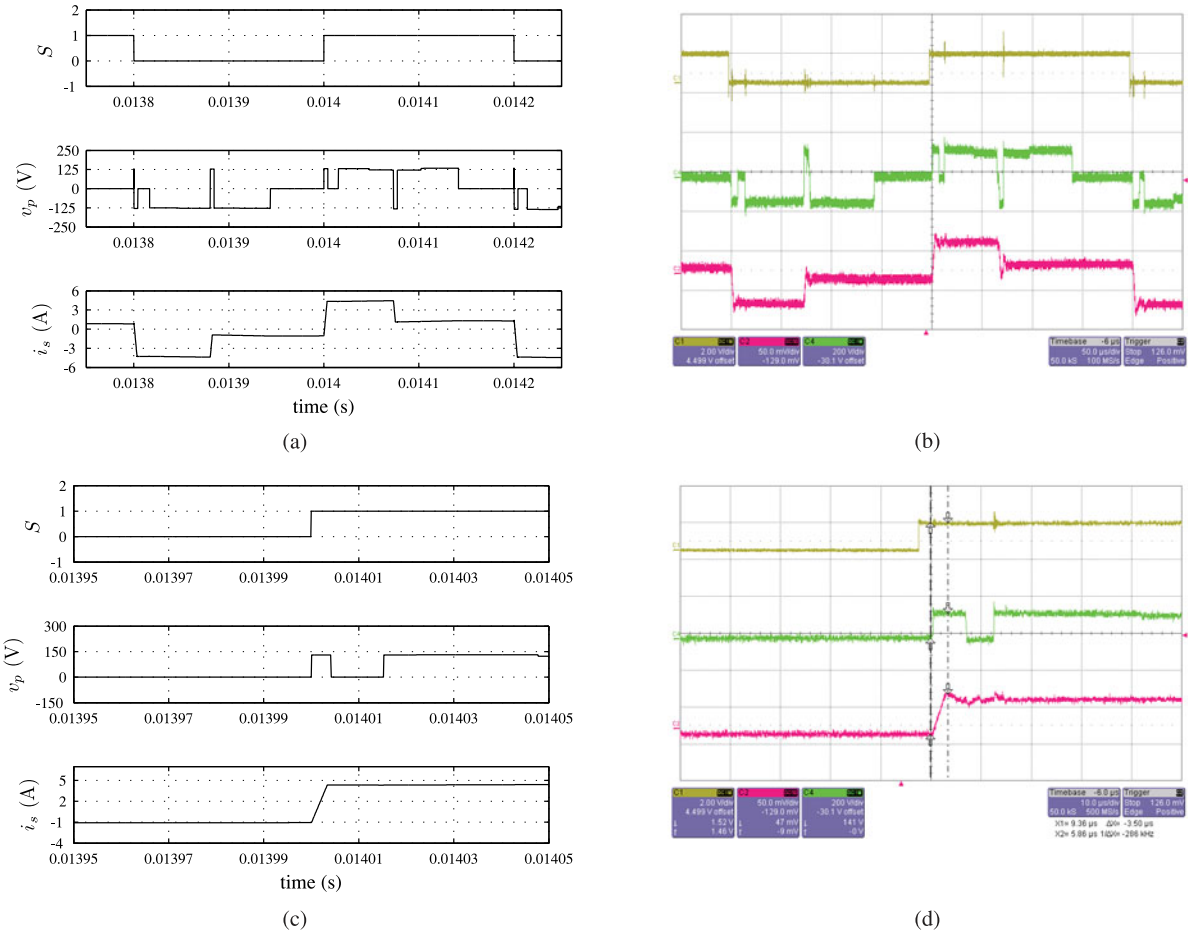


Fig. 14. (Top to bottom) S signal (CH1)(2 V/div), primary voltage (CH4) (200 V/div), secondary current (CH2) (5 A/div), (a) and (b) time 50 μs/div and (c) and (d) time 10 μs/div. (a) Simulation. (b) Experimental. (c) Simulation. (d) Experimental.

chosen to be unity for simplicity. A balanced *R–L* load and an induction machine are used as three-phase loads. A three-phase *LC* filter is used to eliminate switching frequency components from the grid current. Table IV provides the values of different relevant parameters for simulation and experiment. The commutation interval calculated from (15) is 2.6 μs. A commutation interval of $4\mu s$ is chosen for safe operation

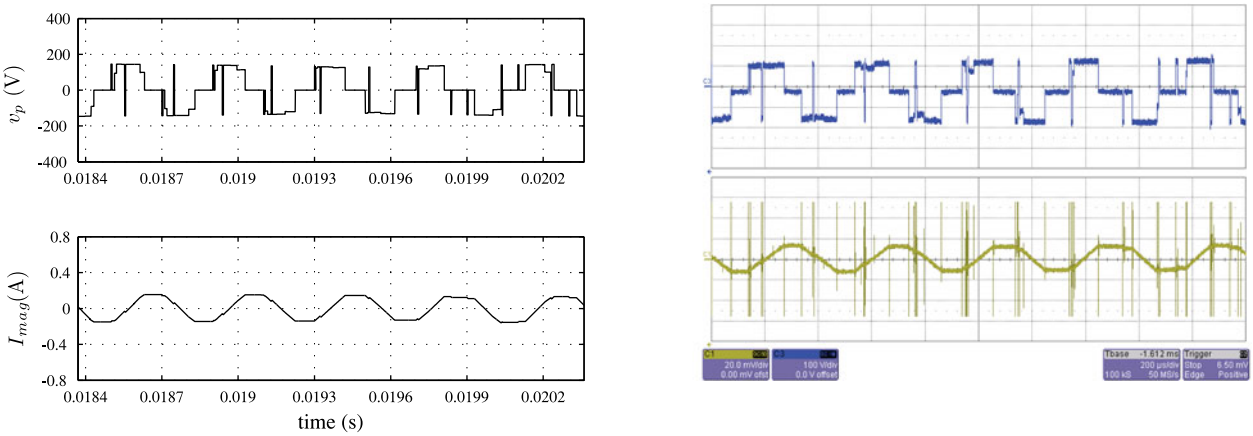
$$A_c = \frac{3m_I V_i}{4B_{pk} f_s N_1} \tag{17}$$

$$A_W K_W = \frac{2I_{s\mathrm{RMS}} N_2}{J} \tag{18}$$

$$I_{s\mathrm{RMS}}^2 = \frac{I_o^2}{8\pi}[4\pi + 9 + 3\sqrt{3} + m_V(3\cos 2\theta_o - 5\sqrt{3}\sin 2\theta_o)] \tag{19}$$

All the results are with series *R–L* load except the one specifically mentioned, is with induction motor (IM). Fig. 12 shows output line current along with line to neutral voltage of phase A. It also shows primary winding voltage and secondary winding current. The peak of the load current obtained from simulation is 4.3 A. A slightly lower peak of 4.15 A in the experimentally observed waveform can be attributed to the voltage drop across the semiconductor switches. Fig. 13 (top) shows the filtered grid line current of phase a along with the corresponding line to neutral voltage. This confirms input power factor correction (power factor = 0.99). Fig. 13 (bottom) presents the frequency spectrum of the grid current. A 1.56 A peak of the experimentally observed grid current waveform closely matches with its analytical prediction of 1.6 A, (10). The observed THD of the grid current is 2.8% from simulation and 3.1% from experiment. The experimentally observed efficiency is 92.22%.

The next set of results correspond to source-based commutation of leakage energy. Fig. 14(a) and (b) shows the voltage across the transformer primary winding along with secondary winding current (this is the current through the leakage inductance) over one cycle of the signal S. The maximum line-to-line voltage is applied by the input converter during commutation (when the secondary current has been changed). Fig. 14(c) and (d) shows a zoomed-in version of Fig. 14(a) and (b) during the transition of the signal S. The leakage inductor current linearly changes as expected from the analysis. The slope of the secondary winding current (experimentally observed value 1.6 A/μ) during commutation closely matches with its analytical prediction [see (14)]. A slight overshoot in the secondary current just after the commutation is due to the reverse recovery of an antiparallel diode in the secondary-side converter. Fig. 15



(a) (b)

Fig. 15. (Top to bottom) primary voltage (CH3)(100 V/div) and transformer magnetizing current(0.2 A/div), time 200 μs/div. (a) Simulation. (b) Experimental.

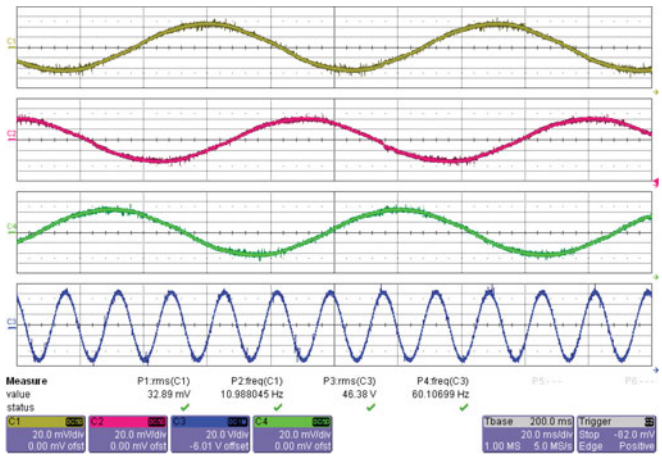


Fig. 16. Motor results: (top to bottom) Output line current phase A (CH1), phase B (CH2) and phase C (CH4) (2 A/div), input line to neutral voltage (CH3)(20 V/div), time 20 ms/div.

shows the primary voltage of the transformer along with the magnetizing current (obtained by taking a difference of primary and secondary current and turns ratio of the HFT is unity). This confirms flux balance.

A 1-hp, three-phase 230/460 V, 60-Hz four pole IM with a dc generator load is run in $\frac{V}{f}$ mode with an output frequency of 11 Hz. Fig. 16 shows three balanced output motor line currents along with input line to neutral voltage of phase A.

The conventional modulation described in Section II has been implemented with same parameters as shown in Table IV. The leakage inductance commutation during the switching of the output converter is done through an external clamp circuit and each leg in the load-side converter is switched with a dead-time of 4 μs (same as the commutation time set for the proposed modulation). Fig. 17 shows the instantaneous output line to neutral voltage of output phase A over one cycle of signal S for proposed and conventional modulation. These plots show substantially increased number of spikes in the line to neural voltage for the conventional method in comparison with the proposed technique. Substantial reduction in the fundamental

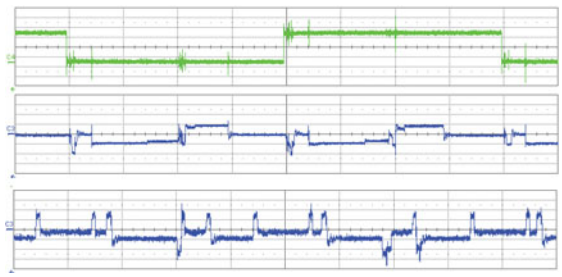


Fig. 17. Comparison results: (top to bottom) Signal S (0.5 V/div), output line to neutral voltage for proposed scheme and same for conventional scheme (50 V/div), time 50 μs/div.

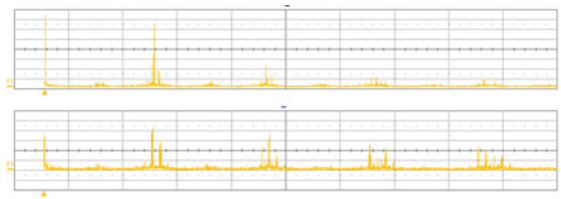


Fig. 18. Comparison results: (top to bottom) FFT of the output line to neutral voltage for proposed method (5 V/div), FFT of the same voltage for conventional scheme (vertical axis-5 V/div, horizontal axis-2.5 kHz/div).

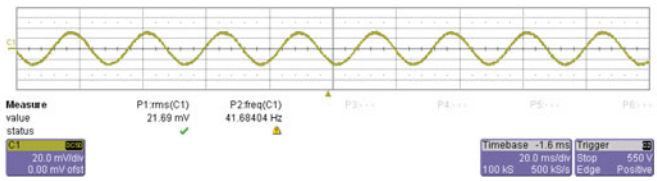


Fig. 19. Output line current of phase A for conventional modulation scheme (2 A/div).

component of the output voltage can be seen from the FFT of the output voltages in Fig. 18. This results in a lower peak of the load current (2.97 A) for the conventional scheme (see Fig. 19). So there is a 28.43 % reduction in the fundamental component of the output voltage.

V. Conclusion

The ac/ac power electronic transformer discussed in this paper has the following advantages: 1) high power density, 2) isolation, 3) single-stage bidirectional power conversion, 4) input power factor correction, 5) fewer semiconductor switches, and 6) minimum use of copper. One disadvantage of this topology is switching common-mode voltage and is an area of further research. In this paper, a novel modulation method along with a commutation technique has been proposed. This not only preserves all of the previously mentioned advantages but also results in 1) commutation of leakage energy without using any additional snubber circuits, 2) recovery of the leakage energy, 3) soft switching of output converter, and 4) minimization of the frequency of leakage inductance commutation which leads to less output voltage loss and increased frequency of operation. One shortcoming of the proposed commutation method is that it requires additional hard switching of the source-side converter. Experimental and simulation results confirm the operation of this converter topology with the proposed control.

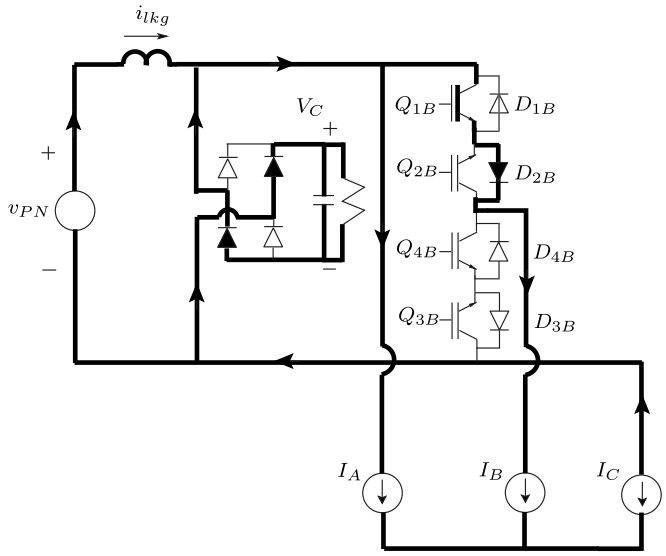


Fig. 20. Commutation with clamp circuit.

Appendix

A. Commutation With Clamp Circuit

The source-based commutation presented in Section III requires hard-switching of the grid-side converter. In certain applications, where the grid voltage is high, the primary-side converter may consist of relatively slow speed devices leading to considerable amount of switching loss. On the other hand, source-based commutation results in soft-switching of the load-side converter along with complete recovery of leakage energy. So purely from the loss point of view, the given application needs to be evaluated for both with and without source-based commutation. The alternative to source-based commutation is to use a snubber or clamp circuit. Commutation of leakage energy with a passive clamp circuit not only results in hard-switching of the load-side converter along with the loss of leakage energy, it also requires additional circuitry. The following analysis shows how to compute the energy lost in a passive clamp circuit. It also shows that to keep the commutation time within certain limits, the clamp voltage may have to be maintained at a higher value leading to higher blocking voltage rating of the switches in the load-side converter or alternatively reduce the frequency of operation.

Let us consider the case described in the commutation section, in the load-side converter the leg corresponding to output phase B is switching from bottom to top and currents I_A and I_B are positive (see Fig. 20). From modulation, voltage $v_{\rm PN} = v_{ab}\frac{N_2}{N_1}$. As a first step, we turn OFF Q_{4B} and turn ON Q_{1B}. If v_{PN} is positive, the commutation will start as described in Section III, but the magnitude of voltage $v_{\rm PN}$ may not be enough to finish the commutation before switch Q_{3B} is turned OFF. This will lead to the activation of the clamp circuit and hard-switching of Q_{3B}. If $v_{\rm PN}$ is negative, the commutation process will not start. Turning OFF of Q_{3B} will be hard-switched and it will activate the clamp circuit (see Fig. 20), and the current through the leakage inductance will start changing. In this stage, (20) holds. i_{lkg} at the beginning of this process is I_A. Solving (20) we get (21). The commutation process will be over when i_{lkg} changes from I_A to $I_A + I_B$. So the commutation time is given in (22). The clamp voltage V_c must be greater than $|v_{\rm PN}|$. To limit the commutation time, V_c must be considerably higher than the reflected maximum input line-to-line voltage. The switches in the load-side converter must be rated to block the clamp voltage V_c. Equation (23) gives an estimation of the energy lost in the clamp circuit for this particular example

$$\left[L_p\left(\frac{N_2}{N_1}\right)^2 + L_s\right]\frac{d}{dt}i_{lkg} = V_c + v_{\rm PN} \tag{20}$$

$$i_{lkg}(t) = I_A + \frac{V_c + v_{\rm PN}}{\left[L_p\left(\frac{N_2}{N_1}\right)^2 + L_s\right]}t \tag{21}$$

$$t_{\rm com} = \frac{\left[L_p\left(\frac{N_2}{N_1}\right)^2 + L_s\right]I_B}{V_c + v_{\rm PN}} \tag{22}$$

$$\int_0^{t_{\rm com}} V_c(I_A + I_B - i_{lkg}(t))dt = \frac{1}{2}\left[L_p\left(\frac{N_2}{N_1}\right)^2 + L_s\right]I_B^2\left(\frac{V_c}{V_c + v_{\rm PN}}\right) \tag{23}$$

References

[1] W. Shen, F. Wang, D. Boroyevich, and C. Tipton, "Loss characterization and calculation of nanocrystalline cores for high-frequency magnetics applications," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 475–484, Jan. 2008.

[2] W. Reass, D. Baca, R. F. Gribble, D. Anderson, J. S. Przybyla, R. Richardson, J. Clare, M. Bland, and P. Wheeler, "High-frequency multimegawatt polyphase resonant power conditioning," *IEEE Trans. Plasma Sci.*, vol. 33, no. 4, pp. 1210–1219, Aug. 2005.

[3] M. Das, C. Capell, D. Grider, R. Raju, M. Schutten, J. Nasadoski, S. Leslie, J. Ostop and A. Hefner, "10 kv, 120 a sic half h-bridge power MOSFET

modules suitable for high frequency, medium voltage applications," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2011, pp. 2689–2692.
[4] W. M. Murray, "Power conversion circuit having a high frequency link," U.S. Patent Application US3 517 300, Apr. 1968.
[5] E. Ronan, S. Sudhoff, S. Glover, and D. Galloway, "A power electronic-based distribution transformer," *IEEE Trans. Power Del.*, vol. 17, no. 2, pp. 537–543, Apr. 2002.
[6] C. G. C. Branco, R. Torrico-Bascope, C. M. T. Cruz, and F. de A Lima, "Proposal of three-phase high-frequency transformer isolation ups topologies for distributed generation applications," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1520–1531, Apr. 2013.
[7] X. She, A. Huang, and R. Burgos, "Review of solid-state transformer technologies and their application in power distribution systems," *IEEE J. Emerging Select. Topics Power Electron.*, vol. 1, no. 3, pp. 186–198, Sep. 2013.
[8] P. Drabek, Z. Peroutka, M. Pittermann, and M. cedl, "New configuration of traction converter with medium-frequency transformer using matrix converters," *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 5041–5048, Nov. 2011.
[9] M. Carpita, M. Marchesoni, M. Pellerin, and D. Moser, "Multilevel converter for traction applications: Small-scale prototype tests results," *IEEE Trans. Ind. Electron.*, vol. 55, no. 5, pp. 2203–2212, May 2008.
[10] M. Glinka and R. Marquardt, "A new AC/AC multilevel converter family," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 662–669, Jun. 2005.
[11] A. Garces and M. Molinas, "A study of efficiency in a reduced matrix converter for offshore wind farms," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 184–193, Jan. 2012.
[12] X. She, A. Huang, F. Wang, and R. Burgos, "Wind energy system with integrated functions of active power transfer, reactive power compensation, and voltage conversion," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4512–4524, Oct. 2013.
[13] H. Krishnamoorthy, P. Enjeti, I. Pitel, and J. Hawke, "New medium-voltage adjustable speed drive (asd) topologies with medium-frequency transformer isolation," in *Proc. 7th Int. Power Electron. Motion Control Conf.*, Jun. 2012, vol. 2, pp. 814–819.
[14] S. Falcones, X. Mao and R. Ayyanar, "Topology comparison for solid state transformer implementation," in *Proc. IEEE Power Energy Soc. General Meeting*, 2010, pp. 1–8.
[15] X. She, R. Burgos, G. Wang, F. Wang and A. Huang, "Review of solid state transformer in the distribution system: From components to field application," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2012, pp. 4077–4084.
[16] M. Sabahi, S. Hosseini, M. Sharifian, A. Goharrizi and G. Gharehpetian, "Zero-voltage switching bi-directional power electronic transformer," *IET Power Electron.*, vol. 3, no. 5, pp. 818–828, 2010.
[17] G. Wang, S. Baek, J. Elliott, A. Kadavelugu, F. Wang, X. She, S. Dutta, Y. Liu, T. Zhao, W. Yao, R. Gould, S. Bhattacharya and A. Huang, "Design and hardware implementation of gen-1 silicon based solid state transformer," in *Proc. IEEE 26th Appl. Power Electron. Conf. Expo.*, Mar. 2011, pp. 1344–1349.
[18] S. Bifaretti, P. Zanchetta, A. Watson, L. Tarisciotti, and J. Clare, "Advanced power electronic conversion and control system for universal and flexible power management," *IEEE Trans. Smart Grid*, vol. 2, no. 2, pp. 231–243, Jun. 2011.
[19] H. Fan and H. Li, "High-frequency transformer isolated bidirectional DC–DC converter modules with high efficiency over wide load range for 20 kVa solid-state transformer," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3599–3608, Dec. 2011.
[20] T. Zhao, G. Wang, S. Bhattacharya, and A. Q. Huang, "Voltage and power balance control for a cascaded h-bridge converter-based solid-state transformer," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1523–1532, Jan. 2013.
[21] M. Kang, P. Enjeti, and I. Pitel, "Analysis and design of electronic transformers for electric power distribution system," *IEEE Trans. Power Electron.*, vol. 14, no. 6, pp. 1133–1141, Nov. 1999.
[22] H. Krishnaswami and V. Ramanarayanan, "Control of high-frequency AC link electronic transformer," *IEE Proc. Electric Power Appl.*, vol. 152, no. 3, pp. 509–516, May 6, 2005.
[23] D. Chen, "Novel current-mode AC/AC converters with high-frequency ac link," *IEEE Trans. Ind. Electron.*, vol. 55, no. 1, pp. 30–37, Jan. 2008.
[24] R. A. X. Mao and S. Falcones, "A modular, interleaved AC-AC flyback topology for solid state transformer," in *Proc. FREEDM Annu. Conf.*, May 2009, pp. 221–224.
[25] D. Chen and Y. Chen, "Step-up AC voltage regulators with high-frequency link," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 390–397, Jan. 2013.
[26] H. Keyhani, H. Toliyat, M. Todorovic, R. Lai, and R. Datta, "An isolated resonant AC-link three-phase AC-AC converter using a single HF transformer," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5174–5183, Oct. 2014.
[27] H. Keyhani and H. Toliyat, "Isolated ZVS high-frequency-link ac-ac converter with a reduced switch count," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4156–4166, Aug. 2014.
[28] H. Qin and J. Kimball, "Solid-state transformer architecture using AC-AC dual-active-bridge converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3720–3730, Sep. 2013.
[29] J. Shah, R. Gupta, K. Mohapatra, and N. Mohan, "Power management with a dynamic power limit by a power electronic transformer for micro-grid," in *Proc. IEEE Power Energy Soc. General Meeting*, 2010, pp. 1–5.
[30] P. Wheeler, J. Rodriguez, J. Clare, L. Empringham, and A. Weinstein, "Matrix converters: A technology review," *IEEE Trans. Ind. Electron.*, vol. 49, no. 2, pp. 276–288, Apr. 2002.
[31] G. Castelino, K. Basu, R. Gupta, and N. Mohan, "Power electronic transformer with reduced number of switches: Analysis of input clamp circuit and a modulation strategy to eliminate input snubber requirement," in *Proc. IEEE 36th Annu. Conf. Ind. Electron. Soc.*, 2010, pp. 656–661.
[32] K. Basu and N. Mohan, "A power electronic transformer for three phase PWM AC/AC drive with loss less commutation and common-mode voltage suppression," in *Proc. IEEE 36th Annu. Conf. Ind. Electron. Soc.*, Nov. 2010, pp. 315–320.
[33] H. Cha and P. Enjeti, "A three-phase AC/AC high-frequency link matrix converter for VSCF applications," in *Proc. IEEE 34th Annu. Power Electron. Spec. Conf.*, Jun. 2003, vol. 4, pp. 1971–1976.
[34] K. Basu, A. Umarikar, K. Mohapatra and N. Mohan, "High-frequency transformer-link three-level inverter drive with common-mode voltage elimination," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2008, pp. 4413–4418.
[35] L. Huber and D. Borojevic, "Space vector modulated three-phase to three-phase matrix converter with input power factor correction," *IEEE Trans. Ind. Appl.*, vol. 31, no. 6, pp. 1234–1246, Nov./Dec. 1995.
[36] C. Klumpner, F. Blaabjerg, I. Boldea, and P. Nielsen, "New modulation method for matrix converters," *IEEE Trans. Ind. Appl.*, vol. 42, no. 3, pp. 797–806, May/Jun. 2006.
[37] T. Nguyen and H. Lee, "Modulation strategies to reduce common-mode voltage for indirect matrix converters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 129–140, Jan. 2012.
[38] T. Nguyen and H. Lee, "A new SVM method for an indirect matrix converter with common-mode voltage reduction," *IEEE Trans. Ind. Informat.*, vol. 10, no. 1, pp. 61–72, Feb. 2014.
[39] M. Matsui, M. Nagai, M. Mochizuki, and A. Nabae, "High-frequency link DC/AC converter with suppressed voltage clamp circuits-naturally commutated phase angle control with self turn-off devices," *IEEE Trans. Ind. Appl.*, vol. 32, no. 2, pp. 293–300, Mar./Apr. 1996.
[40] S. Mazumder and A. K. Rathore, "Primary-side-converter-assisted soft-switching scheme for an AC/AC converter in a cycloconverter-type high-frequency-link inverter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4161–4166, Sep. 2011.
[41] R. Garcia-Gil, J. Espi, E. Dede, and E. Sanchis-Kilders, "A bidirectional and isolated three-phase recepsier with soft-switching operation," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 765–773, Jun. 2005.
[42] A. Shahani, K. Basu and N. Mohan, "A power electronic transformer based on indirect matrix converter for PWM AC drive with lossless commutation of leakage energy," in *Proc. 6th IET Int. Power Electron., Mach. Drives*, Mar. 2012, pp. 1–6.

Kaushik Basu (S'07–M'13) received the B.E. degree from the Bengal Engineering and Science University, Shibpore, India, in 2003, the M.S. degree in electrical engineering from the Indian Institute of Science, Bangalore, India, in 2005, and the Ph.D. degree in electrical engineering from the University of Minnesota, Minneapolis, MN, USA, in 2012, respectively.

He was a Design Engineer with ColdWatt India, Bangalore, India, in 2006. He is currently the Electronics and Control Engineer with Dynapower Company LLC, VT, USA. His research interests include high-frequency link converters, PWM techniques and grid tied converters with storage, and renewable energy sources.

Arushi Shahani was born in Delhi, India, in 1988. She received the Bachelor of Engineering degree in electrical and electronics engineering from the University Institute of Engineering and Technology, Chandigarh, India, in 2006. She has interned at Bharat Electronics Limited and the Indian Institute of Technology Delhi, India. She received the master's degree in electrical engineering from University of Minnesota, Minneapolis, MN, USA, in 2013.

She is currently working in IBM, USA, as a Power Development Engineer. Her research interests include power electronics and motor control.

Ashish Kumar Sahoo (S'12) received the B.Tech. degree in electrical and electronics engineering from the National Institute of Technology, Trichy, India, in 2011, and the M.S. degree in electrical engineering from the University of Minnesota, Minneapolis, MN, USA, in 2013 where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include modular multilevel converters, matrix converters, power electronic transformers, and filter design.

Ned Mohan (S'72–M'73–SM'91–F'96–LF'12) received the B.Tech. degree from the Indian Institute of Technology Kharagpur, Kharagpur, India, in 1967, the M.S. degree in electrical engineering from the University of New Brunswick, Fredericton, Canada, in 1969, and the M.S. degree in nuclear engineering and the Ph.D. degree in electrical engineering from the University of Wisconsin, Madison, Wisconsin, in 1972 and 1973, respectively.

He is currently the Oscar A. Schott Professor of power electronics with the University of Minnesota, Minneapolis, MN, USA, where he has been engaged in teaching since 1976. He has numerous patents and publications in the field of power electronics, electric drives, and power systems. He has authored or coauthored five textbooks, one of which has been translated into six languages. He has graduated 35 Ph.Ds as of 2013.

Dr. Mohan received the 2008 IEEE PES Outstanding Educator Award, 2010 IEEE Undergraduate Teaching Award, 2010 UWIG Achievement Award from Utility Wind Integration Group, 2011 Distinguished Alumnus Award from IIT Kharagpur, India, and 2012 IEEE Power and Energy Society Ramakumar Family Renewable Energy Excellence Award. In 2013, he received the Innovative Program Award from the ECE Department Heads Association made up of more than 250 universities in the United States. He is a Member of National Academy of Engineering.