Systematic Input Filter Design of Matrix Converter by Analytical Estimation of RMS Current Ripple

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***Abstract*—A filter is required to eliminate the high-frequency switching ripple present in the input current of a matrix converter (MC). Design of such a filter requires an estimation of the higher harmonic components present in the input current. This paper presents a simple closed-form analytical expression for the RMS input current ripple injected by the MC. The expression shows the variation with load power factor and is independent of the output frequency. This is used in a step-by-step procedure to design various input filter components from the specifications of allowable total harmonic distortion in the grid current and distortion in the input voltage. The MC is modeled for the grid frequency component in order to evaluate the design for input power factor and voltage drop across the filter. A damping resistance has been designed ensuring minimum ohmic loss. The analytical estimation of the ripple current and the proposed design procedure have been validated by simulations in MATLAB/Simulink and experiments on a laboratory prototype.**

***Index Terms*—Indirect modulation, input power factor, matrix converter (MC), total harmonic distortion (THD).**

Nomenclature

i	Instantaneous.
$\bar{i}$	Averaged over fundamental cycle.
I	Amplitude of fundamental component.
i_{RMS,T_s}	RMS over T_s.
I_{RMS}	RMS over fundamental cycle.
I_{SWRMS}	Ripple component.
$I_{1\mathrm{RMS}}$	Fundamental component.
$\mathbf{I}$	Instantaneous space vector.
$\bar{\mathbf{I}}$	Average reference space vector.

I. Introduction

PULSE-WIDTH MODULATED (PWM) ac–ac converter systems have become widely used in the industry for high power conversion applications. Different converter topologies with and without a dc-link structure have been proposed in the literature [1]. The matrix converter (MC) converts three-phase ac to three-phase PWM ac of desired magnitude and frequency. It uses an array of controlled bidirectional switches to couple a three-phase grid with a three-phase load without the need of any intermediate energy storage. These converters can find use in large energy conversion systems such as motor drives, variable-frequency wind generators, and aircraft applications. Its unique properties such as bidirectional power flow, single-stage power conversion, open-loop input power factor correction, regenerative capability, and, most importantly, its minimum energy storage requirements, which eliminate the bulky dc-link capacitor, give it an upper hand [2], [3]. It has been concluded in [4] and [5] that MCs have lesser passive requirements than voltage-source-based back-to-back converters.

The input currents drawn from the three-phase grid contain higher frequency components along with the desired line frequency component. The fundamental component of the input current is a function of real power only [6], [7]. However, due to PWM, switching frequency components are injected along with the fundamental frequency component. A passive LC filter is used to eliminate these higher order harmonics and to draw high-quality currents from the grid [8]. Unlike MCs, the input filter design of dc-link-based converters has been extensively studied in the literature [9]–[11]. Input filter design for current source inverters can be found in [12] and [13]. A properly designed filter must also ensure the following: 1) minimum voltage drop; 2) high-quality voltage at the converter input; and 3) high grid power factor [14]. An MC, when integrated with filters, also has significantly reduced electromagnetic interference [15]. The input filter design also affects the weight and volume of the overall converter and, hence, the cost of equipment.

A suitable design of the input filter requires an estimation of the input current ripple. It is possible to obtain an analytical expression for the input current based on the modulation scheme [16]. However, estimation using these methods requires computation with complicated Bessel functions. These expressions also do not clearly show dependence of the input current spectrum on output/load power factor. In [17], input current harmonics due to unbalanced grid voltages are analytically evaluated using complex Fourier transforms and approximated by linearizing the input/output equations. In [18] and [19], ripple estimation of the input current is done based on a simulation model to design the input filter. The switching current ripple is approximated to be equal in magnitude to the fundamental

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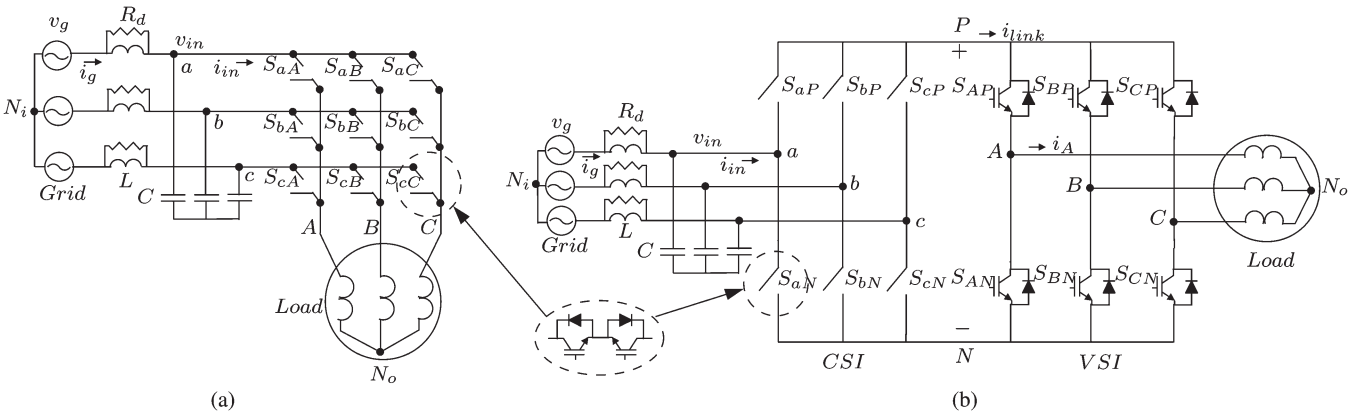

Fig. 1. (a) Conventional DMC topology. (b) Circuit diagram for the IMC.

component in [20]. No simple analytical expression for the input current ripple exists for an MC. In this paper, a simple closed-form analytical expression for the RMS input current ripple has been derived for space vector modulation (SVM) of MCs. This expression, by means of basic trigonometric functions, includes the effects of the modulation index, the load, and its power factor. This eliminates the need for complex calculations using special functions or a simulation model to estimate the input current ripple.

Different procedures have been proposed to design the passive components of the input filter. In [21], a design for a multistage LC filter based on cost function optimization has been provided using genetic algorithms with different constraints such as maximum amplitude of input current ripple, minimum power factor, maximum loss in damping resistor, maximum distortion in input voltage, and stability. In [4], the input filter is designed using a custom-developed automated filter design software. In [22], the proposed design is based on fundamental components. Input filter design for other configurations of an MC can be found in [23] and [24]. This paper presents a step-by-step design procedure for a single-stage LC filter of an MC. From the analytical estimation of the RMS input ripple current, the MC is modeled for the switching frequency component. Analyzing this model, the design equations are derived to get the values of the filter components from the specifications of the total harmonic distortion (THD) in the grid current and the acceptable distortion in the input voltage. A model at the grid frequency is used to evaluate the design for the input power factor, voltage drop across the filter, etc.

A resistance is needed to mitigate oscillations at and around the LC resonance frequency and to improve stability [25]–[27]. Modulation-based virtual damping techniques, although energy efficient, are usually complex and require additional control and sensor cost [28]–[30]. In this paper, the damping resistor is designed for minimum power loss.

The basic content of this paper was first introduced in [31]. Detailed analysis of modulation and derivation of the analytical expression for input RMS current ripple are presented in Section II. Filter design approach is explained in Section III. Extended simulation and experimental results with the same operating parameters are presented in Section IV for a direct comparison. This paper is concluded in Section V.

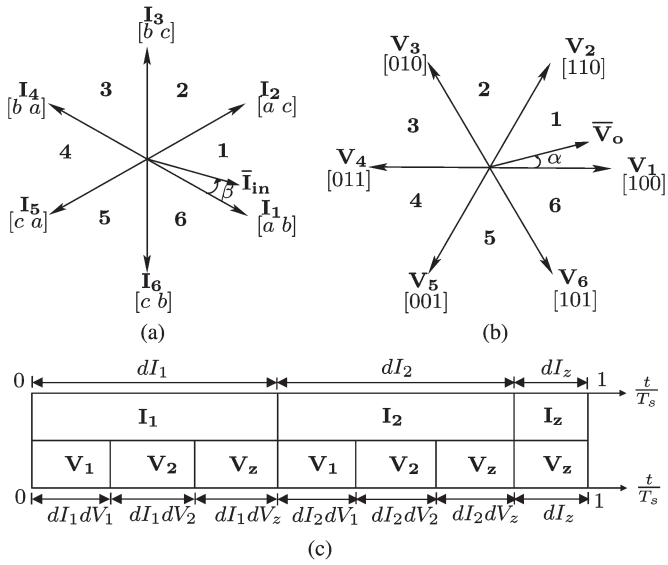

Fig. 2. (a) Current space vectors produced by CSI. (b) Voltage space vectors produced by VSI. (c) Switching sequence of the MC.

II. Analysis

The input filter design described in this paper requires modeling of the MC for different frequency components, which depends on the modulation technique. SVM-based indirect modulation technique is the most widely used modulation strategy to achieve the highest possible voltage transfer ratio and optimized switching pattern in an MC [32], [33] and is hence considered in this paper. This section describes the basic modulation of an MC and its modeling for filter design.

A. Indirect Modulation of MC

In indirect modulation, the MC is represented by two converters, as shown in Fig. 1(b). The grid-side converter acting as a current source inverter (CSI) and the load-side converter acting as a voltage source inverter (VSI) are connected through a virtual dc link. The CSI has six active and three zero switching states, as shown in Fig. 2(a). In this analysis, the space vector corresponding to a set of three-phase quantities x_a, x_b, x_c is a complex vector X, as given in

$$X = x_a + x_b e^{j2\pi/3} + x_c e^{-j2\pi/3}. \quad (1)$$

Here, $[a\ b]$ refers to the switching state when switches S_{aP} and S_{bN} are ON. The zero vectors occur when $[a\ a]$, $[b\ b]$, or $[c\ c]$ exist as switching states. Similarly, Fig. 2(b) shows the six active voltage space vectors of the VSI. [1 0 0] refers to a switching state when the switches S_{AP}, S_{BN}, and S_{CN} are ON. The VSI has two zero states given by [0 0 0] and [1 1 1]. Together, they can produce 18 active switching states of an indirect MC (IMC) or a conventional direct MC (DMC). For example, state $[a\ b\ b]$ in the DMC [see Fig. 1(a)], in which a is connected to output phase A and b is connected to output phases B and C, respectively, can be implemented by simultaneously applying $[a\ b]$ and [1 0 0] in the IMC topology of Fig. 1(b).

In one sampling cycle T_s (carrier frequency of $1/T_s$), the input reference current space vector $\bar{\mathbf{I}}_{\mathbf{in}}$ in Fig. 2(a) and the output reference voltage space vector $\bar{\mathbf{V}}_{\mathbf{o}}$ in Fig. 2(b) are generated from two adjacent active vectors whose duty ratios are respectively given by

$$dI_1 = m_I \sin\left(\frac{\pi}{3} - \beta\right) \quad dI_2 = m_I \sin\beta \tag{2}$$

$$dV_1 = \sqrt{3} m_V \sin\left(\frac{\pi}{3} - \alpha\right) \quad dV_2 = \sqrt{3} m_V \sin\alpha \tag{3}$$

and one zero vector for the remaining time period. Here, m_I is the ratio of peak of the fundamental component of the input current to the average virtual dc-link current, and m_V is the ratio of the peak of the fundamental component of the output voltage to the average virtual dc-link voltage. The switching sequence applied over a sampling cycle is given in Fig. 2(c).

B. Modeling of MC for Filter Design

To the input filter, the MC appears to be a voltage-dependent current source. Here, the MC is modeled as a current source both for the fundamental and higher harmonic components.

The average input current vector is aligned along the input voltage vector to obtain unity power factor. Thus, for the grid frequency, the MC can be modeled as a resistive load R_e. The RMS of the fundamental component of the average output voltage $V_{o1_{\mathrm{RMS}}}$ can be written in terms of the RMS of the fundamental component of the input line-to-neutral voltage $V_{\mathrm{in}1_{\mathrm{RMS}}}$ as

$$V_{o1_{\mathrm{RMS}}} = \frac{3}{2} m_I m_V V_{\mathrm{in}1_{\mathrm{RMS}}}. \tag{4}$$

Similarly, the RMS of the fundamental component of the average input current $I_{\mathrm{in}1_{\mathrm{RMS}}}$ can be written in terms of the peak of load current I_o as

$$I_{\mathrm{in}1_{\mathrm{RMS}}} = \frac{3}{2\sqrt{2}} m_I m_V I_o \cos\phi_o \tag{5}$$

where ϕ_o is the load power factor angle. Using these two equations, the effective resistance of the MC as seen by the input filter can be expressed in terms of the output load impedance ($|Z_L| = \sqrt{2} V_{o1_{\mathrm{RMS}}}/I_o$) as

$$R_e = \frac{V_{\mathrm{in}1_{\mathrm{RMS}}}}{I_{\mathrm{in}1_{\mathrm{RMS}}}} = \frac{|Z_L|}{\frac{9}{4}(m_I m_V)^2 \cos\phi_o}. \tag{6}$$

This is shown on a per-phase basis at the grid frequency in Fig. 3.

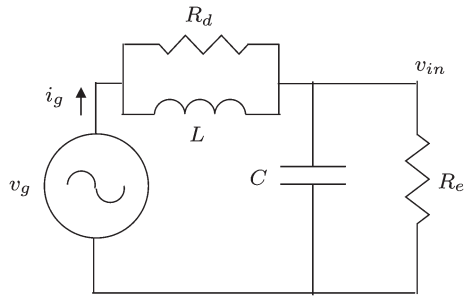

Fig. 3. Per-phase model at fundamental grid frequency.

In order to model the MC for higher order harmonics, the total RMS of the input current is analytically computed. As a first step, it is assumed that the output frequency is the same as the grid frequency. In order to simplify the computation, it is also assumed that the average output voltage vector was aligned along vector $\mathbf{V_1}$ when the average input current vector was aligned along vector $\mathbf{I_1}$. Later, it is shown from simulation and experimental results that the RMS of the input current computed with the two previous assumptions holds true even when 1) the input and output frequencies are different and 2) in case of same input and output frequency with a different alignment of average input current and output voltage vectors.

The average (over T_s) output phase A line-to-neutral voltage and line current are respectively given by

$$\overline{v_A} = V_o \cos(\omega_o t) \tag{7}$$

$$\overline{i_A} = I_o \cos(\omega_o t - \phi_o) \tag{8}$$

where V_o and I_o are amplitudes, ω_o is the output frequency, and ϕ_o is the load power factor angle. As shown in Fig. 2(c), one sampling cycle T_s is composed of time periods $dI_1 dV_1 T_s$, $dI_1 dV_2 T_s$, $dI_2 dV_1 T_s$, and $dI_2 dV_2 T_s$ when only active vectors are applied. In the following analysis, it is assumed that both $\bar{\mathbf{I}}_{\mathbf{in}}$ and $\bar{\mathbf{V}}_{\mathbf{o}}$ are in sector 1. During time period $dI_1 dV_1 T_s$, vector $\mathbf{V_1}$ [1 0 0] is applied by the output converter. Thus, the virtual dc-link current i_{link} is the same as the output phase A current. The switching state of the input converter during the same period is $[a\ b]$, corresponding to $\mathbf{I_1}$. Thus, the input phase a is connected to the output phase A through the virtual dc link, as shown in Fig. 4(a). Likewise, during $dI_1 dV_2 T_s$ period with vectors $[a\ b]$ and [1 1 0] applied, input line current $i_a = i_A + i_B = -i_C$, as shown in Fig. 4(b). Similarly, during $dI_2 dV_1 T_S$ period, $i_a = i_A$, and during $dI_2 dV_2 T_s$ period, $i_a = -i_C$, as shown in Fig. 4(c) and (d), respectively. Here, we assume that the output frequency f_o is much smaller than the sampling frequency of the converter, such that the output currents over a sampling cycle T_s remain constant and can be modeled as current sources. The direction of the load currents is assumed to be positive when it is flowing out of the leg. Hence, in the particular switching cycle shown in Fig. 4, the currents i_A and i_B are positive, and the current i_C is negative.

The RMS square of the input line current i_a over one sampling cycle T_s when both $\bar{\mathbf{I}}_{\mathbf{in}}$ and $\bar{\mathbf{V}}_{\mathbf{o}}$ are in their respective first sectors is given by

$$i^2_{a_{\mathrm{RMS},Ts_{\mathrm{SECTOR1}}}} = (dV_1 dI_1 + dV_1 dI_2)(i_A)^2 + (dV_2 dI_1 + dV_2 dI_2)(-i_C)^2. \tag{9}$$

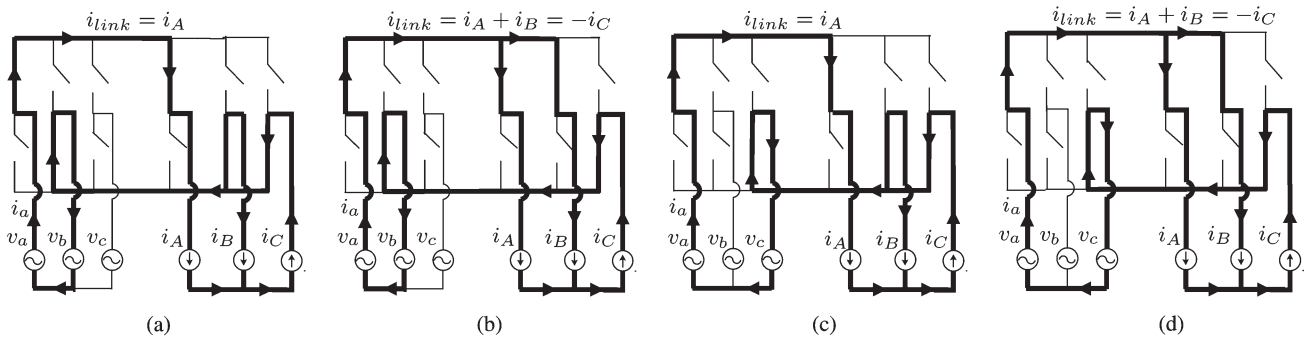

Fig. 4. Current flow paths for time periods (a) $dI_1dV_1T_s$, (b) $dI_1dV_2T_s$, (c) $dI_2dV_1T_s$, and (d) $dI_2dV_2T_s$ in sector 1.

Note that, due to assumptions made at the beginning of this analysis, at any instant, both vectors $\overline{\mathbf{I}}_{\mathbf{in}}$ and $\overline{\mathbf{V}}_{\mathbf{o}}$ will be in the same respective sectors, i.e., when $\overline{\mathbf{I}}_{\mathbf{in}}$ is in sector 2 in Fig. 2(a), $\overline{\mathbf{V}}_{\mathbf{o}}$ will be in sector 2 in Fig. 2(b). Similarly, it is possible to obtain the expressions for the RMS square of the input line current i_a over a sampling cycle when both the input current and output voltage space vector are in their respective second and third sectors, i.e.,

$$i^2_{a_{\mathrm{RMS},Ts_{\mathrm{SECTOR2}}}} = dV_1dI_1(-i_C)^2 + dV_2dI_1(i_B)^2 \quad (10)$$

$$i^2_{a_{\mathrm{RMS},Ts_{\mathrm{SECTOR3}}}} = dV_1dI_2(i_B)^2 + dV_2dI_2(-i_A)^2. \quad (11)$$

These expressions repeat for the other three sectors. Equation (12) shows how to relate RMS over one sampling cycle to the RMS over one sector. Assuming the output line currents are balanced and sinusoidal (8) and using (2), (3), and (12), it is possible to obtain the RMS square of the input line current i_a over one sector. Finally, the RMS square of i_a over one cycle of the fundamental component of input current can be obtained from the RMS square of each sector using (13). Thus,

$$I^2_{a_{\mathrm{RMS}_{\mathrm{SECTOR}}}} = \frac{1}{\pi/3}\int_{\mathrm{SECTOR}} i^2_{a_{\mathrm{RMS},Ts}}\, d(\omega_o t) \quad (12)$$

$$I^2_{a_{\mathrm{RMS}}} = \frac{1}{3}\sum_{i=1,2,3} I^2_{a_{\mathrm{RMS}_{\mathrm{SECTOR}i}}}. \quad (13)$$

Hence, the input RMS square current is obtained as in (14). The RMS square of the switching ripple current is obtained by subtracting the RMS square of the fundamental component from the total input RMS square current (15). Equations (14) and (15) provide simple analytical expressions in terms of modulation index, load current amplitude, and load power factor angle, i.e.,

$$I^2_{a_{\mathrm{RMS}}} = \frac{3\sqrt{3}m_I m_V I_o^2}{\pi^2}\left(\frac{\pi\sqrt{3}}{12}+\frac{3}{8}\right)(1+\cos 2\phi_o) + \frac{3\sqrt{3}m_I m_V I_o^2}{\pi^2}\left(\frac{\pi}{12}-\frac{\sqrt{3}}{16}\right)\sin 2\phi_o \quad (14)$$

$$I^2_{a_{\mathrm{SWRMS}}} = I^2_{a_{\mathrm{RMS}}} - \left(\frac{3}{2\sqrt{2}}m_I m_V I_o \cos\phi_o\right)^2. \quad (15)$$

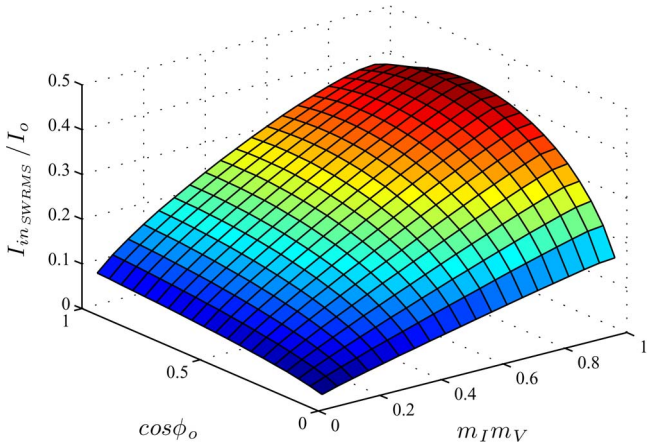

Fig. 5. Per-unit input RMS switching current with variation in load power factor and modulation index.

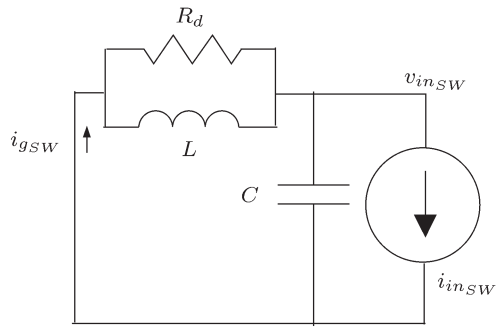

Fig. 6. Per-phase model at switching frequency.

Fig. 5 shows the variation of per-unit input RMS switching current with changes in modulation index and load power factor.

For the filter design at ripple frequency, the MC is modeled as a sinusoidal current source at frequency $1/T_s$, as shown in Fig. 6. The RMS of this current source is assumed to be given by (15). Due to PWM, the first group of dominant harmonic components in the input current waveform appears to be at and around the sampling frequency. The other harmonic components with appreciable magnitude occur at and around multiples of the sampling frequency. In this model, we assume that the entire energy in the input current other than the fundamental is concentrated at the switching frequency resulting in a slight overdesign of the filter components, which is a conservative approximation.

III. Filter Design

This section presents a step-by-step design procedure of a passive LC filter. In this design, the MC is modeled using the analysis given in the previous section. As discussed in the previous section, the input current is composed of a fundamental and a ripple component. In what follows, each of these components is separately considered using superposition principle.

The LC filter is designed such that the RMS of the ripple component of the grid current, i.e., $I_{g\mathrm{SWRMS}}$, must be within a limit in order to maintain a particular THD. According to IEEE 519 [34], THD in the grid current must be less than 5% of the fundamental component. For the proper operation of the MC, the input voltage of the MC must be below a certain amount of higher harmonic ripple, i.e., $V_{\mathrm{in}_{\mathrm{SWRMS}}}$. In order to mitigate oscillations near the LC resonance frequency and to provide stability, a damping resistor is introduced in parallel with L. Other forms of passive damping have been also proposed in the literature, which include a parallel or a series damping resistor with the filter capacitor. However, it has been reported that a parallel damping resistor with the filter inductor results in minimum power consumption and ensures stability of the overall system [25]. The parallel damping resistor in this paper is designed to restrict the power loss to a minimum.

The inputs to the design procedure are rated power of the converter P, grid voltage $V_{g\mathrm{RMS}}$ at frequency f_g, fundamental component of the load voltage magnitude $V_{o1\mathrm{RMS}}$, power factor of the load $\cos\phi_o$, and converter switching frequency f_s. The step-by-step procedure is as follows.

1) Calculate the amplitude of load current I_o and the modulation index of the MC, assuming no power loss in the MC and no voltage drop in the grid frequency component across the input filter inductance. This is as shown in the first step of the flowchart in Fig. 7.
2) From the calculated value of load current magnitude I_o and modulation index $m_I m_V$ in Step 1, the fundamental component of input current is calculated, neglecting the power loss in the MC. The load impedance Z_L is computed as the ratio of the load voltage and load current.
3) For modeling the MC at the grid frequency, the effective resistance R_e is calculated using (6). In addition, compute the input RMS current ripple injected by the MC using (15).
4) Select the grid current THD and the distortion in the input voltage as a function of their fundamental components, as well as the fraction of the allowable power loss to total power in damping resistor, as shown in

$$\lambda_1 = \frac{I_{g\mathrm{SWRMS}}}{I_{\mathrm{in1RMS}}} \quad \lambda_2 = \frac{V_{\mathrm{in}_{\mathrm{SWRMS}}}}{V_{g\mathrm{RMS}}} \quad \lambda_3 = \frac{P_{\mathrm{loss}}}{P}. \tag{16}$$

5) Analyzing the circuit in Fig. 6, it is possible to express the ripple in the grid current $I_{g\mathrm{SWRMS}}$ and the distortion in input voltage $V_{\mathrm{in}_{\mathrm{SWRMS}}}$ in terms of $I_{\mathrm{in}_{\mathrm{SWRMS}}}$, as shown in (17) and (18). Analyzing the circuit for the fundamental component at grid frequency, $\omega_g = 2\pi f_g$ in Fig. 3, it is possible to compute the ratio of the power loss P_{loss} in the damping resistor to the total output power P of the converter as in (19). The power loss is considered only due to the fundamental component of the current as most of the higher order harmonics of the input current pass

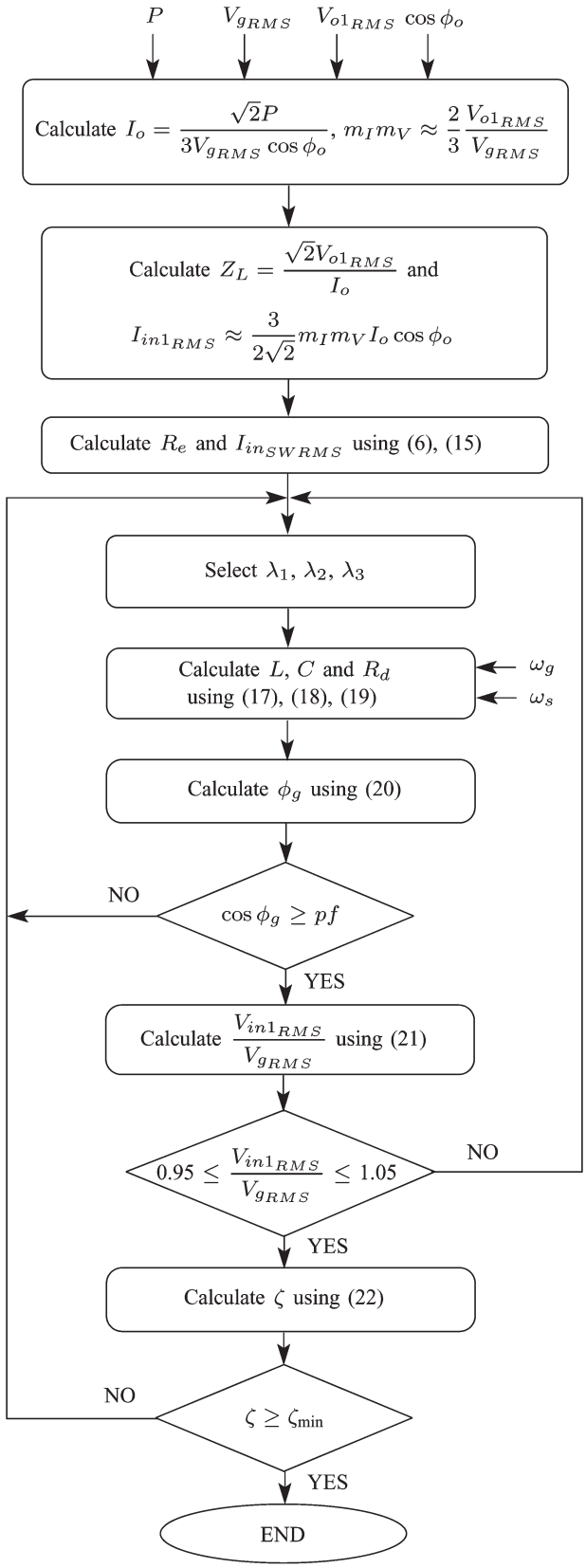

Fig. 7. Flowchart for filter design of MC.

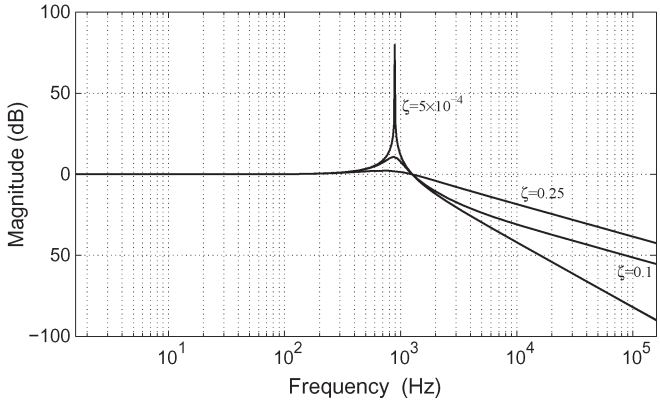

Fig. 8. Bode magnitude plot of the transfer function between grid and input currents of the MC.

through the filter capacitor. Equations (17)–(19) can be simultaneously solved to determine L, C, and R_d, i.e.,

$$I_{g\mathrm{SWRMS}} = \frac{I_{\mathrm{in}\mathrm{SWRMS}}}{\sqrt{1+\frac{(1-\omega_s^2 LC)^2-1}{\left(1+\frac{\omega_s^2 L^2}{R_d^2}\right)}}} \tag{17}$$

$$V_{\mathrm{in}\mathrm{SWRMS}} = \frac{I_{\mathrm{in}\mathrm{SWRMS}}}{\sqrt{\left(\omega_s C-\frac{1}{\omega_s L}\right)^2+\frac{1}{R_d^2}}} \tag{18}$$

$$\frac{P_{\mathrm{loss}}}{P} = \frac{I_{\mathrm{in1}\mathrm{RMS}}}{V_{g\mathrm{RMS}}}\left(\frac{\omega_g^2 L^2 R_d}{\omega_g^2 L^2+R_d^2}\right). \tag{19}$$

6) The design is verified by analyzing the model at grid frequency, as shown in Fig. 3. It is necessary that the grid current must be drawn close to a unity power factor, i.e., the angle ϕ_g in (20) must be close to zero, i.e.,

$$\phi_g = \tan^{-1}\omega_g C R_e + \tan^{-1}\frac{\omega_g L}{R_d} - \tan^{-1}\frac{\omega_g L(R_e+R_d)}{R_e R_d\left(1-\omega_g^2 LC\right)}. \tag{20}$$

If the grid power factor is below a minimum required power factor pf, then the specification of λ_1 needs to be changed, and the filter design process is iterated by going back to Step 4.

7) The voltage drop in the fundamental component across the filter must be negligibly small, i.e., the ratio $V_{\mathrm{in1}\mathrm{RMS}}/V_{g\mathrm{RMS}}$ must be close to unity, i.e.,

$$\frac{V_{\mathrm{in1}\mathrm{RMS}}}{V_{g\mathrm{RMS}}} = \frac{R_e\sqrt{R_d^2+\omega_g^2 L^2}}{\sqrt{\omega_g^2 L^2(R_e+R_d)^2+R_e^2 R_d^2\left(1-\omega_g^2 LC\right)^2}}. \tag{21}$$

If there is a large drop across the filter, the specification λ_2 is modified, and the filter parameters are recalculated.

8) The damping in the system needs to be tuned to provide a proper gain at the resonant frequency and maintain the whole system stable. As shown in the bode plot in Fig. 8 of the transfer function between grid current and input current of the MC, the resonant peak of the transfer function varies with different damping coefficients ζ. The value of ζ is determined by the damping resistance selected according to

$$\zeta = \frac{1}{2R_d}\sqrt{\frac{L}{C}}. \tag{22}$$

The damping coefficient of the input filter must be greater than a specified value for stable operation. The minimum value $\zeta_{\min}$ depends upon the particular application, [35]–[37]. If the value of the damping coefficient ζ of the designed filter is not within appropriate limits, then the specification λ_3 is changed, and the procedure is repeated.

The entire filter design procedure is shown in the flowchart in Fig. 7. The filter design procedure gives the values of L, C, and R_d. This analysis is done without considering the existence of grid-side inductance. Note that, in practical implementation, the grid inductance can be considered as a part of the designed filter inductor L.

This filter designed at rated power performs well at other lower power operations. A lesser power rating results in reduction in load current and, hence, fundamental input current also [see (5)]. Assuming the MC to be running at same modulation index and feeding a load with same power factor, the switching ripple in the input current $I_{\mathrm{in}\mathrm{SWRMS}}$ is also going to reduce likewise, (15). Hence, for the designed filter parameters L, C, and R_d, the ripple component in the grid current (17) and distortion in the input voltage (18) is going to reduce, as $I_{\mathrm{in}\mathrm{SWRMS}}$ reduces. Total demand distortion (TDD) specified by IEEE 519 is the distortion in grid current as a percentage of the fundamental component at rated power. Hence, the TDD improves at a lower operating power. The power loss in the damping resistor is mostly governed by the fundamental current. The fundamental component of the grid current also reduces with the operating power. Hence, the power loss is going to reduce as well. The voltage drop across the filter remains almost same.

At low power operation, the grid power factor angle rises, resulting in a lower grid power factor [25], [26]. This is quite normal at low power conditions, and this problem cannot be addressed with input filter design. The requirement of high grid power factor is generally at operations at higher power close to the rated power of the converter [18]. It has been shown in the literature that it is possible to improve the grid power factor angle at lower power rates by modifying the modulation of the MC in a closed-loop fashion [8].

IV. Simulation and Experimental Results

The power electronic converter system in Fig. 1 with the modulation strategy described in Section II is simulated with ideal switches in MATLAB/Simulink. A scaled-down laboratory prototype of the MC system implemented with the indirect topology is developed, as shown in Fig. 9. This section presents the key simulation and experimental results. The simulation and experimental results are taken under the same set of operating parameters and presented together for a direct comparison.

In the experimental setup, integrated power module APTGT75TDU120PG and APTGT75A60T1G from

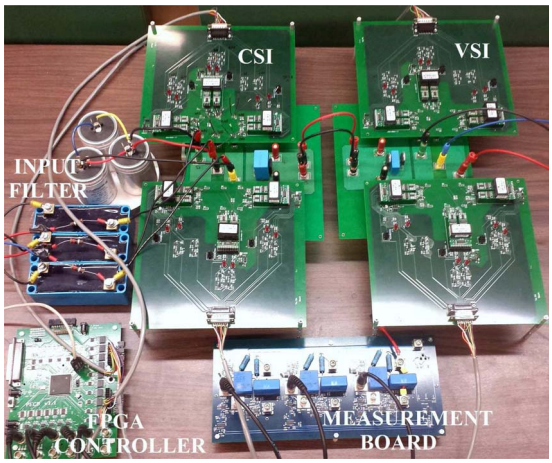

Fig. 9. Hardware setup.

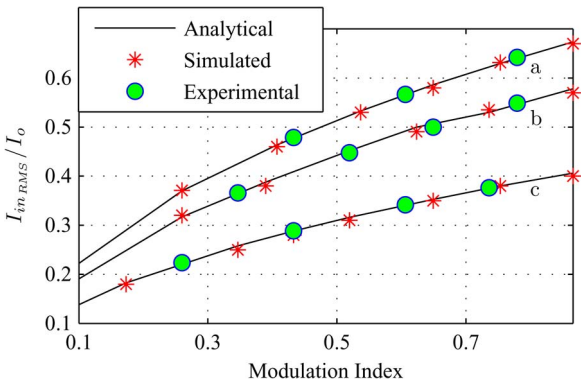

Fig. 10. Variation of input RMS current with modulation index and load power factor ($\cos\phi_o$ a: 0.91; b: 0.75; c: 0.5).

Microsemi is used to implement the CSI and the VSI, respectively. Insulated-gate bipolar transistor driver 2SD106AI from CONCEPT is used. A field-programmable-gate-array-based (Xilinx XC3S500E) control platform is used to generate the PWM signals. A diode-bridge-based clamp circuit is used for protection. The drive supplies a three-phase R–L load with switching frequency $(1/T_s)$ of 5 kHz. Different input and output frequencies of 60 and 30 Hz, respectively, were selected to show that the analytical expression (14), although derived for the same input and output frequencies, remains otherwise unchanged, as explained in Section II. Fig. 10 provides $I_{\text{in}_{\text{RMS}}}/I_o$ as a function of the modulation index and for three load power factors. The simulated and experimental points confirm the analytically predicted continuous plots.

For the rest of the simulation and experimental results, the drive runs a three-phase R–L load and an induction machine. The first set of results is with R–L load. The grid voltage used for the experiments is 150-V line-to-line RMS at 60 Hz. The modulation indices used are $m_I = 0.9$ and $m_V = 0.9/\sqrt{3}$. The PWM switching frequency $(1/T_s)$ is set at 5 kHz. Output three-phase sinusoidal currents are generated at 30 Hz across an R–L load with the following parameters: $R_{\text{load}} = 6\,\Omega$, $L_{\text{load}} = 27.5$ mH, and $\cos\phi_o = 0.75$. Using (6) and (15), it is possible to obtain an MC effective resistance of 21.3 Ω at 60 Hz and an RMS of input switching current ripple of $I_{\text{in}_{\text{SWRMS}}} = 3.9$ A, respectively. The filter parameters are calculated in Section III for an allowable ripple of 3% in grid current and input voltage and power loss in damping resistor $2 \times 10^{-3}\%$ of total power. The designed values are $L = 0.51$ mH, $C = 26.7$ μF, and $R_d = 18\,\Omega$. The designed filter capacitor values are for a star connection. In the experimental setup, the filter capacitors are connected in delta connection, as shown in Fig. 9. For a delta connection, the effective capacitance value required will be one third, as compared with a star configuration $(C/3)$.

Fig. 11 shows three-phase output line currents and line-to-neutral voltage of one phase at 30 Hz. The simulated current has an RMS of 7.66 A, as analytically predicted. The experimental waveforms have a slightly lower current RMS of 7.27 A, as compared with its analytical value of 7.66 A. This can be attributed to the voltage drops across the semiconductor devices. Fig. 12 shows the input line-to-neutral voltage and switched line current of phase a of the MC. The RMS value of the input current is 5.65 A from simulation and 5.64 A from experiments. The analytically calculated RMS value is 5.65 A from (14), which very closely matches the simulation and experimental values. The grid voltage and line current are shown in Fig. 13. It can be seen that the line current is almost in phase with the voltage and is nearly sinusoidal $(\cos\phi_g = 0.98)$. This confirms almost unity power factor correction. The frequency spectrums of the four input side waveforms are shown in Fig. 14. As can be seen, the fundamental components of the input voltage of the MC and grid voltage are almost equal. Thus, there is a negligible drop across the filter. In addition, the THD content in the grid current is very small, which validates the filter design procedure.

A 1-hp three-phase 230-/460-V 60-Hz four-pole induction motor is run by the MC under V/f control. The designed filter values are as follows: $L = 0.47$ mH, $C = 36.2$ μF, and $R_d = 12\,\Omega$. The selected V/f ratio is 3. The output frequency of the MC is set at 11 Hz, and the corresponding waveforms are shown in Fig. 15(a) and (b). Different input and output operating frequencies under V/f control are shown in Fig. 15(a). The nonfiltered input current and voltage with the corresponding filtered grid current and voltage waveforms are shown in Fig. 15(b) (top and bottom, respectively). This shows that the designed filter works well with an induction machine load.

The system was run at different output frequencies with the same 60-Hz input frequency, and the input RMS current was measured and is shown in Fig. 16 (top). Then, the system was run for the same output frequency but different output alignment angles, and results are shown in Fig. 16 (bottom). This was done while maintaining all other parameters constant, and the input current RMS remains constant regardless of the two parameters, as explained in Section II.

The system was run with different sets of filters for different allowable ripple specifications in the grid current. Fig. 17 shows the grid line-to-neutral voltage and grid current for allowable THD $= 1\%$ ($L = 0.51$ mH, $C = 82$ μF), THD $= 2.5\%$ ($L = 0.51$ mH, $C = 32.3$ μF), and THD $= 5\%$ ($L = 0.51$ mH, $C = 15.7$ μF). The resulting input power factors obtained are 0.85, 0.972, and 0.993, respectively. This shows that, with the reduction in the amount of allowable ripple in grid current for a fixed

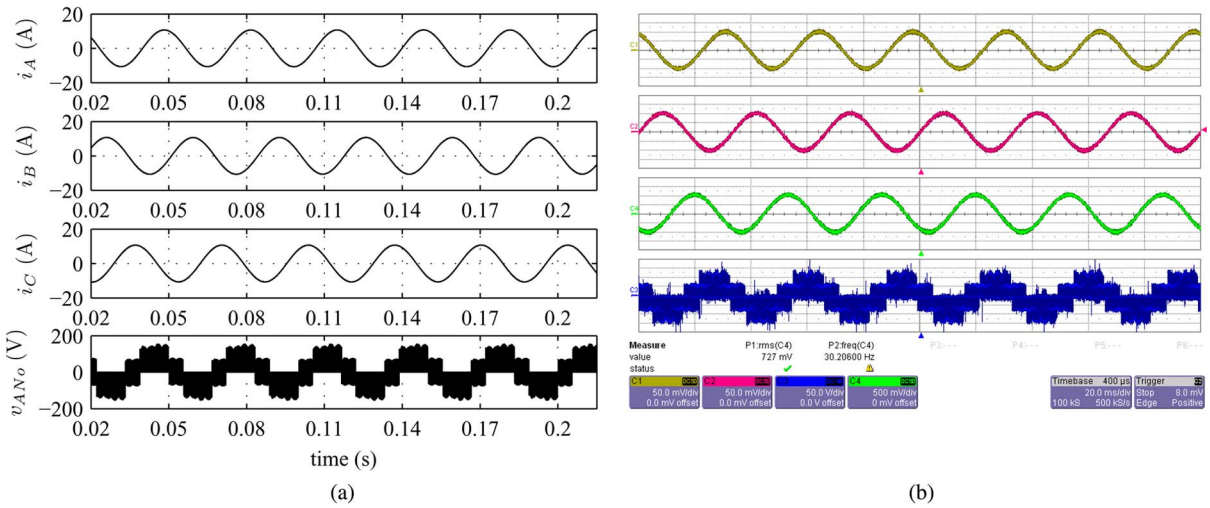

Fig. 11. (Top to bottom) Three output line currents (5 A/div) and output line-to-neutral voltage (50 V/div) of one phase for R–L load, time 20 ms/div. (a) Simulation. (b) Experimental.

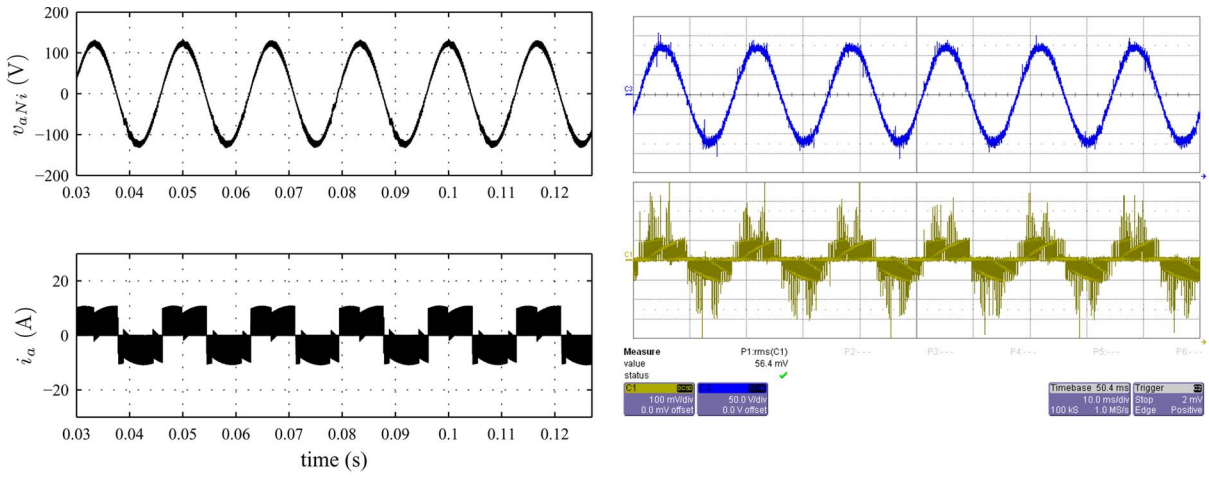

Fig. 12. (Top to bottom) Input line-to-neutral voltage (50 V/div) and input line current (10 A/div) for R–L load, time 10 ms/div. (a) Simulation. (b) Experimental.

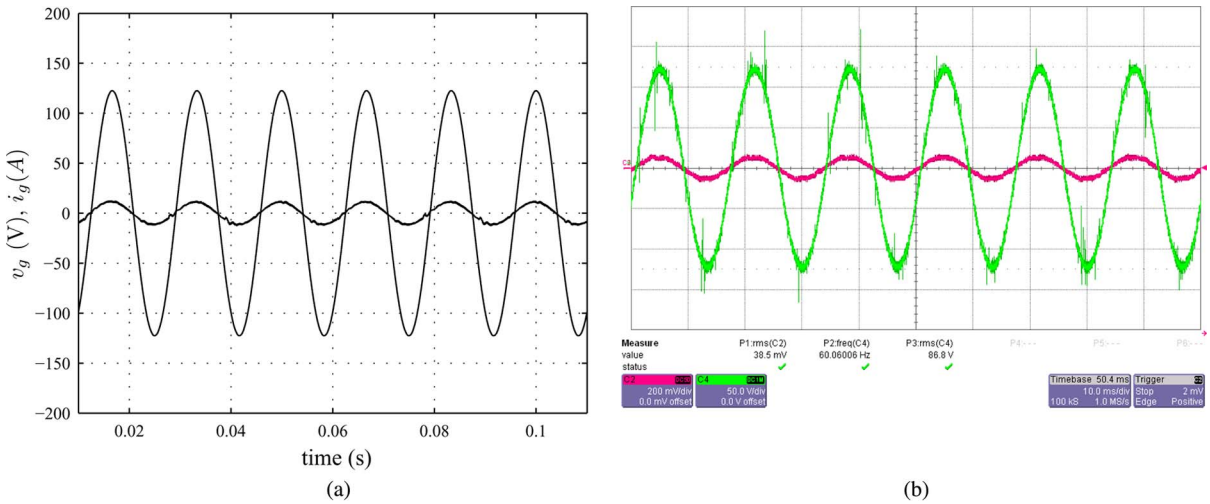

Fig. 13. Grid-side line-to-neutral voltage (50 V/div) and filtered grid-side line current (20 A/div), time 10 ms/div. (a) Simulation. (b) Experimental.

switching frequency, the inductance remains almost the same and the capacitance increases, resulting in a reduction in grid power factor, as shown in Fig. 18.

The MC was run at one half the rated power with the same filter, and the results are shown in Fig. 19. This was done keeping the load power factor and modulation index of the MC

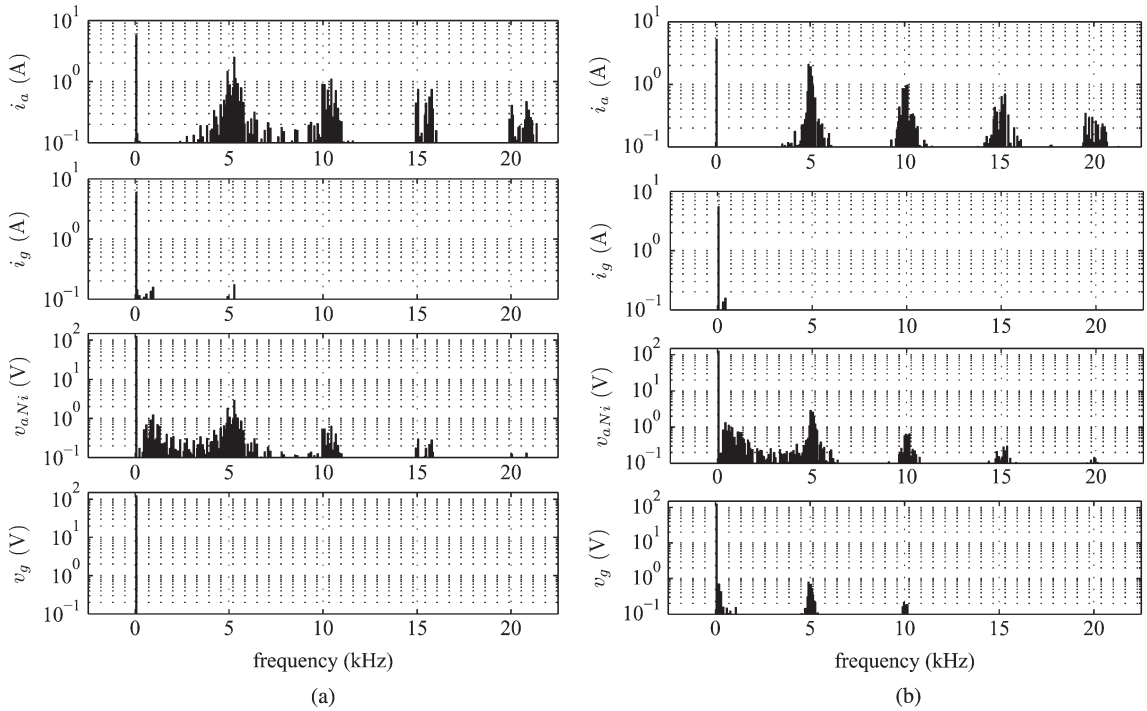

Fig. 14. Frequency spectrum. (Top to bottom) Input line current, filtered grid current, input line-to-neutral voltage, and grid line-to-neutral voltage (frequency scale: 5 kHz/div; Y-scale: logarithmic). (a) Simulation. (b) Experimental.

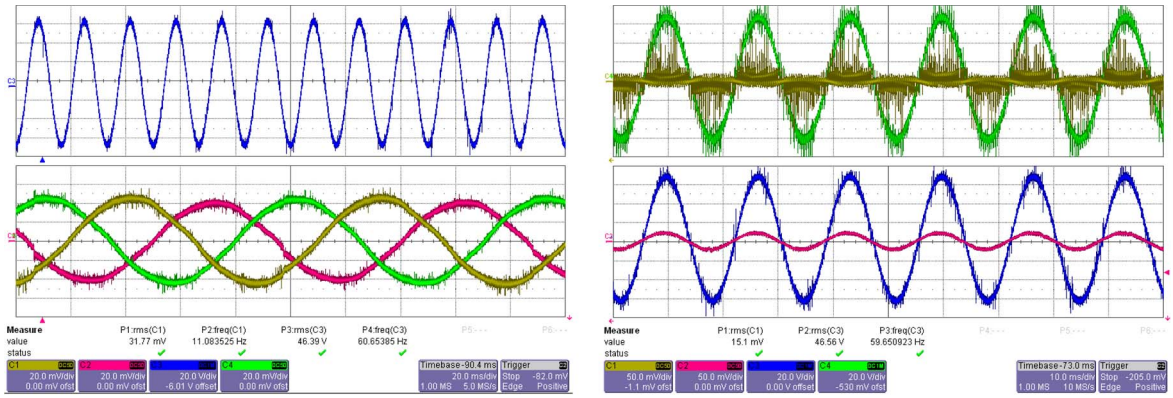

Fig. 15. (a) (top) Grid line-to-neutral voltage (20 V/div) and (bottom) three line currents at motor terminal (2 A/div). (b) (top) Per-phase input voltage (20 V/div) and line current (5 A/div) and (bottom) filtered grid voltage (20 V/div) and current (5 A/div) for induction motor load. (a) Experimental. (b) Experimental.

constant. The fundamental component of grid current has also reduced to one half. As seen from the fast Fourier transform (FFT) of grid current, the filter behaves well in meeting the TDD requirements (TDD $= 1.4\%$). The grid power factor has slightly decreased. The observed grid power factor at half the rated power is 0.93.

V. Conclusion

A step-by-step design to determine the input LC filter components for an MC has been presented. A simple closed-form analytical expression has been derived for the input RMS ripple current. It is found to be independent of the ratio of the input to the output frequency and depends only on the modulation index, the load, and its power factor. Based on this analysis, the MC is modeled for different frequency components, and simultaneous design equations are derived to calculate the LC values, based on specifications of allowable ripple in grid current and distortion in input voltage. The designed filter meets the THD specifications and ensures near-unity power factor, negligible drop across it, and minimum loss across the damping resistor. The MC was simulated in MATLAB/Simulink, and a laboratory hardware prototype was built to verify the results.

Appendix

A. Impact of Input Filter on Grid Power Factor

The design of input filter as described in Fig. 7 aims to meet the specification of THD in the grid current and obtain a high grid power factor. The grid power factor is used as an iterative check for this design. Thus, it is possible that, for a given set of operating parameters (power and grid voltage), the design might not converge. The following analysis in this appendix shows that this will not be the case.

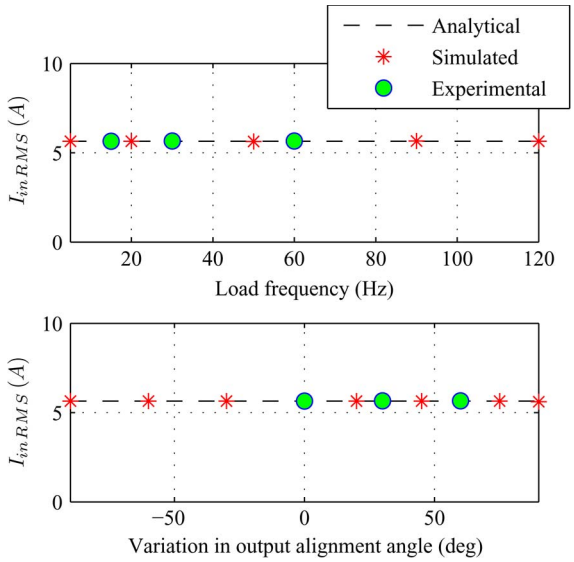

Fig. 16. Variation of input RMS current with (top) output frequency and (bottom) output alignment angle.

The switching ripple taken by the filter capacitor C is given by

$$I_{C_{\mathrm{SWRMS}}} = \sqrt{I^2_{\mathrm{in_{SWRMS}}} - I^2_{g_{\mathrm{SWRMS}}}} = I_o\sqrt{(k_1)^2 - (\lambda_1 k_2)^2}. \tag{23}$$

From (15), the switching ripple in input current $I_{\mathrm{in_{SWRMS}}}$ can be expressed as a function of the peak load current I_o ($I_{\mathrm{in_{SWRMS}}} = k_1 I_o$). In addition, the switching ripple in the grid current is decided by the specification λ_1 ($I_{g_{\mathrm{SWRMS}}} = \lambda_1 I_{in1_{\mathrm{RMS}}} = \lambda_1 k_2 I_o$). Here, k_1 from (15) and k_2 from (5) are functions of modulation index $m_I m_V$ and load power factor $\cos\phi_o$. The distortion in the input voltage is related to the capacitor ripple current by

$$\frac{I_{C_{\mathrm{SWRMS}}}}{2\pi f_s C} = V_{\mathrm{in_{SWRMS}}} = \lambda_2 \left(V_{g_{\mathrm{RMS}}}\right). \tag{24}$$

The real power of the system neglecting the losses can be expressed as

$$P = \frac{3}{\sqrt{2}} V_{o1_{\mathrm{RMS}}} I_o \cos\phi_o \approx \frac{3}{\sqrt{2}} \left(\frac{3}{2} m_I m_V V_{g_{\mathrm{RMS}}}\right) I_o \cos\phi_o. \tag{25}$$

This is assuming that the drop for the fundamental component of the voltage across the filter inductor is small, i.e., $V_{\mathrm{in1_{RMS}}} = V_{C1_{\mathrm{RMS}}} \approx V_{g_{\mathrm{RMS}}}$. The reactive power taken by the filter capacitor is given by

$$Q_C = 3 I_{C1_{\mathrm{RMS}}} V_{C1_{\mathrm{RMS}}} \approx 3\left(2\pi f_g C V_{g_{\mathrm{RMS}}}\right) V_{g_{\mathrm{RMS}}}. \tag{26}$$

Combining (23)–(26) and neglecting the reactive power drop across the filter inductor L, it is possible to obtain an expression of the grid power factor as

$$\begin{aligned}\cos\phi_g &\approx \cos\left(\tan^{-1}\left(\frac{Q_C}{P}\right)\right) \\ &\approx \cos\left(\tan^{-1}\left(\frac{2\sqrt{2}\sqrt{(k_1)^2 - (\lambda_1 k_2)^2}}{3\lambda_2 m_I m_V \cos\phi_o}\frac{f_g}{f_s}\right)\right).\end{aligned} \tag{27}$$

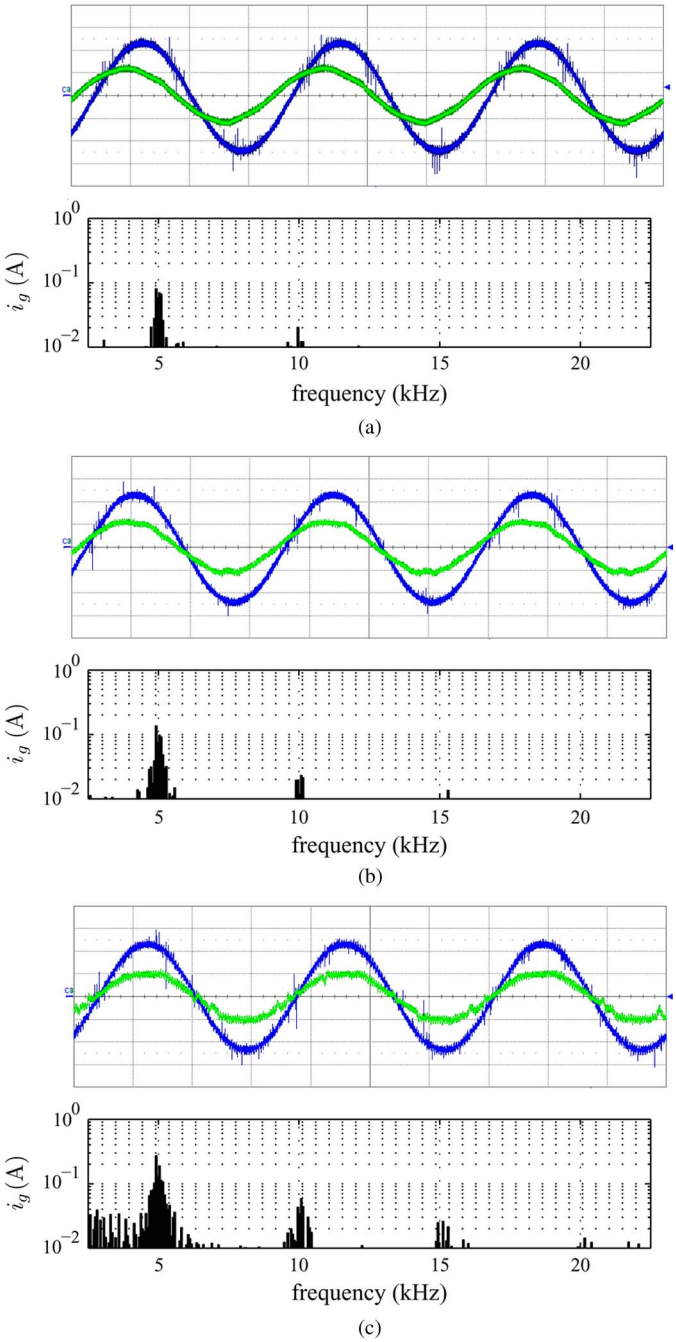

Fig. 17. (Top) Grid voltage (50 V/div) and filtered current (5 A/div) with (bottom) FFT of grid current for (a) allowable THD $= 1\%$, (b) allowable THD $= 2.5\%$, and (c) allowable THD $= 5\%$.

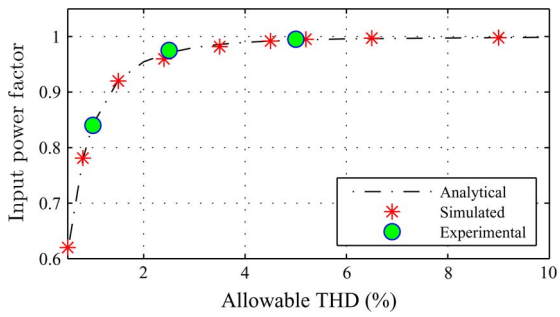

Fig. 18. Variation of input power factor with allowable THD limit.

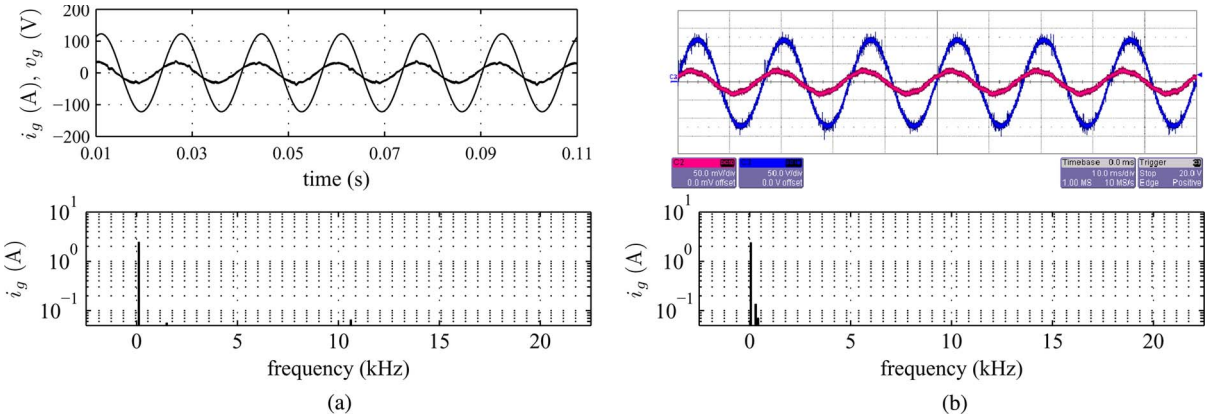

Fig. 19. Results at half the rated power. (Top) Grid-side line-to-neutral voltage (50 V/div) and grid current (5 A/div). (Bottom) FFT of grid current (frequency scale: 5 kHz/div; Y-scale: logarithmic). (a) Simulation. (b) Experimental.

From the utilization point of view, the converter will be operated close to the maximum modulation index of 0.866. A typical value of the load power factor, for example, for an induction machine load, is 0.8. For a nominal specification of grid THD and distortion in input voltage to be less than 5% of fundamental components, the power factor angle depends on the ratio of grid frequency and switching frequency ($\phi_g = \tan^{-1}(14.5(f_g/f_s))$). For a switching frequency of 5 kHz and a grid frequency of 60 Hz, the grid power factor turns out to be generally high ($\cos\phi_g = 0.985$), and it is independent of the chosen input data (power $= P$, and voltage $= V_{g_{\rm RMS}}$). From (27), it can be seen that, to meet a very low THD in grid current, the power factor can go slightly low, as shown in Fig. 18. This analysis also shows, as expected, that increasing the switching frequency results in smaller capacitor and better grid power factor for a similar set of specifications of grid current and input voltage THD.

B. Input Filter Capacitor Selection and Inductor Design

This appendix provides a list of specifications required for the selection of the filter capacitor and the design of the filter inductor. Completion of this step will result in an estimation of the volume and cost of the input filter.

The specifications for capacitor selection are as follows.

1) Its magnitude C.
2) RMS ripple current. For a safe design, it can be taken as the maximum value of $(I_{\rm inswRMS}/I_o)\sqrt{1-(\lambda_1/100)^2}$ in Fig. 5 multiplied by the peak of the maximum load current.
3) The maximum voltage across the capacitance must be approximately the peak of the grid voltage, i.e., $\sqrt{2}V_{g_{\rm RMS}}$. This is because, in a successful design, the voltage drop across the inductor is small and the voltage ripple in the input voltage of the converter is also negligible.

The list of specifications for inductor design is as follows.

1) The magnitude of the inductance L.
2) Maximum value of the peak of the fundamental component of the current, here, the grid current. For a proper design, as the reactive power drawn by the input filter is small at rated power, the peak of the grid current is independent of the designed filter, i.e., $\sqrt{2}P/3V_{g_{\rm RMS}}$.
3) Ripple current in the filter inductor. If the designed filter meets the specifications of grid THD ($< 5\%$), this ripple can be neglected.

From these specifications, following a standard design procedure as described in [38], it is possible to obtain an actual estimate of the volume and cost of the filter inductor.

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