Carrier-Based Implementation of SVPWM for Dual Two-Level VSI and Dual Matrix Converter With Zero Common-Mode Voltage

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***Abstract*—Pulse width modulation (PWM) converters generate switching common-mode voltages (CMVs) across the load terminals. These voltages cause common-mode currents, leading to bearing failure in motor loads and electromagnetic interference problems. This paper presents a generalized carrier-based PWM technique for open-end winding motor drives that completely eliminates switching CMV. The proposed method is applicable to both dual two-level voltage source inverter and dual matrix converter-based open-end winding drives. Detailed analysis shows that the carrier-based method requires significantly less computation compared to the corresponding space vector implementation. This paper also outlines the relationship between the two implementations. The carrier-based method is shown to achieve superior performance in terms of resource requirements and execution time when implemented on a field-programmable gate array-based real-time control platform. Simulation and experimental results have been presented to validate the proposed method.**

***Index Terms*—AC motor drive, carrier-based modulation, common-mode voltage (CMV), dual two-level inverter, dual matrix converter (MC), open-end winding drive, pulse width modulation (PWM).**

I. Introduction

PULSE width modulation (PWM) is the most commonly used switching technique for synthesizing adjustable magnitude and frequency ac due to reasons such as higher quality of the output voltage waveform, reduced filter requirement, and faster dynamic response. However, conventional PWM techniques for dc/ac two-level voltage source inverters (VSI) and three-phase ac/ac matrix converters (MC) cause high-frequency common-mode voltage (CMV) at the load terminals [1]–[5]. In case of a motor load, this can cause common-mode currents to flow through the motor bearings due to electrostatic coupling through parasitic capacitance. This leads to premature failure of motor bearings and undesirable electromagnetic interference (EMI). Passive common-mode filters are employed for impeding these common-mode currents [6]–[8]. Due to the use of additional filter components, this solution leads to reduced power density and reliability along with additional cost. PWM techniques have been proposed in the literature, both for VSI and MC, for the suppression of switching CMV [9], [10]. It can, however, cause a reduction in the quality of the output voltage waveform and achievable maximum voltage transfer ratio [11]. Multilevel converters have also been explored for CMV elimination: For example [12], [13] for three-level neutral-point-clamped converter (NPC), [14] for five-level NPC, and [15] for cascaded multilevel inverters.

Open-end winding drives consisting of two inverters are an alternative to NPC and cascaded multilevel inverters to gain more voltage levels in the output voltage waveform. An open-end winding drive was proposed in [16] and some more open-end winding drive configurations have been presented in [17] and [18]. Open-end winding drives not only give more voltage levels in the output, but the maximum output voltage for a given input voltage is more than that for a single converter. In addition, they can be controlled to eliminate CMV across the load. In [19], a space vector PWM technique has been presented for an open-end winding two-level VSI drive to eliminate switching CMV across the load. In [20], a two winding induction machine drive with dual two-level inverters is presented with a PWM method featuring CMV elimination as well. The idea of open-end winding drives has been extended to MC in [21], where a dual MC drive with CMV elimination and grid power factor control is presented. Dual multilevel converters for open-end winding drives with modulation strategies to eliminate CMV have also been proposed in the literature [22]–[27].

The PWM techniques presented in [9]–[27] use space vector implementation, except for the sine PWM method in [13]. As an alternative to space vector approach, carrier-based techniques are capable of producing same results as space-vector-based approaches, as concluded in [28]. In comparison with space vector modulation, carrier-based techniques can require less computation and result in simple implementation, as seen in [29]. They also give an insight into the relation between the duty ratios for converter switches and the reference output voltages and input voltages. A carrier-based approach for space vector PWM for two-level inverter has been presented in [29]. It is based on simple comparisons of the reference output voltage waveforms rather than computation of the reference output voltage space vector along with the sector identification process required by space vector approach. In [30] and [31], carrier-based PWM methods for MC have been presented. Carrier-based PWM techniques for multilevel and multiphase (more than three phases) inverters have been explored as well [32]–[35]. Carrier-based

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approaches have been studied together with space-vector-based approaches to observe relations between them and to compare them [35]–[37].

The SVPWM techniques with CMV suppression for dual VSI and dual MC have been proposed and developed in isolation. However, there are similarities in the PWM control of these two converters. A carrier-based implementation for the PWM control of the open-end winding dual two-level VSI drive has been presented in [38]. In this paper, the similarities between the PWM control of dual VSI and dual MC with CMV suppression are identified. Then, a generalized carrier-based PWM technique for open-end winding drive that includes both dual VSI and dual MC as the power converter has been presented. The generalized algorithm presented in this paper results in the computation of the duty cycle of each of the switches directly from the sensed input voltage and reference output voltage waveforms. There are no trigonometric and square root operations involved in any computation required for the proposed algorithm as opposed to the space vector approach. Overall, the carrier-based algorithm requires significantly less computation. Both space-vector-based and carrier-based algorithms have been implemented on a field-programmable gate array (FPGA)-based platform to compare resource requirement and the speed of computation. Simulation and experimental results have been presented to demonstrate the working of the carrier-based algorithm.

This paper is structured in a total of eight sections. Section I describes the dual converters and the space vectors to be used for PWM. The discussion in Section III gives the similarities between the two-level and MC cases and defines a general notation for the two platforms. In Section IV, the carrier-based algorithm has been derived, which is then compared to the space-vector-based approach in Section V. The simulation and experimental results are presented in Sections VI and VII, respectively. The conclusions are presented in Section VIII.

II. Dual MC, Dual VSI, and Synchronous Rotating Vectors

A dual converter consists of two converters of a given type, with one converter connected to each side of an open-end winding three phase load. A dual two-level inverter is shown in Fig. 1(a) and a dual MC system is shown in Fig. 1(b). In both systems, one converter is named positive-end converter and the other is named negative-end converter. The dual two-level inverter has two two-level VSIs, while the dual MC has two MCs.

The space vector of positive-end converter (for both dual VSI and dual MC) is defined as

$$\mathbf{U} = v_{\mathrm{AN}} + v_{\mathrm{BN}} e^{j\frac{2\pi}{3}} + v_{\mathrm{BN}} e^{j\frac{-2\pi}{3}} \tag{1}$$

The voltages v_{AN}, v_{BN}, and v_{CN} are voltages of positive-end output terminals A, B, and C, respectively, w.r.t. a point N. The point N is the negative terminal of the dc bus in the case of dual two-level inverter. In the case of dual MC, the point N is the neutral point of the input three-phase ac voltage.

A two-level VSI can synthesize three-phase ac output of adjustable amplitude and frequency from a dc voltage. There are a total of six switches [realized by six insulated-gate bipolar transistors (IGBTs)]. The upper and the lower switches in one leg are switched in complimentary fashion. So, there are eight total combinations, thus forming eight voltage space vectors. Six of these are active vectors while rest two have zero magnitude and are called zero vectors. These vectors are shown in Fig. 2(a). Each of the six active vectors is of magnitude V_{dc} i.e., the dc bus voltage and are fixed in position. As an example when terminal A of the load is connected to dc bus terminal P and load terminals B and C are connected to dc bus terminal N, the switching state (100) is obtained. Thus, the vector $\mathbf{U_1}$ is synthesized.

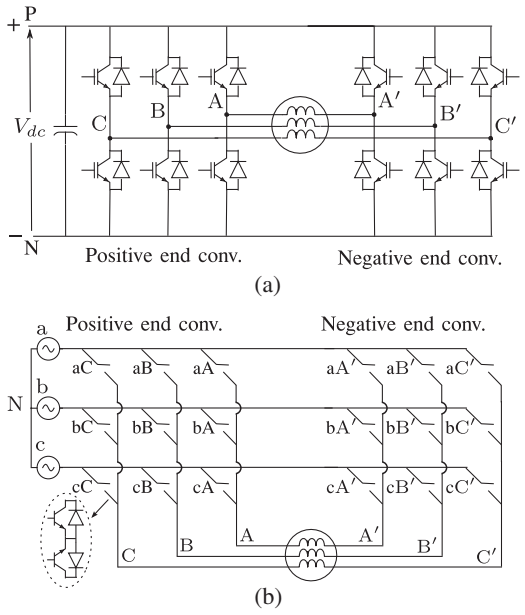

Fig. 1. (a) Dual two-level inverter. (b) Dual MC.

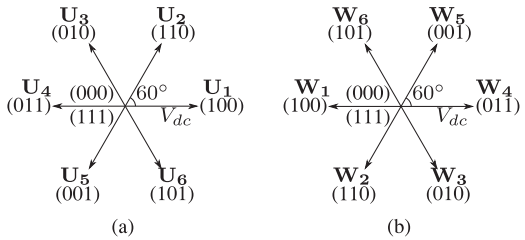

Fig. 2. Two-level VSI space vectors. (a) Positive-end space vectors. (b) Negative-end space vectors.

An MC can synthesize three-phase ac voltage of adjustable frequency and amplitude from a three-phase ac voltage source. The converter consists of nine switches (realized with 18 IGBTs), forming three legs. Each of these three legs can be in three different positions, resulting in 27 total switching states. Thus, there are 27 voltage space vectors for an MC. Out of these 27 space vectors, three vectors are zero vectors and 18 vectors are stationary but of varying magnitude in time. These 18 stationary vectors along with the three zero vectors are used in the indirect MC modulation technique [39]. The remaining six vectors have a constant magnitude of $\frac{3}{2}V_i$ (V_i is input peak

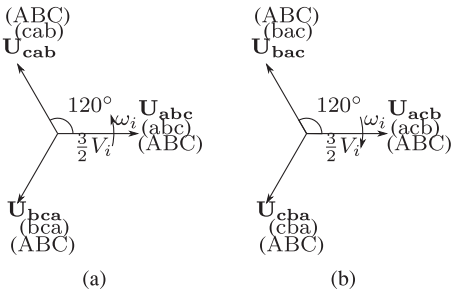

Fig. 3. Synchronously rotating vectors for positive-end MC. (a) CCW vectors. (b) CW vectors.

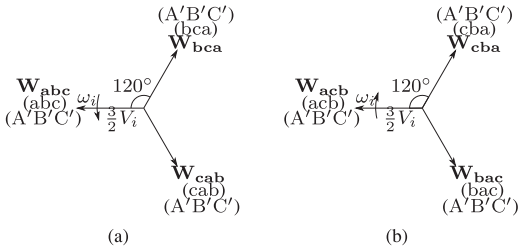

Fig. 4. Synchronously rotating vectors for negative-end MC. (a) CCW vectors. (b) CW vectors.

phase voltage) but keep rotating uniformly and are known as synchronously rotating space vectors. Three of these rotate in counterclockwise (CCW) direction with the input frequency ω_i and are called CCW vectors. The remaining three rotate in clockwise (CW) direction with the input frequency ω_i and are known as CW space vectors. The CCW and CW vectors for the positive-end MC are shown in Fig. 3(a) and (b), respectively. As an example, the switching state (cab) implies that the load terminals A, B, and C are connected to source terminals c, a, and b, respectively. This is done by turning ON switches cA, aB, and bC, and thus, the vector $\mathbf{U_{cab}}$ is applied. Similarly, the other vectors are formed.

The space vectors for the negative-end VSI are shown in Fig. 2(b). Note that the space vectors of the negative-end VSI are opposite in direction of those of corresponding positive-end VSI space vectors. Similarly, the CCW and CW vectors for the negative-end MC are shown in Fig. 4(a) and (b), respectively. These are opposite in direction to the CCW and CW vectors of the positive-end MC. The space vector of negative-end converter (for both dual VSI and dual MC) is defined as

$$\mathbf{W} = -(v_{\mathrm{A'N}} + v_{\mathrm{B'N}} e^{j\frac{2\pi}{3}} + v_{\mathrm{C'N}} e^{-j\frac{2\pi}{3}}) \tag{2}$$

The voltages $v_{\mathrm{A'N}}$, $v_{\mathrm{B'N}}$, and $v_{\mathrm{C'N}}$ are voltages of negative-end output terminals $\mathrm{A'}$, $\mathrm{B'}$, and $\mathrm{C'}$, respectively, w.r.t. a point N. The point N is the negative terminal of the dc bus in the case of dual two-level inverter and the neutral point of the input three-phase ac voltage in the case of dual MC.

For the negative-end VSI, when load terminal $\mathrm{A'}$ is connected to dc bus terminal P and load terminal $\mathrm{B'}$ and $\mathrm{C'}$ are connected to dc bus terminal N, the vector $\mathbf{W_1}$ is synthesized. Similarly, for the negative-end MC, when the load terminals $\mathrm{A'}$, $\mathrm{B'}$, and $\mathrm{C'}$ of the load are connected to terminals c, a, and b of the source, respectively, vector $\mathbf{W_{cab}}$ is synthesized. The other vectors are formed likewise.

The CMV at the load terminals is defined as

$$v_{\mathrm{com,pos}} = \frac{v_{\mathrm{AN}} + v_{\mathrm{BN}} + v_{\mathrm{CN}}}{3}$$
$$v_{\mathrm{com,neg}} = \frac{v_{\mathrm{A'N}} + v_{\mathrm{B'N}} + v_{\mathrm{C'N}}}{3} \tag{3}$$

The differential CMV $v_{\mathrm{com,diff}}$ defined in (4) is what affects circulating currents in open-end winding drives, as explained in [40]. The average of these CMVs defined (5) is what affects EMI, as explained in [1]

$$v_{\mathrm{com,diff}} = v_{\mathrm{com,pos}} - v_{\mathrm{com,neg}} \tag{4}$$

$$v_{\mathrm{com,sum}} = \frac{v_{\mathrm{com,pos}} + v_{\mathrm{com,neg}}}{2} \tag{5}$$

Based on these expressions, for the two-level VSI, vectors $\mathbf{U_1}$, $\mathbf{U_3}$, $\mathbf{U_5}$, $\mathbf{W_1}$, $\mathbf{W_3}$, and $\mathbf{W_5}$ have a CMV $\frac{V_{\mathrm{dc}}}{3}$. The vectors $\mathbf{U_2}$, $\mathbf{U_4}$, $\mathbf{U_6}$, $\mathbf{W_2}$, $\mathbf{W_4}$, and $\mathbf{W_6}$ have CMV of $\frac{2V_{\mathrm{dc}}}{3}$.

Thus, the set $\mathbf{U_1}$, $\mathbf{U_3}$, $\mathbf{U_5}$, $\mathbf{W_1}$, $\mathbf{W_3}$, and $\mathbf{W_5}$ can be used for converter control so that the CMV across the load $v_{\mathrm{com,diff}}$ is zero and the average of the CMVs $v_{\mathrm{com,sum}}$ is constant at $\frac{V_{\mathrm{dc}}}{3}$. The other set of vectors $\mathbf{U_2}$, $\mathbf{U_4}$, $\mathbf{U_6}$, $\mathbf{W_2}$, $\mathbf{W_4}$, and $\mathbf{W_6}$ can also be used to achieve zero differential CMV $v_{\mathrm{com,diff}}$, while keeping the average $v_{\mathrm{com,sum}}$ constant at $\frac{2V_{\mathrm{dc}}}{3}$. The first set is used for this paper. In the case of MC, for all of the CCW and CW synchronously rotating vectors (both positive and negative end), one phase of input is connected to only one phase of output at any given time. Hence, assuming that the input voltages are balanced and only synchronously rotating vectors are used for converter control, the CMVs defined in (3) for both positive and negative ends will always be zero. Hence, both differential ($v_{\mathrm{com,diff}}$) and average ($v_{\mathrm{com,sum}}$) CMVs are held at zero.

It should be noted that all the space vectors mentioned above have a nonzero magnitude. To create a zero vector (which is required in output voltage control), the same space vector is applied to both positive and negative converters (such as $\mathbf{U_1}$ and $\mathbf{W_1}$) to get zero voltage across the load. This is further discussed in the next section.

III. Generalized Analysis for Dual Converter Space Vectors

The space vectors for the positive-end and negative-end converters (both dual two-level VSI and dual MC) to generate zero CMV across the load are shown in Fig. 5(a) and (b), respectively. In Fig. 5, the space vectors $\mathbf{U_x}$, $\mathbf{W_x}$ and others can be related to the two-level inverter space vectors and MC CCW and CW vectors using Table I. The vectors for the positive and negative-end converters can be combined to give six resultant vectors applied across the three-phase load as shown in Fig. 6. For example, when space vectors $\mathbf{U_x}$ and $\mathbf{W_z}$ are simultaneously applied, the combined space vector $\mathbf{V_2}$ is obtained.

The six resultant vectors $\mathbf{V_1}$ to $\mathbf{V_6}$ form six sectors labeled 1 to 6 and their magnitude is $\sqrt{3}$ times the magnitude V of individual converter space vectors. The magnitude V of the

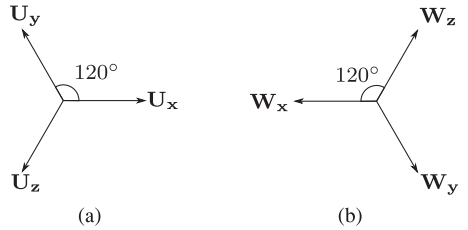

Fig. 5. (a) Generic positive-end space vectors. (b) Generic negative-end space vectors.

TABLE I
SPACE VECTORS FOR CCW, CW, AND TWO-LEVEL CASE

Generic vector	Two-level vector	CCW vector	CW vector
$\mathbf{U_x}$	$\mathbf{U_1}$	$\mathbf{U_{abc}}$	$\mathbf{U_{acb}}$
$\mathbf{U_y}$	$\mathbf{U_3}$	$\mathbf{U_{cab}}$	$\mathbf{U_{bac}}$
$\mathbf{U_z}$	$\mathbf{U_5}$	$\mathbf{U_{bca}}$	$\mathbf{U_{cba}}$
$\mathbf{W_x}$	$\mathbf{W_1}$	$\mathbf{W_{abc}}$	$\mathbf{W_{acb}}$
$\mathbf{W_y}$	$\mathbf{W_3}$	$\mathbf{W_{cab}}$	$\mathbf{W_{bac}}$
$\mathbf{W_z}$	$\mathbf{W_5}$	$\mathbf{W_{bca}}$	$\mathbf{W_{cba}}$

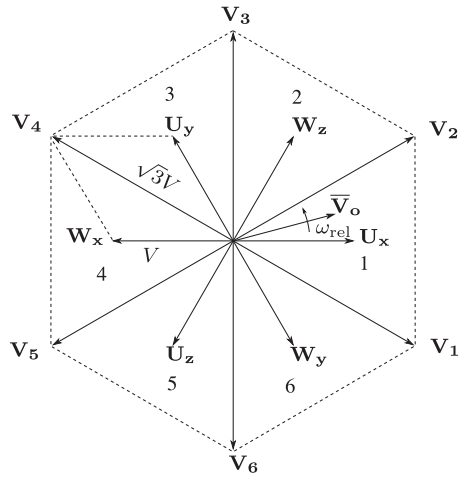

Fig. 6. Space vectors for dual converter.

individual converter space vectors is $V_{\rm dc}$ in the case of two-level vectors and $\frac{3}{2}V_i$ in the case of CCW and CW vectors. These vectors, along with three zero vectors defined in (6), are used to synthesize the reference output voltage vector $\overline{\mathbf{V}}_\mathbf{o}$ (bar indicates average over a switching cycle)

$$\begin{aligned}\mathbf{V_{zero,1}} &= \mathbf{U_x} + \mathbf{W_x} = 0\\ \mathbf{V_{zero,2}} &= \mathbf{U_y} + \mathbf{W_y} = 0\\ \mathbf{V_{zero,3}} &= \mathbf{U_z} + \mathbf{W_z} = 0\end{aligned} \tag{6}$$

The instantaneous output voltage vector $\mathbf{V_o}$ of the dual converter is formed by the sum of the positive-end and negative-end vectors $\mathbf{U}$ and $\mathbf{W}$, as given in (7). It can be seen that this voltage vector is formed by the voltages across the load phases, i.e., $v_{\rm AA'}$, $v_{\rm BB'}$, and $v_{\rm CC'}$

$$\begin{aligned}\mathbf{V_o} = \mathbf{U} + \mathbf{W} &= (v_{\rm AN} + v_{\rm BN}e^{j\frac{2\pi}{3}}\\ &\quad + v_{\rm CN}e^{-j\frac{2\pi}{3}}) + (-(v_{\rm A'N} + v_{\rm B'N}e^{j\frac{2\pi}{3}} + v_{\rm C'N}e^{-j\frac{2\pi}{3}}))\\ &= v_{\rm AA'} + v_{\rm BB'}e^{j\frac{2\pi}{3}} + v_{\rm CC'}e^{-j\frac{2\pi}{3}}\end{aligned} \tag{7}$$

Thus, the reference output voltages across the load phases will be defined between positive and negative-end terminals, i.e., $\overline{v}_{\rm AA'} = V_o\cos(\omega_o t)$, $\overline{v}_{\rm BB'} = V_o\cos(\omega_o t - \frac{2\pi}{3})$, and $\overline{v}_{\rm CC'} = V_o\cos(\omega_o t + \frac{2\pi}{3})$. The average output voltage vector $\overline{\mathbf{V}}_\mathbf{o}$ (averaged over a switching period) is formed using these voltages. The voltage $\overline{v}_{\rm AA'}$ indicates the voltage across output phase AA′ averaged over a single switching period. The voltages $\overline{v}_{\rm BB'}$ and $\overline{v}_{\rm CC'}$ indicate the same for output phases BB′ and CC′.

The absolute speed of rotation of the reference output voltage vector is equal to the desired output frequency ω_o

$$\overline{\mathbf{V}}_\mathbf{o} = \overline{v}_{\rm AA'} + \overline{v}_{\rm BB'}e^{j\frac{2\pi}{3}} + \overline{v}_{\rm CC'}e^{-j\frac{2\pi}{3}} = \frac{3}{2}V_o e^{j\omega_o t} \tag{8}$$

In Fig. 6, however, the frequency $\omega_{\rm rel}$ of $\mathbf{V_o}$ is the relative frequency of $\mathbf{V_o}$ with respect to the dual converter space vectors ($\mathbf{V_1}$, $\mathbf{V_2}$, etc.). This frequency is defined for the two-level, CCW, and CW vectors in (9), (10), and (11), respectively. It can be seen that if input frequency $\omega_i = 0$, then the expression for $\omega_{\rm rel}$ for two-level vectors in (9) is the same as $\omega_{\rm rel}$ for CCW and CW vectors in (10) and (11), respectively

$$\omega_{\rm rel} = \omega_o \quad \text{(for two-level vectors)} \tag{9}$$

$$\omega_{\rm rel} = \omega_o - \omega_i \quad \text{(for CCW vectors)} \tag{10}$$

$$\omega_{\rm rel} = \omega_o + \omega_i \quad \text{(for CW vectors)} \tag{11}$$

The output vector could be in one of the six sectors and the two space vectors bounding that sector are used to synthesize the output voltage vector on an average over a switching cycle. For example in Fig. 6, the output voltage vector is in sector 1, so the space vectors V_1 and V_2 are to be used to synthesize it. Suppose, the duty ratios of $\mathbf{V_1}$, $\mathbf{V_2}$, and $\mathbf{V_{zero,1}}$ are d_1, d_2, and $d_{\rm zero} = 1 - (d_1 + d_2)$, respectively. Then, the output voltage vector is synthesized as

$$d_1\mathbf{V_1} + d_2\mathbf{V_2} + (1 - d_1 - d_2)\mathbf{V_{zero,1}} = \overline{\mathbf{V}}_\mathbf{o} \tag{12}$$

From (6), (12), and Fig. 6, following is obtained:

$$\mathbf{U_x} + d_1\mathbf{W_y} + d_2\mathbf{W_z} + (1 - d_1 - d_2)\mathbf{W_x} = \overline{\mathbf{V}}_\mathbf{o} \tag{13}$$

From (13), it is observed that the positive-end converter vector $\mathbf{U_x}$ is ON for the entire switching period. The negative-end converter vectors $\mathbf{W_y}$ and $\mathbf{W_z}$ are ON with duty ratios d_1 and d_2, respectively, while the vector $\mathbf{W_x}$ is ON for the remaining period, i.e., with a duty ratio of $d_{\rm zero}$ in a switching cycle.

It should be noted that in the case of dual VSI, the proposed PWM scheme uses only one set of vectors out of $\mathbf{U_1}$, $\mathbf{U_3}$, $\mathbf{U_5}$, $\mathbf{W_1}$, $\mathbf{W_3}$, $\mathbf{W_5}$ and $\mathbf{U_2}$, $\mathbf{U_4}$, $\mathbf{U_6}$, $\mathbf{W_2}$, $\mathbf{W_4}$, $\mathbf{W_6}$. This will lead to an imbalance in conduction losses, since the lower IGBTs (connected to negative terminal N of dc bus) in positive and negative-end VSI will have twice the conduction period of upper IGBTs. This can be mitigated by using the two sets in

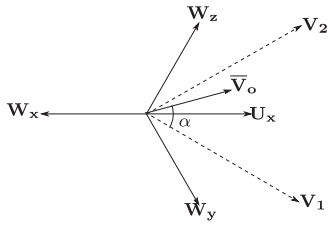

Fig. 7. $\overline{\mathbf{V}}_{\mathbf{o}}$ in Sector 1.

TABLE II
DUTY RATIOS d_1 AND d_2 IN ALL SIX SECTORS

Sector	d_1	d_2
1	$-m_y$	$-m_z$
2	m_x	m_y
3	$-m_z$	$-m_x$
4	m_y	m_z
5	$-m_x$	$-m_y$
6	m_z	m_x

alternate output fundamental frequency periods. This will cause the CMVs at positive and negative end to fluctuate between $\frac{V_{\rm dc}}{3}$ and $\frac{2V_{\rm dc}}{3}$, but at a frequency closer to output frequency rather than at the switching frequency and should not have effect on ground currents mitigation.

The switching losses, however, will be fairly balanced, because during three sectors, the positive-end converter is clamped (both in case of dual MC and dual VSI). The positive-end converter is switching during the rest three sectors and by applying the gate pulses such that each leg (in case of dual VSI) or each bidirectional switch (in case of dual MC) switches four times, thus equalizing number of switching transitions in all legs (dual VSI) or bidirectional switches (dual MC). The negative-end converter also has the same number of switching transitions. Thus, a dual VSI will have a total of four transitions per leg. A single VSI using conventional SVPWM (using all eight vectors) has only two transitions per leg in a switching period in all sectors. Thus, the dual VSI has twice the number of transitions compared to a single VSI. But as the voltage transfer ratio for dual converter is $\sqrt{3}$ times that of a single VSI, we can operate dual VSI at $\frac{1}{\sqrt{3}}$ times the dc bus of the single VSI to achieve same maximum output voltage. Hence, switching losses will increase by $\frac{2}{\sqrt{3}}$ times for the dual converter.

IV. DERIVATION OF CARRIER-BASED ALGORITHM

The duty ratios d_1 and d_2 will now be derived in terms of the reference output phase voltages and input phase voltages. Suppose the output voltage vector is in sector 1, as shown in Fig. 7.

For the CCW vectors, Table I and (13) give

$$\mathbf{U_{abc}} + d_1\mathbf{W_{cab}} + d_2\mathbf{W_{bca}} + (1-d_1-d_2)\mathbf{W_{abc}} = \overline{\mathbf{V}}_{\mathbf{o}} \tag{14}$$

Using (1), (2), (8), (14) and imposing that

$$\overline{v}_{\rm AA'} + \overline{v}_{\rm BB'} + \overline{v}_{\rm CC'} = 0$$

the duty ratios d_1 and d_2 can be derived in terms of input voltages and average output voltages as

$$d_1 = \frac{3\overline{v}_{\rm AA'}v_{\rm cN} + (\overline{v}_{\rm BB'} - \overline{v}_{\rm CC'})v_{\rm ab}}{3(v_{\rm bN}v_{\rm ab} - v_{\rm cN}v_{\rm ca})}$$
$$d_2 = \frac{3\overline{v}_{\rm AA'}v_{\rm bN} + (\overline{v}_{\rm BB'} - \overline{v}_{\rm CC'})v_{\rm ca}}{3(v_{\rm bN}v_{\rm ab} - v_{\rm cN}v_{\rm ca})} \tag{15}$$

The quantity in the denominator is a constant and simplifies to $-\frac{3\times 3}{2}V_i^2$. Also, $v_{\rm aN} = V_i\cos(\omega_i t)$ and $\overline{v}_{\rm AA'} = V_o\cos(\omega_o t)$ and so on. Using these expressions in (15) yields

$$d_1 = -\frac{V_o\cos((\omega_o-\omega_i)t - \frac{2\pi}{3})}{\frac{3}{2}V_i}$$
$$d_2 = -\frac{V_o\cos((\omega_o-\omega_i)t + \frac{2\pi}{3})}{\frac{3}{2}V_i} \tag{16}$$

After repeating the preceding computations for all six sectors for CCW and CW vectors and using the analysis done in [38] for two-level inverter vectors, Table II is obtained, where for CCW vectors, the phase modulation indexes (MIs) m_x, m_y, and m_z are given as

$$m_x = \frac{3\overline{v}_{\rm AA'}v_{\rm aN} + (\overline{v}_{\rm BB'} - \overline{v}_{\rm CC'})v_{\rm bc}}{\frac{9}{2}V_i^2} = \frac{V_o\cos((\omega_o-\omega_i)t)}{\frac{3}{2}V_i}$$
$$m_y = \frac{3\overline{v}_{\rm AA'}v_{\rm cN} + (\overline{v}_{\rm BB'} - \overline{v}_{\rm CC'})v_{\rm ab}}{\frac{9}{2}V_i^2} = \frac{V_o\cos((\omega_o-\omega_i)t - \frac{2\pi}{3})}{\frac{3}{2}V_i}$$
$$m_z = \frac{3\overline{v}_{\rm AA'}v_{\rm bN} + (\overline{v}_{\rm BB'} - \overline{v}_{\rm CC'})v_{\rm ca}}{\frac{9}{2}V_i^2} = \frac{V_o\cos((\omega_o-\omega_i)t + \frac{2\pi}{3})}{\frac{3}{2}V_i} \tag{17}$$

For CW vectors, the MIs m_x, m_y, and m_z are given as

$$m_x = \frac{3\overline{v}_{\rm AA'}v_{\rm aN} - (\overline{v}_{\rm BB'} - \overline{v}_{\rm CC'})v_{\rm bc}}{\frac{9}{2}V_i^2} = \frac{V_o\cos((\omega_o+\omega_i)t)}{\frac{3}{2}V_i}$$
$$m_y = \frac{3\overline{v}_{\rm AA'}v_{\rm bN} - (\overline{v}_{\rm BB'} - \overline{v}_{\rm CC'})v_{\rm ca}}{\frac{9}{2}V_i^2} = \frac{V_o\cos((\omega_o+\omega_i)t - \frac{2\pi}{3})}{\frac{3}{2}V_i}$$
$$m_z = \frac{3\overline{v}_{\rm AA'}v_{\rm cN} - (\overline{v}_{\rm BB'} - \overline{v}_{\rm CC'})v_{\rm ab}}{\frac{9}{2}V_i^2} = \frac{V_o\cos((\omega_o+\omega_i)t + \frac{2\pi}{3})}{\frac{3}{2}V_i} \tag{18}$$

For dual two-level inverter, the MIs m_x, m_y, and m_z are given as

$$m_x = \frac{\overline{v}_{\rm AA'}}{V_{dc}} = \frac{V_o\cos(\omega_o t)}{V_{dc}}$$

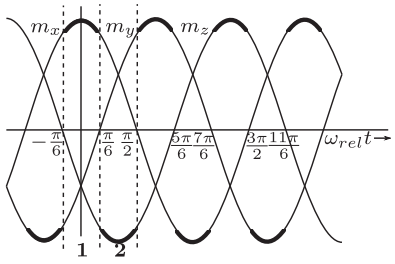

Fig. 8. MIs' waveforms.

$$m_y = \frac{\overline{v}_{\mathrm{BB}'}}{V_{dc}} = \frac{V_o \cos(\omega_o t - \frac{2\pi}{3})}{V_{dc}}$$
$$m_z = \frac{\overline{v}_{\mathrm{CC}'}}{V_{dc}} = \frac{V_o \cos(\omega_o t + \frac{2\pi}{3})}{V_{dc}} \tag{19}$$

Hence, in every sector, the duty ratios are a function of the phase MIs m_x, m_y, and m_z.

For the dual two-level inverter, the MIs are equal to reference phase voltages ($\overline{v}_{\mathrm{AA}'}$, $\overline{v}_{\mathrm{BB}'}$, $\overline{v}_{\mathrm{CC}'}$) divided by the dc bus voltage (V_{dc}). The frequency of these MIs is equal to output frequency ω_o which is also equal to the relative frequency for two-level case defined in (9).

For the dual MC, the amplitude of these MIs is the ratio of peak phase output voltage V_o and 1.5 times of input peak phase voltage V_i. The frequency of the three CCW MIs in (17) is equal to relative frequency ω_{rel} defined in (10). Similarly, the frequency for the CW MIs in (18) is the relative frequency defined in (11).

With these observations, a common algorithm can be used to find the duty ratios for different phases for both dual MC and dual two-level inverter. Fig. 8 shows the three-phase MIs against time.

In the figure, the maximum and the minimum MIs are highlighted in alternate sectors, e.g., sectors 1 and 2 (both bounded by vertical dotted lines) have the maximum MI and the minimum MI highlighted, respectively. Following observations are made.

1) In sector 1, the absolute value of phase modulation index m_x, i.e., $|m_x|$, is maximum among absolute values $|m_x|$, $|m_y|$, and $|m_z|$. In sector 1, the phase modulation index m_x is termed as the absolute maximum MI and the other two MIs (m_y and m_z) are termed nonmaximum MIs.
2) Throughout the sector 1, the positive-end converter is clamped and always applies one space vector, i.e., $\mathbf{U_x}$ and the modulation index m_x is absolute maximum and positive, as seen in Fig. 8. In other sectors as well, the sign of the MI which is absolute maximum decides which converter is clamped (positive for positive-end converter and negative for negative-end converter). The space vector applied by the clamped converter is corresponding to MI which is absolute maximum., i.e., $\mathbf{U_x}$ in sector 1 and so on.
3) In sector 1, for the negative-end converter, the duty ratios for space vectors corresponding to nonmaximum MIs (m_y, m_z), i.e., $\mathbf{W_y}$ and $\mathbf{W_z}$ are equal to d_1 and d_2, respectively. As seen from Table II, $d_1 = -m_y$ and $d_2 = -m_z$, i.e., the negative of nonmaximum MIs. In Fig. 8, the nonmaximum MIs m_y and m_z are negative in sector 1. Hence, $d_1 = |m_y|$ and $d_2 = |m_z|$. Thus, $\mathbf{W_y}$ and $\mathbf{W_z}$ are applied with duty ratios equal to absolute value of corresponding MIs.
4) In sector 1, the duty ratio of the negative-end converter for space vector corresponding to absolute maximum MI (m_x), i.e., $\mathbf{W_x}$, is equal to $1-(d_1+d_2) = 1+(m_y+m_z)$ i.e., $1-m_x$. This can be rewritten as $1-|m_x|$ since m_x is positive in sector 1 as seen in Fig. 8.

TABLE III
DUTY RATIOS IN TERMS OF MIS

Duty ratio	MI with maximum absolute value is positive			MI with maximum absolute value is negative		
	m_x	m_y	m_z	m_x	m_y	m_z
$d_{\mathbf{U_x}}$	1	0	0	1-$\lvert m_x\rvert$	$\lvert m_x\rvert$	$\lvert m_x\rvert$
$d_{\mathbf{U_y}}$	0	1	0	$\lvert m_y\rvert$	1-$\lvert m_y\rvert$	$\lvert m_y\rvert$
$d_{\mathbf{U_z}}$	0	0	1	$\lvert m_z\rvert$	$\lvert m_z\rvert$	1-$\lvert m_z\rvert$
$d_{\mathbf{W_x}}$	1-$\lvert m_x\rvert$	$\lvert m_x\rvert$	$\lvert m_x\rvert$	1	0	0
$d_{\mathbf{W_y}}$	$\lvert m_y\rvert$	1-$\lvert m_y\rvert$	$\lvert m_y\rvert$	0	1	0
$d_{\mathbf{W_z}}$	$\lvert m_z\rvert$	$\lvert m_z\rvert$	1-$\lvert m_z\rvert$	0	0	1

Similar analysis can be done for other sectors to derive the duty ratios for all the vectors. The information for all sectors is summarized in Table III, which gives the duty ratios for all space vectors in terms of MIs m_x, m_y, and m_z.

In the table, the duty ratio of space vector $\mathbf{U_x}$ is denoted by $d_{\mathbf{U_x}}$ and so on. $\mathbf{U_x}$, $\mathbf{U_y}$, and other space vectors can be identified using Table I for CCW, CW, and two-level inverter vectors. Note that the MIs m_x, m_y, and m_z have been defined in (17), (18), and (19) for CCW, CW, and two-level inverter cases, respectively. A flowchart for calculating duty ratios using carrier-based algorithm for open-end winding MC drive is given in Fig. 9. As a preliminary step, the CCW and CW MIs defined in (17) and (18), respectively, are rewritten as shown in (20) and (21), respectively

$$\begin{aligned}
m_x &= \frac{3\overline{v}_{\mathrm{AA}'}v_{\mathrm{aN}} + (\overline{v}_{\mathrm{BB}'} - \overline{v}_{\mathrm{CC}'})v_{\mathrm{bc}}}{\frac{9}{2}V_i^2} \\
&= [3k_{AA'}v_{\mathrm{aN}} + (k_{\mathrm{BB}'} - k_{\mathrm{CC}'})v_{\mathrm{bc}}]\left(\frac{2}{9V_i}\right) \\
m_y &= \frac{3\overline{v}_{\mathrm{AA}'}v_{\mathrm{cN}} + (\overline{v}_{\mathrm{BB}'} - \overline{v}_{\mathrm{CC}'})v_{\mathrm{ab}}}{\frac{9}{2}V_i^2} \\
&= [3k_{\mathrm{AA}'}v_{\mathrm{cN}} + (k_{\mathrm{BB}'} - k_{\mathrm{CC}'})V_{ab}]\left(\frac{2}{9V_i}\right) \\
m_z &= -(m_x + m_y) \\
m_x &= \frac{3\overline{v}_{\mathrm{AA}'}v_{\mathrm{aN}} - (\overline{v}_{\mathrm{BB}'} - \overline{v}_{\mathrm{CC}'})v_{\mathrm{bc}}}{\frac{9}{2}V_i^2} \\
&= [3k_{AA'}v_{\mathrm{aN}} - (k_{\mathrm{BB}'} - k_{\mathrm{CC}'})v_{\mathrm{bc}}]\left(\frac{2}{9V_i}\right)
\end{aligned} \tag{20}$$

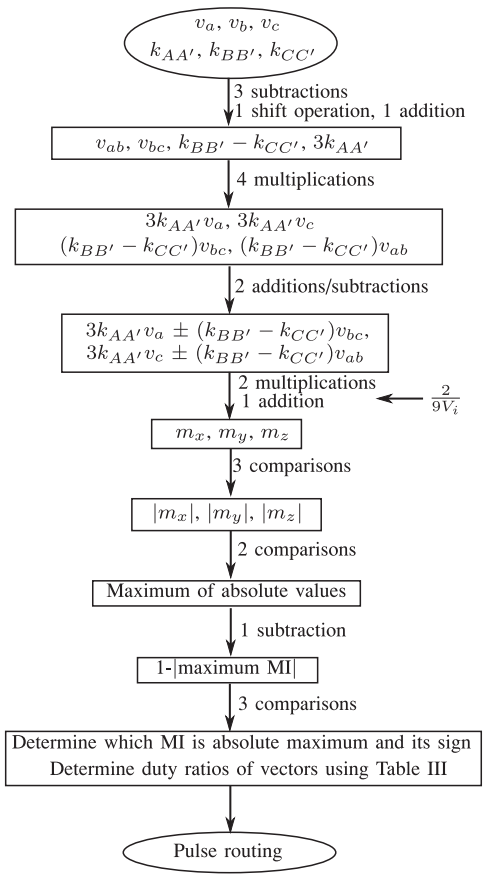

Fig. 9. Carrier-based implementation of MC PWM using CCW and CW vectors.

$$m_z = \frac{3\overline{v}_{\mathrm{AA'}}v_{\mathrm{cN}} - (\overline{v}_{\mathrm{BB'}} - \overline{v}_{\mathrm{CC'}})v_{\mathrm{ab}}}{\frac{9}{2}V_i^2}$$

$$= [3k_{\mathrm{AA'}}v_{\mathrm{cN}} - (k_{\mathrm{BB'}} - k_{\mathrm{CC'}})V_{ab}]\left(\frac{2}{9V_i}\right)$$

$$m_y = -(m_x + m_z) \tag{21}$$

$$k_{\mathrm{II'}} = \frac{\overline{v}_{\mathrm{II'}}}{V_i} \quad \mathrm{I} = \mathrm{A}, \mathrm{B}, \mathrm{C} \tag{22}$$

Thus, the expression $[3k_{\mathrm{AA'}}v_a \pm (k_{\mathrm{BB'}} - k_{\mathrm{CC'}})v_{\mathrm{bc}}](\frac{2}{9V_i})$ equals CCW MI m_x when $+$ sign is used in place of $\pm$ and equals CW MI m_x when $-$ sign is used in place of $\pm$. Also, expression $[3k_{\mathrm{AA'}}v_c \pm (k_{\mathrm{BB'}} - k_{\mathrm{CC'}})V_{ab}](\frac{2}{9V_i})$ equals CCW MI m_y when $+$ sign is used in place of $\pm$ and equals the CW MI m_z when $-$ sign is used in place of $\pm$.

It is assumed that $k_{\mathrm{AA'}}$, $k_{\mathrm{BB'}}$, and $k_{\mathrm{CC'}}$ defined in (22), the input voltages v_{aN}, v_{bN}, and v_{cN}, and the quantity $\frac{2}{9V_i}$ are given at the beginning of the algorithm. The flowchart in Fig. 9 is explained as follows:

1) Compute $3k_{\mathrm{AA'}}$ [*one addition, one shift operation*], v_{ab} [*one subtraction*], v_{bc} [*one subtraction*] and $k_{\mathrm{BB'}} - k_{\mathrm{CC'}}$ [*one subtraction*] . [Total: *three subtractions, one addition, one shift operation*]
2) Compute $3k_{\mathrm{AA'}}v_{\mathrm{aN}}$, $3k_{\mathrm{AA'}}v_{\mathrm{cN}}$, $(k_{\mathrm{BB'}} - k_{\mathrm{CC'}})v_{\mathrm{bc}}$ and $(k_{\mathrm{BB'}} - k_{\mathrm{CC'}})v_{\mathrm{ab}}$, using quantities computed in the previous step. [Total: *four multiplications*]
3) Compute $3k_{\mathrm{AA'}}v_{\mathrm{aN}} \pm (k_{\mathrm{BB'}} - k_{\mathrm{CC'}})v_{\mathrm{bc}}$ [*one addition/subtraction*] and $3k_{\mathrm{AA'}}v_{\mathrm{cN}} \pm (k_{\mathrm{BB'}} - k_{\mathrm{CC'}})v_{\mathrm{ab}}$ [*one addition/subtraction*]. The plus sign $\pm$ is for CCW vectors and the minus sign is for CW vectors. [Total: *two subtractions/additions*]
4) Compute $(3k_{\mathrm{AA'}}v_{\mathrm{aN}} \pm (k_{\mathrm{BB'}} - k_{\mathrm{CC'}})v_{\mathrm{bc}})\frac{2}{9V_i}$ [*one multiplication*] and $(3k_{\mathrm{AA'}}v_{\mathrm{cN}} \pm (k_{\mathrm{BB'}} - k_{\mathrm{CC'}})v_{\mathrm{ab}})\frac{2}{9V_i}$ [*one multiplication*]. This gives CCW MIs m_x and m_y or CW MIs m_x and m_z as explained in (20) and (21). Calculate $m_z = -(m_x + m_y)$ for CCW vectors or $m_y = -(m_x + m_z)$ for CW vectors [*one addition*]. Now all the MIs required for duty ratio computation are obtained. [Total: *two multiplications, one addition*]
5) Find $|m_x|$, $|m_y|$ and $|m_z|$. [Total: *three comparisons*]
6) Compare $|m_x|$, $|m_y|$ and $|m_z|$ to identify maximum of these three. [Total: *two comparisons*]
7) Find 1-|Maximum MI|. [Total: *one subtraction*]
8) Determine which is the MI whose absolute value is maximum by comparing $|m_x|$, $|m_y|$, and $|m_z|$ with the absolute maximum MI found in step 6 [*two comparisons*]. Then, find the sign of this absolute maximum MI [*one comparison*]. [Total: *three comparisons*]
9) Use the Table III to get the duty ratio of individual vectors and, hence, the individual switches using Table I.

As seen from the above explanation, the carrier-based algorithm requires a total of *six multiplications, eight additions/subtractions, eight comparisons, and one shift operation*. These computations have also been shown denoted in Fig. 9.

As an example, let $|m_y|$ be maximum and m_y be positive. Then, using Table III, the positive-end converter is clamped to space vector $\mathbf{U_y}$. The duty ratios of negative-end converter's vectors $\mathbf{W_x}$, $\mathbf{W_y}$, and $\mathbf{W_z}$ are $|m_x|$, $1 - |m_y|$, and m_z, respectively. If the CCW vectors are being used, then using Table I, the positive-end MC is clamped to $\mathbf{U_{cab}}$. The duty ratios of space vectors $\mathbf{W_{abc}}$, $\mathbf{W_{cab}}$, and $\mathbf{W_{bca}}$ are $|m_x|$, $1 - |m_y|$, and m_z, respectively.

It should be noted that despite using space vector equations to arrive at the carrier-based algorithm, the finalized carrier-based algorithm mentioned above does not require any knowledge of space vectors.

The duty ratio waveforms for the three positive-end vectors and the three negative-end vectors derived using the carrier-based algorithm are shown in Fig. 10. In the figure, $d_{\mathbf{U_x}}$ denotes the duty ratio waveform of positive-end generalized vector $\mathbf{U_x}$. The other waveforms similarly denote the duty ratios of corresponding generalized vectors. The six waveforms are identical in shape and size but are displaced in time. The waveforms $d_{\mathbf{U_y}}$ and $d_{\mathbf{U_z}}$ lag $d_{\mathbf{U_x}}$ by 120° and 240°, respectively. The negative-end vector duty ratio waveform $d_{\mathbf{W_x}}$ is displaced by 180° w.r.t. to the corresponding positive-end vector duty ratio waveform $d_{\mathbf{U_x}}$. The negative-end vector duty ratio waveforms are also displaced by 120° w.r.t. to each other. It should be noted that the frequency of all these duty ratio waveforms is the relative frequency ω_{rel}.

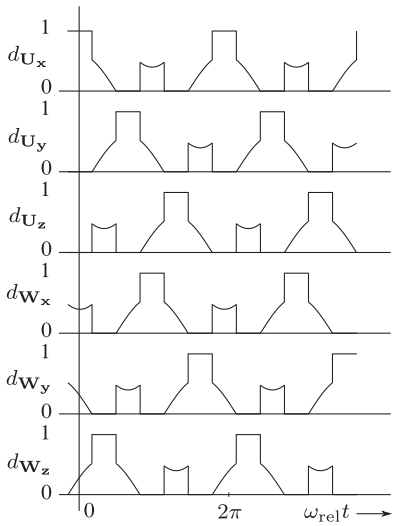

Fig. 10. Duty ratio waveforms for all positive- and negative-end space vectors (and switches).

The waveforms in Fig. 10 are duty ratio signals for space vectors. However, in any of the three sets (two-level, CCW, CW), one leg (in case of dual two-level VSI) or one bidirectional switch (in case of dual MC) is related to only one space vector. As an example (using $\mathbf{U_1}$, $\mathbf{U_3}$, and $\mathbf{U_5}$ for modulating positive-end converter), in the dual two-level VSI, the leg connected to output phase A is turned ON (or connected to dc bus terminal P) only when vector $\mathbf{U_1}$ is applied and is turned OFF (connected to dc bus terminal N) when any other two vectors ($\mathbf{U_3}$, $\mathbf{U_5}$) are applied. Thus, in Fig. 10, the waveform $d_{\mathrm{U_x}}$ corresponds to the duty ratio waveform of $\mathbf{U_1}$ (using Table I) with $\omega_{\rm rel} = \omega_o$ and, hence, is the duty ratio waveform for the inverter leg connected to output phase A. In the MC case, when using CCW vectors, the switches aA, bB, and cC are turned ON only when the CCW vector $\mathbf{U_{abc}}$ is applied and are OFF when any other CCW vector is applied. In Fig. 10, the waveform $\mathrm{d_{U_x}}$ corresponds to the duty ratio waveform of $\mathbf{U_{abc}}$ (using Table I) with $\omega_{\rm rel} = \omega_o - \omega_i$. Hence, this is the duty ratio waveform for switches aA, bB, and cC when using CCW vectors. A similar explanation is applicable for CW vectors.

It must be noted that in the case of simple carrier-based operation of a VSI, modulation/duty ratio signals can be directly compared with a carrier to generate gating waveforms. In this case, an additional simple combinatorial operation with the generated pulses is necessary to avoid over lapping of two active pulses in time. For example, in a carrier/sampling cycle, the pulses for aA ($\mathbf{U_{abc}}$) and cA ($\mathbf{U_{cab}}$) must not overlap in time.

V. Comparison Between Carrier-Based and Space-Vector-Based Approaches for PWM of Dual Matrix and Two-Level VSI

An algorithm for the space-vector-based approach for PWM of open-end winding MC drive using both CCW and CW vectors is shown in Fig. 11. It is assumed that $k_{\rm AA'}$, $k_{\rm BB'}$, and $k_{\rm CC'}$ defined in (22) and the input voltages v_a, v_b, and v_c are given at the starting of the computation.

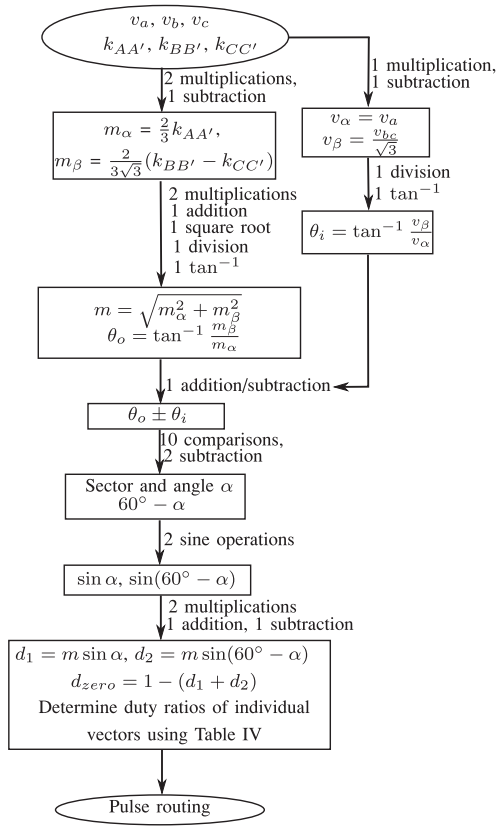

Fig. 11. Space-vector-based PWM of dual MC using CCW and CW vectors.

The flowchart for space-vector-based approach in Fig. 11 is explained below.

1) The input phase voltages $v_{\rm aN}$, $v_{\rm bN}$, and $v_{\rm cN}$ are converted to $\alpha\beta$ axis, using $\mathrm{v}_\alpha = \mathrm{v_{aN}}$ and $\mathrm{v}_\beta = \frac{\mathrm{v_{bc}}}{\sqrt{3}}$ [*one subtraction, one multiplication*]. Input voltage phase θ_i is calculated as $\tan^{-1}\frac{v_\beta}{v_\alpha}$ [*one division, one* $\tan^{-1}$]. [*Total: one multiplication, one subtraction, one division, one* $\tan^{-1}$].
2) $m_\alpha = \frac{2}{3}k_{AA'}$ [*one multiplication*] and $m_\beta = \frac{2}{3\sqrt{3}}(k_{BB'} - k_{CC'})$ [*one subtraction, one multiplication*] are calculated. [*Total: one subtraction, two multiplications*].
3) The output modulation index $m = \sqrt{m_\alpha^2 + m_\beta^2}$ is computed [*two multiplications* (for computing m_α^2 and m_β^2), *two addition, one square root*]. Output voltage angle is computed using $\theta_o = \tan^{-1}\frac{m_\beta}{m_\alpha}$ [*one division, one* $\tan^{-1}$]. [*Total: two multiplications, one addition, one square root operation, one division, one* $\tan^{-1}$].
4) $\theta_i \pm \theta_o$ is computed (either added for CW vectors or subtracted for CCW vectors). [*one subtraction/addition*].
5) To determine the sector, $\theta_o \pm \theta_i$ is compared with the upper and lower angular bounds of each sector [*ten comparisons in worst case*]. Then, angle α is determined by subtracting appropriate multiple of $\frac{\pi}{3}$ from θ_o [*one*

TABLE IV
DUTY RATIOS IN EACH SECTOR

Duty Ratio/Sector	1	2	3	4	5	6
$d_{\mathbf{U_x}}$	1	d_1	0	d_{zero}	0	d_2
$d_{\mathbf{U_y}}$	0	d_2	1	d_1	0	d_{zero}
$d_{\mathbf{U_z}}$	0	d_{zero}	0	d_2	1	d_1
$d_{\mathbf{W_x}}$	d_{zero}	0	d_2	1	d_1	0
$d_{\mathbf{W_y}}$	d_1	0	d_{zero}	0	d_2	1
$d_{\mathbf{W_z}}$	d_2	1	d_1	0	d_{zero}	0

TABLE V
COMPUTATIONS REQUIRED FOR CARRIER-BASED AND SPACE-VECTOR-BASED APPROACHES FOR PWM OF DUAL MC

Computation	Carrier based approach	Space vector based approach
Comparison	8	10
Shift operation	1	0
Addition/Subtraction	8	8
Multiplication	6	7
Division	0	2
Sine	0	2
$\tan^{-1}$	0	2
Square root	0	1

TABLE VI
RESOURCE REQUIREMENTS OF CARRIER-BASED AND SPACE-VECTOR-BASED APPROACHES FOR PWM OF DUAL MC

Resource used	Carrier based approach	Space vector approach
No. of slice flip-flops	71 (1%)	2436 (26%)
No. of 4 input LUTs	461 (4%)	2670 (28%)
No. of Logic slices	271 (5%)	1590 (34%)
No. of MULT18X18SIOs	6 (30%)	7 (35%)

TABLE VII
SIMULATION AND EXPERIMENTAL PARAMETERS FOR DUAL TWO-LEVEL INVERTER AND DUAL MC OPEN-END WINDING DRIVES

Parameter	Dual two level inverter	Dual matrix converter
DC bus voltage	100 V	N/A
Input voltage (line-line rms)	N/A	69.2 V
Input frequency	N/A	60 Hz
Output voltage (line-line rms)	87 V	69.2 V
Output frequency	60 Hz	28 Hz
Switching frequency	5 kHz	5 kHz
Load	$31.0\angle 39.0^\circ\ \Omega$	$15.4\angle 36.0^\circ\ \Omega$

subtraction]. Then, $(60^\circ - \alpha)$ is computed [*one subtraction*]. [*Total: ten comparisons, two subtractions*].

6) Compute $\sin\alpha$ and $\sin(60^\circ - \alpha)$. [*two* $\sin$ *operations*].
7) Compute duty ratios $d_1 = m\sin(\alpha)$ and $d_2 = m\sin(60^\circ - \alpha)$ [*two multiplications*]. Calculate $d_{\mathrm{zero}} = 1 - (d_1 + d_2)$ [*one addition, one subtraction*]. [*Total: two multiplications, one addition, one subtraction*].
8) With sector, d_1, d_2, and d_{zero} known, Tables I and IV are used to determine which space vector is applied with what duty ratio. This part is common with the carrier-based algorithm and takes the same computations (a case or if else statement). Hence, it is not considered in the comparison.

Based on the above discussion, the total computations needed for the space-vector-based implementation of PWM for dual MC using CCW and CW vectors are *one square root, 2* $\tan^{-1}$*, two* $\sin$*, two divisions, seven multiplications, eight additions/subtractions, ten comparisons*. The flowchart in Fig. 9 for the carrier-based approach for dual MC PWM using CCW or CW vectors is explained in Section IV, and the various calculations required for the steps have been explained before as well as shown in the flowchart.

It is observed from the above discussion and the flowcharts that the carrier-based approach takes fewer computations than the space vector approach for the PWM control of dual MC. The computations required are summarized in Table V.

The Verilog code for both the methods was developed and implemented using Xilinx ISE Editor to check the resources. The FPGA used was Xilinx Spartan 3 XC3S500E. The resource requirements of both techniques are given in Table VI, which shows that the resource requirements are much more in the space-vector-based approach. The CORDIC IP core from Xilinx was used to do the square root and all trigonometric operations needed by the space vector approach.

The latencies of Verilog code for carrier-based and space-vector-based approaches for open-end winding MC drive are shown in Fig. 12(a) and (b), respectively. In Fig. 12(a), the inputs $k_{AA'}$, $k_{BB'}$, and $k_{CC'}$ (denoted k_AApr, k_BBpr, and k_CCpr, respectively, in the figure) change at the beginning of the shaded region (marked by an arrow). The output $d_{\mathbf{U_z}}$, i.e., the duty ratio of vector $\mathbf{U_z}$ (top signal denoted as d_Uz in the figure) changes after two clock cycles (shown in the shaded area). In Fig. 12(b), the inputs $k_{\mathrm{AA'}}$, $k_{\mathrm{BB'}}$, and $k_{\mathrm{CC'}}$ (denoted k_AApr k_BBpr, and k_CCpr, respectively, in the figure) change at the beginning of the shaded region. The output d_{zero}, i.e., the duty ratio of the zero vector (top signal denoted as dz in the figure) in the current sector changes after 33 clock cycles (shown in the shaded area). Thus, latency of the carrier-based algorithm, as seen in Fig. 9, is two clock cycles. The latency of the space-vector-based approach, as seen in Fig. 11, has a latency of 33 clock cycles, which is much more than that of the carrier-based approach.

The carrier-based and space-vector-based approaches for PWM of open-end winding two-level inverter drive are special cases of corresponding approaches for PWM of open-end winding MC drive. So, the carrier-based and space-vector-based approaches for PWM of two-level inverter compare similarly.

VI. SIMULATION RESULTS

The parameters used for the simulation of dual two-level inverter drive using carrier-based PWM are given in the second column of Table VII.

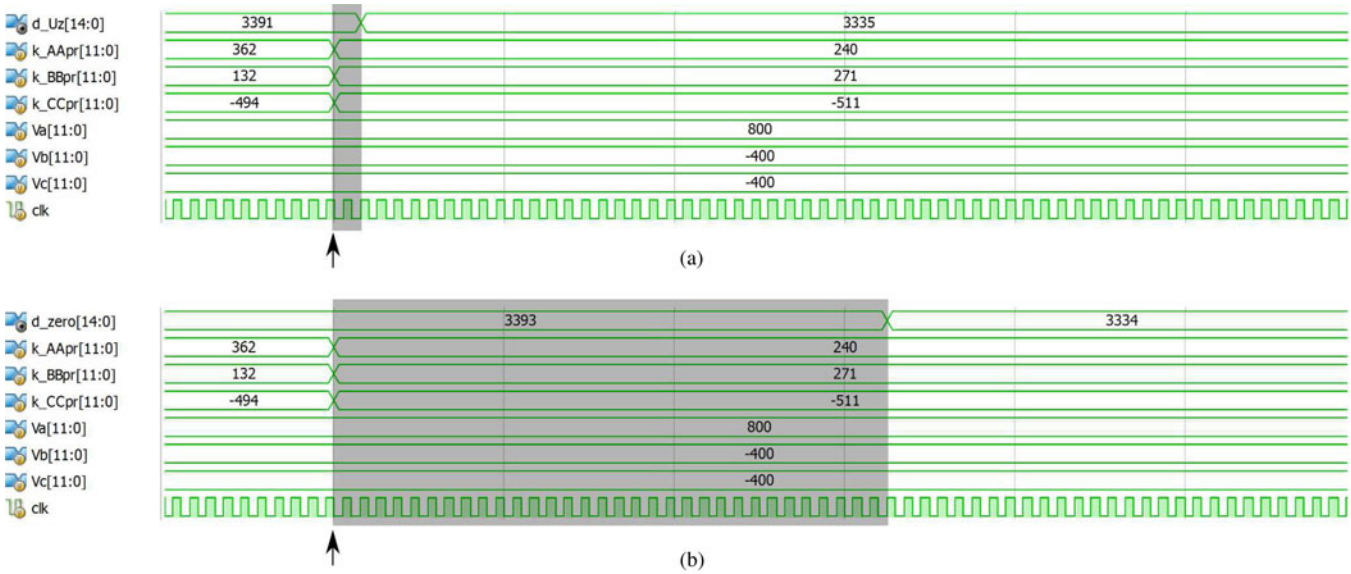

Fig. 12. Latency in Verilog code for PWM of dual MC. (a) Carrier-based approach. (b) Space-vector-based approach.

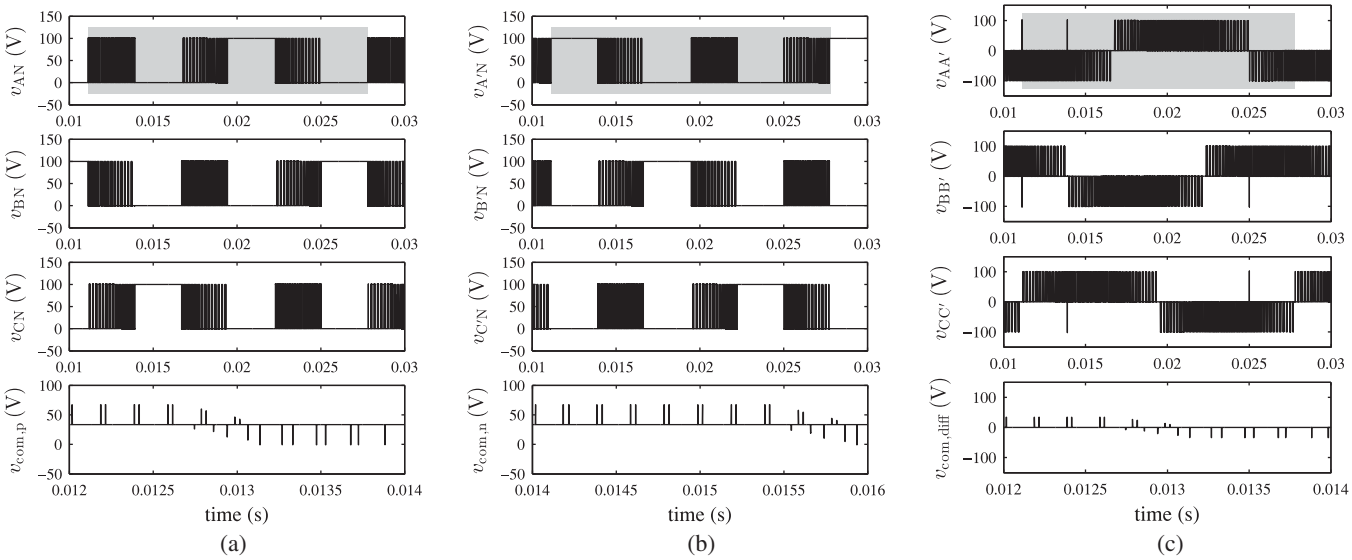

Fig. 13. Simulation results for dual two-level inverter (gray patch in top graphs indicates the length of one cycle of output fundamental frequency). (a) Positive-end pole voltages (top three graphs) and CMV (bottom graph). (b) Negative-end pole voltages (top three graphs) and CMV (bottom graph). (c) Voltages across load phases (top three graphs) and CMV (bottom graph) across load.

The simulation results for dual two-level inverter are shown in Figs. 13–15. The positive-end and negative-end pole voltages and CMV are shown in Fig. 13(a) and (b), respectively. The voltages across output phases and differential CMV are shown in Fig. 13(c). Dead times and device drops have been included in the simulations to remain close to experimental conditions. It is observed that barring the small glitches due to device drops and dead times [40], the positive and negative-end CMVs are held flat at 33.33 V, which is equal to one-third of the dc bus voltage $V_{\rm dc}$. Thus, their average sum and difference should also have constant values (ignoring nonidealities), which should help in mitigating the problems of circulating currents and EMI. In all these figures, a gray patch has been drawn in the top graph to denote one cycle of the output fundamental frequency ω_o. In Fig. 14, the positive-end and negative-end pole voltages and voltage across output phases have been shown for one switching cycle for easier viewing. Fig. 15(a) displays the output currents and the circulating current. The output currents appear balanced and sinusoidal as desired, while the circulating current is much smaller than the output currents. The Fourier spectra of voltage $v_{\rm AA'}$ across output phase A are shown in Fig. 15(b) for carrier-based and space-vector-based techniques, respectively.

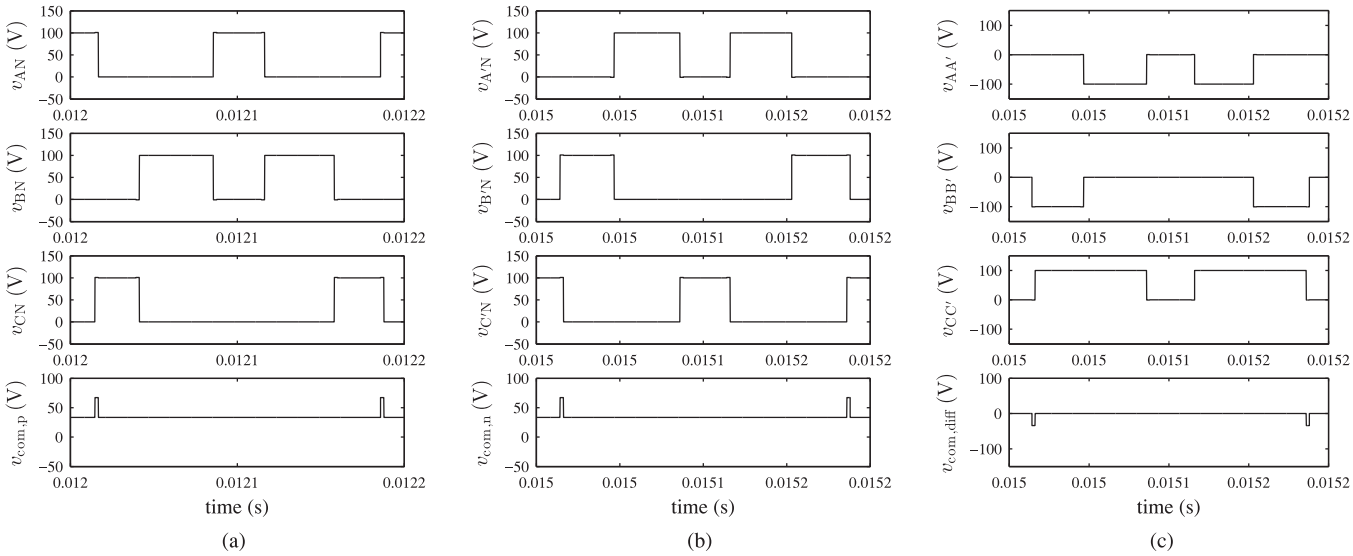

Fig. 14. Simulation results (zoomed voltages for dual two-level inverter). (a) Positive-end pole voltages (top three graphs) and CMV (bottom graph). (b) Negative-end pole voltages (top three graphs) and CMV (bottom graph). (c) Voltages across load phases (top three graphs) and CMV (bottom graph) across load.

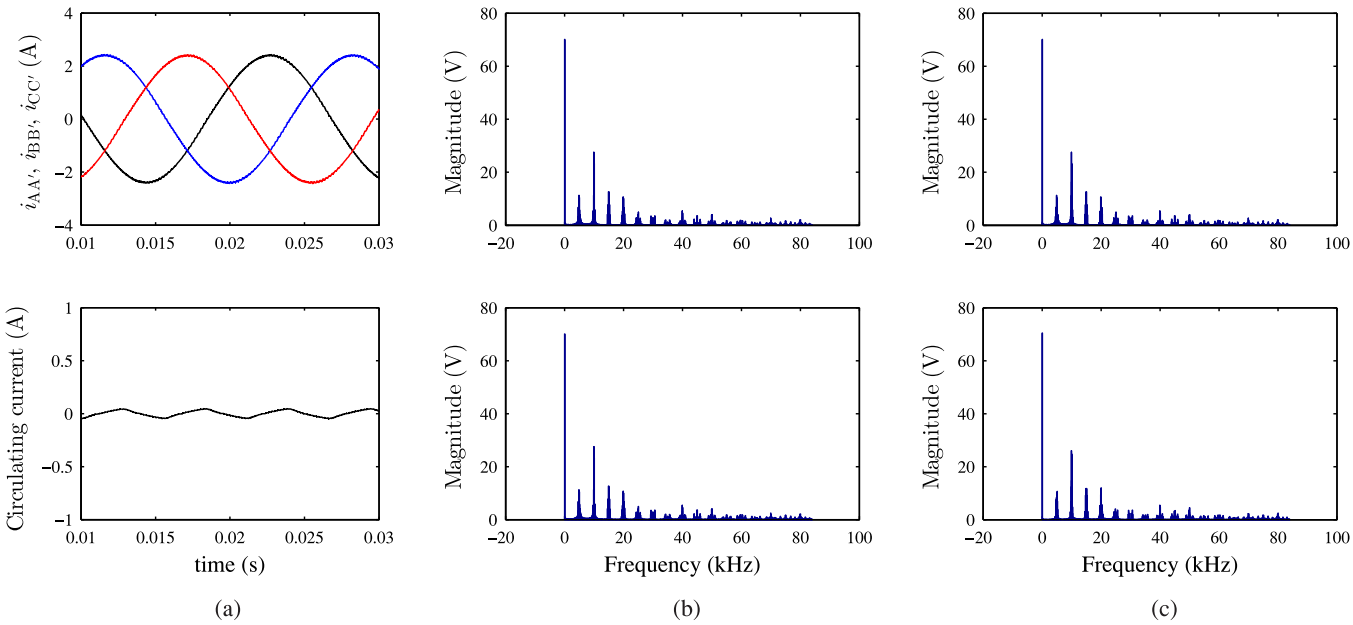

Fig. 15. Simulation results (dual two-level inverter). (a) Three phase load currents (top graph) and circulating current (bottom graph). (b) Fourier spectrum of voltage $v_{AA'}$ across load phase A using carrier based method (top graph) and space vector method (bottom graph). (c) Fourier spectrum of voltage $v_{AA'}$ across phase A for dual VSI (top graph) and Fourier spectrum of output phase voltage v_{An} in single VSI (bottom graph).

The spectra are nearly identical, which implies that the carrier-based method generates identical pulses to that of the space vector approach.

Finally, the Fourier spectra of voltage across load phase A are shown for dual VSI with CMV elimination and single VSI using conventional SVPWM (all eight vectors) in Fig. 15(c). It is seen that they are nearly identical, indicating that the differential mode power quality of dual VSI with CMV elimination is the same as that of single VSI with conventional PWM.

The parameters used for simulation of dual MC using carrier-based PWM are given in the third column of Table VII.

The simulation results for dual MC are shown in Figs. 16–18. The positive-end and negative-end pole voltages and CMV are shown in Fig. 16(a) and (b), respectively. The voltages across output phases and differential CMV are shown in Fig. 16(c). Commutation periods and device drops have been included in the simulations to remain close to experimental conditions. It is observed that excluding the small glitches due to commutation

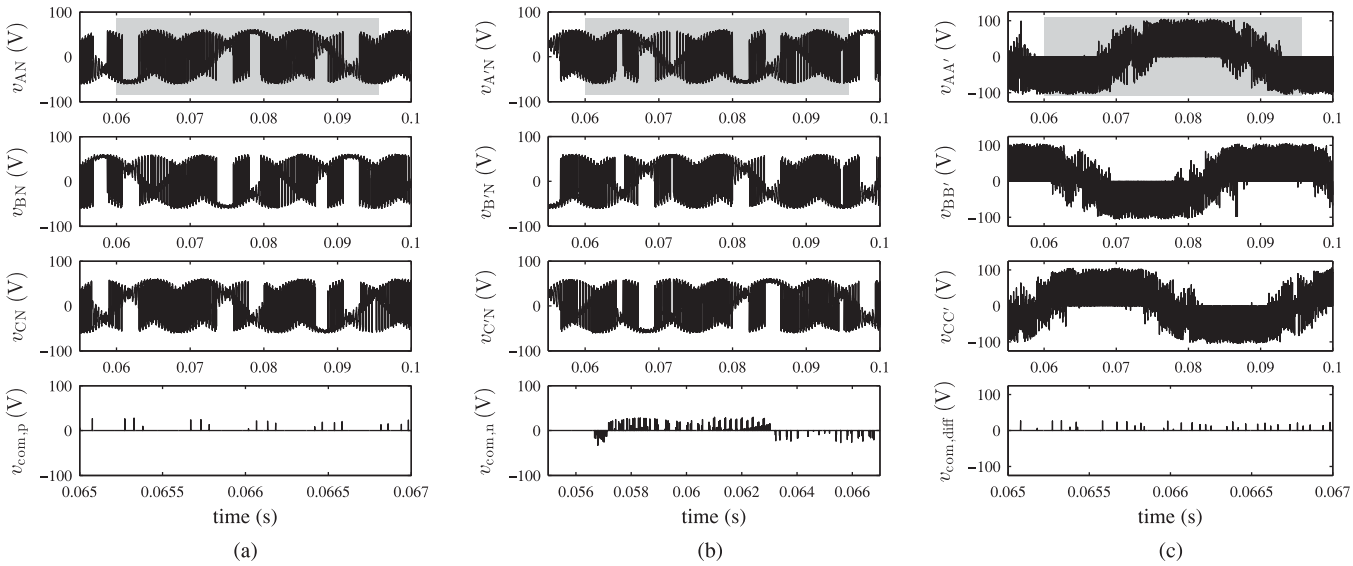

Fig. 16. Simulation results for dual MC (gray patch in top graphs indicates the length of one cycle of output fundamental frequency). (a) Positive-end pole voltages (top three graphs) and CMV (bottom graph). (b) Negative-end pole voltages (top three graphs) and CMV (bottom graph). (c) Voltages across load phases (top three graphs) and CMV (bottom graph) across load.

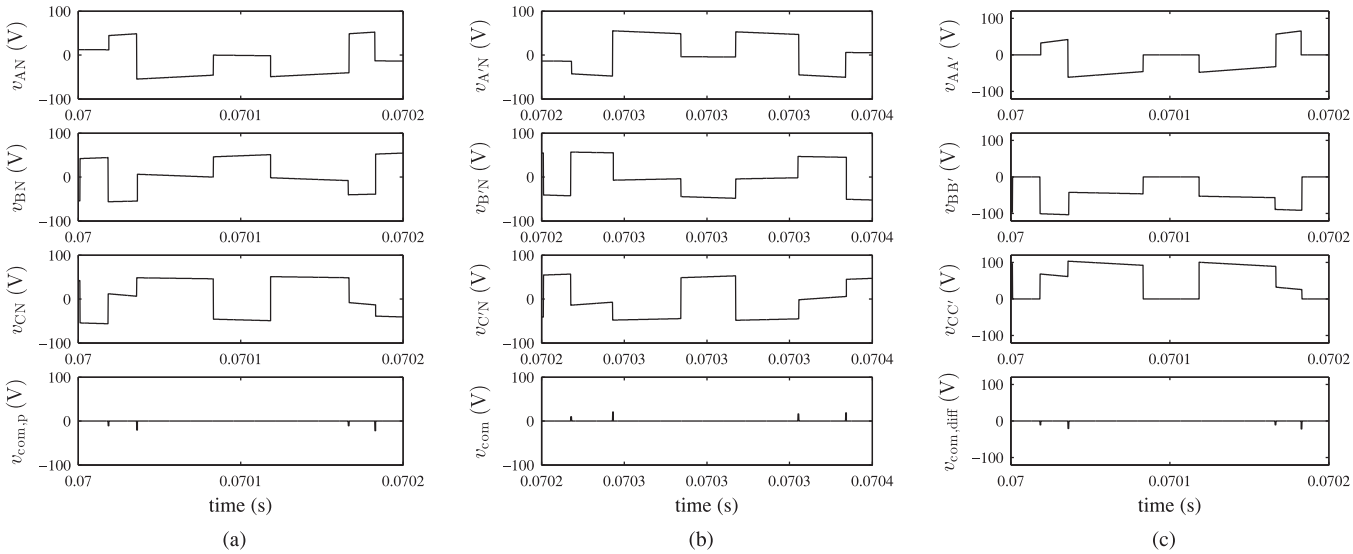

Fig. 17. Simulation results (zoomed voltages for dual MC). (a) Positive-end pole voltages (top three graphs) and CMV (bottom graph). (b) Negative-end pole voltages (top three graphs) and CMV (bottom graph). (c) Voltages across load phases (top three graphs) and CMV (bottom graph) across load.

periods and device drops [40], the positive and negative-end CMVs are held flat at 0 V. Thus, their average sum and difference should also be zero (ignoring nonidealities), which should help in mitigating the problems of circulating currents and EMI. In all these figures, a gray patch has been drawn in the top graph to denote one cycle of the output fundamental frequency ω_o. In Fig. 17, the positive-end and negative-end pole voltages and voltage across output phases have been shown for one switching cycle for easier viewing. In Fig. 18(a), the input voltage v_{aN} and current (filtered and zoomed five times) i_{a} are shown. It can be seen that they are nearly in phase, indicating unity power factor which is due to equal utilization of CCW and CW vectors [21]. Fig. 18(b) displays the output currents and the circulating current. The output currents appear balanced and sinusoidal as desired, while the circulating current is much smaller than the output currents. Finally, in Fig. 18(c), the Fourier spectra of voltage $v_{\mathrm{AA'}}$ across output phase A are shown for carrier-based and space-vector-based techniques, respectively. The spectra are nearly identical, which implies that the carrier-based method generates identical pulses to that of the space vector approach.

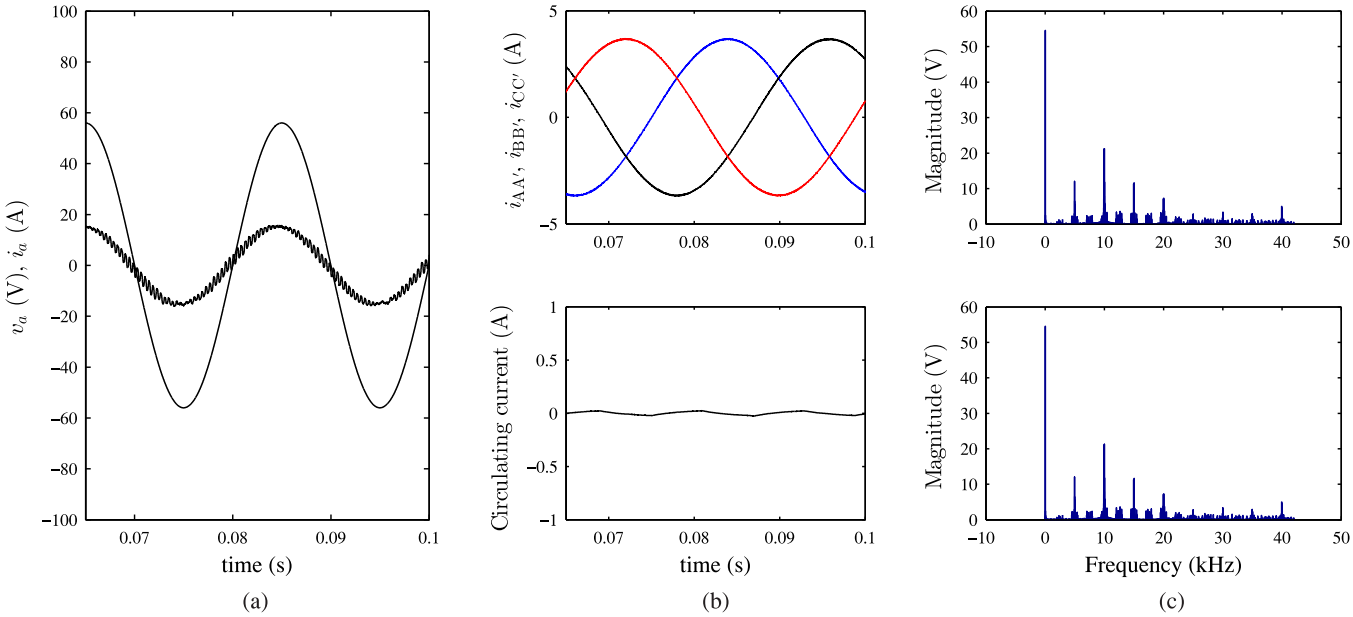

Fig. 18. Simulation results (dual MC). (a) Input current (zoomed five times for viewing ease) and voltage of phase a. (b) Three phase load currents (top graph) and circulating current (bottom graph). (c) Fourier spectrum of voltage $v_{\mathrm{A}\mathrm{A}'}$ across load phase A using carrier based method (top graph) and space vector method (bottom graph).

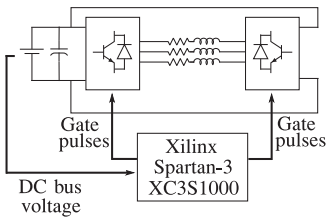

Fig. 19. Diagram of the experimental setup for dual two-level inverter.

VII. Experimental Results

The proposed PWM technique was tested on prototype hardware setups of dual two-level inverter and dual MC open-end winding drives. In this section, a brief description of the hardware setups has been given along with key experimental results.

The dual two-level inverter was built using two Microsemi APTGF90TA60PG IGBT modules. The gate drivers used are Concept 6SD106EI. The proposed PWM technique was implemented using a Digilent Spartan 3 Starter board with Xilinx XC3S1000 FPGA. A diagram of the circuit is given in Fig. 19. A dead band of 2 μs is present between the pulses of upper and lower switch of any leg in the inverter. The experimental settings for two-level inverter setup are given in the second column of Table VII.

The experimental results for dual two-level inverter are given in Figs. 20 and 21. The positive-end and negative-end pole voltages and CMV are shown in Fig. 20(a) and (b), respectively. The voltages across output phases and the differential CMV are shown in Fig. 20(c). A gray patch in the top graphs of these three figures indicates one cycle of output fundamental frequency. It is observed that the positive-end and negative-end CMVs are held at a constant value and the differential CMV is held at zero, barring the glitches due to dead times and device drops [40]. Zoomed versions of all these voltages are provided in Fig. 20(d)–(f) for better viewing. The three-phase load currents and circulating current are shown in Fig. 21(a). The currents appear as balanced and sinusoidal. The circulating current is nonzero, which is, however, much smaller than the load currents. Fourier spectra of the voltage $v_{\mathrm{A}\mathrm{A}'}$ are given for PWM of dual two-level inverter using carrier-based and space-vector-based approaches in Fig. 21(b). It is seen that the spectra are nearly identical and devoid of low-order harmonics.

The dual MC setup was built using six Microsemi APTGT75TDU120PG IGBT modules and the gate drivers used are Concept 2SD106AI. The proposed PWM technique was implemented on a Xilinx XC3S500E FPGA board. A diagram of the setup is shown in Fig. 22. Four-step commutation was used with a total commutation period of 1.5 μs. This requires sensing of the load currents. The experimental settings for dual MC setup are given in the rightmost column of Table VII.

The filter components used are $R_d = 12.5\ \Omega$, $L_f = 1.4$ mH, and $C_f = 35\ \mu$F.

The experimental results for dual MC are given in Figs. 23 and 24. The positive-end and negative-end pole voltages and CMV are shown in Fig. 23(a) and (b), respectively. The voltages across output phases and the differential CMV are shown in Fig. 23(c). A gray patch in the top graphs of these three figures indicates one cycle of output fundamental frequency. It is observed that the positive-end, negative-end, and the differential CMVs are held at zero, barring the glitches due to commutation periods times and device drops [40]. Zoomed versions of all these voltages are

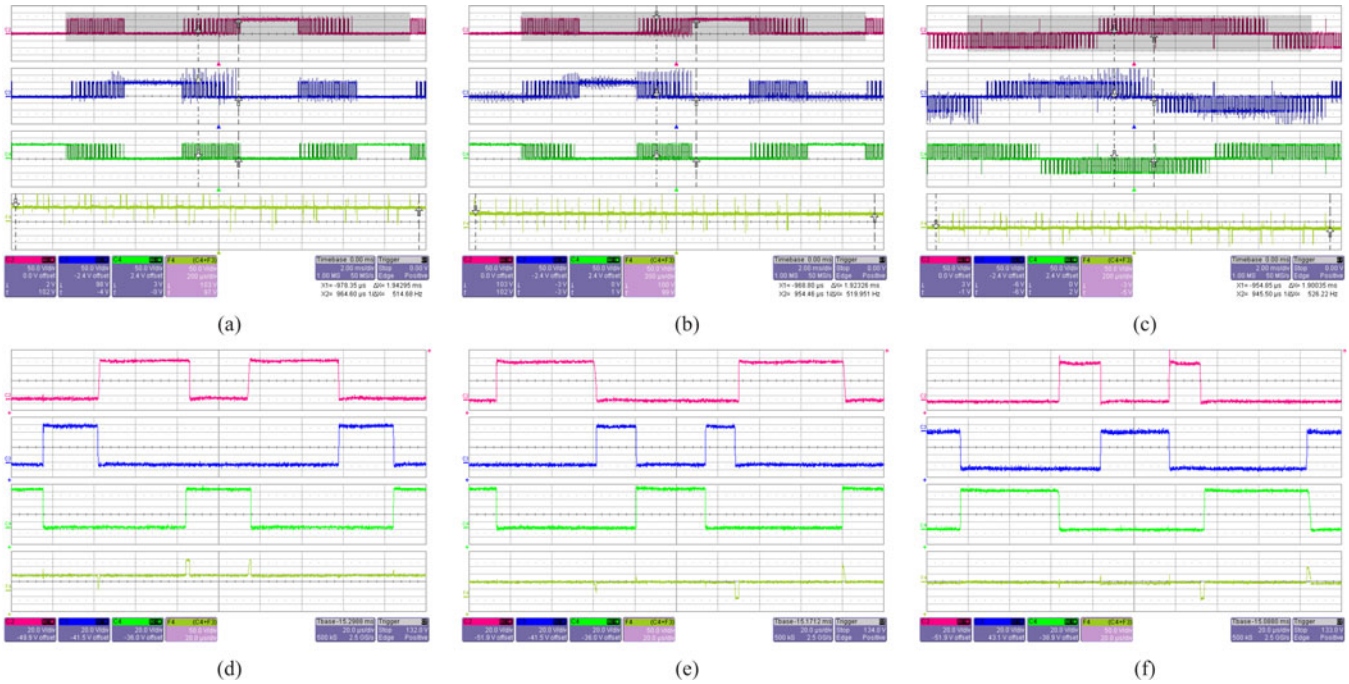

Fig. 20. Experimental results for dual two-level inverter (gray patch in top graphs indicates the length of one cycle of output fundamental frequency). (a) Positive-end pole voltages (top three graphs) and CMV (bottom graph) [*X* axis: 2 ms/div (top three graphs) 200 μs/div (bottom graph), *Y* axis: 50 V/div]. (b) Negative-end pole voltages (top three graphs) and CMV (bottom graph) [*X* axis: 2 ms/div (top three graphs) 200 μs/div (bottom graph), *Y* axis: 50 V/div]. (c) Voltages across load phases (top three graphs) and CMV (bottom graph) across load [*X* axis: 2 ms/div (top three graphs) 200 μs/div (bottom graph), *Y* axis: 50 V/div]. (d) Positive-end pole voltages and CMV (zoomed) [*X* axis: 20 μs/div, *Y* axis: 20 V/div (top three waveforms) 50V/div (bottom waveform)]. (e) Negative-end pole voltages and CMV (zoomed) [*X* axis: 20 μs/div, *Y* axis: 20 V/div (top three waveforms) 50 V/div (bottom waveform)]. (f) Phase voltages and CMV across load (zoomed) [*X* axis: 20 μs/div, *Y* axis: 20 V/div (top three waveforms) 50 V/div (bottom waveform)].

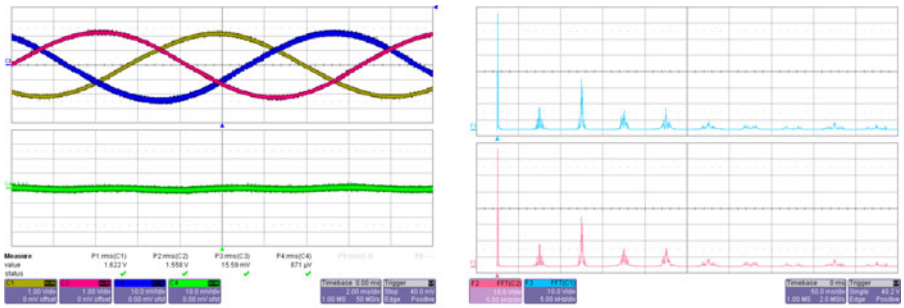

Fig. 21. Experimental results (dual two-level inverter). (a) Three phase load currents (top graph) and circulating current (bottom graph) [*X* axis: 2 ms/div, *Y* axis: 1 A/div]. (b) Fourier spectrum of voltage $v_{\mathrm{AA}'}$ across load phase A using carrier based method (top graph) and space vector method (bottom graph) [*X* axis: 5 kHz/div, *Y* axis: 10 V/div].

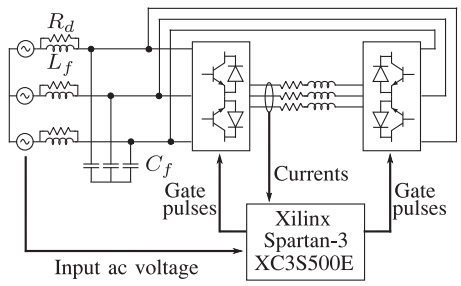

Fig. 22. Diagram of the experimental setup for dual MC.

provided in Fig. 23(d)–(f) for better viewing. The input phase voltage v_{aN} and phase current i_{a} are shown in Fig. 24(a). It can be seen that the input voltage and current (filtered) are nearly in phase (current leads slightly due to input filter), indicating unity power factor due to equal usage of CCW and CW vector [21]. The three-phase load currents and circulating current are shown in Fig. 24(b). The currents appear as balanced and sinusoidal. The circulating current is nonzero, which is, however, much smaller than the load currents. Fourier spectra of the voltage $v_{\mathrm{AA}'}$ are given for PWM of dual MC using carrier-based and

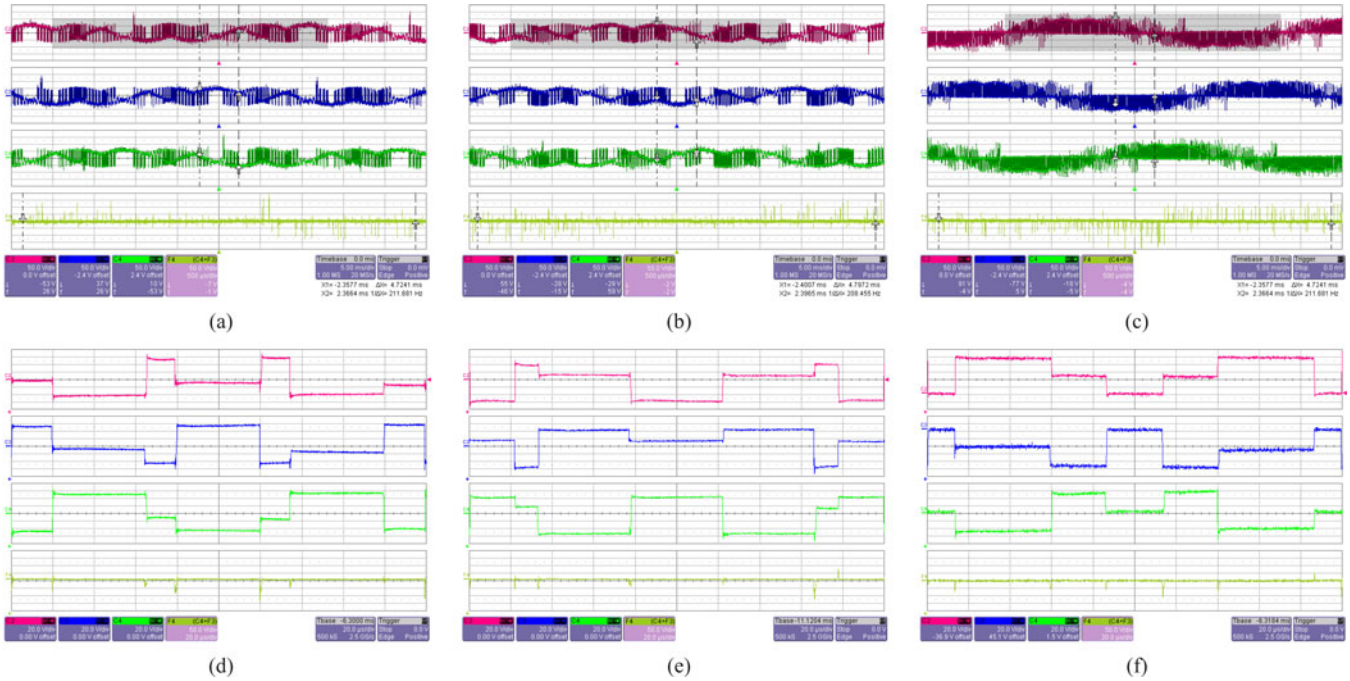

Fig. 23. Experimental results for dual matrix inverter (gray patch in top graphs indicates the length of one cycle of output fundamental frequency). (a) Positive-end pole voltages (top three graphs) and CMV (bottom graph) [*X* axis: 2 ms/div (top three graphs) 200 μs/div (bottom graph), *Y* axis: 50 V/div]. (b) Negative-end pole voltages (top three graphs) and CMV (bottom graph) [*X* axis: 2 ms/div (top three graphs) 200 μs/div (bottom graph), *Y* axis: 50 V/div]. (c) Voltages across load phases (top three graphs) and CMV (bottom graph) across load [*X* axis: 2 ms/div (top three graphs) 200 μs/div (bottom graph), *Y* axis: 50 V/div]. (d) Positive-end pole voltages and CMV [*X* axis: 20 μs/div, *Y* axis: 20 V/div (top three waveforms) 50 V/div (bottom waveform)]. (e) Negative-end pole voltages and CMV [*X* axis: 20 μs/div, *Y* axis: 20 V/div (top three waveforms) 50 V/div (bottom waveform)]. (f) Phase voltages and CMV across load [*X* axis: 20 μs/div, *Y* axis: 20 V/div (top three waveforms) 50 V/div (bottom waveform)].

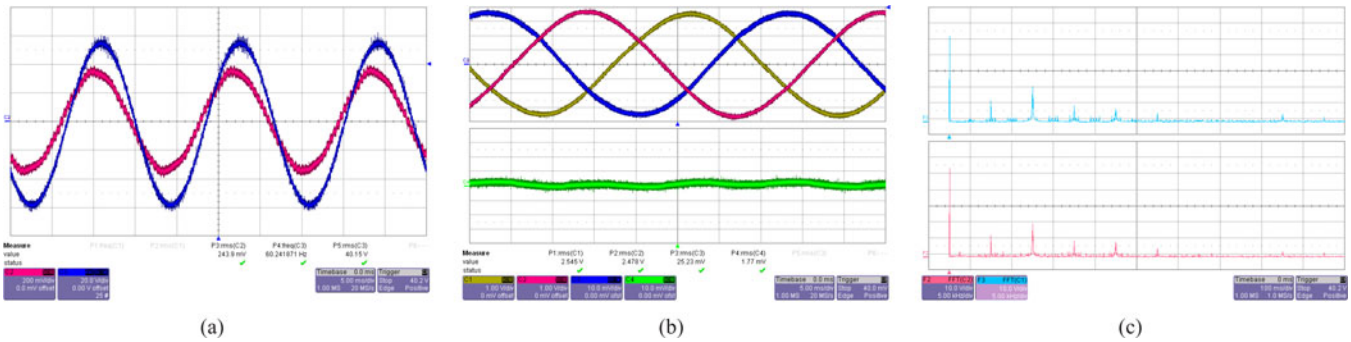

Fig. 24. Experimental results (dual MC). (a) Input current and voltage of phase a [*X* axis: 5 ms/div, *Y* axis: 20 V/div, 2 A/div]. (b) Three phase load currents (top graph) and circulating current (bottom graph) [*X* axis: 2 ms/div, *Y* axis: 1 A/div]. (c) Fourier spectrum of voltage $v_{\mathrm{A\,A'}}$ across load phase A using carrier based method (top graph) and space vector method (bottom graph) [*X* axis: 5 kHz/div, *Y* axis: 10 V/div].

space-vector-based approaches in Fig. 24(c). It is seen that the spectra are nearly identical and devoid of low-order harmonics.

Finally, Fig. 25 shows the high-frequency spectra of CMVs generated by a single two-level VSI, a dual two-level VSI with CMV elimination, and a dual MC with CMV elimination. The single VSI and dual VSI were operated at 100-V dc bus voltage and the dual MC was operated with a line–line peak voltage 97.86 V (rms 69.2 V) for this comparison. It can be seen that the high-frequency CMV generated by the dual converters is nearly an order of magnitude lower than that generated by single VSI.

VIII. Conclusion

In this paper, a generalized carrier-based PWM technique has been developed for open-end winding PWM ac drive. A detailed analysis shows the relationship and a comparison in terms of computational effort of the proposed method with the existing space-vector-based modulation technique. The superior performance of the proposed carrier-based method in terms of resources consumed and execution time has been confirmed by implementing both algorithms on an FPGA-based real-time control platform. Finally, the simulation results verified by

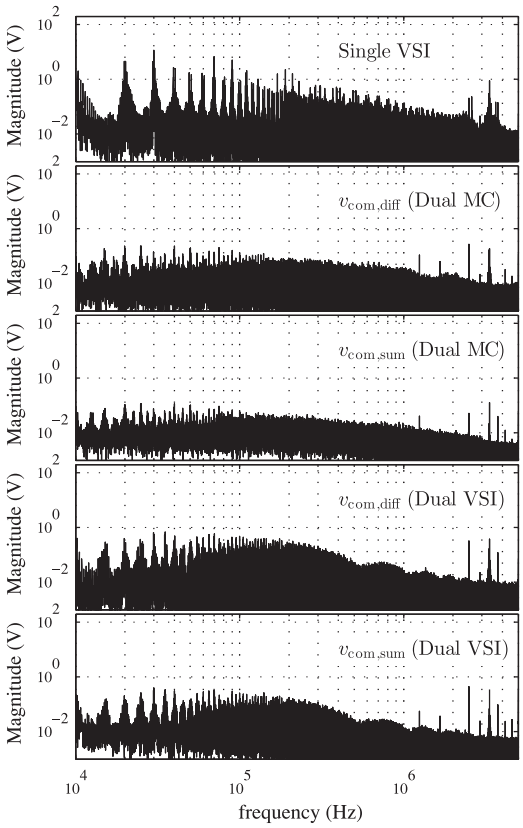

Fig. 25. High-frequency spectrum of CMVs (experimental results). Single VSI (top graph), differential CMV (dual MC) (second graph), average CMV (dual MC) (third graph), differential CMV (dual two-level inverter) (fourth graph), average CMV (dual two-level inverter) bottom graph).

hardware have been presented to demonstrate the proposed technique applied to both two-level and MC cases.

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