

A Single-Stage Dual-Active-Bridge-Based Soft Switched AC–DC Converter With Open-Loop Power Factor Correction and Other Advanced Features

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Abstract—A dual-active-bridge-based single-stage ac/dc converter may find a wide range of emerging applications such as interfacing plug-in hybrid vehicles with the ac grid, interconnection of dc grid, etc. This type of converter can be used due to unique features such as 1) high-frequency isolation resulting in a) high power density and b) safety and voltage matching; 2) bidirectional power flow; 3) soft switching leading to higher efficiency. In this paper, a modulation strategy has been proposed that results in 1) open-loop power factor correction; 2) zero current switching in the ac-side converter for all load conditions; 3) linear power relationship for easy control implementation; and 4) Zero voltage switching in the load side converter. The converter with the proposed control has been analyzed. Simulation and experimental results on a 1-KW prototype confirm the advantages.

Index Terms—AC–DC conversion, bidirectional power flow, high-frequency transformer.

I. INTRODUCTION

SINGLE-PHASE ac/dc converter with isolation finds a large number of applications. A transformer is usually needed for safety and voltage matching. Replacement of a utility frequency transformer with a high frequency one results in considerable reduction in size and weight. Due to high power density, high-frequency link converters are attractive for automotive, naval, and aerospace applications where compactness and light weight are important.

Low power (few watts to several kilowatts) isolated single-stage single-phase ac/dc converters are used as the front end of switched mode power supplies, uninterrupted power supplies (UPS), induction heating, electronic ballast, telecom power supplies, etc. These types of converters are commonly known as isolated power factor correction (PFC) circuits and have been extensively studied in the literature [1], [2]. A comprehensive

review of these converters can be found in [3] and [4]. These converters are usually based on isolated dc/dc converters, i.e., flyback, forward, full bridge, etc., and power flow is unidirectional. Resonant converter-based topologies can be found in [5].

High-power single-phase bidirectional ac/dc converters have been proposed for interfacing plug-in hybrid vehicles [6], propulsion systems, UPS, dc distribution system in ships [7], and as a front end of isolated universal ac/ac converters or power electronic transformers [8]. These converters are usually two stage: An active front-end rectifier followed by a high-frequency link dc/dc converter, [9], [10]. An earlier example of such converter can be found in [11]. Multiple stages of power conversion, partial hard switching, and usage of more reactive elements result in lower efficiency, reliability, and power density. Single-stage high-frequency link dc/ac converters can be used as pulse width modulation rectifiers [12]. These converters are partially hard switched and hence are less energy efficient and have a limited frequency of operation.

Dual-active-bridge-(DAB) based single-stage ac/dc converter considered in this paper can be found in [13] and [14]. Due to high efficiency and power density, DAB-based dc/dc converters are commonly employed in high-power applications such as high-voltage dc distribution systems [15], and electric vehicles [16], [17]. DAB offers most of the features desirable for the ac/dc converter considered in this paper. Some of these properties are: 1) single-stage power conversion with no additional reactive element; 2) bidirectional power flow; 3) soft switching enabling very high frequency of operation, high power density, and high efficiency; 4) isolation and voltage matching; and 5) control of active power flow.

Modulation of DAB is an active area of research. In conventional phase shift modulation (PSM) both the primary and the secondary H-Bridges of the DAB are modulated with 50% duty cycle and active power is controlled by phase shift between these two waveforms [18]. Though simple, PSM results in poor no load efficiency, large reactive current flow, and limited soft switching range in presence of wide variation in input–output voltages [19]. It is possible to overcome these difficulties by modulating the duty cycles of both the bridges [20] [21]. This technique is commonly known as trapezoidal modulation (TPZM) or dual H-bridge modulation (DHBM) and has three degrees of freedom (two duty cycles and phase shift). These control parameters are optimized in [22]. Triangular modulation (TRM) is a special case of TPZM where at one transition in every half cycle both the input and output bridges are switched

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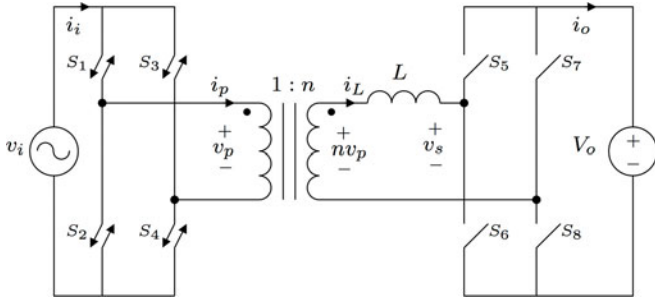


Fig. 1. Topology of ac/dc converter.

together resulting in triangular shape current waveform [23], [24]. Dual-phase-shift (DPS) modulation is a special case of TPZM where both the bridges have the same duty cycle [25], [26]. In [27] and [28], PSM, TRM, and TPZM are combined together to a hybrid modulation in order to achieve optimal efficiency over a wide operating range. Duty cycle modulation of only one/single H-Bridge (SHBM) was first introduced in [29] and extensively studied in [9], [30], and [31]. PSM, DPS, and SHBM are studied in the context of multiport converters in [32]. A combined modulation of SHBM and DHBM can be found in [21]. In [33], a special case of SHBM has been identified as inner mode and shown to achieve zero current switching (ZCS) in one of the bridges and simple linear power relationship. Note that for all other modulation strategies active power is a nonlinear function of the control variable.

This paper introduces a modulation technique based on inner mode of SHBM for the single-stage ac/dc converter as shown in Fig. 1 and achieves the following advantages:

- 1) open-loop PFC;
- 2) ZCS for the ac-side H-bridge for all load conditions;
- 3) the active power is proportional to the control variable (phase shift), this leads to simple closed-loop control in comparison with characteristic nonlinear control of DAB [23];
- 4) zero-voltage switching (ZVS) is achieved for the dc-side H-bridge.

The idea of this paper was first presented in [36]. In this paper, theoretical analysis of the proposed modulation strategy is presented in Section II assuming ideal components. A simulation of the ideal topology is given in Section III with results confirming theoretical predictions. Lastly, experimental results are presented in Section IV and compared with simulation and theoretical predictions.

II. ANALYSIS

This section provides an in-depth analysis of the proposed modulation scheme and the resulting benefits. The proposed modulation scheme utilizes the leakage inductance of the transformer to transfer power in the topology shown in Fig. 1. The ac-side converter is comprised of four-quadrant switches S_1 – S_4 . The transformer has a turns ratio of $1 : n$ and the primary and secondary leakage inductance is lumped on the secondary as L . In this analysis, the magnetizing inductance, winding resistances, and cores losses of the transformer are all neglected and the switches are considered to be ideal. The dc-side converter is

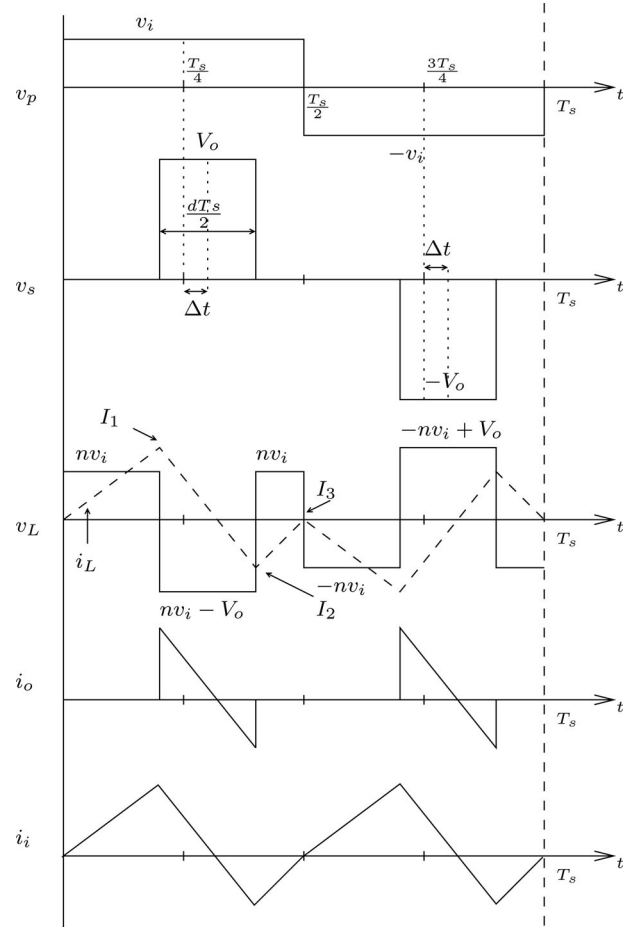


Fig. 2. Modulation cycle [$v_i(t) > 0$].

a H-Bridge comprised of two-quadrant switches, S_5 – S_8 , shown in Fig. 1. The H-bridge is connected to a dc source with voltage V_o .

A. Converter Operation

The ac source connected to the ac-side converter is defined in (1), where V_i is the amplitude and f_i is the frequency of the ac source

$$v_i(t) = V_i \sin(2\pi f_i t). \quad (1)$$

The ac-side H-bridge is switched to apply a quasi-square wave across the transformer primary as shown in Fig. 2 and described by (2). Also note that f_i is much smaller than $f_s = \frac{1}{T_s}$

$$v_p(t) = \begin{cases} v_i, & 0 < t < \frac{T_s}{2} \\ -v_i, & \frac{T_s}{2} < t < T_s. \end{cases} \quad (2)$$

The dc-side H-Bridge applies a voltage pulse to the secondary of the transformer in which the width of the pulse is set by the duty ratio d , defined in (3), and is phase shifted by the time quantity Δt , shown in Fig. 2. Note that given V_i and V_o , n is chosen to keep d less than unity

$$d(t) = \frac{n|v_i(t)|}{V_o}. \quad (3)$$

The phase shift Δt is restricted such that the pulse of V_o applied to v_s remains within its respective $T_s/2$ time period. This restriction results in (4)

$$|\Delta t| \leq \frac{T_s}{4}(1-d). \quad (4)$$

The phase shift ratio δ is defined in (5). The peak duty ratio \hat{d} is defined in (6). The phase shift ratio δ has a range of $-(1-\hat{d})$ to $(1-\hat{d})$, (7)

$$\delta = \frac{\Delta t}{T_s/4} \quad (5)$$

$$\hat{d} = \frac{nV_i}{V_o} \quad (6)$$

$$|\delta| \leq 1 - \hat{d}. \quad (7)$$

Assuming a turns ratio of 1:1, it is clear from (6) and (7) that the input voltage peak needs to be less than output voltage in order to have usable phase shift. If the input voltage peak is close to the output voltage, then the turns ratio can be designed in order to have adequate controllable phase shift. Maintaining (7), the voltage v_s applied by the dc-side H-bridge is defined for one complete cycle of T_s in (8), where λ is $\text{sgn}(v_i(t))$ and is depicted in Fig. 2

$$v_s(t) = \begin{cases} 0, & 0 < t < \frac{T_s}{4}(1+\delta-d) \\ \lambda V_o, & \frac{T_s}{4}(1+\delta-d) < t < \frac{T_s}{4}(1+\delta+d) \\ 0, & \frac{T_s}{4}(1+\delta+d) < t < \frac{3T_s}{4} + \frac{T_s}{4}(\delta-d) \\ -\lambda V_o, & \frac{3T_s}{4} + \frac{T_s}{4}(\delta-d) < t < \frac{3T_s}{2} + \frac{T_s}{4}(\delta+d) \\ 0, & \frac{3T_s}{4} + \frac{T_s}{4}(\delta+d) < t < T_s. \end{cases} \quad (8)$$

Using the voltage at v_s and v_p and the turns ratio of the transformer, the voltage across the inductor, $v_L(t)$, (9), is calculated for one complete cycle of T_s (10) and is also depicted in Fig. 2

$$v_L(t) = nv_p(t) - v_s(t) = L \frac{di_L}{dt} \quad (9)$$

$$v_L(t) = \begin{cases} nv_i, & 0 < t < \frac{T_s}{4}(1+\delta-d) \\ nv_i - \lambda V_o, & \frac{T_s}{4}(1+\delta-d) < t < \frac{T_s}{4}(1+\delta+d) \\ nv_i, & \frac{T_s}{4}(1+\delta+d) < t < \frac{T_s}{2} \\ -nv_i, & \frac{T_s}{2} < t < \frac{T_s}{2} + \frac{T_s}{4}(1+\delta-d) \\ -nv_i + \lambda V_o, & \frac{T_s}{2} + \frac{T_s}{4}(1+\delta-d) < t < \frac{T_s}{2} + \frac{T_s}{4}(1+\delta+d) \\ -nv_i, & \frac{T_s}{2} + \frac{T_s}{4}(1+\delta+d) < t < T_s. \end{cases} \quad (10)$$

For each time interval of T_s , the voltage across the inductor is assumed to be dc, and neglecting the resistances in the path, the current can be calculated for a complete cycle of T_s , shown as a dashed line in Fig. 2. During the first interval, a constant positive voltage of nv_i is applied to the inductor. Assuming that initially the inductor current is zero and v_i is positive, the inductor current increases linearly from zero to the point labeled I_1 . Using (9) and (10), the current at point I_1 is calculated in (11). In the following interval, a negative constant voltage of $nv_i - V_o$ is applied to the inductor and the inductor current linearly decreases to the point I_2 , (12). In the third section, a constant positive voltage of nv_i is applied to the inductor and the inductor current linearly increase to the point I_3 (13)

$$I_1 = \frac{nv_i T_s}{L} \frac{1+\delta-d}{4} \quad (11)$$

$$I_2 = I_1 + \frac{nv_i - V_o}{L} \frac{dT_s}{2} \quad (12)$$

$$I_3 = I_2 + \frac{nv_i T_s}{L} \frac{1-\delta-d}{4}. \quad (13)$$

At time $T_s/2$, the current I_3 is zero. This can be verified by calculating the average voltage across the inductor (14) or by calculating I_3 by substituting (11), (12), (13), into (13)

$$\bar{v}_L = \frac{2}{T_s} \int_0^{\frac{T_s}{2}} v_L(\tau) d\tau = 0. \quad (14)$$

Assuming the inductor current starts at zero at time zero, the inductor current returns to zero at time $T_s/2$. Additionally, since the voltage applied to the inductor during the time span $T_s/2$ to T_s is mirrored about the time axis, the average voltage applied to the inductor is zero, and thus, the inductor current returns to zero at time T_s . The inductor current is zero at time 0, $T_s/2$, and T_s and is the consequence of the selection of duty ratio, (3) and the restriction on δ , (7). The advantage of the inductor current being zero at time 0, $T_s/2$, and T_s can be observed in Fig. 2. The current through the inductor is zero when the ac-side converter switches and the primary current is equivalent to the reflected inductor current therefore the ac-side H-bridge switches S_1-S_4 are soft switched at zero current (ZCS) independent of load condition.

The average current from the ac source is calculated by averaging the inductor current from time 0 to $T_s/2$ and multiplying by the transformer turns ratio (15). Note i_i is periodic at $T_s/2$, Fig. 2

$$\bar{i}_i(t) = \frac{2n}{T_s} \int_0^{\frac{T_s}{2}} i_L(\tau) d\tau. \quad (15)$$

The average ac source current is calculated using (15), (11), (12), (13) and is given in (16)

$$\bar{i}_i(t) = \frac{n\delta V_o}{4Lf_s} d(t). \quad (16)$$

Given that L , f_s , n , and V_o are fixed and assuming the phase shift δ is selected to be constant, the average ac source current is solely dependent on the duty ratio d (16). Allowing the duty ratio

to change in time as in (3) and defining the ac source voltage as in (1) results in the average current from the ac source given in (17)

$$\bar{i}_i(t) = \frac{n^2 \delta}{4L f_s} V_i \sin(2\pi f_i t). \quad (17)$$

The average ac source current clearly is sinusoidal and in phase with the input voltage. This result leads to open-loop PFC. The magnitude of the current and, hence, the power can be changed by adjusting the phase shift δ . Furthermore, the current can be 180° out of phase with the input voltage by adjusting the phase shift to be negative and this results in bidirectional power flow.

The average DC voltage source current is calculated by averaging the current through the DC source over time $T_s/2$. Current only flows through the DC source when $+V_o$ or $-V_o$ is applied; therefore, the average is calculated in (18)

$$\bar{i}_o = \frac{I_1 + I_2}{2} d. \quad (18)$$

Substituting (11), (12), and (3) into (18) results in (19)

$$\bar{i}_o = \frac{n^2 V_i^2}{4L f_s V_o} \delta \sin^2(2\pi f_i t). \quad (19)$$

The average dc source current given in (19) can be written as a sum of an ac component at twice the ac source frequency and a dc component (20). The average dc source current is similar to a PFC circuit output current

$$\bar{i}_o = \bar{i}_{o,dc} + \bar{i}_{o,ac} = \frac{n^2 V_i^2}{8L f_s V_o} \delta [1 - \cos(4\pi f_i t)]. \quad (20)$$

Multiplying the average dc bus current by the dc voltage and assuming the topology is lossless, we get an expression for the switching cycle average of the real power transferred by this circuit (21)

$$P(t) = \frac{n^2 V_i^2}{4L f_s} \delta \sin^2(2\pi f_i t). \quad (21)$$

The average power over one complete cycle of the ac source is calculated in (22)

$$\bar{P} = \frac{n^2 V_i^2}{8L f_s} \delta. \quad (22)$$

The average power in per unit is shown in (23) and the base power is shown in (24). The base power is selected such that the average power per unit of one is the maximum power using the modulation scheme. The power per unit is plotted in Fig. 3(a). It is observed that for a given \hat{d} , power has a linear relationship with the control variable δ . Also note that the envelope in Fig. 3(a) shows the maximum power that can be transferred for a given value of \hat{d} . If the value of \hat{d} is fixed, due to selected input voltage, output voltage, and turns ratio, the value of δ is limited by (7). Furthermore, the range of δ is decreased if \hat{d} is increased and vice versa. Lastly the maximum average power per unit is one at $\hat{d} = 2/3$

$$\bar{P}_{p.u.} = \frac{\pi}{4} \delta \hat{d}^2 \quad (23)$$

$$P_{base} = \frac{V_o^2}{2\pi L f_s} \frac{27}{\pi}. \quad (24)$$

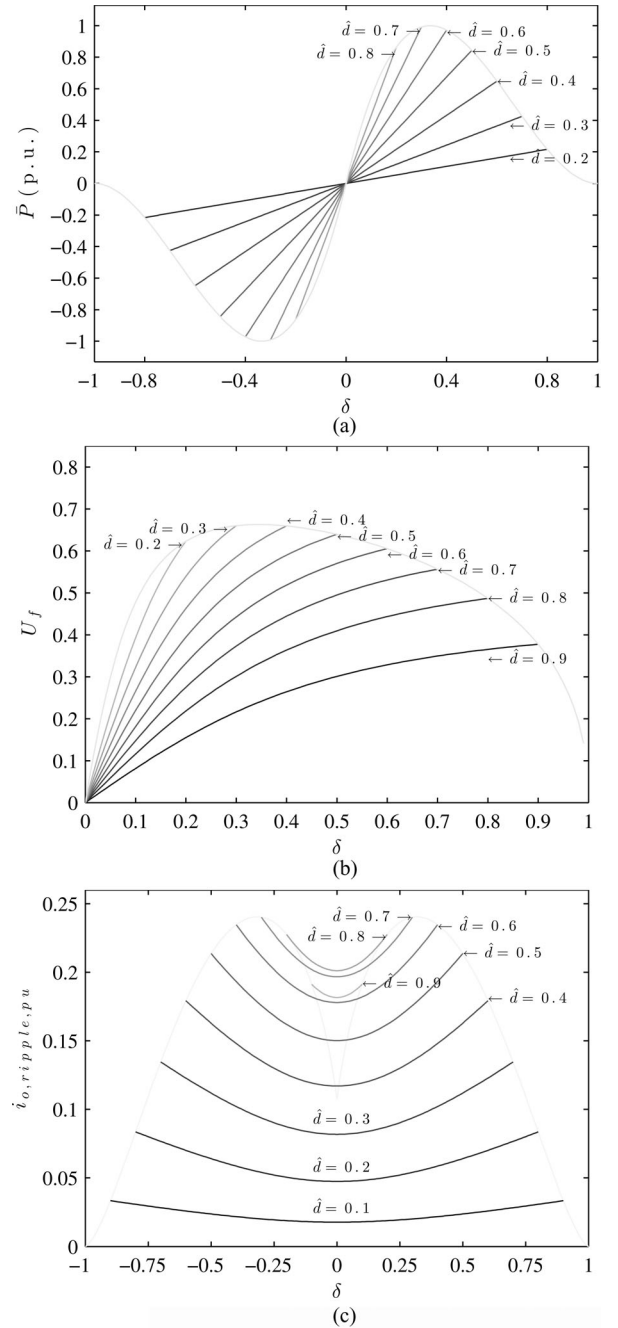


Fig. 3. Performance characteristics of the proposed control method. (a) Cycle average power per unit. (b) Transformer utilization. (c) RMS ripple current per unit.

The root mean square (RMS) over one complete cycle of ac source voltage of the primary and secondary voltages (v_p and v_s in Fig. 2) are calculated and shown in (25) and (26). Similarly the RMS current of the primary and secondary (i_p and i_L in Fig. 2) are calculated and shown in (27) and (28)

$$v_{p,rms} = \frac{V_i}{\sqrt{2}} \quad (25)$$

$$v_{s,rms} = V_o \sqrt{\frac{2}{\pi} \hat{d}} \quad (26)$$

TABLE I
SIMULATION PARAMETERS

L	n	\hat{V}_i	V_o	f_i	f_s
$50\mu\text{H}$	1	100V	250V	60Hz	10kHz

$$i_{p,\text{rms}} = \frac{n^2 V_i}{24L f_s} \sqrt{6 + 18\delta^2 - \frac{32}{\pi} \hat{d} + \frac{9}{2} \hat{d}^2} \quad (27)$$

$$i_{L,\text{rms}} = \frac{n V_i}{24L f_s} \sqrt{6 + 18\delta^2 - \frac{32}{\pi} \hat{d} + \frac{9}{2} \hat{d}^2}. \quad (28)$$

The apparent power of the transformer is defined in (29). The average power (22) divided by the apparent power results in the transformer utilization factor (30)

$$P_T = \frac{1}{2} (v_{p,\text{rms}} i_{p,\text{rms}} + v_{s,\text{rms}} i_{L,\text{rms}}) \quad (29)$$

$$U_f = \frac{12\hat{d}\pi\delta}{2\sqrt{\hat{d} + \hat{d}\sqrt{\pi}}} (12\pi + 36\pi\delta^2 - 64\hat{d} + 9\hat{d}^2). \quad (30)$$

The utilization factor is plotted in Fig. 3(b). The RMS of the dc bus current is calculated in (31). The dc bus ripple current is the current i_o minus the dc value of current flowing in the dc source. The RMS of the dc bus ripple current is calculated using (32) and results in (33)

$$i_{o,\text{rms}} = \frac{n V_i}{24L\sqrt{5}\pi f_s} \sqrt{80\hat{d} + 240\delta^2 \hat{d} - 45\pi\hat{d}^2 + 64\hat{d}^3} \quad (31)$$

$$i_{o,\text{ripple,rms}} = \sqrt{i_{o,\text{rms}}^2 - i_{o,\text{dc}}^2}. \quad (32)$$

The dc bus ripple current is converted to per unit with a base of (34) and is plotted in Fig. 3(c). Note that for a given \hat{d} , both utilization factor and RMS output ripple current are maximum at the maximum permissible power transfer

$$i_{o,\text{ripple,rms}} = \frac{n V_i}{24L\sqrt{5}\pi f_s} \times \sqrt{80\hat{d} + 240\delta^2 \hat{d} + 64\hat{d}^2 - 45\pi\hat{d}^2 - 45\pi\delta^2 \hat{d}^2}. \quad (33)$$

Equation (33) can be used to design the dc-side filter capacitance. Note that the ripple estimation in (33) includes both the second harmonic and switching frequency components

$$I_{\text{base}} = \frac{V_o}{2\pi L f_s}. \quad (34)$$

III. SIMULATION

The topology in Fig. 1 is simulated using the software PLECS by Plexim. The aforementioned modulation scheme is simulated using the circuit parameters given in Table I. The switches, transformer, inductor, ac source, and dc source are all considered to be ideal, therefore the simulation is lossless. A simulation is created to check the analysis given a set of important assumptions like ideal switches, no magnetizing current, etc. Through the analysis, the RMS values of currents, transformer utilization, and the power equations have been calculated as functions of

TABLE II
THEORETICAL VERSUS SIMULATION

	Theoretical	Simulation
\hat{i}_i	15.0A	14.99A
\hat{i}_o	6A	5.99A
\hat{P}_i	750W	749.98W

the circuit parameters. The simulation is necessary to confirm these analytical predictions [i.e. (2)–(32)].

The results of the simulation for $\delta = 0.3$ are shown in Fig. 4. Fig. 4(a) shows voltages v_p , v_s , and the inductor current i_L over three complete switching cycles ($3T_s$) when the input ac voltage is near its peak.

The current through the inductor is zero at each instant the ac-side converter switches and confirms the predicted ZCS. The average ac source current is calculated using an averaging block in PLECS. The average ac source current is shown with the ac source voltage in Fig. 4(b). The average current is sinusoidal and in phase with the input voltage confirming PFC. The peak average ac source current is calculated using (17) and Table I. The theoretical and simulated peak average ac source current is compared in Table II and they closely agree with each other. The simulated ac source current is shown in Fig. 4(c). It contains both fundamental 60-Hz component and multiples of twice the switching frequency 20-kHz components. The frequency components at twice the switching frequency 20 kHz and higher can be removed by the use of a filter. The average dc source current \bar{i}_o is depicted in Fig. 4(d) and has a peak value of 6 A and an average current of 3 A. The theoretical and simulated values of the peak dc source current are shown in Table II and it confirms the analysis. The power with a positive phase shift is flowing from the ac source into the dc source and is confirmed by observing Fig. 4(b) and Fig. 4(d).

The second simulation is completed using a fixed phase shift of -0.3 and the circuit parameters listed in Table I. The results of this simulation are shown in Fig. 5. Three switching cycles of the modulation scheme are shown in Fig. 5(a). The voltage produced at the secondary is phase shifted to the left demonstrating negative phase shift. The current through the leakage inductance is zero at each instance the ac-side H-bridge switches and illustrates ZCS. The condition for ZCS is given in (7) and does not depend on any other circuit parameters. The ac source voltage and average current is shown in Fig. 5(b) and shows the current 180° out of phase with respect to the voltage. With negative phase shift, the power is flowing from the dc source to the ac source and demonstrates the capability for bidirectional power transfer. The ac source switched current is shown in Fig. 5(c) and contains high-frequency content and the switching frequency and also the fundamental at 60 Hz. The average dc source current is shown in Fig. 5(d). The current has a sinusoidal shape at twice the ac source frequency (20) and has a negative average current of -3 A. The simulation results for positive and negative phase shift confirm the discussed analysis and demonstrate bidirectional power flow and ZCS.

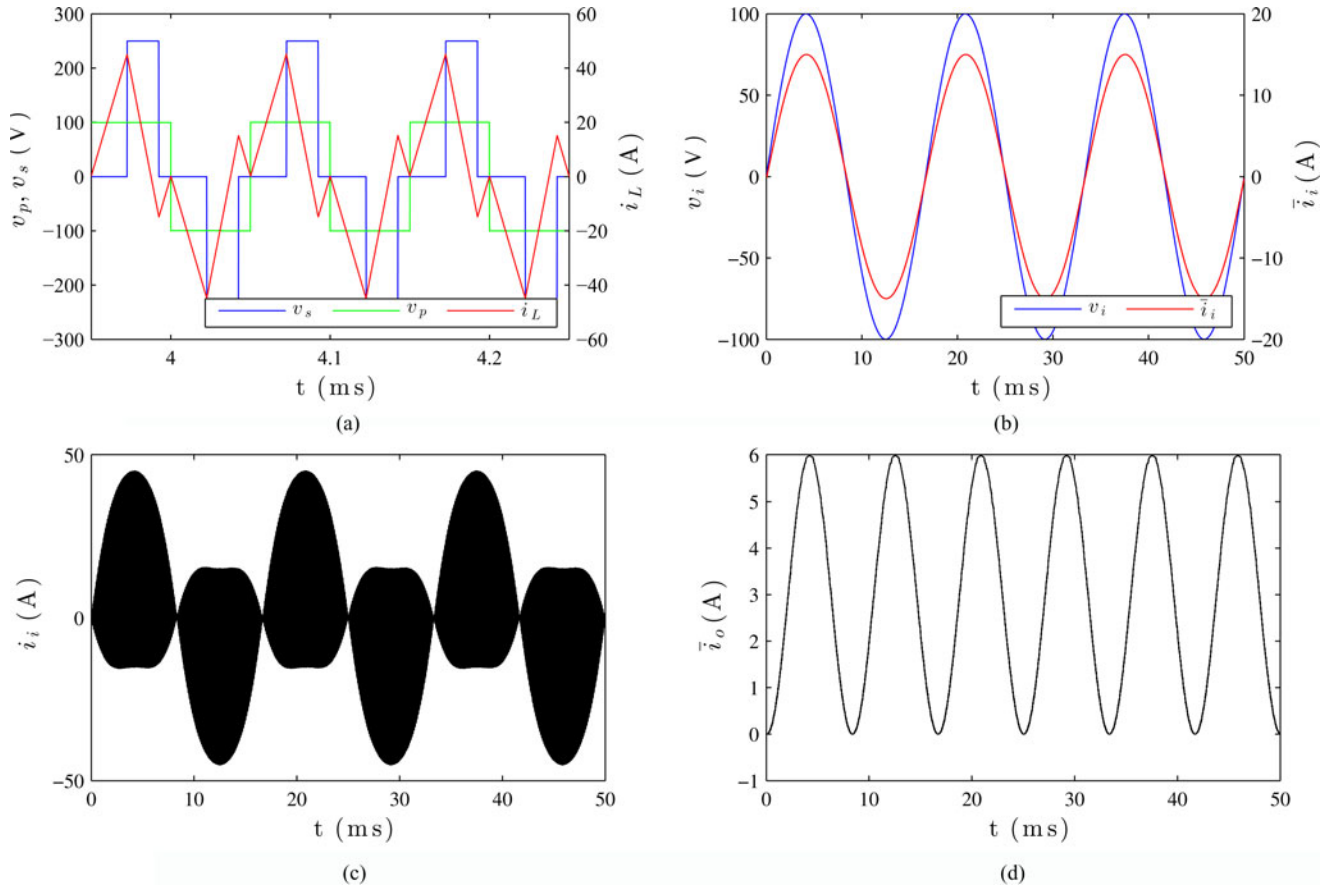


Fig. 4. Simulation results, $\delta = 0.3$. (a) Transformer voltages and current. (b) AC source voltage and average current. (c) AC source actual current. (d) Switching cycle average dc source current.

IV. EXPERIMENTAL RESULTS

The schematic of the experimental setup is shown in Fig. 6. The input filter, which is essential for eliminating high-frequency harmonic currents from the ac source current, is comprised of inductor L_f and capacitor C_f . The bidirectional switches are realized with two emitter tied insulated-gate bipolar transistor (IGBTs) and their antiparallel diodes (S_1, S_2, S_3, S_4). The current i_p is sensed and four-step current commutation is implemented for the ac-side converter, furthermore a clamp circuit is added for protection during faults. The switches on the DC source side are comprised of IGBTs with antiparallel diodes (S_5, S_6, S_7, S_8). The DC source V_o , in series with a small impedance Z_o , is in parallel with the capacitor C_o for the high-frequency current and second harmonic components. All of the devices used to implement the topology in Fig. 6 are described in Table III.

The ac-side converter and output H-bridge are modulated as described in Section II. The experiment is run at two different phase shifts, $\delta = 0.25$ and $\delta = -0.25$, and steady state measurements are taken. Due to finite magnetizing inductance and voltage drop across the switches, there is a small but nonzero inductive current in the primary winding. The ac-side converter is switched with four-step commutation [34], it essentially provides the required overlap time for the inductive current to flow during switching.

For a positive phase shift of $\delta = 0.25$, the transformer primary voltage, transformer primary current, and transformer secondary voltage are shown in Fig. 7(a). The switches in the ac-side H-bridge have some finite current at the instant of switching. In theory, this current is exactly zero; however, due to non-ideal switches and finite magnetizing current this current will not be zero in practice.

Voltage v_s is applied by the dc-side H-bridge. Note that in Figs. 7(a) and 8(a) when the voltage v_s makes a transition from 0 to V_o and $-V_o$ to 0, the inductor current is positive. This current is negative for the other two transitions. This observation confirms ZVS [35].

The input voltage and filtered source current are shown in Fig. 7(b). It is observed that the input current is sinusoidal, in phase with respect to voltage, and shows presence of minimal amount of high-frequency components. An FFT is computed on the input current, normalized to the fundamental, and is shown in Fig. 9(a). It is observed that the input current contains minimum harmonics.

For a negative phase shift of $\delta = -0.25$, the transformer primary voltage, transformer primary current, and transformer secondary voltage are shown in Fig. 8(a). The input voltage and current are shown in Fig. 8(b). The input current is out of phase with the input voltage denoting reversal of power flow. The input current also contains minimal harmonics. A FFT was computed on the input current and is shown in Fig. 9(b).

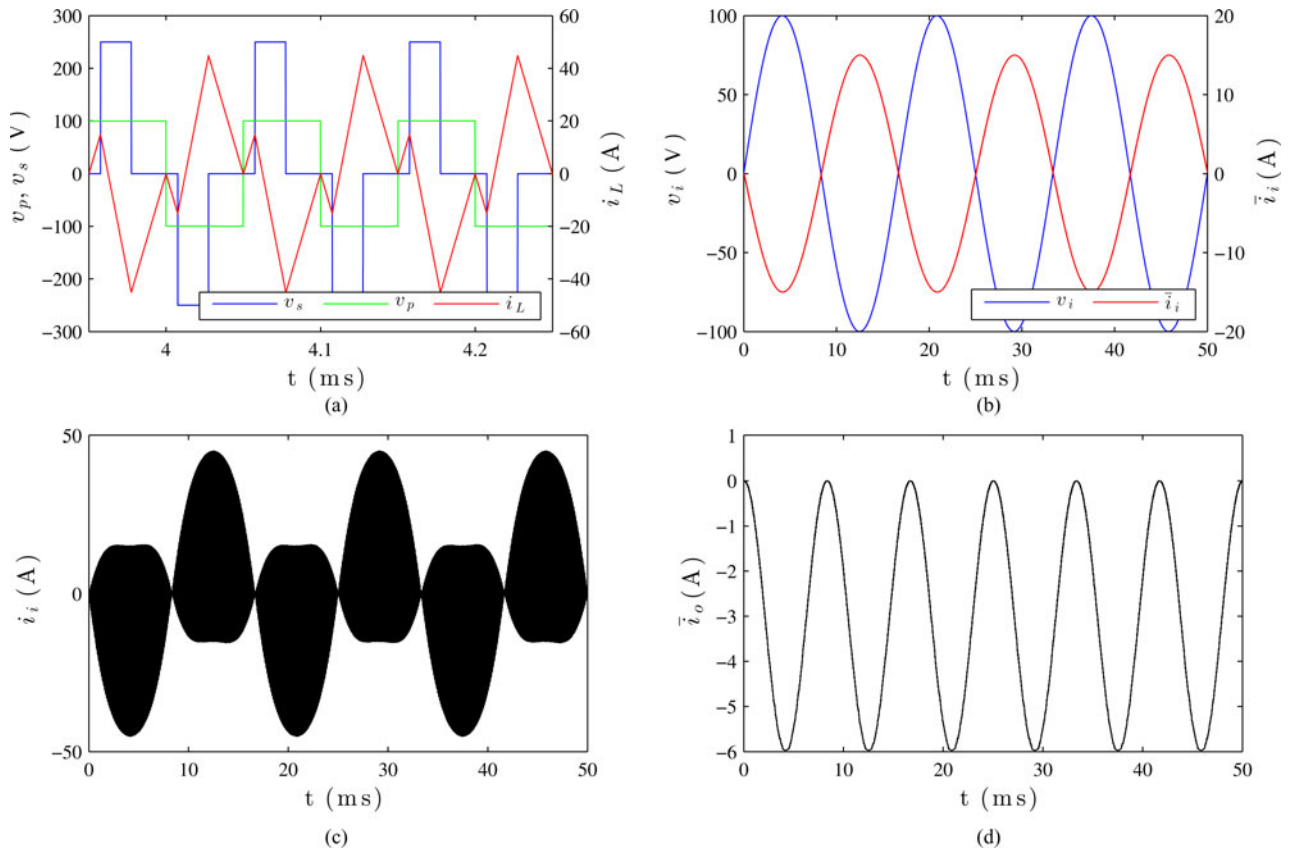


Fig. 5. Simulation results, $\delta = -0.3$. (a) Transformer voltages and current. (b) AC source voltage and average current. (c) AC source actual current. (d) Switching cycle average dc source current.

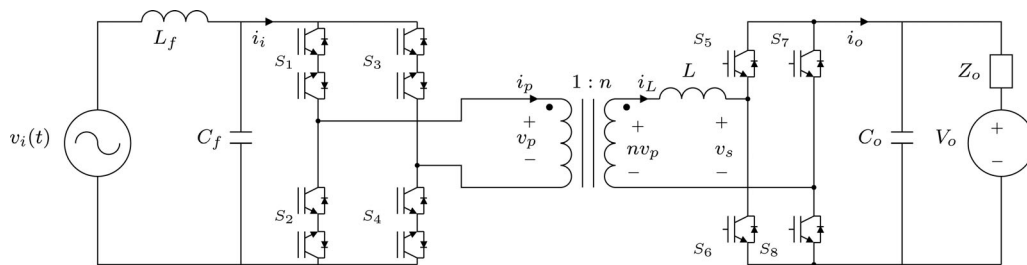


Fig. 6. Experimental topology setup.

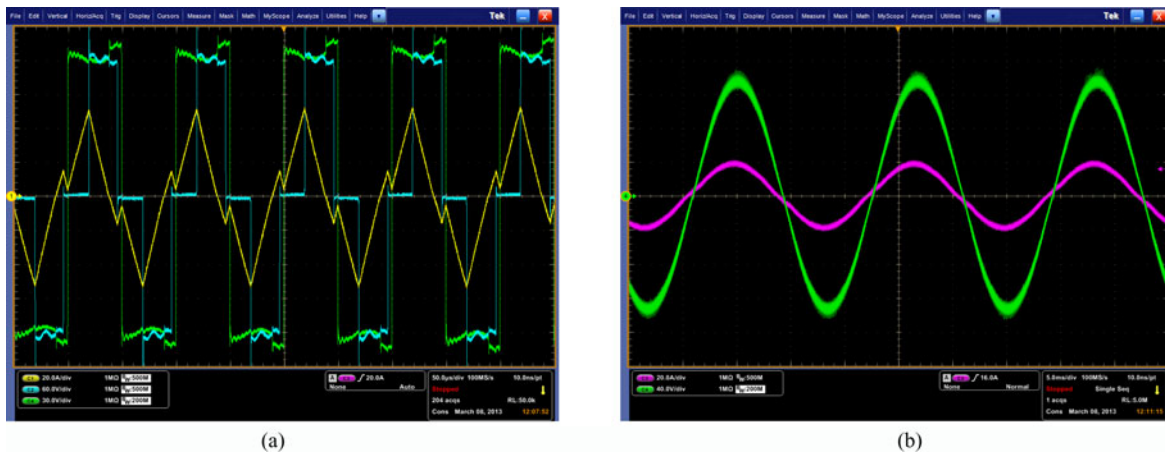


Fig. 7. Experimental results, positive phase shift $\delta = 0.25$, $\bar{P}_i = 1217$ W. (a) Primary voltage (30 V/div), secondary voltage (60 V/div), Inductor current (20 A/div), time (50 μ s/div). (b) AC source voltage (40 V/div), current (20 A/div), time (5 ms/div).

TABLE III
EXPERIMENTAL PARAMETERS

Part	Manufacturer	Part Number	Rating
AC Side IGBTs $S_1 - S_4$	Microsemi	APTG75TDU120PG	1200V 75A
DC Side IGBTs $S_5 - S_8$	Microsemi	APTGL120TA120TPG	1200V 120A
Input Inductor L_f	Magnetics Inc	K8020E060	497 μ F 2 Strands of Litz 30/31, 52 Turns
Input Capacitor C_f	Epcos	M108326076	20 μ F
Output Capacitor C_o	Epcos	M110897989	110 μ F
Transformer T_1	Magnetics Inc	0P49928EC	2 Strands of Litz 165/36 - 30 Turns Pri and Sec

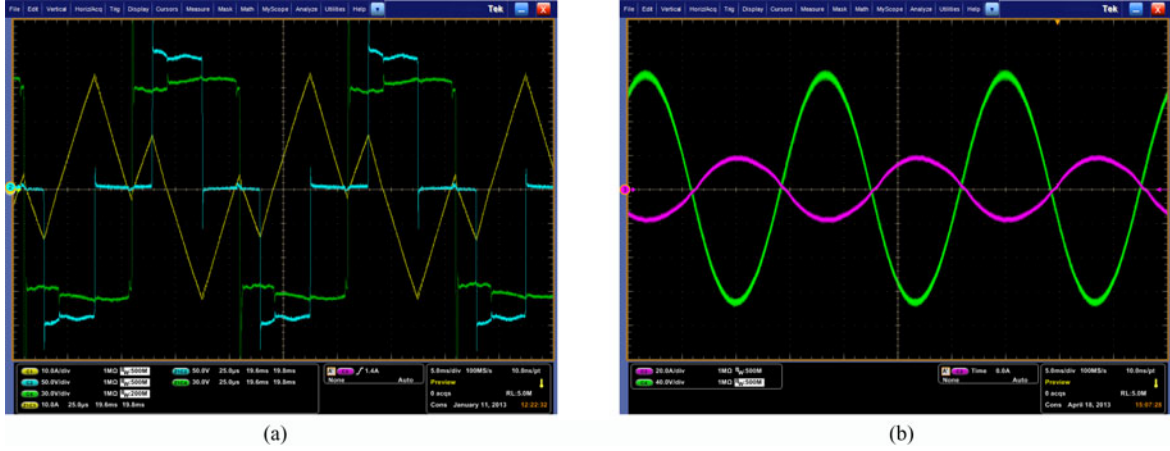


Fig. 8. Experimental results, negative phase shift $\delta = -0.25$, $\bar{P}_i = -1242$ W. (a) Primary voltage (30 V/div), secondary voltage (50 V/div), Inductor current (10 A/div), time (25 μ s/div). (b) AC source voltage (40 V/div), and current (20 A/div), time (5 ms/div).

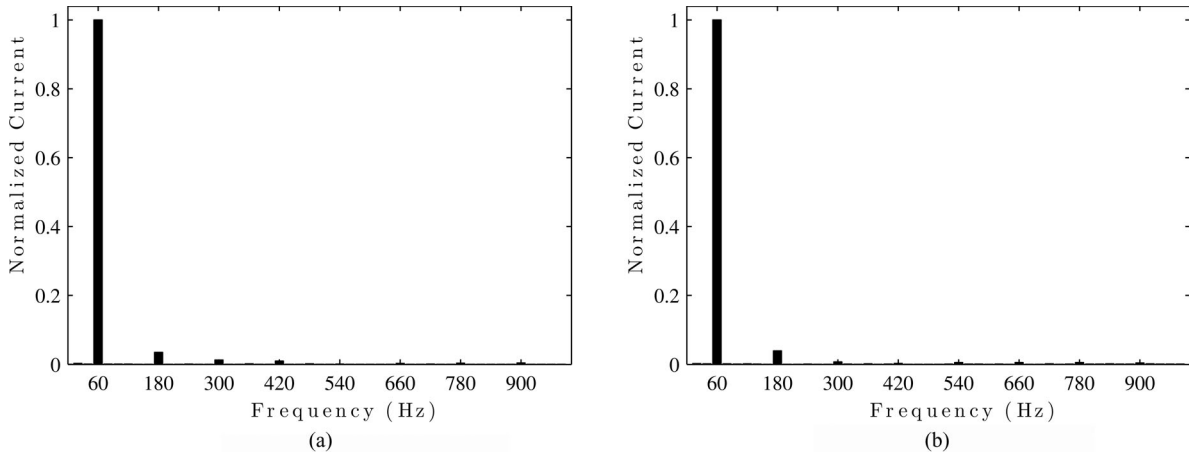


Fig. 9. Input current harmonics. (a) $\delta = 0.25$. (b) $\delta = -0.25$.

The peak of the average input current $\hat{i}_i = \frac{n^2 V_i \delta}{4L f_s}$ and average power for two different operating phase shifts were theoretically calculated and are shown in Table IV. The average power and peak of the filtered source current have been experimentally measured and are shown in Table IV for comparisons. From Table IV, it can be seen that theoretical predictions closely agree with experimental results. Experimental efficiency results are shown in Table V. Note the prototype was not designed to maximize efficiency, therefore these are preliminary efficiency

TABLE IV
THEORETICAL VERSUS EXPERIMENTAL

	Theoretical	Experimental	Theoretical	Experimental
δ		0.25	-0.25	
\hat{i}_i	17.67A	17.2A	17.67A	17.56A
\bar{P}_i	1250W	1217W	-1250W	-1242W

results. Many designs aspects can be considered to increase efficiency, for example: proper selection and sizing of switches, etc.

TABLE V
EXPERIMENTAL EFFICIENCY

Power	1441W	1349W	1264W	1179W	1101W	1015W	924W	842W	754W	672W	585W	499W
Efficiency	88.86%	89.96%	89.64%	89.44%	88.86%	88.98%	87.20%	86.67%	87.17%	86.02%	82.75%	80.05%

V. CONCLUSION

In this paper, a modulation scheme was proposed for a single-phase, bidirectional, isolated, ac–dc converter. Theoretical analysis, simulation, and experimental results were presented. The experimental results confirm the following predictions: 1) open-loop PFC; 2) ZCS for the switches in the ac-side converter; 3) transferred active power is proportional to the control variable; and 4) ZVS in the dc-side converter. Experimental results show that, due to nonideal effects such as voltage drop across the switches and presence of finite magnetizing currents, the ac-side converter switches at a very low current (not exactly zero). This converter with the proposed control is a promising solution for high-power applications, where isolation is necessary and efficiency and power density are important.

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