Grid-Side AC Line Filter Design of a Current Source Rectifier With Analytical Estimation of Input Current Ripple

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***Abstract*—This paper presents a systematic step-by-step design procedure for the input filter of a current source rectifier (CSR). The design is based on the specifications of allowable ripple in the input voltage of the CSR and high-frequency harmonic components in the grid current. Analytical techniques have been developed to estimate the ripple present in the input current and to model the converter for fundamental or grid frequency. The analysis is done for carrier-based and space-vector modulation of the current source rectifier and the model at grid frequency is used to evaluate the design of the filter for grid power factor, voltage drop across filter, etc. A damping resistance is designed ensuring a minimum power loss. The analysis and design of the input filter have been verified by simulations in MATLAB/Simulink and experimental tests on a laboratory prototype.**

***Index Terms*—Carrier-based modulation (CM), current source rectifier (CSR), input power factor, space-vector modulation (SVM), total harmonic distortion (THD).**

LIST OF SYMBOLS

i	Instantaneous.
$\bar{i}$	Averaged over T_s.
$\langle i \rangle_{\mathrm{RMS},T_s}$	RMS over T_s.
$\mathbf{I}$	Instantaneous space vector.
$\widetilde{i}$	Ripple component.
i_1	Fundamental component.

I. INTRODUCTION

A DC current link ac/ac converter, as shown in Fig. 1, employs a current source rectifier (CSR) to interface with the grid and a current source inverter (CSI) to generate adjustable frequency and magnitude-balanced three-phase current at the load end. This converter is used for high-voltage ac motor drives due to the following advantages: 1) inherent short-circuit protection; 2) easier fault management (no over current fault); 3) fast dynamic response due to direct current control; 4) regenerative capability; 5) high-quality waveforms resulting in reduced EMI and torque pulsations; and 6) no unreliable dc-link capacitor, etc [1]–[4]. Current source converters (CSR and CSI) have been considered for wind power generation [5]–[7] and hybrid electric vehicles [8]. Due to its inherent step-up capability current source converters (CSC) can be used to interface renewable energy sources with the grid [9]. One disadvantage of the current link system leading to its limited use is the loss in the dc-link inductor (L_{dc} in Fig. 1). Further advancement in super conducting magnetic energy storage (SMES) technology may help to overcome this limitation [10], [11]. Another significant drawback is that the current always has to pass through two semiconductors.

A CSR generates three-phase PWM current waveform from a dc current source. It is possible to align the average input current vector with the input voltage vector to draw current at a high power factor from the grid. The PWM current waveform is discontinuous and has harmonic components at the multiples of the switching/carrier frequency. An LC filter is used to minimize these unwanted high-frequency components from the grid current. Design and implementation of dc voltage link-based ac/ac converters (back to back converter) [12]–[15] and direct link matrix converters [16], [17] has been studied extensively in the literature. Due to its limited use, the input filter design of dc current link systems is less developed.

The design of the input LC filter requires an estimation of the higher harmonic ripple component present in the PWM line current. It is indicated in [18] that it is possible to compute the spectrum of the PWM line current but no explicit method is mentioned. Analytical estimation using modulation theory has been used in the case of matrix converters [19] and back to back converters [20]. However, such an approach requires computation with complicated Bessel function. An input current ripple for a matrix converter has been estimated from a simulation model in [21] and [22]. In this paper, a closed-form analytical expression for the RMS of the ripple component of line current has been derived. The computation is done for both carrier based modulation (CM) and space vector modulation (SVM). In comparison with offline techniques, such as selective harmonic elimination (SHE), CM, or SVM, can achieve fast dynamic response, high-input power factor, etc [23]–[25]. The design of an input filter for CSR modulated with SHE can be found in [26]–[28]. High-voltage IGBTs can be used to switch at a relatively higher frequency to implement CM or SVM [29], [30]. It has been shown that the results are identical for both

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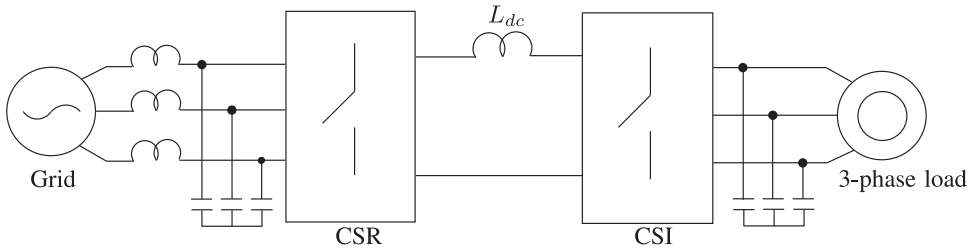

Fig. 1. Topology of the dc current link ac/ac converter.

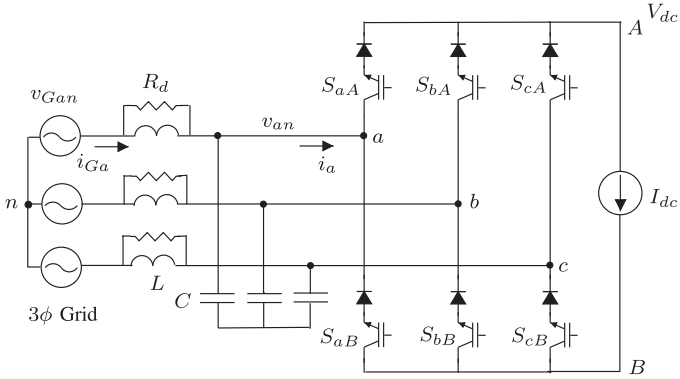

Fig. 2. CSR topology.

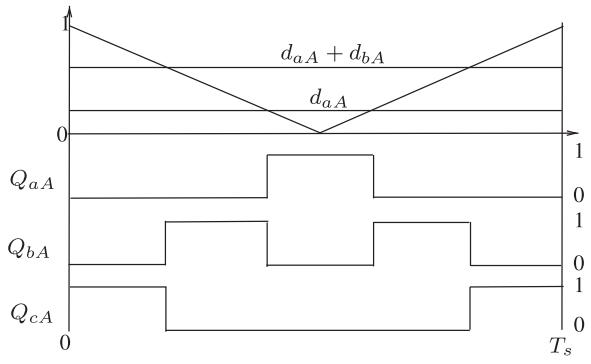

Fig. 3. Pulse Generation for the top leg.

CM and SVM. A simple expression of the RMS current ripple as a function of modulation index and magnitude of the dc-link current obviates need for computation with special functions or using a simulation model for ripple estimation.

To design the filter, CSR as shown in Fig. 2 has been modeled for the high-frequency component using the analytical estimation of the RMS current ripple. The values of different filter components are obtained from the specifications of the allowable THD in the grid current and distortion in the input voltage. The converter has been modeled for the fundamental component of the grid voltage in order to evaluate the design for: 1) minimum voltage drop across the filter; and 2) high grid power factor. A damping resistance is needed to eliminate oscillation at the LC resonant frequency and to improve the stability [31]. Virtual damping techniques are lossless, but require additional computation and sensing [32]–[35]. In this paper, a damping resistance is designed for the minimum power loss.

The organization of this paper is as follows. In Section II, the RMS value of the ripple component of the line current of a CSR has been computed for both space vector and carrier based modulation. A detailed step-by-step design of the input filter has been presented in Section III by modeling the CSR for different frequency components. The key simulation and experimental results are given in Section IV and V, respectively, and the paper concludes in Section VI.

II. Analysis

The CSR is modeled for different frequency components for filter design. For the switching frequency component, the input RMS current ripple is analytically computed. This computation along with modeling of the converter is dependent on the modulation strategy used. In this paper, two different commonly used modulation techniques CM and SVM are considered, as described in the next two sections. The list of symbols shows the convention used to represent different states of a particular variable.

A. Ripple Computation for CM

The topology of the CSR along with the input LC filter is shown in Fig. 2. For this analysis, let us assume the voltage drop across the inductor is small and the distortion in the input voltage is small. Equation (1) gives the grid and input voltages, where V is the peak and ω_G is the angular frequency. The converter consists of two legs, upper and lower. Each leg of the CSR consists of three switches, i.e., the switches in the top leg are S_{aA}, S_{bA}, and S_{cA}. In any one leg, no two switches can be ON simultaneously (to avoid the short circuit between the grid phases) and at least one switch has to be ON (to avoid an open circuit of inductive dc side current). In order to satisfy the second condition, the duty ratios of the switches S_{aA}, S_{bA}, S_{cA}, S_{aB}, S_{bB}, and S_{cB} should satisfy (2). The first condition is met by placing the pulses according to Fig. 3. T_s is the sampling or equivalent carrier period

$$\begin{aligned} v_{Gan} &= V\cos\omega_G t \approx v_{an} \\ v_{Gbn} &= V\cos\left(\omega_G t - \frac{2\pi}{3}\right) \approx v_{bn} \\ v_{Gcn} &= V\cos\left(\omega_G t + \frac{2\pi}{3}\right) \approx v_{cn} \end{aligned} \tag{1}$$

$$d_{ai} + d_{bi} + d_{ci} = 1 \qquad i \in [A, B]. \tag{2}$$

Four offset duty cycles D_a, D_b, D_c, and Δ are defined as in (3) and (4). These duty cycles are added to fundamental component of the duty cycle (for example $m\cos\omega_G t$ for d_{aA}) in order to satisfy (2) and to keep the duty cycles between 0 and 1. Modulation index m is defined as the ratio of the peak of the average synthesized input current to the dc-link current and can have a maximum value of 1 ($m = \frac{I}{I_{\rm dc}}$). The duty ratios for the array of switches S_{aA}, S_{bA}, S_{cA} and of S_{aB}, S_{bB}, S_{cB} are given in (5) and (6), respectively. Fig. 3 shows the pulse generation for switches S_{aA}, S_{bA}, and S_{cA} (top leg). A triangular carrier of frequency $f_s = \frac{1}{T_s}$ is used to generate the switching signals. Q_{aA} is 1 when switch S_{aA} is ON and 0 otherwise. The switching signals of the bottom leg are generated in the same way

$$D_a = 0.5|\cos\omega_G t|$$
$$D_b = 0.5\left|\cos\left(\omega_G t - \frac{2\pi}{3}\right)\right|$$
$$D_c = 0.5\left|\cos\left(\omega_G t + \frac{2\pi}{3}\right)\right| \tag{3}$$
$$\Delta = \frac{1-(D_a+D_b+D_c)}{2} \tag{4}$$
$$d_{aA} = 0.5m\cos\omega_G t + D_a + \Delta$$
$$d_{bA} = 0.5m\cos\left(\omega_G t - \frac{2\pi}{3}\right) + D_b$$
$$d_{cA} = 0.5m\cos\left(\omega_G t + \frac{2\pi}{3}\right) + D_c + \Delta \tag{5}$$
$$d_{aB} = -0.5m\cos\omega_G t + D_a + \Delta$$
$$d_{bB} = -0.5m\cos\left(\omega_G t - \frac{2\pi}{3}\right) + D_b$$
$$d_{cB} = -0.5m\cos\left(\omega_G t + \frac{2\pi}{3}\right) + D_c + \Delta. \tag{6}$$

As $i_a = (Q_{aA} - Q_{aB})I_{\rm dc}$, the average input current of phase a over a sampling period T_s is given in (7). Using (5) and (6), it is possible to note that the average input current is in phase with the input voltage. So for the fundamental component, the CSR can be modeled as an equivalent resistance R_e (8)

$$\overline{i_a} = (d_{aA} - d_{aB})I_{\rm dc}$$
$$= mI_{\rm dc}\cos\omega_G t$$
$$= I\cos\omega_G t \tag{7}$$
$$R_e = \frac{V\cos\omega_G t}{I\cos\omega_G t} = \frac{V}{mI_{\rm dc}}. \tag{8}$$

Fig. 4 shows the instantaneous i_a current over the kth carrier cycle. The pattern may change from cycle to cycle but the current will always have an amplitude of $I_{\rm dc}$ and will be flowing for $|d_{aA} - d_{aB}|T_s = m|\cos\omega_G(kT_s)|T_s$ amount of time. So, the RMS of this current over a switching cycle is given by (9). Provided $T_s \ll T$, the RMS of the input current over the kth fundamental cycle ($T = \frac{2\pi}{\omega_G}$) is given by (10). Using (9) and (10), we get an expression for the RMS value of the input current; see (11). The square RMS value of the ripple component

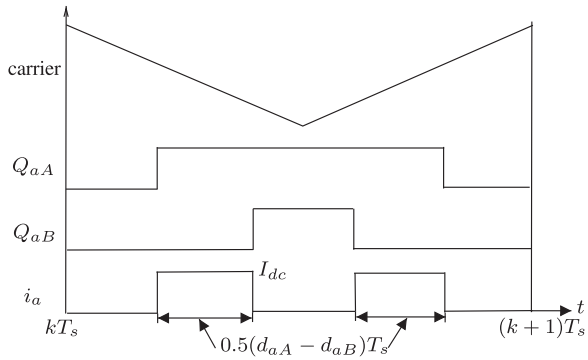

Fig. 4. i_a waveform over a switching cycle T_s.

of current $\langle\widetilde{i_a}\rangle_{{\rm RMS},T}$ is then given by the difference of square RMS value of total current and that of fundamental component of the current (12)

$$\langle i_a\rangle^2_{{\rm RMS},T_s}(kT_s) = I^2_{\rm dc}m|\cos\omega_G(kT_s)| \tag{9}$$
$$\langle i_a\rangle^2_{{\rm RMS},T} = \frac{1}{T}\sum_k \langle i_a\rangle^2_{{\rm RMS},T_s}(kT_s)T_s$$
$$\approx \frac{1}{T}\int_0^T I^2_{\rm dc}m|\cos\omega_G t|dt \tag{10}$$
$$\langle i_a\rangle^2_{{\rm RMS},T} = \frac{2I^2_{\rm dc}m}{\pi} \tag{11}$$
$$\langle\widetilde{i_a}\rangle^2_{{\rm RMS},T} = \langle i_a\rangle^2_{{\rm RMS},T} - \frac{I^2}{2} = m\left(\frac{2}{\pi} - \frac{m}{2}\right)I^2_{\rm dc}. \tag{12}$$

B. Space Vector Implementation

This section presents the analysis of the CSR for SVM. The current space vector is defined in (13). The two switching rules described in the previous section results in nine allowable switching states. Each of these states corresponds to one current space vector. The six active and three zero vectors of CSR are shown in Fig. 5(a). These six active vectors divides the complex plane into six symmetrical sectors (I, ..., VI). Here, [a b] refers to the switching state when switch S_{aA} and S_{bB} are ON. The zero vectors occur when we have [a a], [b b], or [c c] as switching states. In one sampling cycle T_s (carrier frequency of $1/T_s$), the reference input current vector $\overline{\mathbf{I}}$ is generated using two adjacent active vectors and one zero vector, whose duty ratios are given by (14), where β is the angular position of the average input current space vector with respect to the lagging vector or the first vector in the corresponding sector. The reference input current vector is aligned along the average input voltage vector in order to get power factor correction

$$\mathbf{I} = i_a + i_b e^{j2\pi/3} + i_c e^{-j2\pi/3} \tag{13}$$
$$dI_1 = m\sin\left(\frac{\pi}{3} - \beta\right)$$
$$dI_2 = m\sin\beta$$
$$dI_z = 1 - dI_1 - dI_2. \tag{14}$$

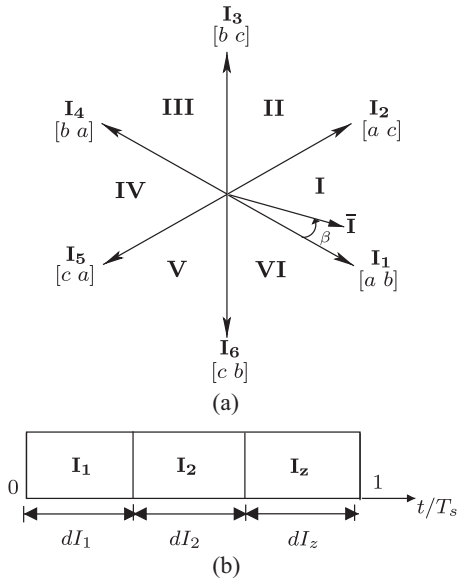

Fig. 5. (a) Current space vectors produced by CSR. (b) Switching sequence.

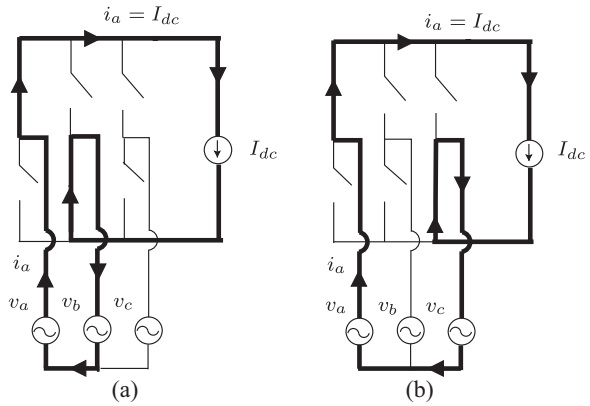

Fig. 6. Current flow paths for time periods (a) dI_1T_s and (b) dI_2T_s in Sector I.

In order to model the CSR for the ripple component of the input current, the total RMS of the input current is analytically computed. As shown in Fig. 5(b), one sampling cycle T_s is composed of time periods dI_1T_s, dI_2T_s, and dI_zT_s. Consider the position of average input current space vector to be in first sector (I) as shown in Fig. 5(a). During time period dI_1T_s, vector $\mathbf{I_1}$ ($[a\ b]$) is applied. So, the input phase a is connected to the dc-link. This implies during this time period, i_a is equal to $I_{\rm dc}$ as shown in Fig. 6(a). Similarly in dI_2T_s period with vectors $[a\ c]$ applied, the input line current is again $i_a = I_{\rm dc}$; see Fig. 6(b). When a zero vector $[a\ a]$ is applied, i_a is zero.

The square RMS of the input line current i_a over one sampling cycle T_s when $\bar{\mathbf{I}}$ is in the first (I) sector is given by (15). Similarly, it is possible to obtain the expressions for the square RMS of the input line current i_a over a sampling cycle when the input current space vector is in the second (II) and third (III) sectors, respectively, (15). In the second sector, $i_a = I_{\rm dc}$ for dI_1T_s period of time and in the third sector $i_a = I_{\rm dc}$ for dI_2T_s period of time, respectively, and it is zero otherwise. These

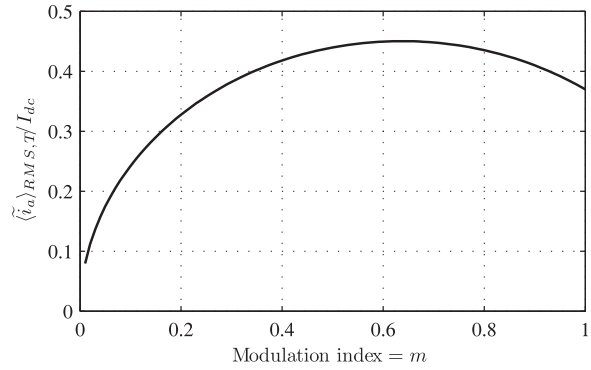

Fig. 7. Variation of $\langle \widetilde{i_a} \rangle_{\rm RMS,T}/I_{\rm dc}$ over m.

expressions repeat for other three sectors. Note $\bar{\mathbf{I}}$ moves over one sector in $T/6$ period of time. Equation (16) shows how to relate RMS over one sampling cycle to the RMS over one sector assuming $T \gg T_s$. Using (14) and (16), it is possible to obtain the RMS of the input line current i_a over one sector. Finally the RMS of i_a over one cycle of the fundamental component of input current can be obtained from the RMS of each sector using (17). Hence, the input RMS current is obtained as a function of modulation index as shown in (18). The RMS of the ripple current is obtained by subtracting the RMS of the fundamental component from total input RMS current (19). Equation (19) provides an analytical expression for the input RMS current ripple in terms of modulation index and the dc-link current. Note that this result is identical to (12). Fig. 7 shows a plot of $\langle \widetilde{i_a} \rangle_{\rm RMS,T}/I_{\rm dc}$ as a function of m and it is maximum at $m = \frac{2}{\pi} \approx 0.6366$

$$\langle i_a \rangle^2_{{\rm RMS},T_s} = \begin{cases} dI_1 I_{\rm dc}^2 + dI_2 I_{\rm dc}^2 & \text{SECTOR I} \\ dI_1 I_{\rm dc}^2 & \text{SECTOR II} \\ dI_2 I_{\rm dc}^2 & \text{SECTOR III} \end{cases} \tag{15}$$

$$\begin{aligned} \langle i_a \rangle^2_{\rm RMS,SECTOR} &= \frac{6}{T} \sum_k \langle i_a \rangle^2_{{\rm RMS},T_s}\,(kT_s) T_s \\ &\approx \frac{6}{T} \int_{\rm SECTOR} \langle i_a \rangle^2_{{\rm RMS},T_s}\, dt \end{aligned} \tag{16}$$

$$\langle i_a \rangle^2_{{\rm RMS},T} = \frac{1}{3} \sum_{i={\rm I,II,III}} \langle i_a \rangle^2_{{\rm RMS,SECTOR}_i} \tag{17}$$

$$\langle i_a \rangle^2_{{\rm RMS},T} = \frac{2m}{\pi} I_{\rm dc}^2 \tag{18}$$

$$\langle \widetilde{i_a} \rangle^2_{{\rm RMS},T} = m \left(\frac{2}{\pi} - \frac{m}{2} \right) I_{\rm dc}^2. \tag{19}$$

III. Filter Design

The switching of the CSR injects high-frequency harmonics into its line currents. To eliminate these switching frequency components and draw smooth continuous sinusoidal currents from the grid, a passive LC filter is employed. This section

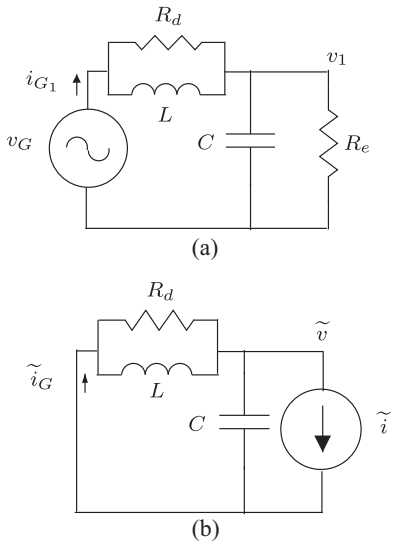

Fig. 8. (a) Perphase equivalent circuit at fundamental frequency. (b) Perphase equivalent circuit at switching frequency.

presents a step-by-step design procedure of this filter. In this design, the CSR is modeled using the analysis given in the previous sections.

The input current consists of higher frequency switching components along with the fundamental grid frequency component. Using the principle of superposition, the CSR is modeled and analyzed independently for both these components. By appropriate modulation, the input current is aligned in phase with the input voltage. Hence for the fundamental component, the converter appears as an effective resistance R_e to the input filter, as shown in Fig. 8(a). R_e has been derived in (8). The RMS of the ripple component is analytically computed in (12) and (19). Due to pulse-width modulation, the first group of dominant harmonic components in the input current waveform appears to be at and around the sampling or equivalent carrier frequency $f_s = 2\pi/\omega_s$. The other harmonic components occurs at and around the multiples of sampling frequency. Assuming the entire energy in the input current spectrum other than the fundamental to be concentrated at the switching frequency, the CSR is modeled as a sinusoidal current source at frequency f_s with a RMS given in (12) or (19); see Fig. 8(b). This results in a slight over design of the filter components. A damping resistance is introduced in parallel with the filter inductor L to mitigate oscillations near the resonance frequency of the LC network. The parallel damping resistor is designed to restrict the power loss to a minimum.

The LC filter is designed such that the RMS of the ripple component of the grid current, must be within a limit in order to maintain a particular THD. According to IEEE 519, THD in the grid current must be less than 5% of the fundamental current. For the proper operation of the CSR, the input voltage of the CSR must have a limited amount of higher harmonic ripple $\langle\widetilde{v}\rangle_{\mathrm{RMS},T}$. Analyzing the circuit as shown in Fig. 8(b), it is possible to express both of these ripple components in terms of $\langle\widetilde{i}\rangle_{\mathrm{RMS},T}$ (20), (21). Fig. 9 shows the magnitude plot of the transfer function between the grid current and the input current.

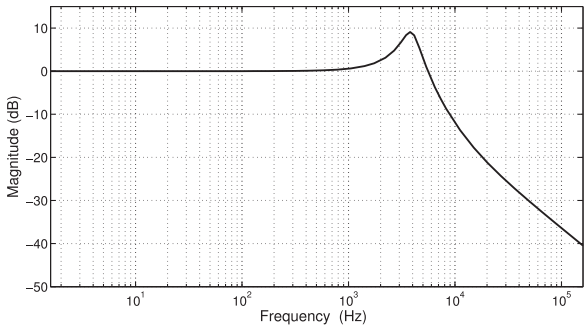

Fig. 9. Bode magnitude plot of the transfer function between grid current and input current of the CSR considering the model at high frequency.

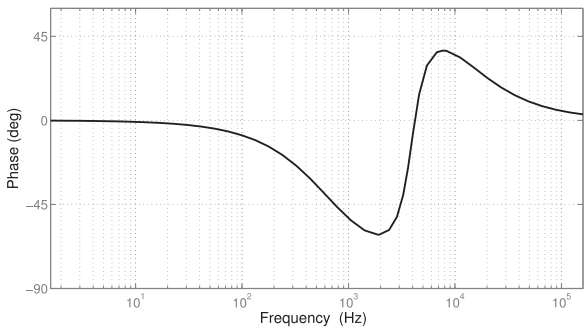

Fig. 10. Phase plot of the transfer function between grid voltage and grid current of the CSR considering the model for fundamental/grid frequency.

It has a low-pass filter characteristic. The slight overshoot in the magnitude plot exists at the resonant frequency of the LC network. The damping resistor limits this resonant peak. Analyzing the circuit for the fundamental component, it is possible to compute the ratio of the power loss P_{loss} in the damping resistor to the total output power P of the converter, (22). The power loss is considered only due to the fundamental component of the current as most of the higher order harmonics of the line current passes through the filter capacitor. Equations (20), (21), and (22) can be solved simultaneously to determine L, C, and R_d

$$\langle\widetilde{i}_G\rangle_{\mathrm{RMS},T} = \frac{\langle\widetilde{i}\rangle_{\mathrm{RMS},T}}{\left(1+\frac{(1-\omega_s^2LC)^2-1}{\left(1+\frac{\omega_s^2L^2}{R_d^2}\right)}\right)^{1/2}} \tag{20}$$

$$\langle\widetilde{v}\rangle_{\mathrm{RMS},T} = \frac{\langle\widetilde{i}\rangle_{\mathrm{RMS},T}}{\left((\omega_sC-\frac{1}{\omega_sL})^2+\frac{1}{R_d^2}\right)^{1/2}} \tag{21}$$

$$\frac{P_{\mathrm{loss}}}{P} = \frac{\langle i_{G_1}\rangle_{\mathrm{RMS},T}}{\langle v_G\rangle_{\mathrm{RMS},T}}\left(\frac{\omega_G^2L^2R_d}{\omega_G^2L^2+R_d^2}\right). \tag{22}$$

The filter design is checked by analyzing the model at the fundamental frequency. In (23), θ_G is the power factor angle. It is necessary that the grid current must be drawn close to unity power factor or the angle θ_G must be close to zero. As shown in Fig. 10, the phase angle is very close to zero at low frequency (grid frequency). The voltage drop in the fundamental

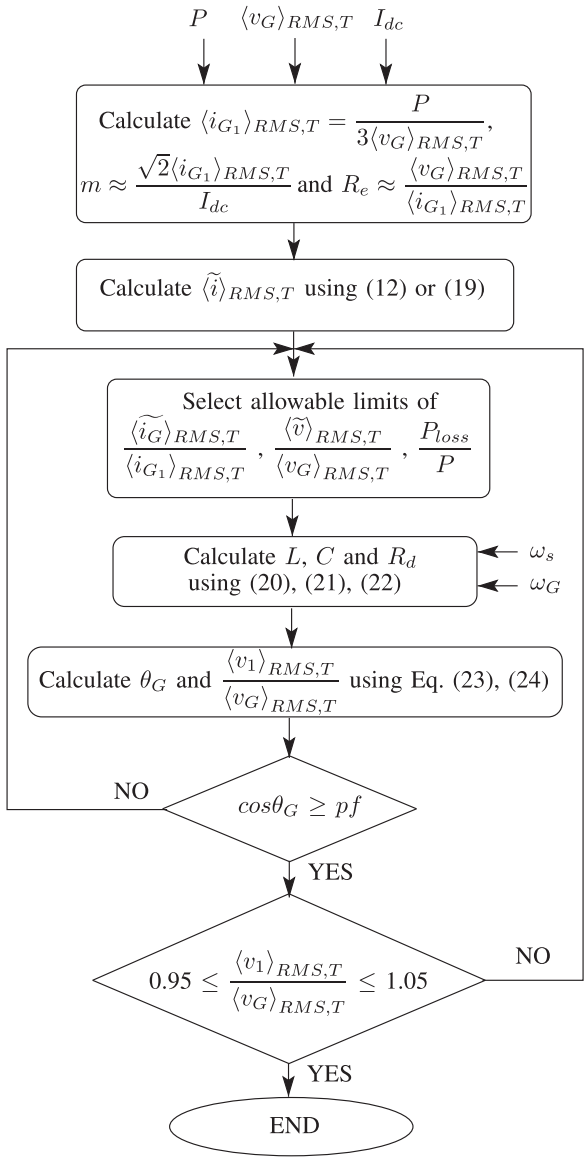

Fig. 11. Flowchart for the filter design of CSR.

component across the filter must be small or the ratio of the fundamental component of the grid voltage to that of the input voltage of the CSR must be close to unity (24). If these values are not within appreciable limits, then we need to go back and change the specifications and recalculate the values of L, C, and R_d. If the grid power factor is below a minimum required power factor pf and does not fall within appreciable limits, then the specification of $\langle\widetilde{i_G}\rangle_{\mathrm{RMS},T}/\langle i_{G_1}\rangle_{\mathrm{RMS},T}$ needs to be changed, and if there is a large drop across the filter, specification of $\langle\widetilde{v}\rangle_{\mathrm{RMS},T}/\langle v_G\rangle_{\mathrm{RMS},T}$ should be modified, and filter parameters are recalculated. The entire design procedure is shown in the flowchart in Fig. 11

$$\theta_G = \tan^{-1}\omega_G C R_e + \tan^{-1}\frac{\omega_G L}{R_d} - \tan^{-1}\frac{\omega_G L(R_e+R_d)}{R_e R_d(1-\omega_G^2 LC)} \tag{23}$$

$$\frac{\langle v_1\rangle_{\mathrm{RMS},T}}{\langle v_G\rangle_{\mathrm{RMS},T}} = \frac{R_e\left(R_d^2+\omega_G^2L^2\right)^{0.5}}{\left(\omega_G^2L^2(R_e+R_d)^2+R_e^2R_d^2(1-\omega_G^2LC)^2\right)^{0.5}}. \tag{24}$$

IV. Simulation Results

The CSR as shown in Fig. 2 is simulated with ideal switches in MATLAB/Simulink with SVM technique. The simulation results are presented in this section. The converter is supplied from a three-phase grid of 3.3 kV (line to line RMS) at 60 Hz and $I_{\mathrm{dc}} = 124$ A. The switching frequency ($f_s = 1/T_s$) is set at 2 kHz. The variation of $\langle\widetilde{i}\rangle_{\mathrm{RMS},T}/I_{\mathrm{dc}}$ with the modulation index of the CSR is shown in Fig. 12(a). The simulated points confirm the analytically predicted continuous plot. Hence, this verifies the analytical estimation of the RMS input current described in Section II.

The rest of the simulation is done at a full modulation index of 1. At 3.3 kV and 0.5 MW, the peak of the fundamental component of the grid current is 123.7 A. This implies I_{dc} must be 123.7 A for $m = 1$. The dc side is simulated using an ideal current source of 124 A. Following the first step of calculation in the flowchart in Fig. 11, the effective resistance R_e of the CSR is close to 21.78 Ω. The RMS of the switching current ripple, $\langle\widetilde{i}\rangle_{\mathrm{RMS},T}$ is 45.7 A, see (19). The maximum allowable ripple in the grid current and distortion in the input voltage are assumed to be 2.5% of fundamental component of the input current and grid voltage, respectively. The power loss in damping resistor is restricted to be 0.1% of rated power. Input filter components $L = 2.4$ mH, $C = 34.64$ μF and $R_d = 50\,\Omega$ are designed according to the procedure described in Section III. Fig. 12(b) shows the dc-link voltage and Fig. 12(c) shows the dc-link current. Fig. 12(d) shows the line to neutral voltage and Fig. 12(e) shows the line current of phase a of the CSR. The input current RMS obtained from simulation is 98.5 A, which very closely matches the analytical value of 98.7 A as computed from Section II. The filtered grid voltage and corresponding line current (5 times) are shown in Fig. 12(f). The line current i_G is almost in phase with the grid voltage v_G ($\cos\phi = 0.9725$). The frequency spectrum of various voltage and current waveforms are plotted in Fig. 13. As can be seen from Figs. 12(f) and 13(d), the grid current is almost sinusoidal with a THD content of 1.91%. Also, the input voltage to the CSR v_{an} is almost sinusoidal as seen from Figs. 12(d) and 13(a). From Fig. 13(a) and (c), it can be noted that the voltage drop across the filter at fundamental frequency (60 Hz) is negligibly small or $\frac{v_{an1}}{v_{Gan}} \approx 1$.

V. Experimental Results

This section presents the experimental results obtained on a laboratory prototype of the CSR as shown in Fig. 14. The CSR is implemented using two *Microsemi's* triple dual common source IGBT power modules, APTGT75TDU120PG. IGBT driver 2SD106AI from CONCEPT is used to generate isolated gate pulses for the switches. The entire modulation strategy is coded in verilog onto a control platform based on FPGA (Xilinx XC3S500E). The setup is operated with both the modulation schemes described in Section II. The experimental

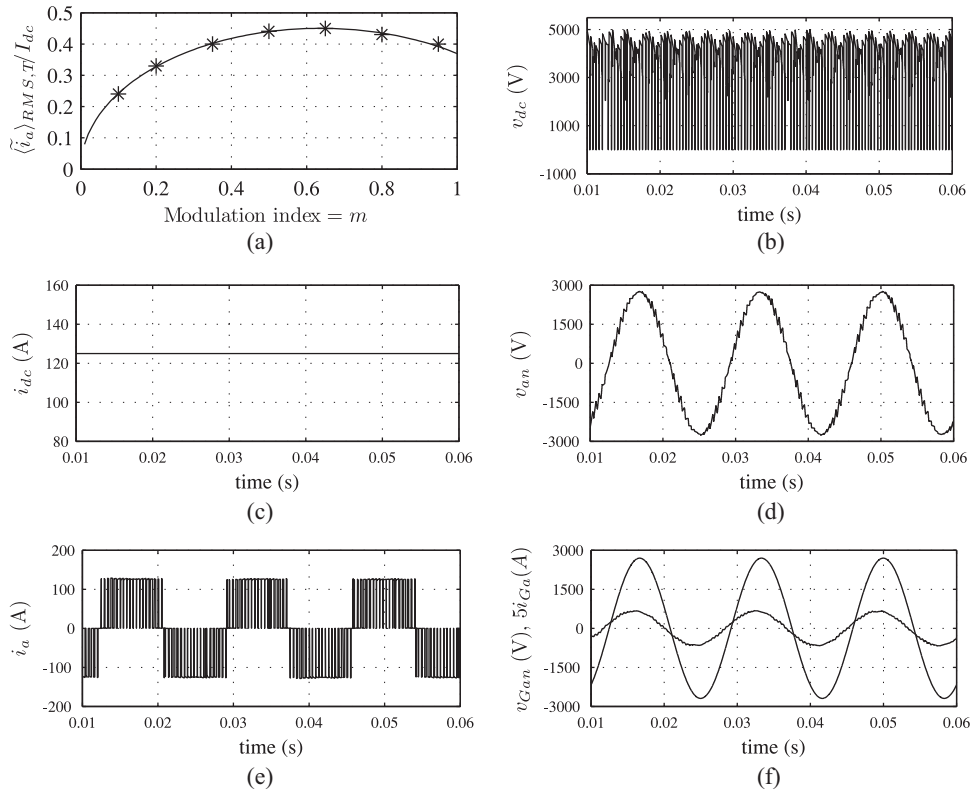

Fig. 12. (a) RMS ripple current with modulation index. (b) DC-link voltage. (c) DC-link current. (d) Line to neutral voltage. (e) Line current. (f) Grid voltage and current.

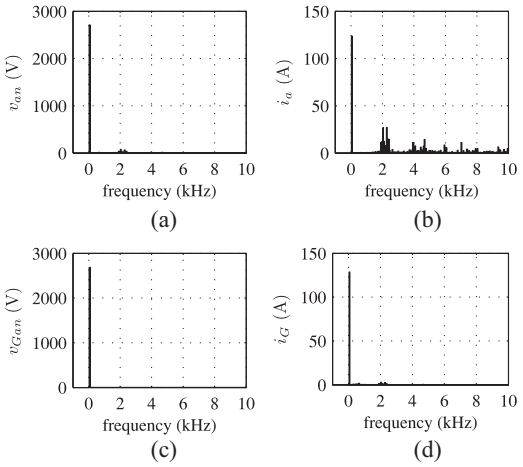

Fig. 13. Simulation results: Frequency spectrum.

parameters are $\langle v_G \rangle_{\mathrm{RMS},T} = 50\,\mathrm{V}$, $m = 0.5$, $f_G = 60$ Hz, $f_s = 5$ kHz. The dc-link current is realized with a series R–L circuit, $R_{\mathrm{dc}} = 10.4\,\Omega$, $L_{\mathrm{dc}} = 27$ mH. The corner frequency $\frac{R_{\mathrm{dc}}}{2\pi L_{\mathrm{dc}}} = 61.3$ Hz is chosen to be much lower than the switching frequency $f_s = 5$ kHz so that the current through it is close to dc. Assuming no voltage drop across the input LC filter and no power loss in the CSR, the dc component of the dc-link voltage will be 53 V ($V_{\mathrm{dc}} = \frac{3}{2} m(\sqrt{2}\langle v_G \rangle_{\mathrm{RMS},T})$). This implies I_{dc} will be approximately 5.09 A ($I_{\mathrm{dc}} = \frac{V_{\mathrm{dc}}}{R_{\mathrm{dc}}}$). From (18), $\langle \widetilde{i} \rangle_{\mathrm{RMS},T} = 2.24$ A. Again assuming no power loss ($3\langle v_G \rangle_{\mathrm{RMS},T} \langle i_{G_1} \rangle_{\mathrm{RMS},T} = V_{\mathrm{dc}} I_{\mathrm{dc}}$), one can estimate $\langle i_{G_1} \rangle_{\mathrm{RMS},T}$ to be 1.8 A and the effective resistance of the CSR ($R_e \approx \frac{\langle v_G \rangle_{\mathrm{RMS},T}}{\langle i_{G_1} \rangle_{\mathrm{RMS},T}}$) to be 27.3 Ω. For an allowable ripple of 2.5% in grid current ($\frac{\langle \widetilde{i}_G \rangle_{\mathrm{RMS},T}}{\langle i_{G_1} \rangle_{\mathrm{RMS},T}}$) and line voltage ($\frac{\langle \widetilde{v} \rangle_{\mathrm{RMS},T}}{\langle v_G \rangle_{\mathrm{RMS},T}}$) and a power loss ($\frac{P_{\mathrm{loss}}}{P}$) of 0.001% in the damping resistor, the filter values are calculated using (20), (21), and (22). The designed values are $L = 0.37$ mH, $C = 32.3\,\mu$F and $R_d = 12\,\Omega$. The current and voltage ratings of all semiconductor devices and passive components are chosen to be higher than the operating conditions.

The results corresponding to carrier-based implementation are shown in Fig. 15. Fig. 15(a) shows the dc-link current and voltage of the CSR. As seen from the waveform, the experimental current magnitude of 4.94 A is slightly lower as compared to its analytical value of 5.09 A. This can be attributed to the power loss in the CSR and nonunity voltage gain of the LC filter at the fundamental frequency. Fig. 15(b) shows the line to neutral voltage and switched line current of one phase. The RMS value of the input current is 2.7 A which closely matches the analytically calculated RMS value of 2.78 A. The grid voltage and line current are shown in Fig. 15(c) and are nearly sinusoidal. The grid power factor is close to unity ($\cos\theta_G = 0.95$). The frequency spectrum of the four ac-side waveforms are shown in Fig. 15(d). As can be seen the fundamental component of the input voltage of the CSR and grid voltage are almost equal. Thus, there is a negligible drop across the filter. Fig. 15(d) also confirms that the line current is almost sinusoidal.

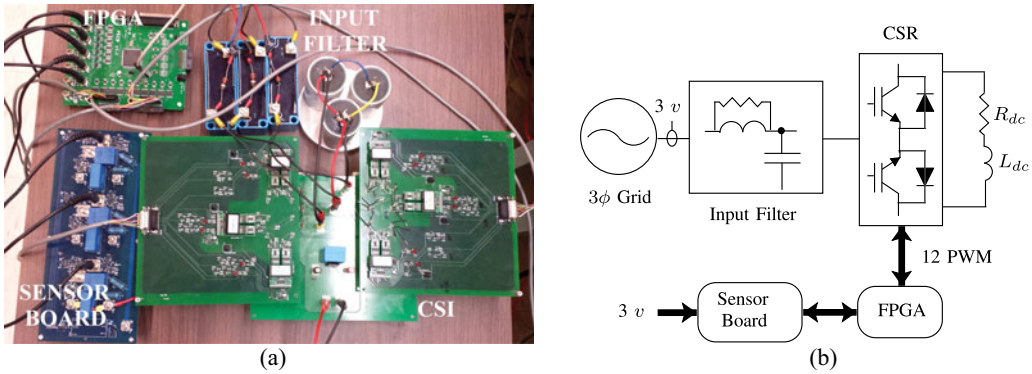

Fig. 14. Hardware setup.

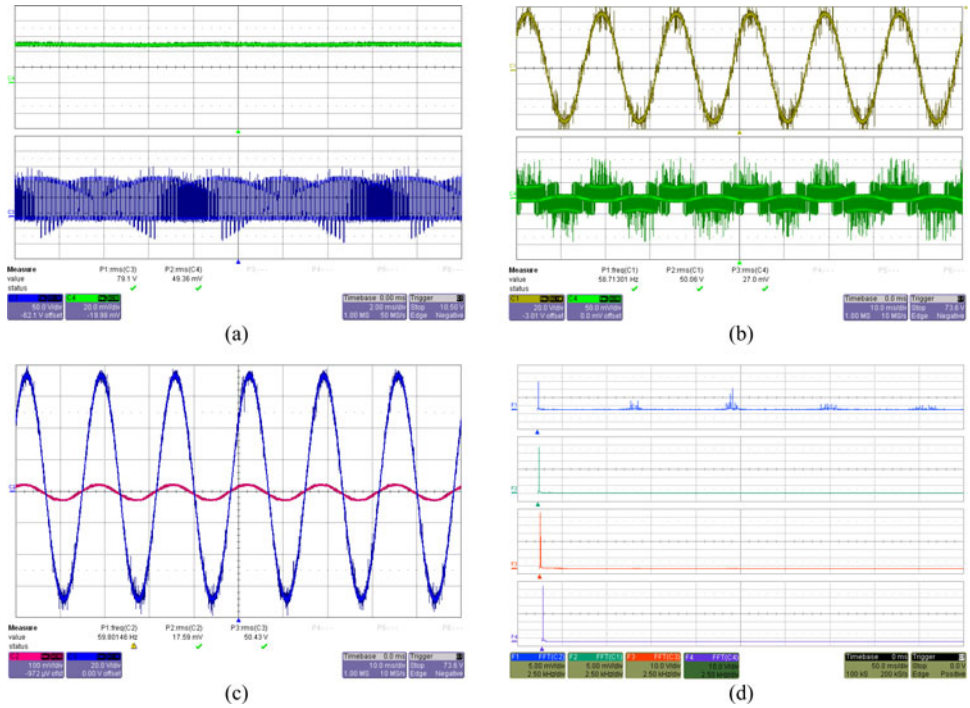

Fig. 15. Carrier-based PWM results: (a) (top) dc current (2 A/div), (bottom) dc voltage (50 V/div) (Timescale: 2 ms/div); (b) (top) Line to neutral voltage (20 V/div), (bottom) Line current (5 A/div) (Timescale: 10 ms/div); (c) Grid voltage (20 V/div) and grid current (10 A/div) (Timescale: 10 ms/div); (d) Frequency spectrum: (top) Line current (5 A/div), (second from top) grid current (5 A/div), (third from top) line to neutral voltage (20 V/div), (bottom) grid line to neutral voltage (20 V/div). (Sampling frequency: 2 MS/s).

The same setup with the same set of parameters was operated with SVM described in Section II. Same results are plotted for SVM in Fig. 16. It is possible to observe that the pattern of instantaneous dc-link voltage and line current are different from CM implementation. The measured RMS of the line currents is 2.6 A. This closely matches the analytically computed value of 2.78 A. Thus, it verifies the claim that the analytical expression of input RMS current obtained is independent of the modulation strategy.

The system was run with different set of filters for different allowable ripple specifications in the grid current. Fig. 17 shows the grid line to neutral voltage and current for allowable THD $= 1\%$ ($L = 0.37$ mH, $C = 81.7\,\mu$F), THD $= 2.5\%$ ($L = 0.37$ mH, $C = 32.3\,\mu$F) and THD $= 5\%$ ($L = 0.37$ mH, $C = 15.8\,\mu$F). The resulting input power factor obtained is 0.77, 0.95, and 0.99, respectively. The observation was made that with the reduction in amount of allowable ripple in grid current, for a fixed switching frequency, the inductance remains same and capacitance increases, leading to poor grid power factor.

VI. Conclusion

A systematic design procedure for the input filter required to attenuate the switching components present in the input currents of a CSR has been presented in this paper. The design procedure needs an estimation of the ripple component present in the input line currents. This paper presented an analytical method to estimate this ripple for two most commonly used modulation strategies. The derived equations are a function of the modulation index of the CSR and the dc-link current. The design is based on the specifications of the THD of the grid current

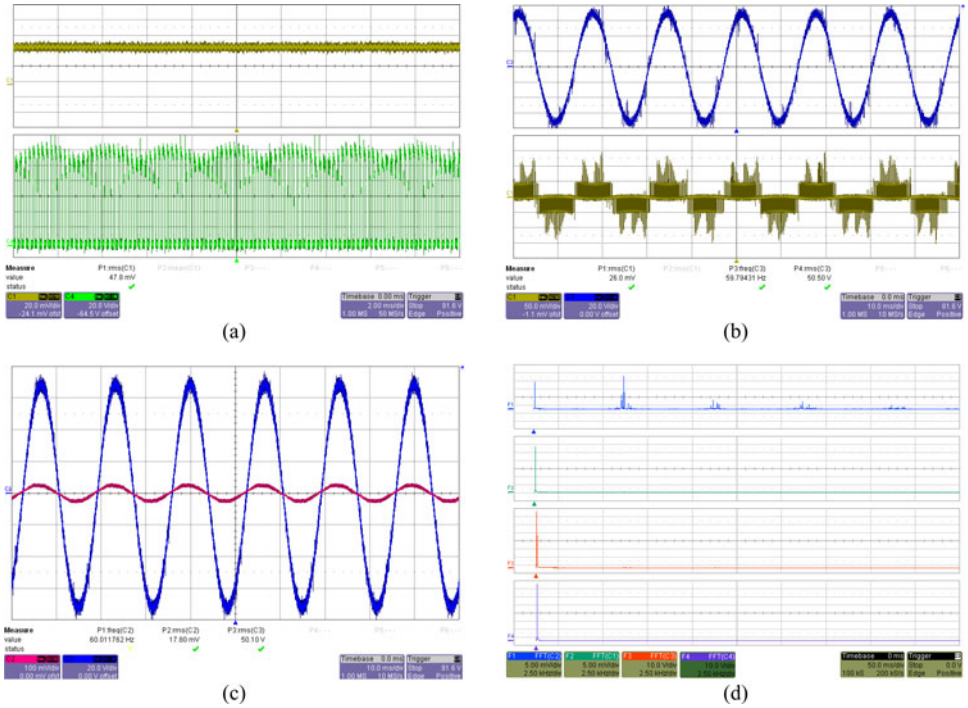

Fig. 16. Space vector PWM results: (a) (top) dc current (2 A/div), (bottom) dc voltage (20 V/div) (Timescale: 2 ms/div); (b) (top) Line to neutral voltage (20 V/div), (bottom) Line current (5 A/div) (Timescale: 10 ms/div); (c) Grid voltage (20 V/div) and grid current (10 A/div) (Timescale: 10 ms/div); (d) Frequency spectrum: (top) Line current (5 A/div), (second from top) grid current (5 A/div), (third from top) line to neutral voltage (20 V/div), (bottom) grid line to neutral voltage (20 V/div). (Sampling frequency: 2 MS/s).

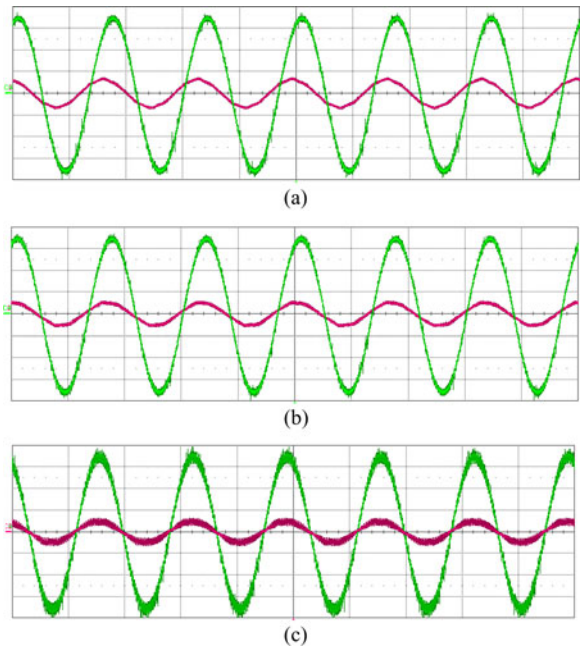

Fig. 17. (a) Grid voltage (20 V/div) and current (5 A/div) for allowable THD $= 1.0\%$, (b) Grid voltage (20 V/div) and current (5 A/div) for allowable THD $= 2.5\%$, and (c) Grid voltage (20 V/div) and current (5 A/div) for allowable THD $= 5.0\%$.

and the allowable ripple voltage at the input of the converter. The designed filter ensures high input power factor, low voltage drop in the filter and minimum ohmic loss in damping resistor. A detailed simulation and experimental validation of the entire system confirms the analytical estimation of the input current ripple of the CSR and the proposed filter design.

APPENDIX

A. *Differential Mode EMI Filter Design of the CSR*

The main objective of the input ac line filter is to eliminate the switching frequency components of the input current and to achieve a THD less than 5% (IEEE 519). But this is not the complete story. One needs to design another filter (EMI) to meet the regulations in the frequency range of 150 kHz to 30 MHz. Here, a procedure for the differential mode EMI filter design of a CSR is presented. This EMI filter is designed as a next step after designing the input ac line filter following the procedure shown in the main paper. The common-mode EMI filter design follows a very similar procedure but requires evaluation of parasitics and is out of the scope of this study. Measurement of the high-frequency component (150 kHz to 30 MHz) in the grid current is done by a network called line impedance stabilization network (LISN) as shown in Fig. 18. According to FCC regulation the measured voltage across the 100 Ω resistance in the frequency range of 150 kHz to 30 MHz must be less than 1 mV (60 dB$\cdot\mu$V). The measured voltage of the CSR with the input line filter as designed in Section IV is 8 mV (78 dB$\cdot\mu$V). Fig. 19 shows the spectrum of the measured voltage in the range 150 kHz to 1 MHz. It peaks near 150 kHz and keeps reducing afterward (that is why spectrum beyond 1 MHz is not shown). In this frequency range, the LISN can be approximated as 100 $\Omega = Z_L$ resistive load. Again CSR can be modeled as a current source (I_s). Fig. 20

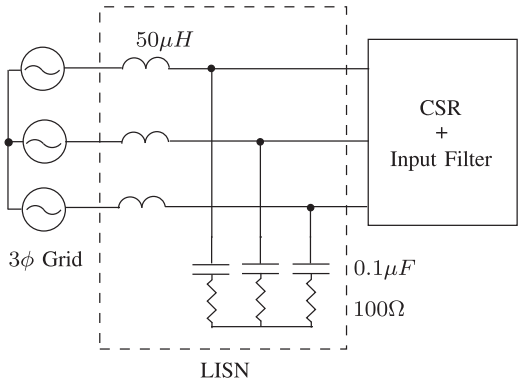

Fig. 18. Line impedance stabilization network (LISN).

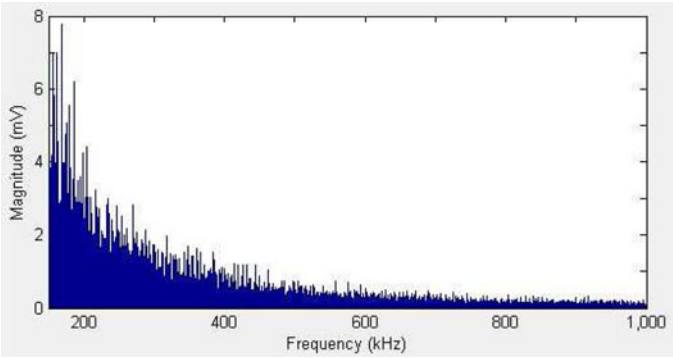

Fig. 19. Simulation results: Frequency spectrum of grid current without EMI filter using LISN.

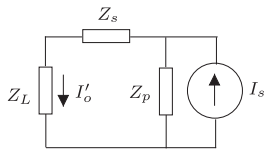

Fig. 20. CSR with AC input line filter.

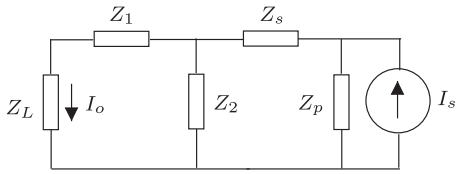

Fig. 21. CSR with AC input line filter and the EMI filter.

shows the equivalent circuit of the input line filter along with the CSR and the LISN, where $Z_p = \frac{1}{j\omega C}$ ($C = 34.64$ μF), $Z_s = R_d \| j\omega L$ ($R_d = 50\,\Omega, L = 2.4$ mH). The current through the LISN, I_o' is given in (25). Fig. 21 shows the EMI filter to be designed (Z_1, Z_2). The current through the LISN with this filter is given in (26). At 150 kHz, $Z_s \approx 50\,\Omega$ and $Z_p \approx -j0.03\,\Omega$. This implies $|Z_s| \gg |Z_p|$ and $Z_L \approx 2Z_s$. Intuitively Z_1 and Z_2 will form an LC filter with cutoff frequency much higher than 552 Hz (this is the corner frequency of LC filter designed in Section IV). The capacitive impedance of Z_2 will be small in comparison with Z_s (50 Ω) at 150 kHz, $|Z_s| \gg |Z_2|$. With these assumptions, the gain G in (27) can be simplified to (28).

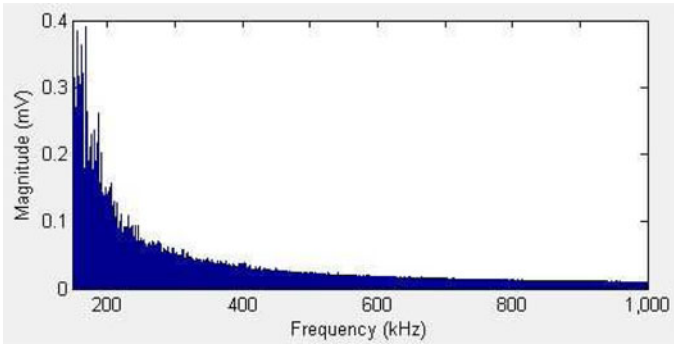

Fig. 22. Simulation results: Frequency spectrum of grid current with EMI filter using LISN.

Following the impedance mismatch criterion as described in [36] (for EMI filter design of a voltage source inverter) the gain G can be increased if we choose Z_1 and Z_2 such that $Z_2 < Z_L$ and $(Z_1 + Z_2) > Z_L$. Increasing Z_1 implies, increasing the drop in the fundamental component of the voltage across the filter. So here Z_2 is chosen to be small in comparison with Z_L. It is chosen to be a small capacitance of 350 nF such that at 150 kHz its impedance is $-j3\ \Omega$. Z_1 is chosen as an inductor of 35 μH and its impedance at 150 kHz is $j30\ \Omega$. This results in a gain of 11.1 at 150 kHz. The observed peak of the voltage with this EMI filter measured across the $100\ \Omega$ of the LISN is 0.4 mV or 52 dB·μV; see Fig. 22. Note that the corner frequency of this *LC* filter is at 45 kHz and is much higher than that of the ac input line filter (552 Hz). This explains why the EMI filter does not affect the input power factor and voltage drop across the filter for the fundamental frequency component

$$I_o' = \frac{Z_p}{Z_L + Z_s + Z_p} I_s \tag{25}$$

$$I_o = \frac{Z_2 Z_p}{(Z_L + Z_1 + Z_2)(2Z_p + Z_s + Z_2) - {Z_2}^2} I_s \tag{26}$$

$$G = \frac{I_o'}{I_o} = \frac{\left(1 + \frac{Z_1 + Z_2}{Z_L}\right)\left(1 + \frac{Z_2 + Z_s + Z_p}{Z_p}\right) - \frac{Z_2^2}{Z_p Z_L}}{\frac{Z_2}{Z_p Z_L}(Z_L + Z_s + Z_p)} \tag{27}$$

$$G \approx \frac{1}{3}\left(1 + \frac{Z_1 + Z_2}{Z_L}\right)\frac{Z_L}{Z_2}. \tag{28}$$

B. Correction Factor for THD Specification

The design procedure described in Section IV assumes all of the ripple component (anything other than the fundamental) of the input current is at the switching/equivalent carrier frequency (f_s). In reality most of the energy of the ripple part is concentrated at the switching frequency and at its next few multiples. So the above assumption leads to a slight over-design of the input filter. The following analysis provides a way to compensate for this. In the following analysis, we consider components of the input current spectrum at the multiples of the fundamental frequency (f_G). I_k denotes the amplitude of the kf_G component of the input current, where k is a positive integer. As seen

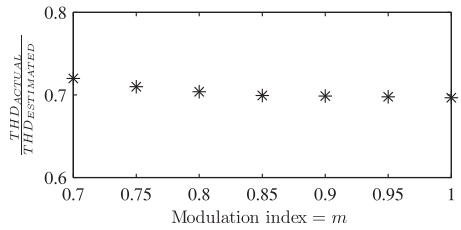

Fig. 23. Ratio between actual and estimated THD.

from Fig. 9, the designed filter has a 40 dB/decade roll off at and beyond the switching frequency (f_s) and f_c be the corner frequency of this filter. So for any $kf_G > f_s$, the kth component of the grid current will have an amplitude of $I_k(\frac{f_c}{kf_G})^2$. According to the assumption this component must be $I_k(\frac{f_c}{f_s})^2$. Assuming all the components of the input current waveform between the fundamental frequency and the switching frequency f_s (or $f_s - rf_G$, considering a part of the side band) are zero, (29) and (30) give the estimated and the actual THDs, where $N_o = [\frac{f_s}{f_G} - rf_G]$ and I_1 is the fundamental component of the grid current. In this computation, r is chosen to be 10. So, the ratio of actual to the estimated THD is given in (31). This ratio depends on the modulation index. For a proper utilization, the CSR will be designed at a higher modulation index. Fig. 23 shows this ratio for higher values of modulation index. This plot is obtained from simulation. The intended THD in the grid current must be divided by this ratio before using it in the procedure described in Fig. 11. For example for the design in Section V this ratio from Fig. 23 at modulation index $m = 1$ is 0.7 and the observed ratio is 0.76. Note that this computation is approximate as it assumes components in the input current spectrum only at the multiples of the fundamental frequency and the corner frequency f_c is considerably smaller than f_s. For a practical design these approximations hold and Fig. 23 can be used as a starting point for the actual design

$$\mathrm{THD}^2_{\mathrm{ESTIMATED}} = \frac{\sum_{k=N_o}^{\infty} I_k^2 \left(\frac{f_c}{f_s}\right)^4}{I_1^2} \tag{29}$$

$$\mathrm{THD}^2_{\mathrm{ACTUAL}} = \frac{\sum_{k=N_o}^{\infty} I_k^2 \left(\frac{f_c}{kf_G}\right)^4}{I_1^2} \tag{30}$$

$$\phi(m) = \frac{\mathrm{THD}_{\mathrm{ACTUAL}}}{\mathrm{THD}_{\mathrm{ESTIMATED}}} = \left(\frac{\sum_{k=N_o}^{\infty} I_k^2 \frac{1}{k^4}}{\sum_{k=N_o}^{\infty} I_k^2}\right)^{1/2} \left(\frac{f_s}{f_G}\right)^2 \tag{31}$$

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