A High-Frequency Link Single-Stage PWM Inverter With Common-Mode Voltage Suppression and Source-Based Commutation of Leakage Energy

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***Abstract*—This paper presents a single-stage bidirectional high-frequency transformer (HFT) link dc/ac converter topology for a three-phase adjustable magnitude and frequency PWM ac drive. This type of converters find a wide range of applications including UPS systems, drives involving renewable energy sources (Solar, Fuel cell), and energy storage systems (typically low voltage dc to high voltage PWM ac). The HFT results in reduction in cost and weight along with a considerable increase in power density. The adverse effects of common-mode voltage are well known in this kind of applications. The proposed topology along with a modulation technique reduces common-mode voltage to practically zero and generates high-quality output voltage waveform comparable to conventional space vector PWM (CSVPWM). A source-based commutation method, presented in this paper, to commute the energy stored in the leakage inductance of the HFT resulting in the following advantages 1) no need for any auxiliary circuits with passive components; 2) almost complete recovery of the leakage energy; 3) soft switching of the output side converter for all load conditions; and 4) minimization of common-mode voltage switching due to commutation. The converter along with the suggested control has been analyzed in detail. The presented simulation and experimental results confirm the operation of the proposed converter.**

***Index Terms*—Common-mode voltage, high-frequency transformer, leakage commutation, PWM inverter.**

NOMENCLATURE

V_{dc}	Input dc voltage.
N_1, N_2	HFT number of turns.
T_s	Sampling period.
L_m	Magnetizing inductance.
L_A, L_{a_1}, L_{a_2}	Leakage inductances (phase a).
i_A, i_{a_1}, i_{a_2}	HFT winding currents (phase a).
i_o	Output load current (i_a for phase a).
I_o	Peak of i_o.
$\overline{v_{an}}$	Average output voltage of phase a.
V_o, ω_o	Peak and the frequency of $\overline{v_{an}}$.
$\mathbf{V_{ref}}$	Reference output voltage space vector.
v_{cm}	Common-mode voltage.
m	Modulation index.
d_1, d_2	Duty ratio of the vectors $\mathbf{V_1}$ and $\mathbf{V_2}$.
α	Angular position of $\mathbf{V_{ref}}$ with respect to $\mathbf{V_1}$.
i_m	Magnetizing current.
t_{com}	Maximum commutation time.
v_{pcom}	Primary winding voltage during commutation.
i_p	Primary winding current.

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I. INTRODUCTION

TRANSFORMERS are typically used to connect systems at different voltage levels and to provide galvanic isolation often necessary for safety. The replacement of a line frequency transformer with a high-frequency transformer leads to a large reduction in weight and cost. Due to high power density, high-frequency link inverters may find a wide range of applications including uninterruptible power sources (UPS), distributed power generation from renewable energy sources like solar and wind (connecting HVdc grid to offshore wind generators [1]), energy storage systems (battery interfaced grid tied inverters), vehicle to grid applications, fuel cell powered electric motor drives, and also in space and naval applications where a compact solution is necessary.

A conventional system involves a three-stage power conversion (dc-high frequency ac–dc-adjustable frequency ac) and requires intermediate passive elements leading to reduced reliability, efficiency, and power density [2]–[4]. High-frequency link resonant inverters use additional reactive components and usually experience higher switching stress and total harmonic distortion, [5]. Buck converter derived high-frequency inverters, [6], [7], are more attractive in comparison with Fly-back or Cuk converter derived topologies, [8], due to inherent filtering capability of most of the three-phase loads (motor drives), leading to a more compact all silicon solution (no passive components among the power stages).

Single-phase high-frequency link inverters have widely been discussed in the literature [9]–[18]. Single-stage three-phase high-frequency link inverters so far discussed in the literature can be broadly classified into two types. In both of these topologies, an H-bridge is used to generate high-frequency ac from the dc source and apply the same to the primary of a single-phase high-frequency transformer (HFT). In the rectifier type of this topology (RHFT) another H-bridge is used on the secondary side of the HFT to convert the high-frequency ac to dc (no capacitor is used) and finally a two-level voltage source inverter (VSI) is employed to connect to the three-phase ac load, [19]–[22]; see Fig. 1. A single phase version of this topology can be

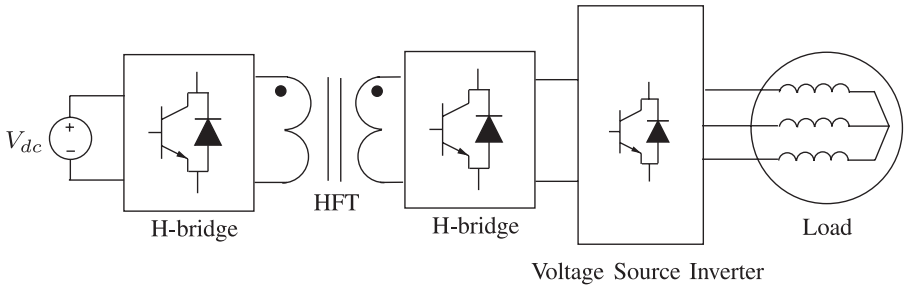


Fig. 1. RHFT topology.

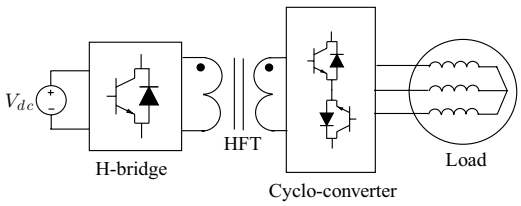


Fig. 2. CHFT topology.

found in [23] and [24]. In this topology, additional snubber circuits involving passive components are required for the proper commutation of leakage energy. In [25], a new topology has been proposed, where the secondary side H-bridge rectifier is replaced with a three-phase diode bridge, and the primary side converter is modified to incorporate a bank of three HFTs. In this topology, along with a novel hybrid modulation strategy, proper commutation of leakage energy has been achieved without any additional circuits and partial soft switching is obtained in the input side converter for an essentially unidirectional active power flow. The soft-switching range is extended in [26].

In the other type, a single-phase to three-phase cyclo-converter (CHFT) is used to directly connect the secondary of the HFT to load, Fig. 2. The cyclo-converter first rectifies the high-frequency ac and then generates three-phase PWM ac similar to a two-level inverter [27]–[29], [30]. For both of these topologies, it is known that it is possible to switch the primary-side H bridge at zero current by applying a zero state in the output side converter. Modulation strategies have been proposed for the partial or complete soft switching of the secondary-side converter, and auxiliary circuits are used for the commutation of leakage energy [31], [32]. In [33], a source-based commutation of the leakage energy has been proposed that obviates the need of additional circuits. This idea has been extensively applied to the single-phase high-frequency link inverters.

The adverse effects (shaft voltage build up, bearing currents, and EMI issues) of switching the common-mode voltage in a two-level inverter have been extensively studied in the context of PWM ac drives [34]–[38]. One solution to this problem is the use of active or passive common-mode filter [39]–[41]. It is well known that modulation-based schemes for common-mode voltage elimination that do not require extra filter circuits usually results in the reduction in the quality and the range of the output voltage [42]. Dual-inverter-based topologies with a single dc link for an open-end winding machine (with usual and parallel phase windings) are presented in [43] and [44] for the common-mode voltage elimination. The problem of ground leakage current in PV and battery connected inverters is well known [45]–[47]. Some applications even require grounding of the PV panel or negative rail of the battery. Isolation may reduce the effect but does not eliminate it [48].

This paper presents a single-stage high-frequency link inverter topology with a modulation strategy that leads to the suppression of the common-mode voltage; see Fig. 3. The three wire nature of the ac side connection also avoids the flow of the additional circulating currents [49]. Power flow is completely bidirectional. A source-based commutation technique similar to [33] has been outlined that results in the complete recovery of leakage energy without any additional circuits along with minimization of common-mode voltage switching due to commutation. The secondary-side converter is soft switched. This feature is particularly desirable in a high-voltage ac application due to the slow switching speed of high-voltage switches. It has been shown in this paper that additional switching transitions of the input side converter required for leakage inductance commutation can be made loss less. The proposed modulation strategy results in high-quality PWM voltage generation similar to conventional space vector modulation (CSVPWM), [50]. The proposed topology is particularly applicable to high-quality motor drives with a low dc bus voltage.

This paper is organized as follows. Section II is further divided into two major sections 1) Modulation for output voltage generation with practically zero common-mode voltage. 2) Source-based leakage commutation. Section III first outlines various aspects of design and implementation followed by the presentation of key simulation and experimental results.

II. Control

The control of the proposed converter is divided into two parts: modulation or the power transfer and commutation of leakage energy. The various control signals are shown in Fig. 4. Modulation of this topology has two stages and controlled by the signal S. In the first half of modulation when the signal S goes high, the power is transferred through the upper half of the secondary windings of the three HFTs, Fig. 3. During the next half when signal S goes low, power is transferred through the lower half of the secondary windings. Commutation happens when power flow changes from one stage to the consecutive one. During commutation the signal C goes high.

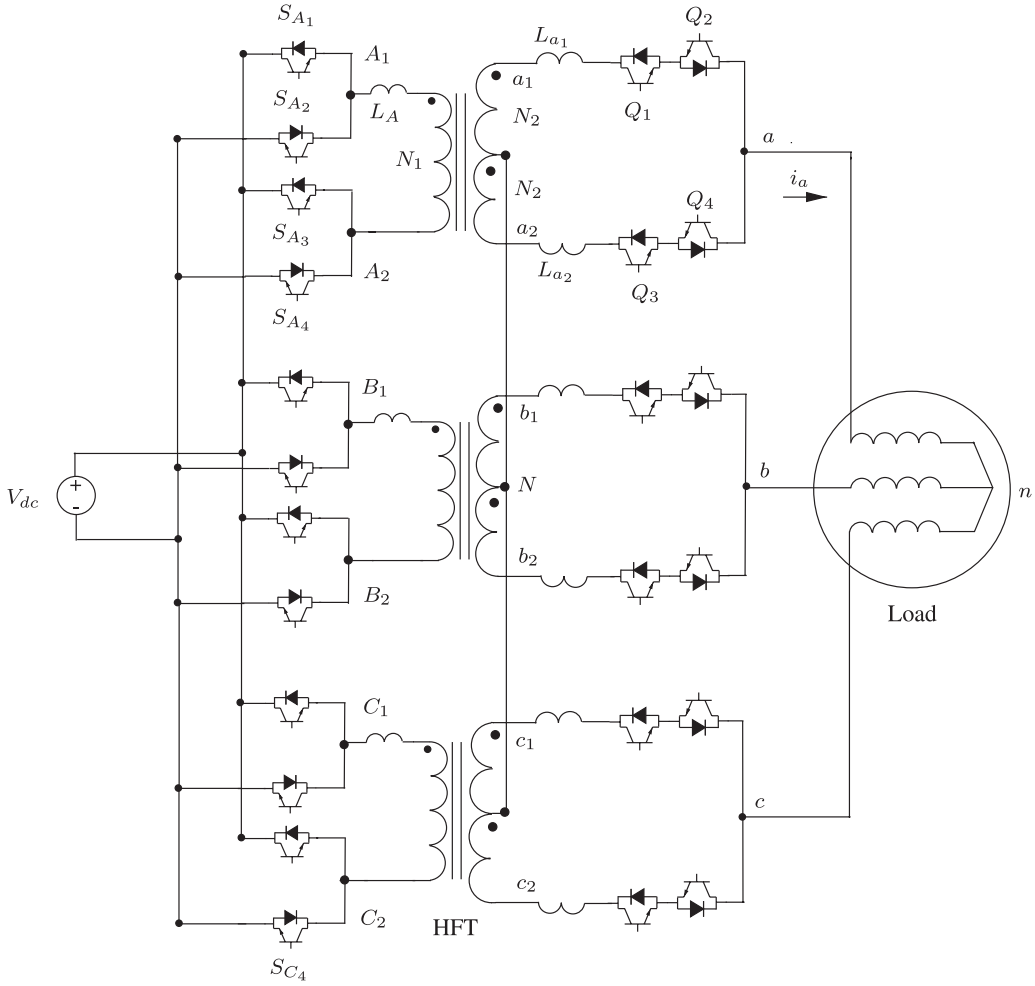


Fig. 3. Circuit diagram of the proposed topology.

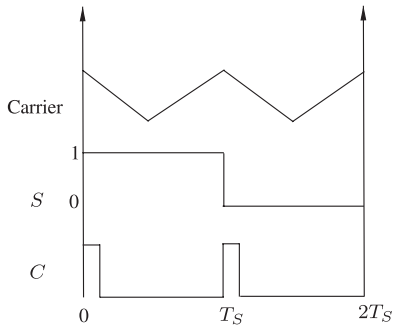


Fig. 4. Control signals.

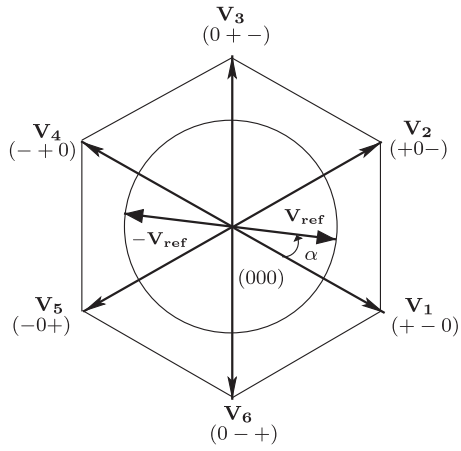


Fig. 5. Available voltage space vectors with zero common-mode voltage.

A. Modulation

During each stage of modulation the required (adjustable frequency and magnitude) three-phase output voltages are synthesized on an average at the load terminals. The three-phase balanced voltages are given in (1). V_o is the magnitude and ω_o is the angular frequency of the average output voltage to be synthesized at the load end. The definition of the output voltage space vector $\mathbf{V_o}$ is given in (2). In (3), $\mathbf{V_{ref}}$ is the reference or the average output voltage space vector. Using (1) $\mathbf{V_{ref}}$ turns out to be a constant magnitude ($\frac{3}{2}V_o$) synchronously rotating voltage space vector rotating with an angular frequency of ω_o. The tip of this vector traces a circle as shown in Fig. 5. The voltage space vector for the voltages induced in the upper half of the secondary windings is defined in (4). These voltages are measured with respect to the star point N formed by the mid

points of the secondary windings. Similarly, (5) provides the definition of the voltage space vector formed by the voltages induced in the lower half of the secondary windings. In (6), $\mathbf{V_p}$ refers to the voltage space vector formed by the primary-side voltages of the three HFTs. During modulation or power transfer stage, we can neglect the voltage drop in the leakage impedances of the transformer. This implies (7) holds. Using (4), (5), (6), and (7) it is possible to obtain (8)

$$\begin{aligned}\overline{v_{an}} &= V_o \cos(\omega_o t)\\ \overline{v_{bn}} &= V_o \cos\left(\omega_o t - \frac{2\pi}{3}\right)\\ \overline{v_{cn}} &= V_o \cos\left(\omega_o t + \frac{2\pi}{3}\right) \end{aligned} \tag{1}$$

$$\mathbf{V_o} = v_{an} + v_{bn}e^{j\frac{2\pi}{3}} + v_{cn}e^{-j\frac{2\pi}{3}} \tag{2}$$

$$\begin{aligned}\mathbf{V_{ref}} &= \overline{v_{an}} + \overline{v_{bn}}e^{j\frac{2\pi}{3}} + \overline{v_{cn}}e^{-j\frac{2\pi}{3}}\\ &= \frac{3}{2}V_o e^{j\omega_o t}\end{aligned} \tag{3}$$

$$\mathbf{V_{s_1}} = v_{a_1N} + v_{b_1N}e^{j\frac{2\pi}{3}} + v_{c_1N}e^{-j\frac{2\pi}{3}} \tag{4}$$

$$\mathbf{V_{s_2}} = v_{a_2N} + v_{b_2N}e^{j\frac{2\pi}{3}} + v_{c_2N}e^{-j\frac{2\pi}{3}} \tag{5}$$

$$\mathbf{V_p} = v_{A_1A_2} + v_{B_1B_2}e^{j\frac{2\pi}{3}} + v_{C_1C_2}e^{-j\frac{2\pi}{3}} \tag{6}$$

$$\begin{aligned}v_{a_1N} &= -v_{a_2N} = \left(\frac{N_2}{N_1}\right)v_{A_1A_2}\\ v_{b_1N} &= -v_{b_2N} = \left(\frac{N_2}{N_1}\right)v_{B_1B_2}\\ v_{c_1N} &= -v_{c_2N} = \left(\frac{N_2}{N_1}\right)v_{C_1C_2}\end{aligned} \tag{7}$$

$$\mathbf{V_{s_1}} = -\mathbf{V_{s_2}} = \left(\frac{N_2}{N_1}\right)\mathbf{V_p} \tag{8}$$

$$v_{cm} = \frac{v_{aN} + v_{bN} + v_{cN}}{3}. \tag{9}$$

In the first half of the modulation, only the upper half of the secondary windings conduct. For example, during this stage as shown in Fig. 3 for phase a the switches Q_1 and Q_2 are ON and Q_3 and Q_4 are OFF. As $v_{an} - v_{aN} = v_{Nn}$ holds for all three phases, $\mathbf{V_o}$ is equal to $(\frac{N_2}{N_1})\mathbf{V_p}$. Note that in each phase the primary winding of the transformer is connected to the dc-bus through an H-bridge. For example, in phase a this bridge consists of four two-quadrant switches S_{A_1} to S_{A_4}. In each leg, the switches are controlled in a complementary fashion in order to avoid the short circuit of the input voltage source. For example at any instant of time either of the switches S_{A_1} or S_{A_2} is ON but they are never turned ON simultaneously. Considering this switching strategy each H bridge has four switching states. Two of them are active. During these states the possible applied primary voltages (v_p) are $+V_{dc}$ or $-V_{dc}$. The rest of the two are zero states, i.e. the primary winding is short circuited. These states are given in Table I. In this analysis, the positive active state of a bridge is denoted by $+$, negative state is by $-$, and zero state is by 0. As each bridge has three different available

TABLE I
SWITCHING STATES

State	0	+	−	0
S_1	ON	ON	OFF	OFF
S_3	ON	OFF	ON	OFF
v_p	0	V_{dc}	$-V_{dc}$	0

voltage levels, all the three bridges can apply 27 possible voltage combinations to the three primary windings of the HFT. Out of these possibilities here only six active states are considered that leads to the zero common mode voltage at the load terminals. The common-mode voltage is defined in (9). Please see Appendix A for a brief explanation of (9). For example, when the a phase bridge applies a positive voltage, the b phase applies a negative voltage, and the c phase applies zero voltage, the sum of the three voltages is zero. In this discussion, this particular switching state is referred to as $(+-0)$. These six active states produce six active voltage vectors at the primary terminals. These vectors, scaled with the turns ratio $(\frac{N_2}{N_1})$, are given in Fig. 5. The state $(+-0)$ generates voltage vector $\mathbf{V_1}$. As in this state $V_{A_1A_2} = V_{dc}$, $V_{B_1B_2} = -V_{dc}$ and $V_{C_1C_2} = 0$, by (6) $\mathbf{V_p} = V_{dc}\sqrt{3}e^{-j\frac{\pi}{6}}$ and $\mathbf{V_1} = \mathbf{V_p}(\frac{N_2}{N_1}) = \mathbf{V_o}$ (When S is high). Similarly, it is possible to obtain other five active voltage vectors as shown in Fig. 5.

In the first half of the power transfer the output reference voltage vector $\mathbf{V_{ref}}$ is synthesized by applying these six active voltage vectors and the zero vectors. This situation is similar to a two-level VSI. The six active space vectors divide the complex plane into six symmetrical sectors. The output voltage vector is generated by using the two active vectors that form the sector in which the output reference voltage vector is located at that particular instant of time. For example in Fig. 5, the reference voltage vector is synthesized on an average using vectors $\mathbf{V_1}$ and $\mathbf{V_2}$, (10). The duty ratios (d_1 and d_2) or the fraction of time for which these active vectors need to be applied are given in (11). Here m is the modulation index and is equal to $\frac{V_o}{V_{dc}(\frac{N_2}{N_1})}$.

During the second half of the modulation, the signal S goes low. During this period power is transferred through the lower half of the secondary windings of all three HFTs, see Fig. 3. As switches Q_3, Q_4 are ON and Q_1, Q_2 are OFF the output voltage space vector $\mathbf{V_o}$ is equal to $\mathbf{V_{s_2}}$. Due to (8), $\mathbf{V_o}$ is equal to $-(\frac{N_2}{N_1})\mathbf{V_p}$. Note that the voltage vectors shown in Fig .5 are the possible voltage vectors generated by the input converter across the primary winding scaled by $(\frac{N_2}{N_1})$. So in this stage the input converter is modulated to generate average of $(\frac{N_2}{N_1})\mathbf{V_p}$ to be equal to $-\mathbf{V_{ref}}$, see Fig. 5. As the three HFTs are identical the magnetizing inductances forms a balanced three-phase load at the primary side. Over one full cycle of the S signal, the net average voltage vector applied to the magnetizing inductances is zero. This results in flux balance in the cores of the three HFTs.

The sequence in which voltage vectors are applied in one sampling cycle are according to CSVPWM. Fig. 6 shows the sequence of applied voltage space vectors over one full cycle of signal S when the reference voltage vector is placed as in Fig. 5

$$\mathbf{V_{ref}} = d_1\mathbf{V_1} + d_2\mathbf{V_2} \tag{10}$$

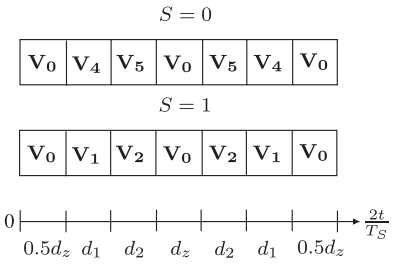


Fig. 6. Sequence of the applied voltage vectors.

TABLE II
SWITCHING STATES AND PRIMARY VOLTAGE DURING COMMUTATION FOR POSITIVE LOAD CURRENT

	Q_1	Q_2	Q_3	Q_4	D_1	D_2	D_3	D_4	V_p
1	1	X	0	0	0	1	0	0	X
1→0	1	0	1	0	0	1	0	1	$-V_{dc}$
0	0	0	1	X	0	0	0	1	X
0→1	1	0	1	0	0	1	0	1	V_{dc}

TABLE III
SWITCHING STATES AND PRIMARY VOLTAGE DURING COMMUTATION FOR NEGATIVE LOAD CURRENT

	Q_1	Q_2	Q_3	Q_4	D_1	D_2	D_3	D_4	V_p
1	X	1	0	0	1	0	0	0	X
1→0	0	1	0	1	1	0	1	0	V_{dc}
1	0	0	X	1	0	0	1	0	X
1→0	0	1	0	1	1	0	1	0	$-V_{dc}$

$$d_1 = m \sin\left(\frac{\pi}{3} - \alpha\right)$$
$$d_2 = m \sin\alpha. \tag{11}$$

This completes our discussion on adjustable magnitude and frequency PWM output voltage generation with zero common-mode voltage.

B. Commutation

The windings of the transformer have leakage inductance. Due to the inductive nature of the three-phase load each time the secondary converter makes a switching transition, currents through the leakage inductor must be changed by the application of suitable voltage. This process, referred as commutation, is described in detail in this section.

Commutation happens at each transition of the signal S-low to high or high to low. Commutation refers to the following processes: 1) change in the direction of the current in the primary leakage inductance (L_A) and 2) the exchange of the output current between the leakage inductances (L_{a_1} and L_{a_2}) of the two halves of the secondary winding, see Fig. 3. Commutation is done on a per phase basis by applying a voltage in the proper direction ($+V_{dc}$ or $-V_{dc}$) across the primary winding and controlling the individual IGBTs ($Q_{1,2,3,4}$) in the secondary-side converter. Depending on the sign of the output current and two possible transitions of signal S, four cases are possible. The switching scheme for $Q_{1,2,3,4}$ and the required primary voltage is given in Tables II and III for all of these four cases. In these tables for a switch, i.e., Q_1, 1 implies its ON, and 0 means it is

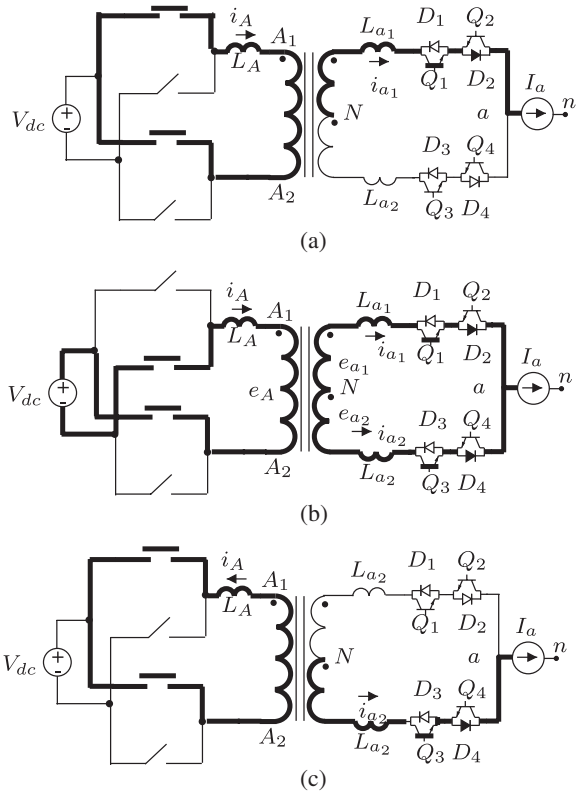
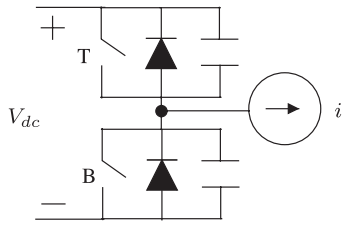


Fig. 7. Commutation.

OFF. For a diode, i.e., D_1, 1 implies it is conducting and 0 means otherwise. The first column in these tables refer to the state of the S signal as in Fig. 4. For example, 1→0 means a transition from 1 to 0 or high to low. V_p denotes that the voltage needs to be applied across the transformer primary during commutation. X denotes not relevant.

Here, the case when output current is positive and S is making a transition from high to low is described in detail. This implies initially power was flowing through the upper half of the primary winding. Fig. 7(a) depicts the circuit just before C goes high. Note that usually before commutation, zero voltage vector is applied. Let us assume in this case S_{A_1} and S_{A_3} are ON. The commutation process goes through four distinct steps. As a first step the nonconducting IGBT Q_2, out of the bidirectional switch pair $Q_{1,2}$, that is going out of operation, is switched OFF. At the same time, the input converter is switched to apply a negative voltage across the transformer primary according to Table II. After waiting for the primary to switch, Q_3 is turned ON. Note that Q_3 will be conducting among the switch pair $Q_{3,4}$ in the upcoming state. The commutation stage is shown in Fig. 7(b). The application of a negative primary voltage and turning ON of Q_3 (at zero current) forward biases diode D_4. In this analysis, magnetizing currents are neglected. According to transformer relationships, (12) and (13) are true. I_a is the value of i_a during the commutation period. Here, it is assumed that i_a appears to be a dc current source in this analysis. This is because commutation happens in a period of time that is much smaller than the time period of the output current. By KCL at point a, we get (14). The application of KVL on primary and secondary windings



(a)

Transition	$i > 0$	$i < 0$
T → B	S	H
B → T	H	S

(b)

Fig. 8. Switching in a leg, S: Soft transition. H: Hard transition.

leads to (15) and (16), respectively. Solving these equations we get (17). When i_{a_2} reaches I_a, i_{a_1} and i_A becomes zero and $-I_a$, respectively, and the commutation process comes to a natural end. The commutation time is maximum when the output current is at its peak (I_o). So we wait in this state for t_{com} period of time, (18). As the last two steps, Q_1 is switched OFF (with zero current) and then with a delay Q_4 is turned ON (with zero voltage). Fig. 7(c) depicts the circuit configuration after the commutation process is completed

$$\frac{e_A}{N_1} = \frac{e_{a_1}}{N_2} = \frac{e_{a_2}}{N_2} \tag{12}$$

$$i_A N_1 - i_{a_1} N_2 + i_{a_2} N_2 = 0 \tag{13}$$

$$I_a = i_{a_1} + i_{a_2} \tag{14}$$

$$V_{\rm dc} = L_A \frac{d}{dt} i_A + e_A \tag{15}$$

$$e_{a_1} + e_{a_2} = L_{a_1} \frac{d}{dt} i_{a_1} - L_{a_2} \frac{d}{dt} i_{a_2} \tag{16}$$

$$\frac{d}{dt} i_{a_2} = \frac{V_{\rm dc} \left(\frac{N_2}{N_1}\right)}{\left(\frac{L_{a_1} + L_{a_2}}{2}\right) + 2L_A \left(\frac{N_2}{N_1}\right)^2} \tag{17}$$

$$t_{com} = \left[\frac{\left(\frac{L_{a_1} + L_{a_2}}{2}\right) + 2L_A \left(\frac{N_2}{N_1}\right)^2}{V_{dc} \left(\frac{N_2}{N_1}\right)} \right] I_o. \tag{18}$$

Note that even though the output converter is soft switched, it requires additional switching of the primary-side converter for the commutation of leakage energy. It turns out that if the output capacitance of the switches in the input side converter is considered (this will be the case if MOSFETs are used) the additional switching due to leakage commutation is loss less. Fig. 8(a) depicts a leg of the primary-side converter. T stands for top and B is for bottom switch, for example T and B may refer to S_{A_1} and S_{A_2}, respectively. The switch can be a MOSFET. A switching transition from top to bottom (T→B) for a positive leg current ($i > 0$) is soft switched (S), i.e., T turns OFF with ZVS and B turns ON with ZCS. The reverse transition (B→T) with a positive leg current is hard switched (H). The table in Fig. 8(b) summarizes all possible transitions, [51], [52]. A brief explanation of this mechanism is given in Appendix B.

Fig. 9 shows the voltage applied across the primary winding ($v_{\rm pcom}$) during commutation along with the primary current both for a positive and negative load currents (i_o). Out of eight

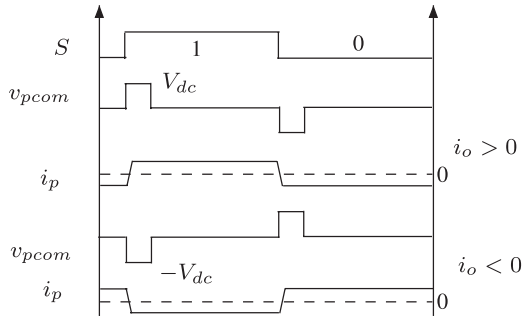


Fig. 9. Primary-side voltage and current during commutation.

possible transitions of $v_{\rm pcom}$ let us analyze the case that has been discussed for describing commutation, i.e., S is making a transition from 1 to 0 and with a positive load current. Prior to the commutation, a zero voltage is applied by the input bridge. Also, note that the primary current is positive. There are two possibilities, either the zero may have been applied by turning ON two top switches ($S_{A_{1,3}}$) or the two bottom switches ($S_{A_{2,4}}$). Now to apply a negative voltage (required for commutation) either the leg (S_{A_1}, S_{A_2}) has to switch from top to bottom (T→B) with a positive leg current or the other leg (S_{A_3}, S_{A_4}) has to go from bottom to top (B→T) with a negative leg current. According to table in Fig. 8(b) both of these will result in soft transition (S). Similarly, it is possible to check the other seven possibilities for soft switching.

III. Simulation and Experimental Results

The proposed topology as shown in Fig. 3 along with the control described in the previous section has been verified both in simulation (MATLAB/Simulink) and experiment. This section presents a detailed description of the hardware prototype along with key experimental and simulation results.

Even though simulation and experiments are performed with the same set of parameters listed in Table IV. The diodes are considered to be ideal in simulation (no reverse recovery and forward voltage drop).

A. Experimental Setup

Fig. 10 shows the schematic of the actual experimental setup. The input side converter uses six-phase legs (two series connected IGBTs) and output side converter has six bidirectional

TABLE IV
PARAMETERS

L_{load}	R_{load}	L_{A,a_1,a_2}	R_{A,a_1,a_2}	L_m	$\frac{N_2}{N_1}$	V_{dc}	$f_s = \frac{1}{T_s}$	$f_o = \frac{2\pi}{\omega_o}$	m
$30mH$	16Ω	$10\mu H$	0.1Ω	$180\ mH$	1	90V	5kHz	60Hz	0.8

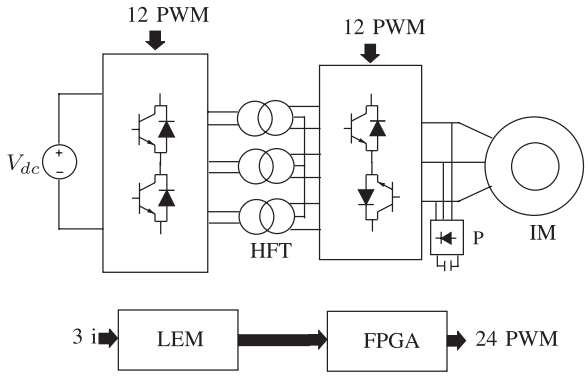


Fig. 10. Experimental setup.

switches (two common-emitter connected IGBTS). These are implemented using integrated power modules (IPM) from Microsemi (APTGT75A60T1G and APTGT75DU120TG, respectively). A gate resistance of 18 Ω is chosen to get a difference between approximate ON and OFF time of the IGBTs to be equal to 600 ns. The dead time for the input converter and the time for different states of the output converter during commutation is chosen based on this time. An FPGA-based control platform (Xilinx, XC3S500E) has been used to generate the PWM signals.

The turns ratio is chosen to be unity. The design of these transformers are done using area product method. The flux swing in each cycle of the S signal is not constant. The maximum flux swing occurs when the corresponding average output voltage is peaking. The average volt-seconds applied to the transformer primary in one half of the S signal is $V_o T_s$. This leads to the first design equation (19), where A_c is the core area, $B_{\rm pk}$ is the peak flux density, and N_1 is the number of turns of the primary winding. Assuming the rms of the output line current to be $I_{o_{\rm RMS}}$, the rms current through each of the secondary windings is $\frac{I_{o_{\rm RMS}}}{\sqrt{2}}$ and that of the primary current is $I_{o_{\rm RMS}}$. The effective window area is given by (20), where $A_w K_w$ is the effective window area and J is the current density. A FINEMET C core (F1AH0803, F3CC series) from Hitachi is used. The number of turns used is 115. A protection circuit P as shown in Fig. 10 used at the load end to protect against a sudden opening of the output side converter. A balanced Y connected R-L network and an induction machine (IM) is used as three-phase loads

$$A_c = \frac{V_o}{2N_1 f_s B_{\rm pk}} \tag{19}$$

$$A_w K_w = \frac{N}{J} I_{o_{\rm RMS}} (1 + \sqrt{2}) \tag{20}$$

B. Results

This section presents key simulation and experimental results together for a direct comparison. All the results are with the R-L load unless otherwise specified.

Fig. 11 shows output line current, primary winding, and upper-half of the secondary winding current along with the line to neutral voltage of phase a. The three phase load acts as a low-pass filter and eliminates the response due to switching frequency components. The simulated output current waveforms have approximately a peak of 3.6 A as predicted analytically. The experimental waveforms have a lower peak of 2.9 A. This can be attributed to the voltage drop across the semiconductor switches. The measured efficiency is 89 %. The three output line voltages (with respect to transformer neutral N) are plotted in Fig. 12 over one cycle of signal S. The common-mode voltage is obtained by directly summing these waveforms. The common-mode voltage switches only once in one sampling cycle ($f_s = 5$ kHz) due to leakage commutation and remains zero otherwise. The input voltage to the transformer primary along with the magnetizing current over one cycle of the signal S is given in Fig. 13. Magnetizing current is obtained by summing the three winding currents (note in the transformer all of the three windings have same number of turns). The experimental result for magnetizing current appears to be different from the simulation result due to the following reasons: 1) the vertical scale is different (0.05 A/div for simulation and 1 A/div for the experimental result). 2) Noise present in the experimental result is of similar order as of the original signal. Although the experimental result clearly indicates flux balance.

The next set of results correspond to leakage inductance commutation, see Fig. 14. The two secondary- and primary-winding currents are plotted with the primary voltage. The secondary current waveforms are complementary to each other and composed of 50% duty cycle modulated output load current. The primary current is the 50% duty cycle modulated chopped version of the load current. The magnified version of these waveforms clearly shows the application of suitable voltage by the input converter and linear change in winding currents at the end of each sampling cycle T_s due to commutation. The measured slope of the inductor currents during commutation matches with its analytical estimation. The currents in experimental results show a small overshoot at the end of leakage inductance commutation. This is due to the reverse recovery of the antiparallel diode that is turning OFF in the secondary-side converter. The output capacitance (collector-emitter) of the IGBTs used in the primary-side converter are too small to result in soft switching transitions of the input converter during commutation. Appendix B briefly explains why an appreciable amount of output capacitance is necessary to achieve zero voltage switching (ZVS).

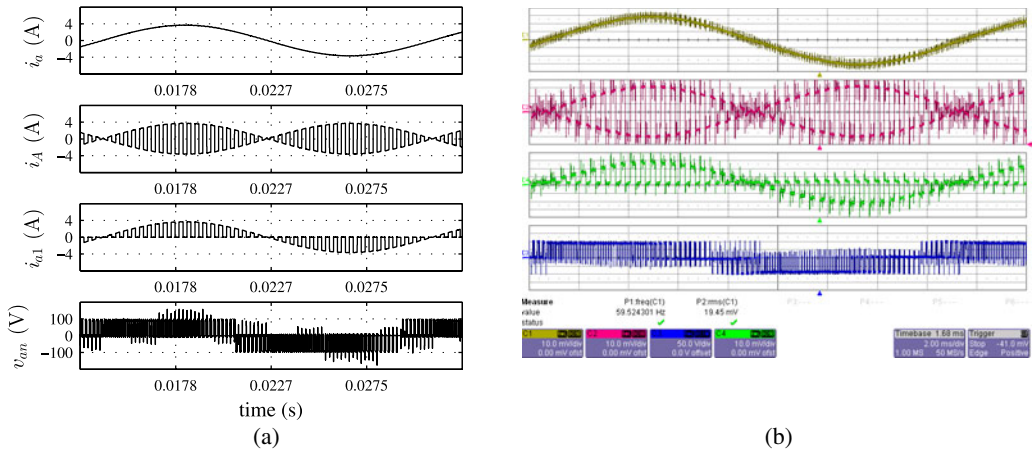


Fig. 11. Output line Current (CH1), primary current (CH2), upper-half of the secondary winding current (CH3) [1 A/div (b)], output line to neutral voltage (CH4) [50 V/div (b)] and time 2 ms/div. (a) Simulation. (b) Experimental.

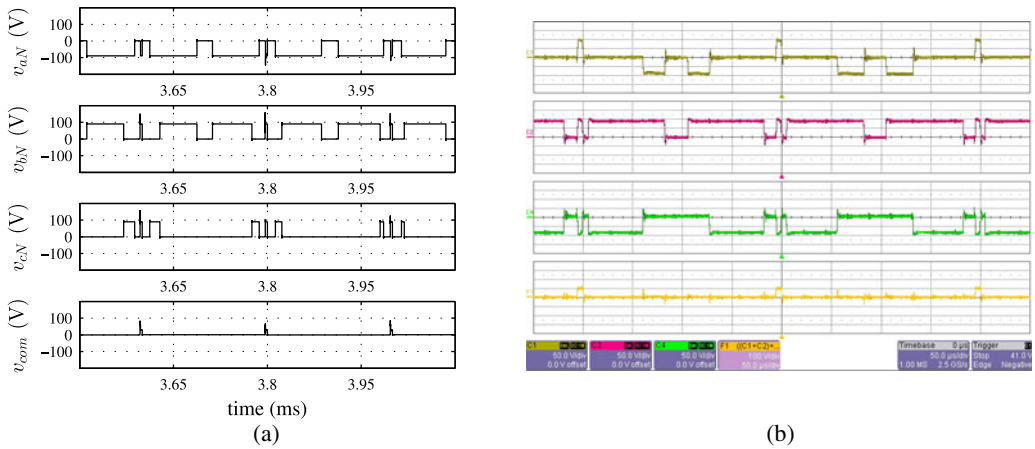


Fig. 12. Three output line voltages (CH1-3) [50 V/div (b)], common-mode voltage (CH4) [scaled 3X, 100 V/div (b)] and time 50 μs/div. (a) Simulation. (b) Experimental.

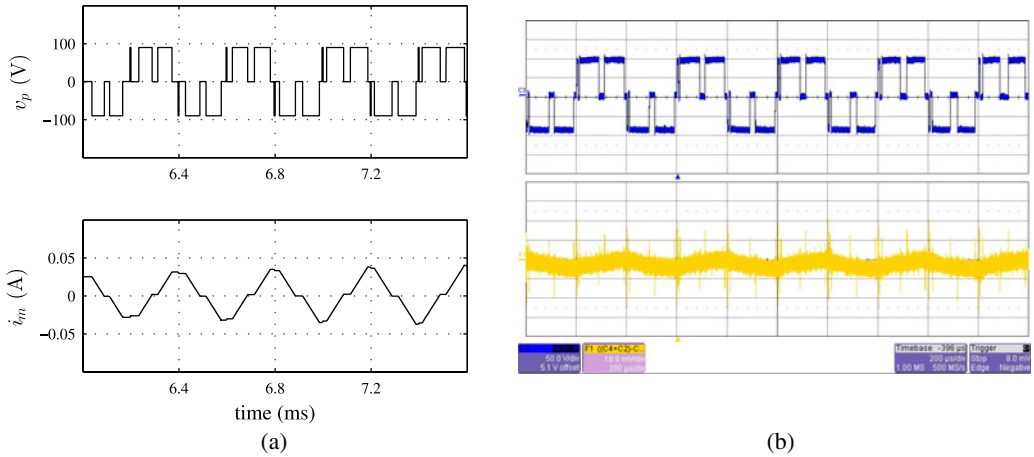


Fig. 13. Primary voltage (CH-1) [50 V/div (b)], magnetizing current (CH2) [1 A/div (b)], and time 200 μs/div. (a) Simulation. (b) Experimental.

The proposed HFT link inverter has been implemented as an open loop $\frac{V}{f}$ drive as shown in Fig. 15(a)(top). A four-pole induction machine with a dc generator load has been run with a reference frequency, f_{ref}, of 40 Hz and $\frac{V}{f} = 3$. Fig. 15(b) shows the three-phase motor line currents. The measured shaft speed is 1172 r/min (Synchronous speed is 1200 r/min and slip is 2.3%.). The proposed converter can be implemented as a closed-loop vector control drive to maintain a reference speed, ω_{ref}, as shown in Fig. 15(a)(bottom). Note in both of these cases the controller provides the reference voltage vector, $\mathbf{V_{ref}}$, to the

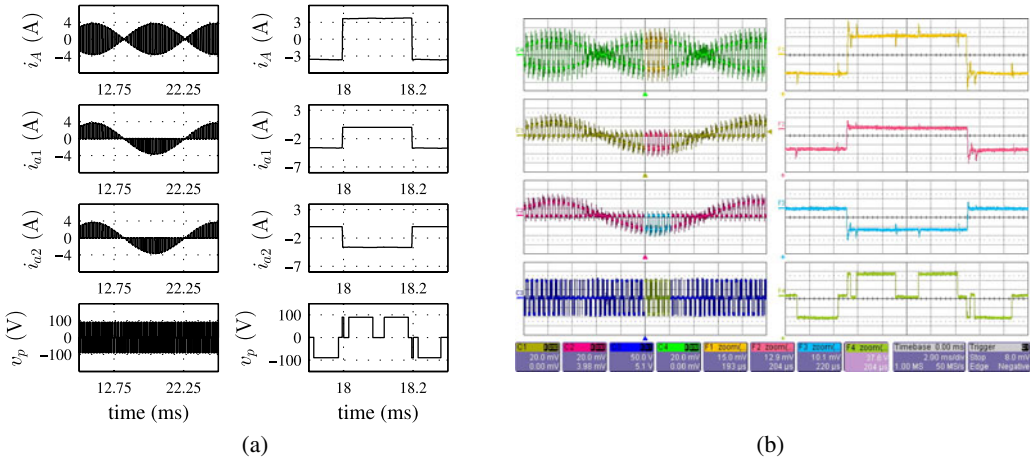


Fig. 14. Primary current (CH1), two secondary winding currents (CH2-3) [2 A/div (b)], primary voltage [50 V/div (b)], and time 40 μs/div in (b). (a) Simulation. (b) Experimental.

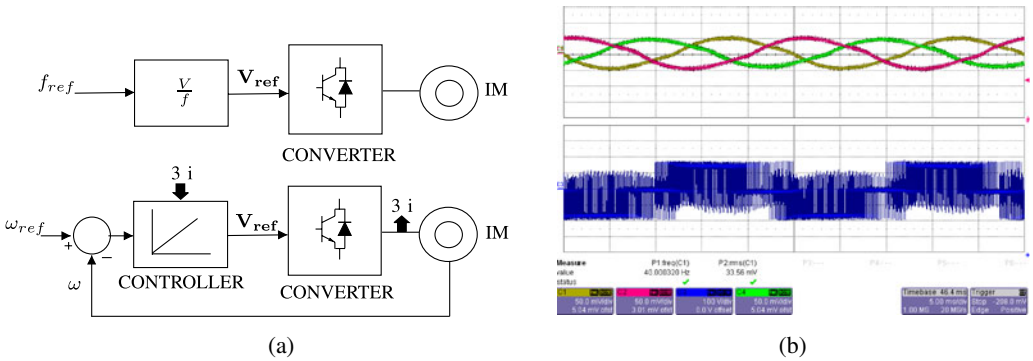


Fig. 15. (a) Implementation as a motor drive. (b) Motor line currents (CH1) (5 A/div), output line to neutral voltage (CH2)(100 V/div) and time 5 ms/div. (a) Control block diagram. (b) Results for $\frac{V}{f}$ control.

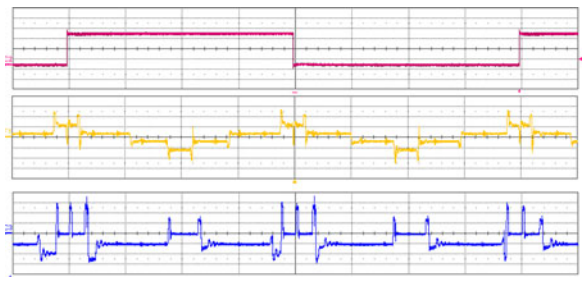


Fig. 16. CHFT Results: S signal (CH1), scaled (3 times) common-mode voltage (CH2)(200 V/div), line to neutral voltage (CH3) (50 V/div), time 50 μs/div

proposed converter in order to generate required PWM output voltage.

This topology is compared with CHFT topology of Fig. 2. The transformer has a turns ratio of 1:2. The input voltage and the modulation index are set in order to get the same amount of output voltage. The frequency of flux balance and the PWM of output voltage generation are kept same. A clamp circuit is used for leakage inductance commutation. The input converter is operated with 50% duty cycle, while the output converter is modulated with CSVPWM with 2 μs deadtime.

Fig. 16 shows the common-mode voltage (measured with respect to the mid-point of the secondary winding) and one of the output line to neutral voltage over one cycle of the S signal. A comparison of these plots with the first and fourth plots of Fig. 12 shows the advantage of the proposed method.

IV. Conclusion

In this paper, a converter topology along with a control technique for a high frequency ac-link dc/ac converter for a three-phase PWM drive has been proposed. The proposed topology has the following advantages: 1) single stage all silicon solution with bidirectional power flow; 2) galvanic isolation and voltage matching with high power density and low cost due to high-frequency transformers; 3) reduced common-mode voltage switching (zero during power transfer and switches only once in a sampling cycle during commutation); 4) high-quality output voltage profile comparable to CSVPWM; 5) almost the complete recovery of the leakage energy without using any auxiliary circuit; and 6) soft switching of the output side converter

(potentially high voltage and slow speed). The converter has been analyzed in detail. The presented experimental and simulation results verify the converter's operation and confirm the stated advantages. One of the short comings of this topology is that it has more number of switches particularly in the dc side. This is a promising solution for compact low-voltage, renewable energy source fed modern PWM ac drives.

APPENDIX

A. Common-Mode Voltage Analysis

Let us assume S is high and power is flowing through the upper half of the secondary windings of each of the HFTs in Fig. 3. Fig. 17 shows the equivalent circuit for common-mode analysis. The common-mode impedances of both the three-phase electrical machine load and the transformer are modeled as Z_n and Z_N, respectively, and connected to the ground G from their respective neutral points [35], [36]. Z is the sum of the internal impedance of the load and the leakage impedance of the transformer. e_a is the induced or internal voltage of the machine in phase a. It is possible to obtain (21) by applying KVL from point N to n along phase a. The common-mode voltage in (22) can be derived by summing (21) for all three phases and assuming balanced load ($e_a + e_b + e_c = 0$). Common-mode current or sum of the three phase line currents can be expressed as in (23) by considering the voltage drop across the common-mode impedances Z_N and Z_n. Combining (22) and (23) its possible to get (24). This paper aims at the minimization of i_{cm} by making v_{cm} effectively zero

$$v_{a_1N} = i_a Z + e_a + v_{nN} \tag{21}$$

$$v_{cm} = \frac{(v_{a_1N} + v_{b_1N} + v_{c_1N})}{3} = \frac{(i_a + i_b + i_c)}{3} Z + v_{nN} \tag{22}$$

$$i_{cm} = i_a + i_b + i_c = \frac{v_{nN}}{Z_N + Z_n} \tag{23}$$

$$i_{cm} = \frac{v_{\mathrm{cm}}}{Z_N + Z_n + \frac{Z}{3}} \tag{24}$$

B. Zero Voltage Switching

Consider a transition from top to bottom switch (T→B) with positive load current ($i > 0$). Before the transition, as the top switch T is conducting the voltage across the capacitor C_T is zero and the entire dc bus voltage appears across the bottom capacitor, see Fig. 18. When T switches OFF, the bottom diode cannot immediately come into conduction. Due to the presence of the bottom capacitor, the voltage v_{C_T} being at V_{dc} keeps the diode in the reverse biased condition during switching of T. T switches OFF at zero voltage (ZVS) and the load current is shared by the capacitances C_T and C_B. When the load current charges C_T to V_{dc} and discharges C_B to zero and the bottom diode starts conducting. A simple analysis shows the time this process takes is $\frac{2V_{dc}C}{i}$. Note that this time must be larger than the turn OFF time of *T*, in order to get ZVS. This implies we need to have appreciable amount of capacitance to achieve ZVS.

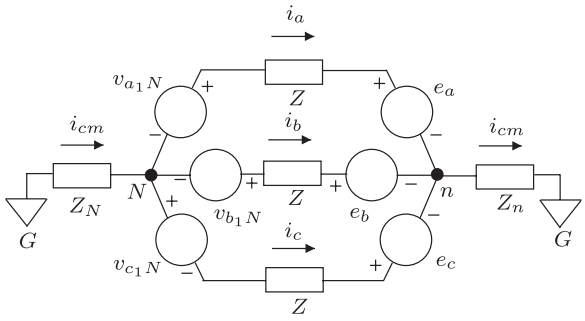


Fig. 17. Common-mode voltage analysis.

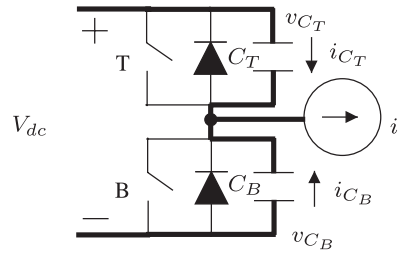


Fig. 18. ZVS switching in a leg.

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