A Single-Stage Power Electronic Transformer for a Three-Phase PWM AC/AC Drive With Source-Based Commutation of Leakage Energy and Common-Mode Voltage Suppression

Kaushik Basu, *Member, IEEE*, and Ned Mohan, *Fellow, IEEE*

***Abstract*—This paper presents a novel topology for the generation of adjustable frequency and magnitude pulsewidth-modulated (PWM) three-phase ac from a balanced three-phase ac source with a high-frequency ac link. The proposed single-stage power electronic transformer (PET) with bidirectional power flow capability may find application in compact isolated PWM ac drives. This topology along with the proposed control has the following advantages: 1) input power factor correction; 2) common-mode voltage suppression at the load end; 3) high-quality output voltage waveform (comparable with conventional space vector PWM); and 4) minimization of output voltage loss, common-mode voltage switching, and distortion of the load current waveform due to leakage inductance commutation. A source-based commutation of currents associated with energy in leakage inductance (termed as leakage energy) has been proposed. This results in soft-switching of the output-side converter and recovery of the leakage energy. The entire topology along with the proposed control scheme has been analyzed. The simulation and experimental results verify the analysis and advantages of the proposed PET.**

***Index Terms*—Common-mode voltage, high-frequency transformer (HFT), leakage commutation, matrix converter, power electronic transformer (PET), pulsewidth-modulated (PWM) drive, soft-switching, solid-state transformer (SST).**

I. Introduction

REPLACEMENT of a line frequency transformer with a high-frequency transformer (HFT) results in considerable reduction in size and cost. These power-electronics-assisted HFTs are known as power electronic transformers (PETs) or solid-state transformers (SSTs). Due to additional features such as on-demand reactive power support, voltage and frequency regulation, etc., PETs have been identified as an enabling technology for the modernization of the electric power distribution system [1], [2]. PETs can be also employed for high-power-density electrical machine drives, for example, in wind power generation [3], [4], traction drives [5], [6], and medium-voltage adjustable-speed drives [7].

Manuscript received May 3, 2013; revised August 19, 2013 and November 21, 2013; accepted January 20, 2014. Date of publication March 12, 2014; date of current version June 6, 2014. This work was supported by the Office of Naval Research under Grant N00014-07-1-0968.

K. Basu is with Dynapower Company, LLC, South Burlington, VT 05403 USA.

N. Mohan is with the University of Minnesota, Minneapolis, MN 55455 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TIE.2014.2311393

Detailed classification of different types of PETs can be found in [8]. A two-stage PET has either a high-voltage [9] or a low-voltage dc link [5], [6]. A three-stage PET usually involves a high-frequency-link dc/dc converter [10]–[13]. To match with the grid voltage, most of these topologies use input-series–output-parallel connection of modular units or use multilevel structures. Due to the multistage configuration, these topologies tend to be less efficient with a possible reduction in reliability and power density.

Single-phase single-stage ac/ac PETs are either based on full-bridge [14]–[16] or flyback converters [17]. Usually, these type of converters are fixed frequency and do not provide power factor correction [8], [18]. Single- [19] and three-phase [20] dual-active bridge-converter-based PETs suffer from the additional limitations of higher current stress and high sensitivity of the active power flow on the leakage inductance.

Three-phase single-stage PETs are based on matrix converters [21] and provide an all-silicon solution with grid power factor control and adjustable voltage and frequency pulsewidth-modulated (PWM) voltage generation. These types of PETs are classified in [22]. The first type of PETs are based on either push–pull [23] or full-bridge [24] converters. Low switch count and soft-switching of the grid-side converter are major advantages of this type of PETs [23]. The other type of PETs is based on the indirect modulation of matrix converters, [25], [26]. This type of PETs uses the least amount of copper and has fairly a small number of switches.

The windings of the HFT have leakage inductance. Each switching transition of the secondary-side converter requires commutation of leakage energy, resulting in output voltage loss, common-mode voltage switching, and reduction in switching frequency. Commutation of leakage energy by additional snubber circuits leads to power loss, reduction in reliability, and power density. Source-based commutation of leakage energy has been studied in the context of high-frequency-link dc/ac [27], single-phase ac/ac [28], and bidirectional rectifier [29]. Source-based commutation is not possible in the first type of PETs with a push–pull structure [30]. Partial commutation is possible in the full-bridge configuration [24]. Source-based commutation is possible in the other type of PETs, based on indirect modulation of the matrix converter, at the expense of the output voltage quality [26].

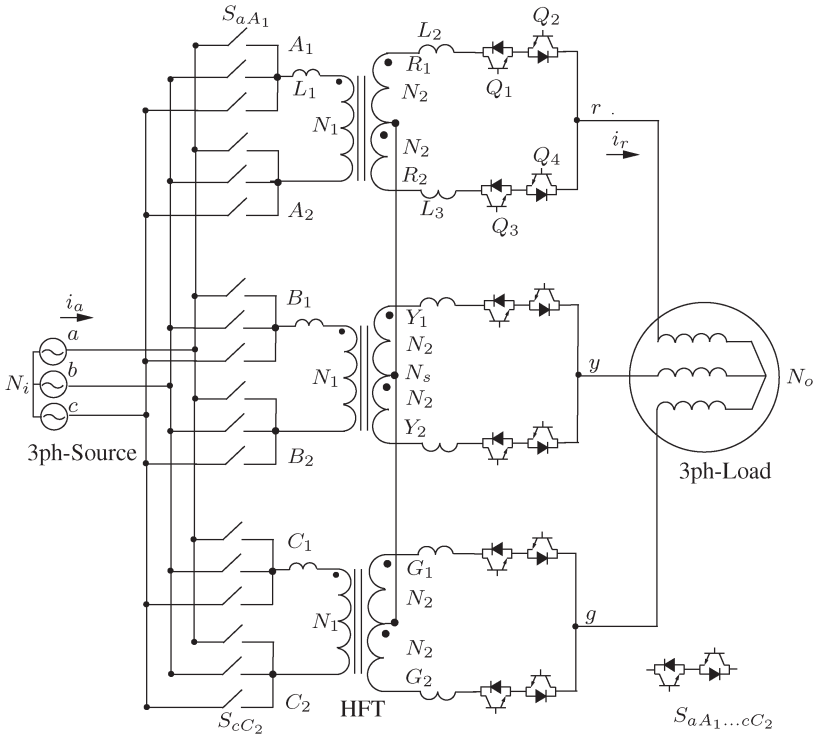

Fig. 1. Circuit diagram of the proposed topology.

The adverse effects (shaft voltage buildup, bearing currents, and electromagnetic interference issues) of pulsating common-mode voltage in a two-level inverter have been extensively studied in the context of PWM ac drives [31]. A dual-matrix converter-based topology for an open-end winding machine is presented in [32] for the elimination common-mode voltage. In none of the previous types of single-stage three-phase PETs, common-mode voltage elimination is possible if the commutation of leakage energy is considered.

In this paper, a novel topology (see Fig. 1) has been developed to minimize the frequency of the leakage commutation by moving the modulation to the primary-side converter. A novel modulation strategy has been proposed that leads to suppression of the common-mode voltage along with input power factor correction. The three-wire nature of the ac-side connection also avoids the flow of additional circulating currents as described in [33], in the context of open-end winding drives. Power flow is completely bidirectional. A source-based commutation technique similar to [27] has been outlined that results in recovery of leakage energy without any additional circuits along with the minimization of common-mode voltage switching due to commutation. The secondary-side converter is soft-switched for all load conditions. The proposed PWM strategy results in high-quality output voltage generation similar to conventional space vector PWM (CSVPWM), [34]. The proposed topology is particularly applicable to high-quality compact motor drives.

The content of this paper was first introduced in [35]. In this paper: 1) introduction is completely rewritten to include the current literature; 2) Section II-A on modulation contains extended analysis; 3) Section II-B on commutation is rewritten from the point of view of implementation through finite-state machines (FSMs); 4) a new section, i.e., Section III, has been added on experimental results; and 5) simulation is rerun with the same parameters as the experiment for a direct comparison.

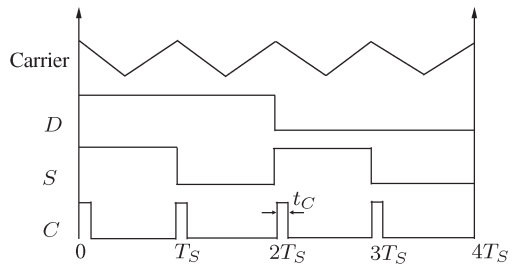

Fig. 2. Control signals.

II. Analysis

This section presents a detailed description of the proposed control and how it leads to several advantages. The operation of the proposed power electronic system is described using a set of signals shown in Fig. 2. T_s is the period over which the average output voltages are synthesized. Essentially, S is the signal over which flux balance is achieved. C is related to the commutation of the leakage inductance. Signal D is associated with input power factor correction. The role of these signals is explained in the following sections. The operation of this converter can be divided into two parts, namely, modulation and commutation.

A. Modulation

Modulation implies synthesis of adjustable frequency and magnitude high-quality PWM voltage at the load end. In this analysis, any variable in bold implies that it is a vector, and a

bar over a variable indicates an average over a sampling cycle T_s. Following is a list of symbols for different voltages and corresponding voltage space vectors. Note that any of these voltages is between a pair of points in Fig. 1. N_i and N_o are the star points of the input voltage source and output load, respectively. N_s is the common midpoints of the secondary windings of the HFTs (see Fig. 1).

$v_{aN_i}, v_{bN_i}, v_{cN_i}, \mathbf{V_i}$	Input voltages.
$v_{rN_o}, v_{yN_o}, v_{gN_o}, \mathbf{V_o}$	Output voltages.
$v_{A_1N_i}, v_{B_1N_i}, v_{C_1N_i}, \mathbf{V_{P_1}}$	Primary winding positive terminal voltage.
$v_{A_2N_i}, v_{B_2N_i}, v_{C_2N_i}, \mathbf{V_{P_2}}$	Primary winding negative terminal voltage.
$v_{A_1A_2}, v_{B_1B_2}, v_{C_1C_2}, \mathbf{V_P}$	Primary winding voltage.
$v_{R_1N_s}, v_{Y_1N_s}, v_{G_1N_s}, \mathbf{V_{S_1}}$	Upper half of the secondary winding voltage.
$v_{R_2N_s}, v_{Y_2N_s}, v_{G_2N_s}, \mathbf{V_{S_2}}$	Lower half of the secondary winding voltage.

When S is high (see Fig. 2), power is transferred through the upper half of the secondary winding of each of the HFTs (Q_1 and Q_2 are on; see Fig. 1). Power flows through the lower half of the secondary winding when S is low. Here, the modulation of the output voltages when S is high is explained in detail. Phase a of the three-phase balanced input voltages (v_{aN_i}, v_{bN_i}, v_{cN_i}) is given in (1). Similarly, Phase r of the three-phase balanced average output voltages ($\overline{v_{rN_o}}$, $\overline{v_{yN_o}}$, $\overline{v_{gN_o}}$) is given in (2). Equation (3) defines the instantaneous output voltage space vector. The reference average output voltage vector is given in (4). Using transformer relationship (5) and definitions (6)–(9), it is possible to get (10).

$$v_{aN_i} = V_i \cos\,\omega_i t \tag{1}$$

$$\overline{v_{rN_o}} = V_o \cos(\omega_o t + \phi) \tag{2}$$

$$\mathbf{V_o} = v_{rN_o} + v_{yN_o} e^{j\frac{2\pi}{3}} + v_{gN_o} e^{-j\frac{2\pi}{3}} \tag{3}$$

$$\mathbf{V_{ref}} = \overline{v_{rN_o}} + \overline{v_{yN_o}} e^{j\frac{2\pi}{3}} + \overline{v_{gN_o}} e^{-j\frac{2\pi}{3}} = \frac{3}{2} V_o e^{j(\omega_o t + \phi)} \tag{4}$$

$$v_{R_1N_s} = -v_{R_2N_s} = \frac{N_2}{N_1}(v_{A_1N_i} - v_{A_2N_i})$$

$$v_{Y_1N_s} = -v_{Y_2N_s} = \frac{N_2}{N_1}(v_{B_1N_i} - v_{B_2N_i})$$

$$v_{G_1N_s} = -v_{G_2N_s} = \frac{N_2}{N_1}(v_{C_1N_i} - v_{C_2N_i}) \tag{5}$$

$$\mathbf{V_{P_1}} = v_{A_1N_i} + v_{B_1N_i} e^{j\frac{2\pi}{3}} + v_{C_1N_i} e^{-j\frac{2\pi}{3}} \tag{6}$$

$$\mathbf{V_{P_2}} = v_{A_2N_i} + v_{B_2N_i} e^{j\frac{2\pi}{3}} + v_{C_2N_i} e^{-j\frac{2\pi}{3}} \tag{7}$$

$$\mathbf{V_{S_1}} = v_{R_1N_s} + v_{Y_1N_s} e^{j\frac{2\pi}{3}} + v_{G_1N_s} e^{-j\frac{2\pi}{3}} \tag{8}$$

$$\mathbf{V_{S_2}} = v_{R_2N_s} + v_{Y_2N_s} e^{j\frac{2\pi}{3}} + v_{G_2N_s} e^{-j\frac{2\pi}{3}} \tag{9}$$

$$\mathbf{V_P} = v_{A_1A_2} + v_{B_1B_2} e^{j\frac{2\pi}{3}} + v_{C_1C_2} e^{-j\frac{2\pi}{3}} = \mathbf{V_{P_1}} - \mathbf{V_{P_2}} = \frac{N_1}{N_2}\mathbf{V_{S_1}} = -\frac{N_1}{N_2}\mathbf{V_{S_2}}. \tag{10}$$

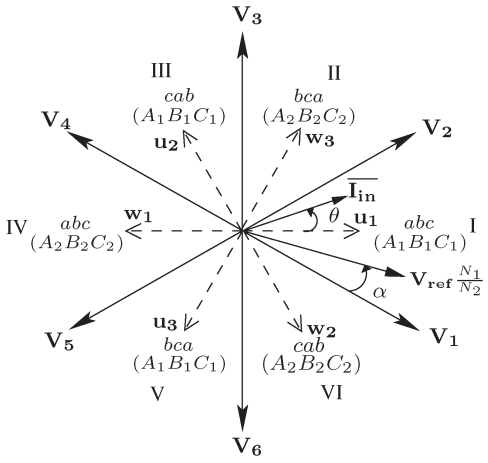

Fig. 3. Modulation with CCW vectors; I–VI are sectors.

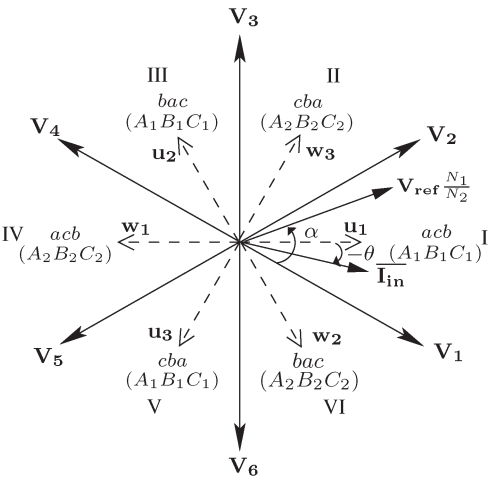

Fig. 4. Modulation with CW vectors; I–VI are sectors.

During power flow, the drop across the leakage impedance of the transformer can be neglected. Thus, when S is 1, the output voltage vector $\mathbf{V_o}$ is equal to the reflected primary voltage vector $(N_2/N_1)\mathbf{V_p}$, as shown in the following equation:

$$\mathbf{V_o} = \begin{cases} \mathbf{V}_{S_1} = +\frac{N_2}{N_1}\mathbf{V_P}, & S = 1 \\ \mathbf{V}_{S_2} = -\frac{N_2}{N_1}\mathbf{V_P}, & S = 0. \end{cases} \tag{11}$$

A set of switching combinations in the primary converter produces six ($\mathbf{V_1}$–$\mathbf{V_6}$) counterclockwise (CCW) synchronously rotating voltage space vectors across the transformer primary, as shown in Fig. 3. Another set of switching combinations produces six clockwise (CW) rotating vectors (see Fig. 4). CCW vectors are used when D goes high in Fig. 2; otherwise, CW vectors are used. $\mathbf{u_1}$, as shown in Fig. 3, corresponds to the connection (abc—$A_1B_1C_1$). This implies that terminals A_1, B_1, and C_1 are connected to phases a, b, and c, respectively, and that switches S_{aA_1}, S_{bB_1}, and S_{cC_1} are on. Thus, $\mathbf{V_{P_1}} = \mathbf{u_1} = v_{aN_i} + v_{bN_i} e^{j(2\pi/3)} + v_{cN_i} e^{-j(2\pi/3)} = V_i \cos\,\omega_i t + V_i \cos(\omega_i t - (2\pi/3)) e^{j(2\pi/3)} + V_i \cos(\omega_i t + (2\pi/3)) e^{-j(2\pi/3)} = (3/2) V_i e^{j\omega_i t}$. $\mathbf{w_2}$, as shown in Fig. 3, corresponds to the connection (cab—$A_2B_2C_2$). This implies that terminals A_2, B_2, and C_2 are connected to

TABLE I
RESULTANT VECTORS

$\mathbf{V_1}$	$\mathbf{V_2}$	$\mathbf{V_3}$	$\mathbf{V_4}$	$\mathbf{V_5}$	$\mathbf{V_6}$
$\mathbf{u_1}+\mathbf{w_2}$	$\mathbf{u_1}+\mathbf{w_3}$	$\mathbf{u_2}+\mathbf{w_3}$	$\mathbf{u_2}+\mathbf{w_1}$	$\mathbf{u_3}+\mathbf{w_1}$	$\mathbf{u_3}+\mathbf{w_2}$

phases c, a, and b, respectively, and that switches S_{cA_2}, S_{aB_2}, and S_{bC_2} are on. Thus, $-\mathbf{V_{P_2}} = \mathbf{w_2} = -(v_{cN_i} + v_{aN_i}e^{j(2\pi/3)} + v_{bN_i}e^{-j(2\pi/3)}) = -(V_i\cos(\omega_i t + (2\pi/3)) + V_i\cos\omega_i t e^{j(2\pi/3)} + V_i\cos(\omega_i t - (2\pi/3))e^{-j(2\pi/3)}) = (3/2)V_i e^{j(\omega_i t-(\pi/3))}$. According to Table I, when $\mathbf{u_1}$ and $\mathbf{w_2}$ are applied together across the transformer primary, we get vector $\mathbf{V_1}$. This implies that $\mathbf{V_P} = \mathbf{V_1} = \mathbf{u_1} + \mathbf{w_2} = (3\sqrt{3}/2)V_i e^{j(\omega_i t-(\pi/6))}$ (see Fig. 3). Following similar analysis, it is possible to show that when $\mathbf{u_1}$ (acb—$A_1B_1C_1$) and $\mathbf{w_2}$ (bac—$A_2B_2C_2$), as shown in Fig. 4, are applied together, we get CW vector $\mathbf{V_P} = \mathbf{V_1} = \mathbf{u_1} + \mathbf{w_2} = (3\sqrt{3}/2)V_i e^{j(-\omega_i t-(\pi/6))}$ It is possible to show that application of these vectors results in zero common-mode voltage ($v_{\rm com} = (1/3)(v_{rN_s} + v_{yN_s} + v_{gN_s})$).

With six available voltage space vectors ($\mathbf{V_1}$–$\mathbf{V_6}$) (CCW or CW), the modulation is similar to that of a two-level voltage source inverter. For example, if at a particular instant of time $\mathbf{V_{ref}}$ is located in a sector formed by vectors $\mathbf{V_1}$ and $\mathbf{V_2}$, $\mathbf{V_{ref}}$ is synthesized, on average, using these two vectors, i.e.,

$$\mathbf{V_{ref}} = \frac{N_2}{N_1}(\mathbf{V_1}d_1 + \mathbf{V_2}d_2) \tag{12}$$

$$me^{j\left(\omega_o t+\phi-\left[\omega_i t-\frac{\pi}{6}\right]\right)} = d_1 + d_2 e^{j\frac{\pi}{3}} \tag{13}$$

$$d_1 = m\frac{\sin\left(\frac{\pi}{3}-\alpha\right)}{\sin\frac{\pi}{3}}$$

$$d_2 = m\frac{\sin\alpha}{\sin\frac{\pi}{3}} \tag{14}$$

where d_1 is the fraction of time for which $\mathbf{V_1}$ is applied, m is equal to $(N_1/N_2)(V_o/\sqrt{3}V_i)$, and $\alpha = \omega_o t + \phi - (\omega_i t - (\pi/6))$. The zero vector is obtained by the simultaneous use of $\mathbf{u_1}$ and $\mathbf{w_1}$. The zero vector is applied for $d_z = 1 - d_1 - d_2$ period of time.

Subsequently, when S goes low (11), the negative of the reference voltage vector is synthesized. This results in flux balance over full cycle of signal S. The sequence in which voltage vectors are applied is similar to CSVPWM [34], leading to a high-quality output voltage waveform.

Let us assume that the load power factor angle is θ, the peak of the output load currents is I_o ($i_r = I_o\cos(\omega t + \theta)$), and CCW vectors are used. When vector $\mathbf{V_1}$ is applied ($S = 1$), $i_a = (N_2/N_1)(i_r - i_y)$, as a is connected to A_1 and B_2. Similarly, during the application of $\mathbf{V_2}$ ($S = 1$), $i_a = (N_2/N_1)(i_r - i_g)$. The average input currents during this state are given in (15). Using definition (16) and (14) and (15), it is possible to obtain an expression for the average input current vector during this state, as given by (17). Note that, in this case, the average input line current vector is leading the input voltage vector ($\mathbf{V_i} = v_{aN_i} + v_{bN_i}e^{j(2\pi/3)} + v_{cN_i}e^{-j(2\pi/3)} = (3/2)V_i e^{j\omega_i t}$) by the output load power factor angle θ.

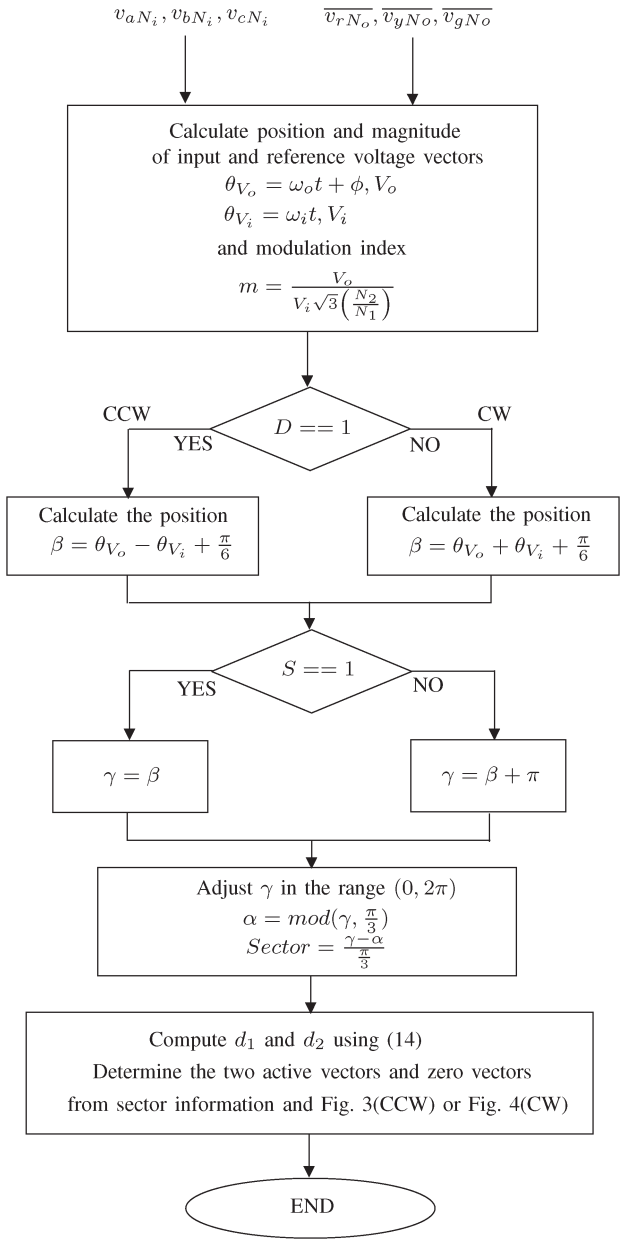

Fig. 5. Flowchart for the proposed modulation technique.

Similarly, when CW vectors are used, the average input current space vector is given in (18). Equal application of CW and CCW vectors over a complete cycle of D results in power factor correction (19). The aforementioned equations are given as follows:

$$\overline{i_a} = \frac{N_2}{N_1}\left[(i_r - i_y)d_1 + (i_r - i_g)d_2\right]$$

$$\overline{i_b} = \frac{N_2}{N_1}\left[(i_y - i_g)d_1 + (i_y - i_r)d_2\right]$$

$$\overline{i_c} = \frac{N_2}{N_1}\left[(i_g - i_r)d_1 + (i_g - i_y)d_2\right] \tag{15}$$

$$\overline{\mathbf{I}_{in}} = \overline{i_a} + \overline{i_b}e^{j\frac{2\pi}{3}} + \overline{i_c}e^{-j\frac{2\pi}{3}} \tag{16}$$

$$\overline{\mathbf{I_{in_{CCW}}}} = \left(\frac{N_2}{N_1}\right)\frac{3}{2}I_o\sqrt{3}me^{(j\omega_i t+\theta)} \tag{17}$$

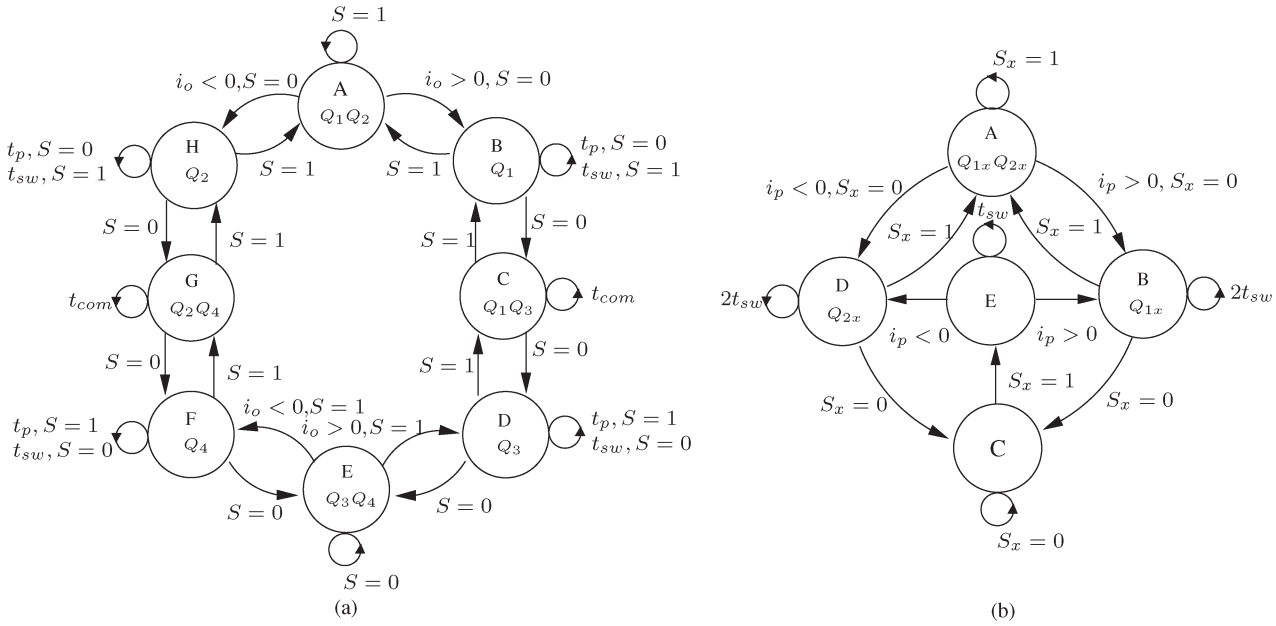

Fig. 6. FSM for (a) leakage commutation and (b) four-step commutation.

$$\overline{\mathbf{I}_{\mathrm{in_{CW}}}} = \left(\frac{N_2}{N_1}\right)\frac{3}{2}I_o\sqrt{3}me^{(j\omega_i t-\theta)} \tag{18}$$

$$\overline{\mathbf{I}_{\mathrm{in}}} = \frac{\overline{\mathbf{I_{inCCW}}}+\overline{\mathbf{I_{inCW}}}}{2} = \left(\frac{N_2}{N_1}\right)\frac{3}{2}I_o\sqrt{3}m\,\cos\theta e^{j\omega_i t}. \tag{19}$$

The flowchart in Fig. 5 presents a systematic step-by-step procedure to synthesize the average output voltage vector from the three input voltages v_{aN_i}, v_{bN_i}, and v_{cN_i} and reference average output voltages $\overline{v_{rN_o}}$, $\overline{v_{yN_o}}$, and $\overline{v_{gN_o}}$. This flowchart shows how signal S (see Fig. 2) is used in the modulation. It also shows how signal D (see Fig. 2) is used to control the application of CCW and CW vectors.

The primary winding of each HFT is connected to the input phases through two legs. For example, for output phase r (see Fig. 1), one leg is connected to the positive end (S_{aA_1} S_{bA_1}, S_{cA_1}) and another to the negative end (S_{aA_2} S_{bA_2}, S_{cA_2}). Note that, at any particular instant, only one leg is switched. During a switching transition of the primary-side converter, the secondary-side converter is not switched. The transformer leakage inductance comes in series with the inductive load current. The switching in a leg with an inductive leg current (similar to a matrix converter) is controlled by a mechanism called four-step commutation. This process is discussed in detail in the next section. A switching transition in any of these legs with four-step commutation results in hard-switching of only one insulated gate bipolar transistor (IGBT). Note that, in a particular sector, only one set of legs switches (either positive or negative). For example, when $\mathbf{V_{ref}}$ lies between vectors $\mathbf{V_1}$ and $\mathbf{V_2}$, as shown in Fig. 3, only negative legs switch to apply $\mathbf{w_1}$, $\mathbf{w_2}$, and $\mathbf{w_3}$, and positive legs are clamped to apply $\mathbf{u_1}$. Thus, from a modulation point of view, a switching loss is comparable with that of a matrix converter modulated with rotating vectors.

B. Commutation

Here, source-based commutation of leakage energy is presented in detail. At each transition of the flux balance signal S, power flow exchanges between the two halves of the secondary winding. Leakage inductance commutation refers to reversal of the primary leakage inductance current and exchange of the load current between the leakage inductance of the two halves of the secondary winding. Commutation is done on a per-phase basis by the application of appropriate voltage at the transformer primary by switching the input converter and controlling the individual IGBTs $Q_{1,2,3,4}$ in the secondary side converter (see Fig. 1).

The control of the commutation process is implemented with an FSM [see Fig. 6(a)]. As the commutation time period is much smaller than that of the input voltage and output current waveforms, it is possible to model them as dc sources during commutation.

Inputs of this FSM are the sign of the load current and the flux balance signal S. The outputs of this FSM are the control signals for the four switches $Q_{1,2,3,4}$ and two other binary signals C (see Fig. 2) and S_{com}, respectively. An active C indicates that the system is in the commutation mode. S_{com} is high or 1 when the required primary voltage to be applied for commutation is positive and is negative otherwise. Note that the S_{com} signal is relevant only when $C=1$. C is equal to zero only in states A and E. It turns out that $S_{\mathrm{com}}=S$ when the FSM is in states B, C, and D and $S_{\mathrm{com}}=\overline{S}$ for states F, G, and H.

Here, the case when load current is positive and S is making a transition from high to low is described in detail. At the initial stage of this transition, the S signal was high, and the converter was in modulation stage. Power was flowing through the upper half of the secondary winding, Q_1 and Q_2 were on, and the current state was A. According to modulation (CSVPWM) toward the end of a carrier cycle, a zero voltage was applied

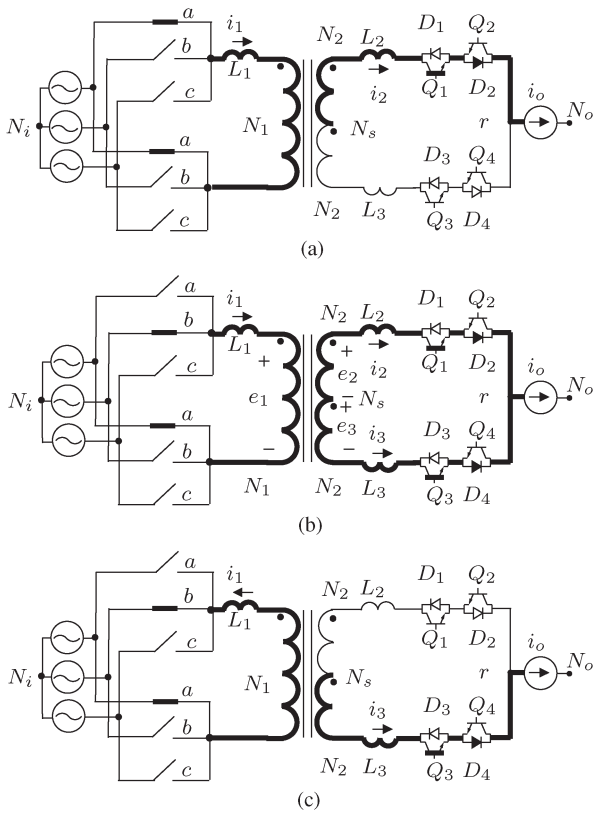

Fig. 7. Circuit configurations at various stages of leakage commutation.

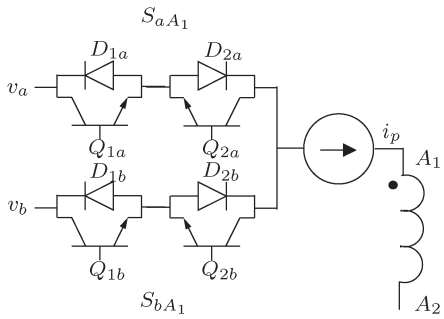

Fig. 8. Four-step commutation.

across the primary winding, and we may assume that both ends of the primary winding were connected to the input a phase [see Fig. 7(a)]. Once the S signal makes a transition from high to low as the load current is positive $(i_o > 0)$, in this case, the FSM moves to state B by turning off Q_2 in zero current (ZCS). In order to change the currents in the leakage inductance, a negative voltage must be applied, $S_{\rm com} = S = 0$, across the transformer primary. It takes a finite amount of time t_p for the input converter to apply the required voltage, and we need to wait in state B.

To design the waiting time t_p, it is important to understand the switching mechanism of the input converter. Each leg of the input converter comprises three four-quadrant switches. Each of these switches is implemented with two IGBTs (with antiparallel diodes) connected in a common–emitter configuration. The switching in one leg is done using four-step commutation to avoid short circuit of input voltage sources and to ensure a continuous path for the leg current. Switching of each of these pairs of IGBTs in one four-quadrant switch (Q_{1x} and Q_{2x}, where $x = a, b, c$) is controlled by an FSM, as shown in Fig. 6(b). The FSM of the four-step commutation has two inputs, namely, the switching signal S_x and the sign of the leg current i_p. The outputs are the switching signals for the individual IGBTs Q_{1x} and Q_{2x}. The details of the four-step process and an estimation of t_p are presented considering one typical example case.

Let us assume that, when the commutation FSM is in state B, v_{ba} is the maximum negative line to line voltage. Thus, v_{ba} must be applied across the primary for commutation. In Fig. 7, the top leg of the input converter must switch from phase a to phase b. This implies that S_a goes from high to low and S_b does the opposite. Fig. 8 shows the corresponding switches in the input converter in more details. Note that, at this instant of time, the top leg current is positive $(i_1 = i_p > 0)$. Thus, the FSM of phase a moves from state A to B and that of phase b moves from C to E. This implies that Q_{2a} (the nonconducting IGBT) is switched off and that both Q_{1b} and Q_{2b} continue to be off. The FSM of phase b waits in this state for t_{sw} period of time. This time period is to avoid short circuit and must be more than the absolute difference between the off and on time of the IGBTs. After this, phase b FSM moves from state E to B by turning on Q_{1b}. The FSM of phase a waits in the state B for $2t_{sw}$ time. When the FSM of phase b enters state B, both Q_{1a} and Q_{1b} are on. Transfer of the current from phase a to phase b depends on the sign of voltage v_{ab}. If v_{ab} is negative, the diode D_{2b} becomes forward biased, and the current transfers from phase a to b, and the pole voltage changes. In the present case, v_{ab} is positive, and natural commutation does not happen. At the end of this period, the FSM for phase a moves from state B to C by switching off Q_{1a}. At this point, current transfers from phase a to b, and Q_{1b} starts conducting. The FSM of phase b waits in state B for another t_{sw} amount of time before moving on to the next state A by turning on Q_{2b}. In conclusion, the total time to make this transition (change the primary voltage from v_{aa} to v_{ba}) may take from $2t_{sw}$ to a maximum of $3t_{sw}$ $(= t_p)$.

The commutation FSM after waiting t_p amount of time moves from the current state B to the next state C by turning on Q_3 with zero current (ZCS). As the currents in the leakage inductance $L_{1,2,3}$ cannot instantaneously change, application of negative primary voltage and turning on of switch Q_3 forward biases diode D_4. This is the starting point of the actual commutation process [see Fig. 7(b)].

In this analysis, magnetizing currents are neglected. Diodes are considered to be ideal. According to transformer relationships, (20) and (21) are valid. By KCL at the point where the output load is connected, we get (22). Equations (23) and (24) are obtained by applying KVL to the primary and secondary windings, respectively. Solution of these equations leads to (25). This gives the rate of change of the leakage inductance current i_3. The commutation time is maximum when the output load current is at its peak $(I_{\rm opk})$ and the available maximum line to line voltage is at its minimum $(V_i\sqrt{3}\,\cos(\pi/6))$. The time period for which the FSM waits in state C is $t_{\rm com}$ [see (26)]. When i_3 reaches i_o, i_2, and i_1 become zero and $-(N_2/N_1)i_o$,

TABLE II
PARAMETERS

$\|Z_L\|$	$\cos\theta_L$	$L_{1,2,3}$	$R_{1,2,3}$	L_m	$\frac{N_2}{N_1}$	V_{in}	f_i	$f_s = \frac{1}{T_s}$	f_o	m	L_F	C_F
20.26Ω	0.903	$10\mu H$	0.1Ω	180 mH	1	$40\sqrt{2}$V	60 Hz	5kHz	42 Hz	0.7	$0.5mH$	$80\mu F$

respectively, and the commutation process comes to a natural end. The aforementioned equations are given as follows:

$$\frac{e_1}{N_1} = \frac{e_2}{N_2} = \frac{e_3}{N_2} \tag{20}$$

$$i_1 N_1 - i_2 N_2 + i_3 N_2 = 0 \tag{21}$$

$$i_o = i_2 + i_3 \tag{22}$$

$$v_{ba} = L_1 \frac{d}{dt} i_1 + e_1 \tag{23}$$

$$e_2 + e_3 = L_2 \frac{d}{dt} i_2 - L_3 \frac{d}{dt} i_3 \tag{24}$$

$$\frac{d}{dt} i_3 = -\frac{v_{ba}\left(\frac{N_2}{N_1}\right)}{\left(\frac{L_2+L_3}{2}\right) + 2L_1\left(\frac{N_2}{N_1}\right)^2} \tag{25}$$

$$t_{\rm com} = \left[\frac{\left(\frac{L_2+L_3}{2}\right) + 2L_1\left(\frac{N_2}{N_1}\right)^2}{V_i\sqrt{3}\cos\frac{\pi}{6}\left(\frac{N_2}{N_1}\right)}\right] I_{\rm opk}. \tag{26}$$

After waiting for $t_{\rm com}$ period of time in state C, the commutation FSM moves to the next state D by turning off Q_1 with zero current. After waiting in this state for t_{sw} time, the FSM moves to state E by turning on Q_4 in zero current (ZCS). Fig. 7(c) shows the circuit configuration just after the commutation process is over. Note that all of the IGBTs in the secondary-side converter are soft-switched.

Signal C is one of the binary outputs of the commutation FSM [see Fig. 6(a)]. C goes high at each transition of the signal S (see Fig. 2). $C = 1$ in transitory states B, C, and D for $i_o > 0$ and F, G, and H for $i_o < 0$ indicates that the converter is in commutation mode. This implies from Fig. 6(a) that C remains high for a total time of $t_C = t_{\rm com} + t_p + t_{sw}$. As $t_{\rm com}$ given in (20) dominates in this sum, the duration for which C remains high depends on the leakage inductances L_1, L_2, and L_3 and the peak of the input voltage V_i and output current $I_{\rm opk}$.

In this converter, it is not necessary to design the leakage inductance for a specific value, but it must be within a range for a proper operation. In order to get soft-switching in the secondary-side converter, the commutation time $t_{\rm com}$ must be greater than the turn on or off time of the switches. From (20), given a particular turns ratio N_2/N_1, peak of the input voltage V_i, and output current $I_{\rm opk}$, the leakage inductances (L_1, L_2, and L_3) must be large enough so that $t_{\rm com}$ is more than the switching times. On the other hand, a larger value of leakage inductance puts limitations on the operation. Note that the commutation happens at the transition of signal S (see Fig. 2). As CSVPWM is used, the sequence in which vectors are applied over a sampling cycle is $\mathbf{V_0 V_1 V_2 V_0 V_2 V_1 V_0}$. The zero vectors are equally applied between the active vectors. Commutation happens when zero vectors are supposed to be applied due to modulation. During commutation, zero voltage is applied across the load. The zero vector time (at the transition of signal S) $(d_z/4)T_s$ must be greater than $t_{\rm com}$. Given a particular value of $t_{\rm com}$ or leakage inductances, this puts a limit either on the maximum value of the modulation index m that can be achieved given a particular sampling frequency $f_s = (1/T_s)$ or vice versa. A limit on sampling frequency implies a reduction in the output frequency f_o and an increase in the size of the magnetics. Note that one of the major objectives of this paper is to reduce this effect by minimizing the number of leakage commutation over one sampling cycle.

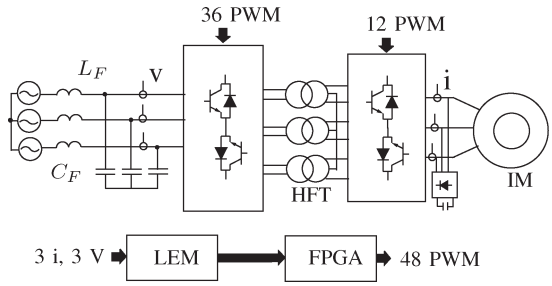

Fig. 9. Experimental setup.

III. Experimental and Simulation Results

This section presents a description of the experimental setup followed by important experimental and simulation results verifying the operation. Simulation (MATLAB/Simulink) and experiments are conducted with the same set of parameters, as shown in Table II.

The schematic of the actual experimental setup is shown in Fig. 9. The input-side converter is implemented using an integrated power module (IPM) from Microsemi (APTGT75TDU120PG). IPM APTGT75DU120TG is used for the secondary-side converter. A gate resistance of 18 Ω is chosen to get a difference between approximate on and off times of the IGBTs to be equal to 500 ns. t_{sw} is set at 600 ns ($>$ 500 ns). t_p is designed to be equal to 2 μs ($> 3t_{sw}$). Using (26), the maximum commutation time turns out to be equal to 1.3 μs. $t_{\rm com}$ is set at 4 μs for safe operation.

A field-programmable gate array-based control platform (Xilinx, XC3S500E) has been used to generate all of the 48 PWM signals. The HFTs are designed using the area product method. The key design equations for core (27) and window (28) areas can be obtained by noting that the maximum flux swing happens when the output voltage is at its peak and each of the secondary winding conducts only half the time, i.e.,

$$A_c = \frac{mV_{in}\sqrt{3}}{2N_1 f_s B_{\max}} \tag{27}$$

$$A_w K_w = \frac{N_2}{J_{\max}} I_{o_{\rm RMS}}(1+\sqrt{2}). \tag{28}$$

A balanced set of $R-L$ load and an induction machine is used as a three-phase load.

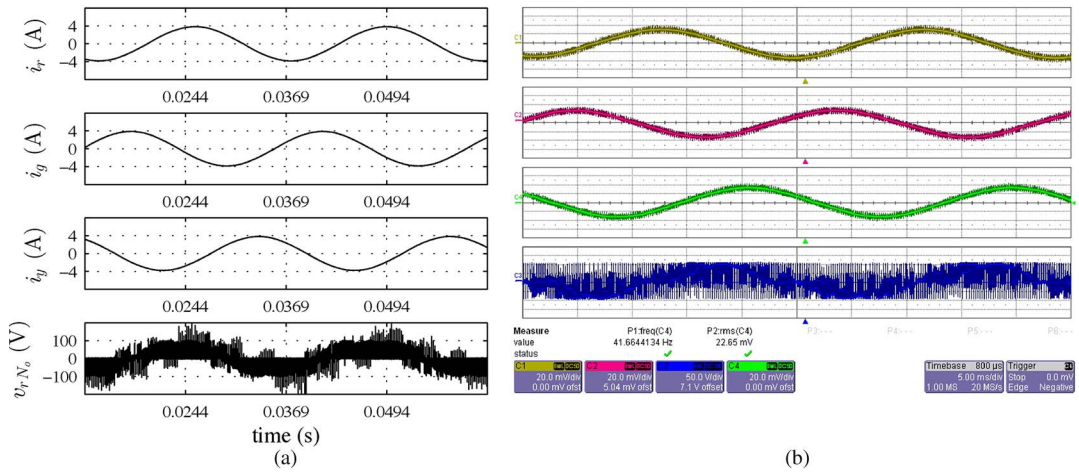

Fig. 10. (a) Simulation. (b) Experimental. Output line current phase r (CH-C1), phase g (CH-C2), phase y (CH-C4) [2 A/div in (b)], output line to neutral voltage phase r (CH-C3) [50 V/div in (b)], and time 5 ms/div.

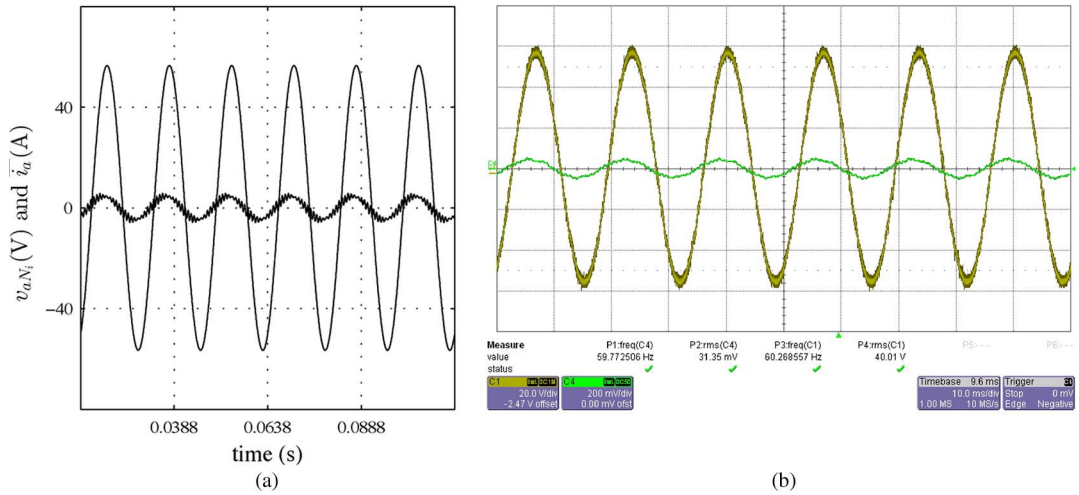

Fig. 11. (a) Simulation. (b) Experimental. Source line to neutral (CH-C1) [20 V/div in (b)] voltage, filtered/source line current (CH-C4) [20 A/div in (b)], and time 10 ms/div.

Simulation and experimental results are presented together for a direct comparison.

Fig. 10 shows the three output line currents along with the line to neutral voltage of phase r. The three-phase load acts as a low-pass filter and eliminates the response due to switching frequency components of the PWM output voltage waveforms. The simulated output current waveforms have approximately a peak of 3.7 A as predicted analytically. The experimental waveforms have a lower peak of 3.2 A. This implies that V_o is 64.83 V. Thus, there is an approximately 3.75 V drop in the output voltage's observed value from its predicted value of 68.58 V ($\sqrt{3}mV_i$). This can be due to the voltage drop across the switches. When a switch conducts, one IGBT conducts in series with a diode, and the total voltage drop is approximately 1.3 V. Note that during modulation for each of the output phases, three such switches are on (two switches in the primary converter connect the input source to the HFT's primary, and one switch in the secondary converter connects one of the HFT's secondary winding to the load). This adds up to 3.9 V. This also implies that if we consider an equal number of turns, the conduction loss of this converter is three

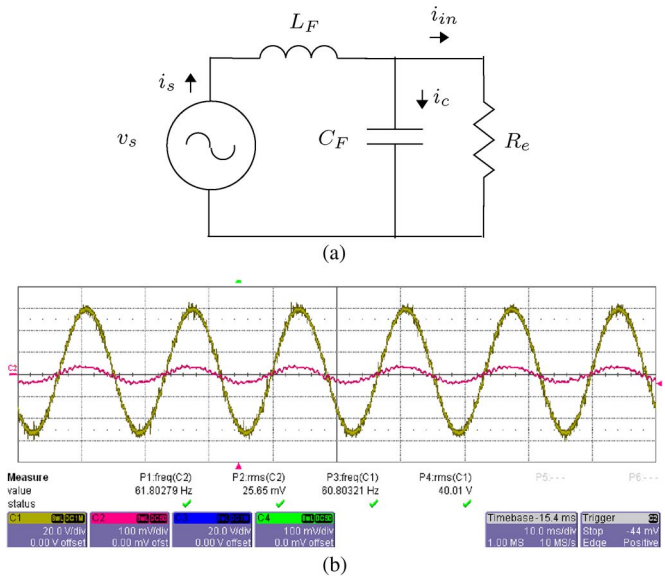

Fig. 12. (a) Equivalent circuit. (b) Source line to neutral (CH-C1) (20 V/div) voltage, filtered/source line current (CH-C4) (10 A/div), and time 10 ms/div.

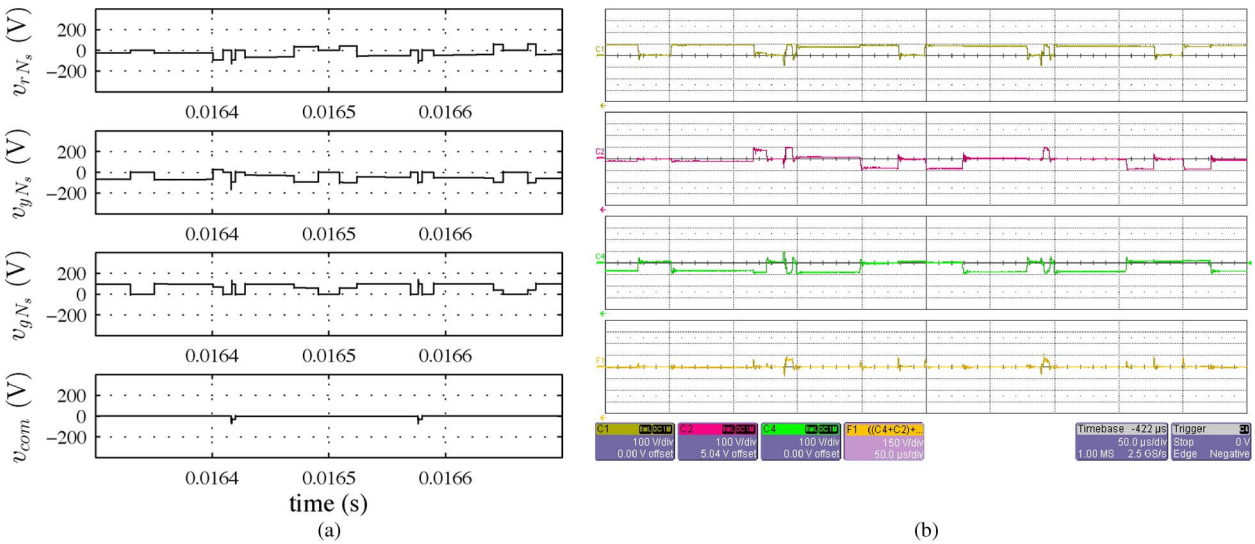

Fig. 13. (a) Simulation. (b) Experimental. Three output line voltages (CH-C1, CH-C2, and CH-C4) [100 V/div in (b)], common-mode voltage (CH-F1) [scaled 3×, 150 V/div in (b)], and time 50 μs/div.

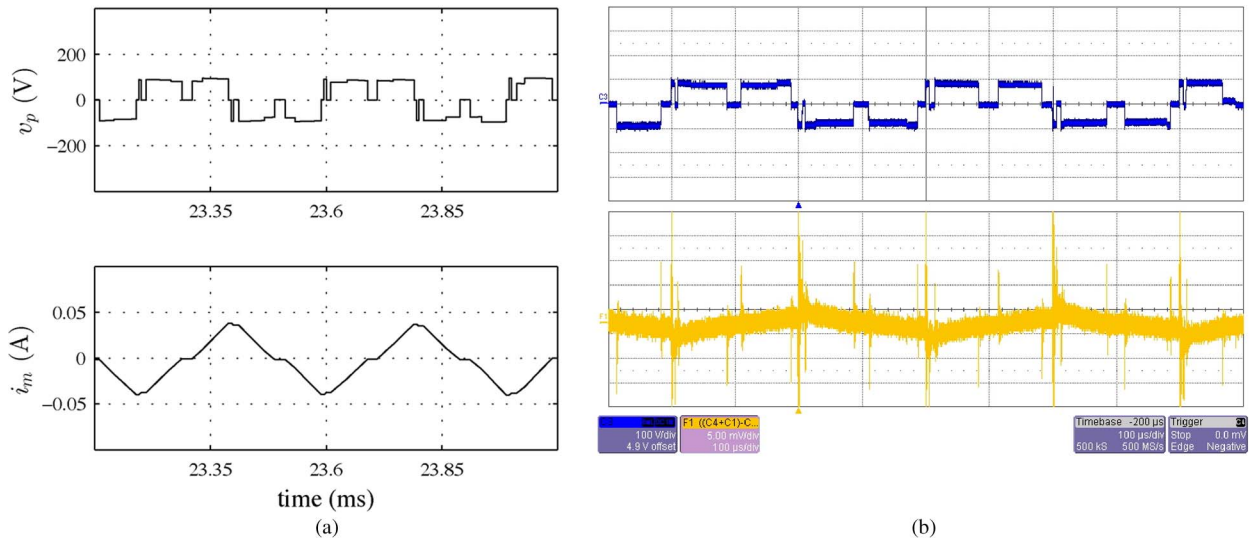

Fig. 14. (a) Simulation. (b) Experimental. Primary voltage (CH-C3) [100 V/div in (b)], magnetizing current (CH-F1) [0.5 A/div in (b)], and time 100 μs/div.

times that of the matrix converter. The output power is 281 W ($1.5V_oI_{\rm opk}\cos\theta_L$).

The source current and voltage of phase a are plotted in Fig. 11. It can be seen that source current and the voltage are not in phase and the current is leading by an angle of $\theta_i = 26^\circ$. This power factor angle is due to the input L–C filter. As the average input current vector $\overline{\mathbf{I_{in}}}$ in (19) is aligned along the input voltage vector, the converter for the fundamental frequency ω_i can be modeled as a resistance R_e [see Fig. 12(a)]. R_e can be estimated from the input power $R_e = (3V_i^2/2P_i)$. Analyzing the equivalent circuit in Fig. 12(a), it is possible to estimate the source power factor angle θ_i, i.e.,

$$\theta_i = \tan^{-1}\omega_i C_F R_e - \tan^{-1}\frac{\omega_i L_F}{R_e\left(1-\omega_i^2 L_F C_F\right)}. \qquad (29)$$

The estimated angle of $\theta_i = 24.58^\circ$ closely matches the observation. The input L–C filter components are redesigned to be $L_F = 0.9$ mH and $C_F = 26.4$ μF to improve the power factor to 0.9898 ($\theta_i = 8.2^\circ$) [see Fig. 12(b)]. The peak of the input current is $I_{\rm inpk} = 3.63$ A, and the input power is 304.87 W ($1.5V_{in}I_{\rm inpk}\cos\theta_i$). This implies that the observed efficiency is 92.17%.

The three output line voltages (with respect to transformer neutral N_s) are plotted in Fig. 13 over one complete cycle of signal S. The common-mode voltage is obtained by summing these waveforms. The common-mode voltage switches only once in one sampling cycle ($f_s = 5$ kHz) during leakage commutation and remains zero otherwise.

The input voltage to the transformer primary along with the magnetizing current over one cycle of the flux balance signal S is shown in Fig. 14. The magnetizing current is obtained from the three winding currents. As the magnetizing current is very small (in milliamperes), it was difficult to measure it experimentally. However, the experimental result clearly indicates flux balance in the core.

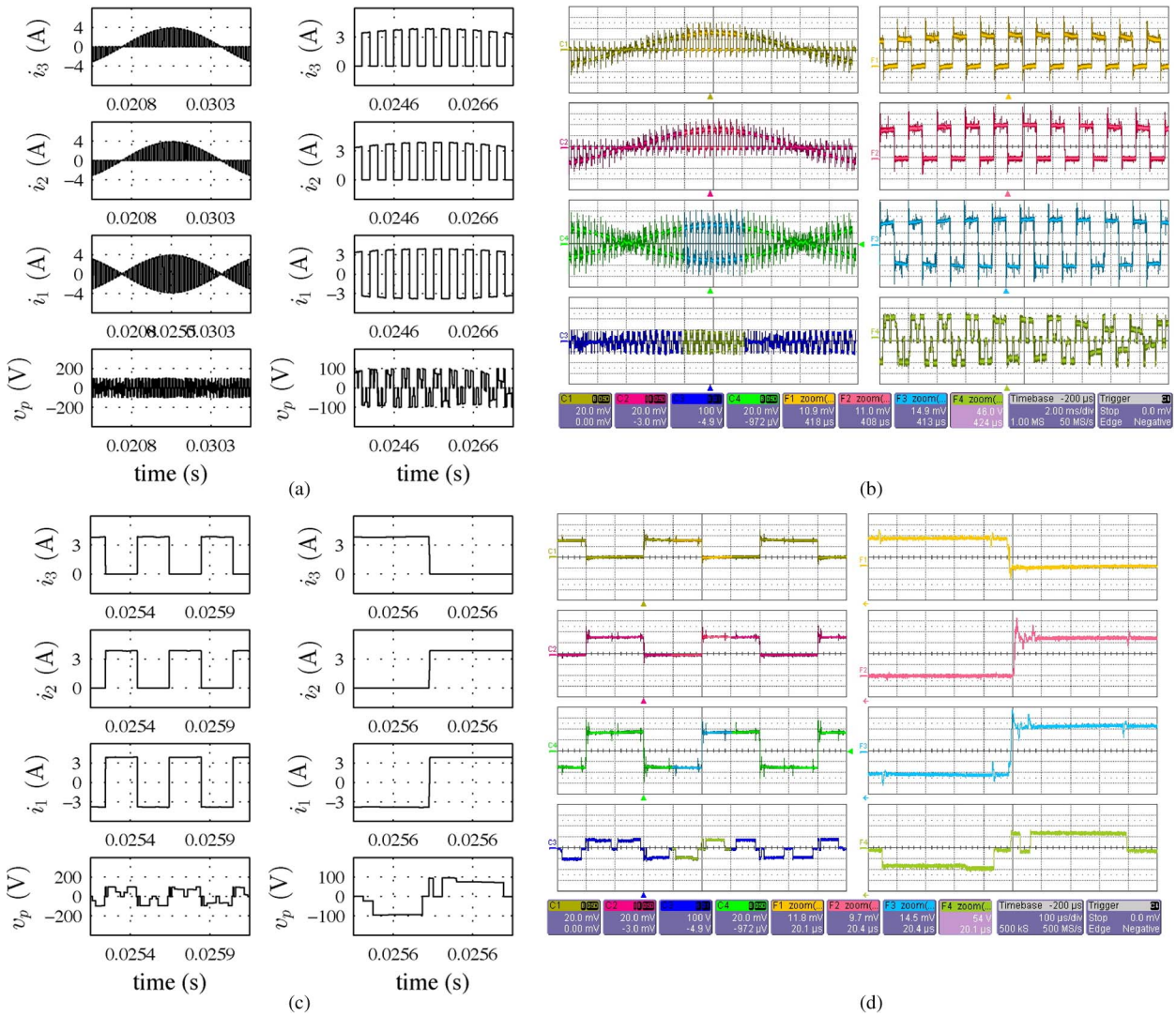

Fig. 15. (a) and (c) Simulation. (b) and (d) Experimental. Primary current (CH-C4), two secondary winding currents (CH-C1 and CH-C2) [2 A/div in (b) and (d)], primary voltage (CH-C3) [100 V/div in (b) and (d)], and time 2 ms/div in (b) and 100 μs/div in (d).

The next set of results corresponds to the commutation of leakage energy (see Fig. 15). The two secondary and primary winding currents are plotted with the primary winding voltage. The secondary current waveforms are complementary to each other and composed of 50% duty cycle modulated output current. The primary current is the 50% duty cycle modulated chopped version of the output current. The zoomed version of these waveforms clearly shows the application of proper voltage by the input converter and linear change in winding currents at the end of each sampling cycle T_s due to commutation. The measured slope of the inductor currents during commutation matches with analytical prediction of (25). In experimental results at the end of leakage inductance commutation, the winding currents show a small overshoot. This is due to the reverse recovery of the antiparallel diode that is turning off in the output-side converter.

Figs. 16 and 17 present various experimentally observed waveforms that show how soft-switching (ZCS) is achieved in all secondary-side converter switches. These waveforms correspond to the case discussed in detail in the commutation section (see Fig. 7). In this discussion, please refer to Fig. 7 for currents i_2 and i_3. From Fig. 16, when Q_1 is switched (its gate–emitter voltage changed), the current through Q_1, i.e., i_2, is zero. In Fig. 16, i_2 is positive when Q_2 is switched (its gate–emitter voltage changed). A positive i_2 implies that diode D_2 is conducting and the current through Q_2 is zero. Similarly from Fig. 17, it is possible to see that Q_4 is switched with zero current. These observations confirm zero-current soft-switching of Q_1, Q_2, and Q_4. Turning on of Q_3 initiates the commutation process, and the current through Q_3, i.e., i_3, starts to rise. However, the commutation process starts only when the voltage across Q_3 falls, which, in turn, forward biases diode D_4. Fig. 17 shows the fall of the collector–emitter voltage across Q_3 with zero current through it, resulting in zero-current soft-switching.

Fig. 18 shows experimentally observed waveforms related to the example of the four-step commutation discussed in Section II (see Fig. 8). The first three plots in Fig. 19 show the output line currents when a four-pole induction machine with a dc generator load is run by this converter at rated $V/f = 3$

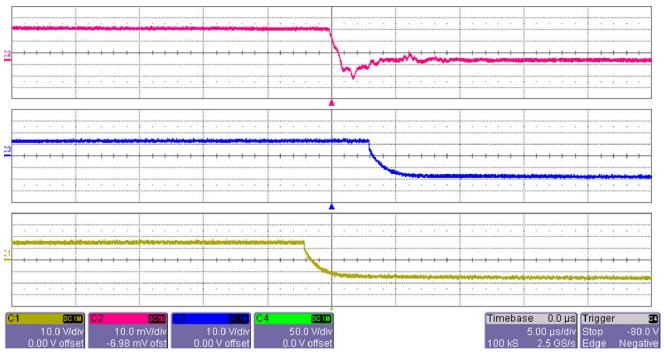

Fig. 16. i_2 (CH-C2) (1 A/div), gate–emitter voltage of Q_1 (CH-C3) (10 V/div), gate–emitter voltage of Q_2 (CH-C1) (10 V/div), and time 5 μs/div.

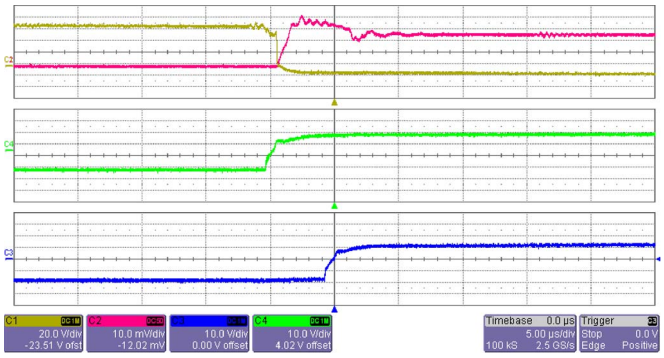

Fig. 17. i_3 (CH-C2) (1 A/div), collector–emitter voltage of Q_3 (CH-C1) (20 V/div), gate–emitter voltage of Q_3 (CH-C4) (10V/div), gate–emitter voltage of Q_4 (CH-C3) (10 V/div), and time 5 μs/div.

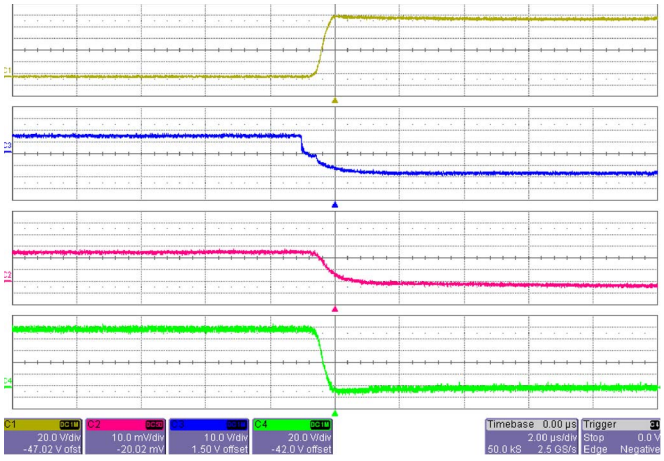

Fig. 18. Collector–emitter voltage (CH-C1) (20 V/div), gate–emitter voltage (CH-C3) (20 V/div), and collector current (CH-C2) (1 A/div) of Q_{1a} along with the primary voltage $v_{A_1A_2}$ (CH-C4) (20 V/div) and time 5 μs/div.

(ratio of the peak of the line to neutral voltage to the frequency) at a frequency of 11 Hz. The fourth plot shows input voltage at the frequency of 60 Hz. All of the results presented in this section, except the one in Fig. 19, are with a series $R-L$ load.

IV. Conclusion

In this paper, a new single-stage high-frequency-link PWM ac/ac converter with a control strategy has been

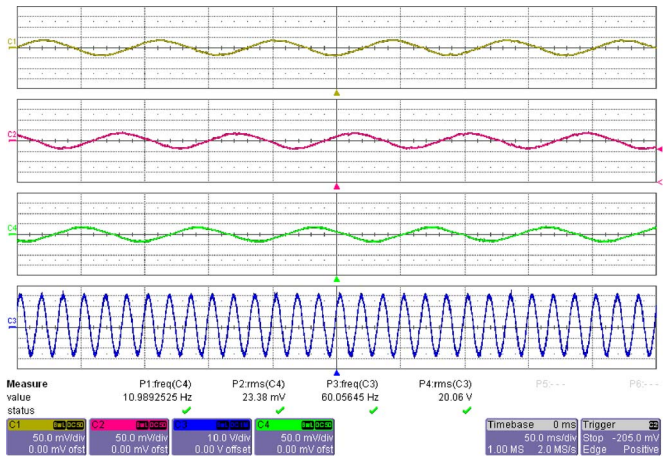

Fig. 19. Motor output line currents (CH-C1, CH-C2, and CH-C4) (5 A/div), input line to neutral voltage (CH-C3) (10 V/div), and time 5 ms/div.

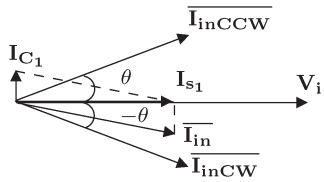

Fig. 20. Reactive power compensation.

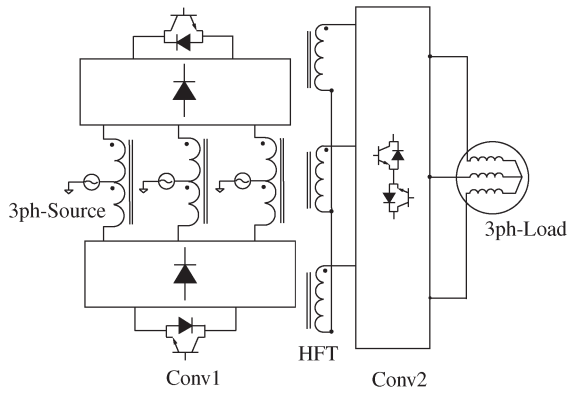

Fig. 21. PET type I.

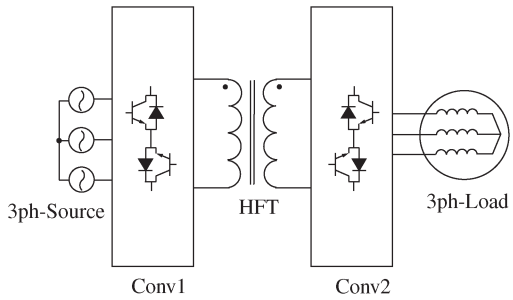

Fig. 22. PET type II.

proposed. The following advantages of the proposed topology have been confirmed through the presented experimental and simulation results: 1) bidirectional power flow; 2) input power factor correction; 3) common-mode voltage suppression;

TABLE III
COMPARISON

Topologies	Number of switches	Quality of output voltage comparable to CSVPWM	Common-mode voltage suppression	Flux swing	Source based commutation	Number of commutation over one sampling cycle
Type I	20	No	No	Variable	No	> 1
Type II	24	No	No	Constant	Yes	> 1
Proposed	48	Yes	Yes	Variable	Yes	1

4) minimum number of switching transitions between the load and the transformer secondary windings, which implies lower output voltage loss, common-mode voltage switching during commutation, and possible higher frequency of operation; 5) source-based commutation of leakage energy without using any additional circuit leads to recovery of leakage energy; 6) ZCS in all secondary-side switches; and 7) high-quality output voltage synthesis comparable with CSVPWM. The drawbacks of this topology are relatively large switch count, high conduction loss, and limited ride-through capability. The source-based commutation requires additional hard-switching of the primary-side converter. This topology achieves almost all of the advanced features of PWM ac drives and can become a promising solution for compact isolated motor drives.

APPENDIX A
REACTIVE POWER COMPENSATION

It is possible to compensate for the input power factor angle or any reactive power drawn from the source due to the LC filter. Note that the input filter is designed such that, at rated condition, the fundamental component of the voltage drop across the filter inductor is negligible. Thus, the input voltage and source voltage at fundamental frequency ω_i are approximately the same for all load conditions. The fundamental component of source current space vector $\mathbf{I_{s_1}}$ can be written as $\overline{\mathbf{I_{in}}} + \mathbf{I_{C_1}}$. $\mathbf{I_{C_1}}$ corresponds to the fundamental component of the current flowing into the filter capacitor, i.e., $|\mathbf{I_{C_1}}| = (3/2)V_i\omega_i C_F$. The source current leads the input voltage due to this reactive component of current. It is possible to compensate for this reactive component by a duty cycle modulation in the application of the CCW and CW vectors. In the modulation described in Section II, both CCW and CCW vectors are equally applied, and signal D in Fig. 2 has 50% duty cycle. If we apply CW vectors for $d_{\rm CW}$ fraction of time and CCW vectors for the rest of the time, the average input current vector will be given as $\overline{\mathbf{I_{in}}} = \overline{\mathbf{I_{in_{CCW}}}}(1 - d_{\rm CW}) + \overline{\mathbf{I_{in_{CW}}}}d_{\rm CW}$. $d_{\rm CW}$ can be selected to compensate for $\mathbf{I_{C_1}}$ [see Fig. 20; (30) and (31)]. $K = (N_2/N_1)(3/2)I_o\sqrt{3}m$ is the magnitude of the average input current vector when the CW or CCW vector is applied. Note that this compensation has a limited range and that $d_{\rm CW}$ in (31) must be less than unity. It is possible to obtain $d_{\rm CW}$ in closed-loop fashion by controlling the source reactive power to zero.

$$\frac{3}{2}V_i\omega_i C_F + K(1 - d_{\rm CW})\sin\theta = Kd_{\rm CW}\sin\theta \quad (30)$$

$$d_{\rm CW} = \frac{1}{2}\left[1 + \frac{1.5V_i\omega_i C_F}{K\sin\theta}\right]. \quad (31)$$

APPENDIX B
COMPARISON OF DIFFERENT SINGLE-STAGE THREE-PHASE PETS

A brief comparison of different types of single-stage three-phase ac/ac PETs is presented here. In the type-I PET [23] (see Fig. 21), the input converter (Conv1) chops the input ac grid voltage to a 50% duty cycle high-frequency ac and passes through a bank of three HFTs. The secondary-side converter (Conv2) operates as a matrix converter to generate a three-phase PWM ac at the load end. The type-II PETs are based on the indirect modulation of matrix converters. In this type of PETs [26] (see Fig. 22), the input-side converter (Conv1) first rectifies the three-phase ac to a virtual dc link, and then, the dc is chopped with a 50% duty cycle to pass through a single-phase HFT. The load-side converter (Conv2) first rectifies the high-frequency ac to the virtual dc and then inverts it to generate a three-phase PWM ac. A comparison of type-I and type-II PETs with the proposed converter is presented in Table III.

ACKNOWLEDGMENT

The authors would like to thank Dr. C. Henze for the support.

REFERENCES

[1] E. Ronan, S. Sudhoff, S. Glover, and D. Galloway, "A power electronic-based distribution transformer," *IEEE Trans. Power Del.*, vol. 17, no. 2, pp. 537–543, Apr. 2002.
[2] C. G. C. Branco, R. Torrico-Bascope, C. M. T. Cruz, and F. de A Lima, "Proposal of three-phase high-frequency transformer isolation UPS topologies for distributed generation applications," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1520–1531, Apr. 2013.
[3] A. Garces and M. Molinas, "A study of efficiency in a reduced matrix converter for offshore wind farms," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 184–193, Jan. 2012.
[4] X. She, A. Huang, F. Wang, and R. Burgos, "Wind energy system with integrated functions of active power transfer, reactive power compensation, and voltage conversion," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4512–4524, Oct. 2013.
[5] P. Drabek, Z. Peroutka, M. Pittermann, and M. Cedl, "New configuration of traction converter with medium-frequency transformer using matrix converters," *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 5041–5048, Nov. 2011.
[6] M. Carpita, M. Marchesoni, M. Pellerin, and D. Moser, "Multilevel converter for traction applications: Small-scale prototype tests results," *IEEE Trans. Ind. Electron.*, vol. 55, no. 5, pp. 2203–2212, May 2008.
[7] H. Krishnamoorthy, P. Enjeti, I. Pitel, and J. Hawke, "New medium-voltage adjustable speed drive (ASD) topologies with medium-frequency transformer isolation," in *Proc. 7th IPEMC*, Jun. 2012, vol. 2, pp. 814–819.
[8] S. Falcones, X. Mao, and R. Ayyanar, "Topology comparison for solid state transformer implementation," in *Proc. IEEE Power Energy Soc. Gen. Meet.*, Jul. 2010, pp. 1–8.
[9] M. Sabahi, S. Hosseini, M. Sharifian, A. Goharrizi, and G. Gharehpetian, "Zero-voltage switching bi-directional power electronic transformer," *IET Power Electron.*, vol. 3, no. 5, pp. 818–828, Sep. 2010.

[10] T. Zhao, G. Wang, S. Bhattacharya, and A. Q. Huang, "Voltage and power balance control for a cascaded H-bridge converter-based solid-state transformer," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1523–1532, Apr. 2013.
[11] S. Bifaretti, P. Zanchetta, A. Watson, L. Tarisciotti, and J. Clare, "Advanced power electronic conversion and control system for universal and flexible power management," *IEEE Trans. Smart Grid*, vol. 2, no. 2, pp. 231–243, Jun. 2011.
[12] J.-S. Lai, A. Maitra, A. Mansoor, and F. Goodman, "Multilevel intelligent universal transformer for medium voltage applications," in *Conf. Rec. IEEE IAS Annu. Meet.*, Oct. 2005, vol. 3, pp. 1893–1899.
[13] H. Fan and H. Li, "High-frequency transformer isolated bidirectional dc–dc converter modules with high efficiency over wide load range for 20 kVA solid-state transformer," *IEEE Trans. Ind. Electron.*, vol. 26, no. 12, pp. 3599–3608, Dec. 2011.
[14] M. Kang, P. Enjeti, and I. Pitel, "Analysis and design of electronic transformers for electric power distribution system," *IEEE Trans. Power Electron.*, vol. 14, no. 6, pp. 1133–1141, Nov. 1999.
[15] H. Krishnaswami and V. Ramanarayanan, "Control of high-frequency ac link electronic transformer," *Proc. Inst. Elect. Eng.—Elect. Power Appl.*, vol. 152, no. 3, pp. 509–516, May 6, 2005.
[16] D. Chen, "Novel current-mode ac/ac converters with high-frequency ac link," *IEEE Trans. Ind. Electron.*, vol. 55, no. 1, pp. 30–37, Jan. 2008.
[17] R. A. Xiaolin Mao and S. Falcones, "A modular, interleaved ac–ac flyback topology for solid state transformer," in *Proc. FREEDM Annu. Conf.*, May 2009, pp. 221–224.
[18] D. Chen and Y. Chen, "Step-up ac voltage regulators with high-frequency link," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 390–397, Jan. 2013.
[19] H. Qin and J. Kimball, "Solid-state transformer architecture using ac–ac dual-active-bridge converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3720–3730, Sep. 2013.
[20] J. Shah, R. Gupta, K. Mohapatra, and N. Mohan, "Power management with a dynamic power limit by a power electronic transformer for microgrid," in *Proc. IEEE Power Energy Soc. Gen. Meet.*, 2010, pp. 1–5.
[21] P. Wheeler, J. Rodriguez, J. Clare, L. Empringham, and A. Weinstein, "Matrix converters: A technology review," *IEEE Trans. Ind. Electron.*, vol. 49, no. 2, pp. 276–288, Apr. 2002.
[22] K. Basu *et al.*, "Research in matrix-converter based three-phase power-electronic transformers," in *Proc. IPEC*, Jun. 2010, pp. 2799–2803.
[23] G. Castelino, K. Basu, R. Gupta, and N. Mohan, "Power electronic transformer with reduced number of switches: Analysis of input clamp circuit and a modulation strategy to eliminate input snubber requirement," in *Proc. 36th IEEE IECON/IECON*, 2010, pp. 656–661.
[24] S. Nath, K. Mohapatra, K. Basu, and N. Mohan, "Source based commutation in matrix converter fed power electronic transformer for power systems application," in *Proc. SPEEDAM*, Jun. 2010, pp. 1682–1686.
[25] H. J. Cha and P. Enjeti, "A three-phase ac/ac high-frequency link matrix converter for VSCF applications," in *IEEE PESC/IEEE Power Electron. Spec. Conf.*, Jun. 2003, vol. 4, pp. 1971–1976.
[26] A. Shahani, K. Basu, and N. Mohan, "A power electronic transformer based on indirect matrix converter for PWM ac drive with lossless commutation of leakage energy," in *Proc. 6th IET Int. Conf. PEMD*, Mar. 2012, pp. 1–6.
[27] M. Matsui, M. Nagai, M. Mochizuki, and A. Nabae, "High-frequency link dc/ac converter with suppressed voltage clamp circuits-naturally commutated phase angle control with self turn-off devices," *IEEE Trans. Ind. Appl.*, vol. 32, no. 2, pp. 293–300, Mar./Apr. 1996.
[28] S. Mazumder and A. K. Rathore, "Primary-side-converter-assisted soft-switching scheme for an ac/ac converter in a cycloconverter-type high-frequency-link inverter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4161–4166, Sep. 2011.
[29] R. Garcia-Gil, J. Espi, E. Dede, and E. Sanchis-Kilders, "A bidirectional and isolated three-phase rectifier with soft-switching operation," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 765–773, Jun. 2005.
[30] G. Castelino, K. Basu, and N. Mohan, "Power electronic transformer with reduced number of switches: Analysis of clamp circuit for leakage energy commutation," in *Proc. Joint. Int. Conf. PEDES Power India*, Dec. 2010, pp. 1–8.
[31] U. Shami and H. Akagi, "Experimental discussions on a shaft end-to-end voltage appearing in an inverter-driven motor," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1532–1540, Jun. 2009.
[32] R. Gupta, K. Mohapatra, A. Somani, and N. Mohan, "Direct-matrix-converter-based drive for a three-phase open-end-winding ac machine with advanced features," *IEEE Trans. Ind. Electron.*, vol. 57, no. 12, pp. 4032–4042, Dec. 2010.
[33] A. Somani, R. Gupta, K. Mohapatra, and N. Mohan, "On the causes of circulating currents in PWM drives with open-end winding ac machines," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3670–3678, Sep. 2013.
[34] K. Basu, J. Prasad, and G. Narayanan, "Minimization of torque ripple in PWM ac drives," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 553–558, Feb. 2009.
[35] K. Basu and N. Mohan, "A power electronic transformer for three phase PWM ac/ac drive with loss less commutation and common-mode voltage suppression," in *Proc. 36th IEEE IECON/IECON*, Nov. 2010, pp. 315–320.

Kaushik Basu (S'07–M'13) received the B.E. degree in electrical engineering from Bengal Engineering and Science University, Shibpore, India, in 2003; the M.S. degree in electrical engineering from the Indian Institute of Science, Bangalore, India, in 2005; and the Ph.D. degree in electrical engineering from the University of Minnesota, Minneapolis, MN, USA, in 2012.

He was a Design Engineer with ColdWatt India Private Limited, Bangalore, India, in 2006. He is currently an Electronics and Control Engineer with Dynapower Company, LCC, South Burlington, VT, USA. His research interests include high-frequency-link converters, PWM techniques, and grid-tied converters with storage and renewable energy sources.

Ned Mohan (S'72–M'73–SM'91–F'96) received the B.Tech. degree in electrical engineering from the Indian Institute of Technology (IIT), Kharagpur, India, in 1967; the M.S. degree in electrical engineering from the University of New Brunswick, Fredericton, NB, Canada, in 1969; and the M.S. degree in nuclear engineering and the Ph.D. degree in electrical engineering from the University of Wisconsin, Madison, WI, USA, in 1972 and 1973, respectively.

He is currently the Oscar A. Schott Professor of Power Electronics at the University of Minnesota, Minneapolis, MN, USA, where he has been engaged in teaching since 1976. He has authored or coauthored five textbooks, one of which has been translated into six languages. He has numerous patents and publications in the field of power electronics, electric drives, and power systems.

Dr. Mohan is a member of the National Academy of Engineering. He was the recipient of the 2008 IEEE Power and Energy Society Outstanding Educator Award, the 2010 IEEE Undergraduate Teaching Award, the 2010 UWIG Achievement Award from the Utility Wind Integration Group, the 2011 Distinguished Alumnus Award from the Indian Institute of Technology Kharagpur, and the 2012 IEEE Power and Energy Society Ramakumar Family Renewable Energy Excellence Award. In 2013, he received the Innovative Program Award from the Electrical and Computer Engineering Department Heads Association.