A Unidirectional Soft-switched Isolated Three Level Inverter for Grid Integration of Renewable Energy Sources

Anirban Pal and Kaushik Basu
Department of Electrical Engineering,
Indian Institute of Science, Bangalore- 560012, India
Email: palanirban@ee.iisc.ernet.in, basu@ee.iisc.ernet.in

***Abstract*—This paper presents a single stage, unidirectional, three level, three phase high frequency link inverter topology. The proposed topology can be used for applications like grid integration of renewable energy sources such as fuel cell, solar photovoltaic where power flow is mainly unidirectional. The use of high frequency transformer reduces overall system volume and cost as well as improves power density. The switches in primary side of the proposed converter are soft-switched. As the primary side converter has multilevel structure, voltage stress on the switches are also reduced. The secondary side switches are switched only at line frequency leading to negligible switching loss. An analysis of operation of the proposed converter is discussed in details. Key simulation results are presented demonstrating the effectiveness of the proposed topology.**

Index Terms- Three level diode clamp inverter, high frequency link, modulation technique, soft-switching.

I. Introduction

Single stage isolated high frequency link (HFL) inverter topologies are receiving attention for applications like grid integration of renewable sources [1], uninterruptible power supply (UPS) system [2], energy storage system, hybrid and electric vehicle energy management. Compared to conventional isolated inverter system with line frequency transformer, the high-frequency-transformer (HFT) based inverter system has following advantages- higher power density, lower volume and weight and low cost. Like the conventional line frequency transformer, HFT provides required voltage magnification as well as galvanic isolation to reduce the leakage current and to ensure safety.

The HFL inverters so far discussed in literature could be classified into two major categories- multi-stage and single stage. In multi-stage topology an isolated DC-DC stage is cascaded with DC-line frequency AC stage through a bulky DC link filter capacitor, facing long term reliability issues. Single stage topologies do not use any intermediate stage filter capacitor. Two most discussed single stage topologies are- rectifier type and cyclo-converter type. In rectifier type [3] two back to back H bridge are used in the secondary of HFT to convert the high frequency AC to controllable magnitude and line frequency AC. In cyclo-converter type [4], instead of two H bridge, a cyclo-converter is used in the secondary. A number of modulation strategies with additional snubber circuits are discussed in literature to achieve soft-switching of the mentioned topologies. In [5] source based commutation technique is employed to achieve soft switching with out using any additional snubber circuit. In [6] leakage energy of HFT is used to achieve soft switching of a primary side push-pull based HFL inverter.

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In [7]–[9] unidirectional 3ϕ high frequency link inverter topologies are discussed. The DC side converter of these unidirectional three phase topologies have three H-bridges. This paper proposes a three level structure for the DC side converter, in Fig. 1. This structure, assuming same DC voltage level and switching frequency has the following advantages- 1) same number of switches with lower (half) voltage blocking capacity and hence has better switching and conduction characteristics [10], [11]; 2) same number of switches conduct but due to lower blocking voltage rating the conduction loss will be reduced; 3) Lower switching loss (if hard switched) due to reduced DC bus voltage and better switching loss characteristics of the devices; 4) smaller filter requirement due to improvement in the quality of the PWM output voltage waveform [10], [11].

The proposed topology with suggested modulation scheme has following attributes: (i) single stage architecture with no interstage DC capacitor and suitable for unidirectional power flow, (ii) DC side high frequency inverter has diode clamped three level structure⇒ lower switching and conduction loss, lower voltage blocking devices without increasing number of control switches and smaller filter, (iii) soft-switched DC side high frequency inverter, (iv) Active switches in the AC side converter are line frequency switched, which implies negligible switching loss. This feature also opens up the possibility of direct integration of medium voltage AC grid using inherently slow high voltage blocking semiconductor devices, (v) galvanic isolation using compact and high power density high frequency transformer.

The paper is organized as follows. Section II presents modulation strategy and soft-switching technique of the converter for unity power factor operation. Key simulation results are presented in section III.

II. Steady state operation and analysis

This section presents a detailed description of steady state operation of the proposed converter. The analysis is divided into two subsections- (a) modulation strategy to generate 3ϕ line frequency AC voltage and (b) soft switching techniques of the primary side high frequency inverter.

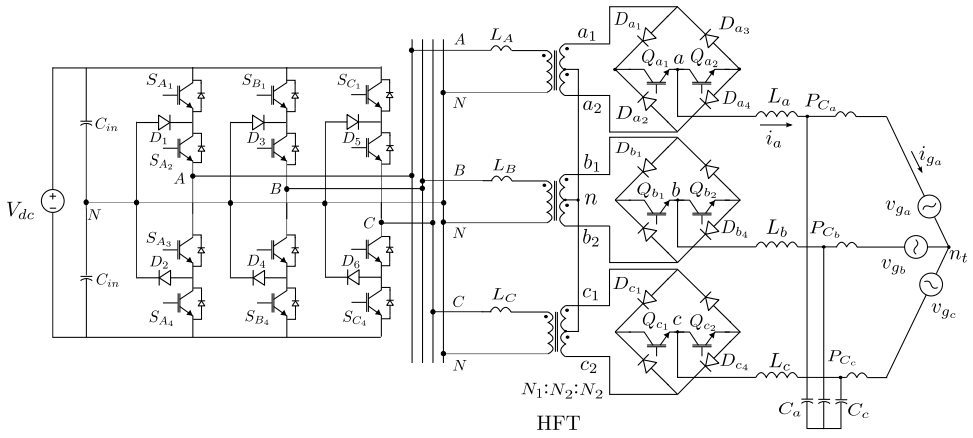


Fig. 1: Proposed three level 3ϕ HF link inverter

A. *Modulation strategy*

The modulation strategy to generate balanced 3ϕ AC voltage at the grid end is similar for all three phases and the modulation is done in primary side high frequency inverter. Here the modulation scheme to generate phase a voltage is discussed in details and is shown in Fig.2. The reference voltage signals $v_{ref_{a,b,c}}$ are in same phase with the line current $i_{a,b,c}$. The a phase voltage reference v_{ref_a} is given as-

$$v_{ref_a}(t) = M|\sin(2\pi f t)| \tag{1}$$

where M and f are peak modulation index and the grid frequency respectively. The voltage reference is compared with an unipolar high frequency ($\frac{1}{T_S}$) triangular carrier to generate the PWM signal P.

$$P(t) = \begin{cases} 1, & v_{ref_a} \geq v_{carrier} \\ 0, & otherwise \end{cases} \tag{2}$$

A high frequency ($\frac{1}{2T_S}$) square wave signal X is used to generate the gating signals of S_{A_1,A_4}. For k^{th} switching cycle $X(t)$ is defined as-

$$X(t) = \begin{cases} 1, & 2(k-1)T_S \leq t \leq (2k-1)T_S \\ 0, & (2k-1)T_S \leq t \leq 2kT_S \end{cases} \tag{3}$$

The gating signals of S_{A_1,A_4} are given as-

$$G_{S_{A_1}} = P \bullet X \tag{4}$$

$$G_{S_{A_4}} = P \bullet \overline{X} \tag{5}$$

S_{A_2} and S_{A_3} are turned ON with S_{A_1} and S_{A_4} respectively. But S_{A_2} is turned OFF when S_{A_4} is gated ON. Similarly, S_{A_3} is turned OFF when the gating signal at S_{A_1} is applied. The described switching scheme applies a PWM high frequency ($\frac{1}{2T_S}$) square wave voltage across the transformer primary v_{AN} as shown in Fig. 2a. The applied voltage ensures the flux balance of the transformer over a period of $2T_S$. The applied voltage at the transformer primary has three levels- $+\frac{V_{dc}}{2}$, zero and $-\frac{V_{dc}}{2}$. Active power transfer happens during non zero state. The secondary side diode bridge $D_{a_1} - D_{a_4}$ rectifies the high frequency AC to get the PWM line frequency AC v_{an} as shown in Fig. 2a. The switches Q_{a_1} and Q_{a_2} are line frequency switched (see Fig.

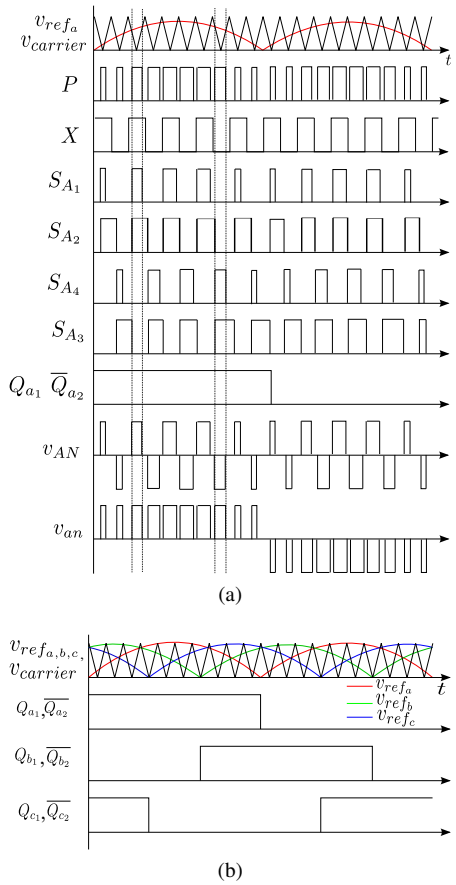


Fig. 2: Modulation strategy- (a) switching scheme of primary side converter for phase a shown in a line frequency cycle, (b) carrier, reference waveforms and gating signals of secondary side switches.

2b) and are turned on based on the direction of the line current i_a. The average PWM line frequency AC output v_{an} is expressed as-

$$\overline{v}_{an}(t) = T_r M V_{dc} \sin(2\pi f t) \tag{6}$$

where, $T_r = \dfrac{N_2}{N_1}$ is turns ratio of the HFT.

B. Soft-switching strategy of the primary side high frequency inverter

The secondary side switches Q_{a_1,a_2}, Q_{b_1,b_2}, Q_{c_1,c_2} are line frequency switched, resulting negligible switching losses. The primary side high frequency inverter is soft-switched over most part of the line frequency cycle. The line frequency currents $i_{a,b,c}$ are inductive and are slowly varying quantities. Properly filtered line currents can be modelled as a constant current source $I_{a,b,c}$ in one switching frequency cycle. Soft-switching of the primary side converter is achieved using transformer leakage inductance and device parasitic capacitance. The soft-switching strategy is similar for all the three phases and independent of the polarity of the line currents $i_{a,b,c}$. The switching strategy of phase a is discussed in detail when the line current i_a is positive and Q_{a_1} is conducting. The commutation process described here shows the reversal of transformer primary current polarity from positive to negative. Negative to positive transition of the transformer current follows the similar switching sequence with other symmetrical switches. The commutation process and the switching waveforms are shown in Fig. 3 and Fig. 4 respectively.

1) Mode 1: (Fig. 3a, $t < t_0$): In primary side the switches S_{A_1}, S_{A_2} are conducting and a positive voltage $\frac{V_{dc}}{2}$ is applied across the transformer primary winding AN. The polarity of the transformer primary current i_{p_a} is positive. In secondary side, the diode D_{a_1} and the switch Q_{a_1} are conducting. The power transfer is happening from DC to AC side. The primary and secondary side switch currents are $i_{p_a} = T_r I_a$ and $i_{D_{a_1}} = I_a$ respectively. Considering equal device capacitances, the voltage across the devices S_{A_3,A_4} are $\frac{V_{dc}}{2}$. The voltage across the diodes $D_{1,2}$ are $\frac{V_{dc}}{2}$ and zero respectively.

2) Mode 2: (Fig. 3b, $t_0 < t < t_1$): At $t = t_0$ the switch S_{A_1} is turned OFF. Considering the device capacitance, the voltage across the device can not change instantly. So, the turn OFF of S_{A_1} is considered as soft (zero voltage) turn OFF. In this interval the primary current i_{p_a} does not change and is same as in last interval. i_{p_a} starts charging the device capacitance of S_{A_1} and discharging the capacitances of S_{A_3,A_4}. The device capacitances of S_{A_1,A_2,A_3,A_4} are denoted as $C_{1,2,3,4}$ respectively. The governing circuit equations are given as-

$$v_{C_1} + v_{C_3} + v_{C_4} = V_{dc} \tag{7}$$

where v_{C_1,C_3,C_4} are the voltages across the devices S_{A_1,A_3,A_4}.

$$C_1 \frac{dv_{C_1}}{dt} = C_3 \frac{dv_{C_3}}{dt} + i_{p_a} \tag{8}$$

$$C_3 \frac{dv_{C_3}}{dt} = C_4 \frac{dv_{C_4}}{dt} \tag{9}$$

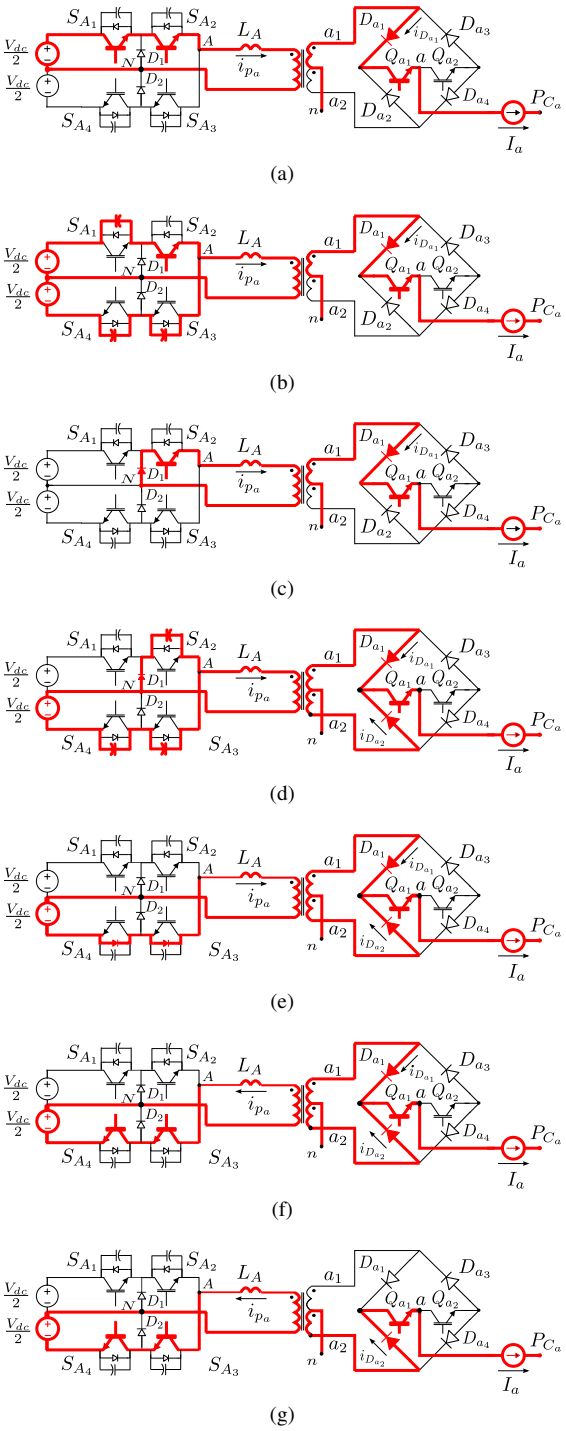


Fig. 3: Commutation process- (a) $t < t_0$, (b) $t_0 < t < t_1$, (c) $t_1 < t < t_2$, (d) $t_2 < t < t_3$, (e) $t_3 < t < t_4$, (f) $t_4 < t < t_5$, (g) $t > t_5$.

Using equations (7)- (9), the voltage across the devices are expressed as-

$$v_{C_1}(t) = \frac{T_r I_a}{C_{eq1}} \cdot (t - t_0) \tag{10}$$

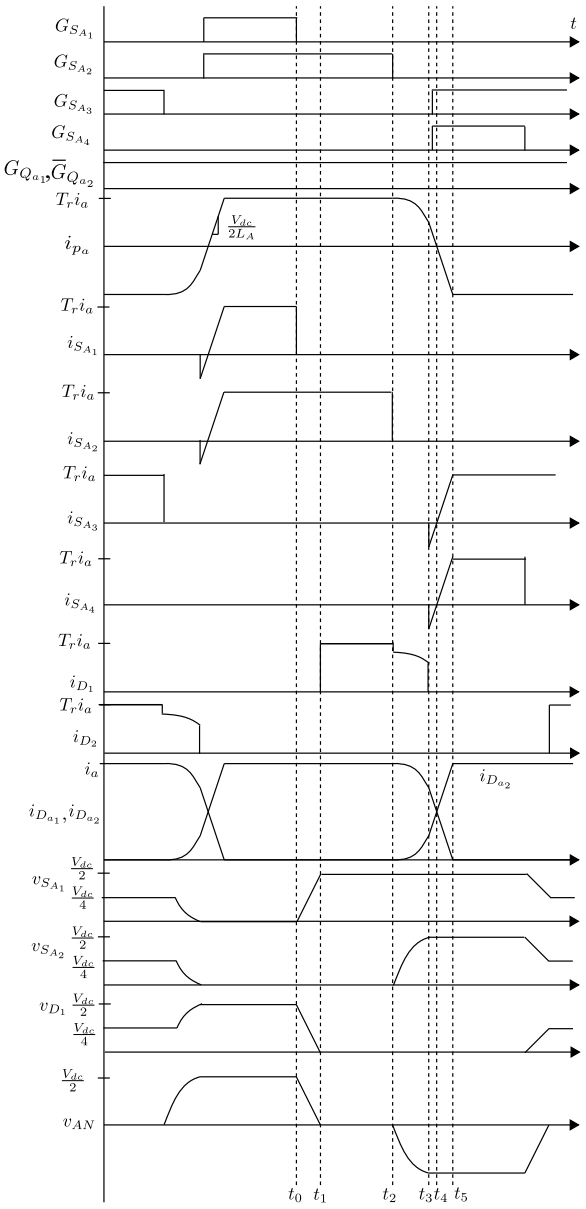


Fig. 4: Switching waveforms illustrating soft-switching operation

Where, C_{eq1} is expressed as $\left(\frac{C_1C_3 + C_1C_4 + C_3C_4}{C_3 + C_4}\right)$.

$$v_{C_3}(t) = \frac{V_{dc}}{2} - \left(\frac{C_4}{(C_3 + C_4)} \cdot \frac{T_r I_a}{C_{eq1}} \cdot (t - t_0)\right) \quad (11)$$

$$v_{C_4}(t) = \frac{V_{dc}}{2} - \left(\frac{C_3}{(C_3 + C_4)} \cdot \frac{T_r I_a}{C_{eq1}} \cdot (t - t_0)\right) \quad (12)$$

$$v_{D_1}(t) = \frac{V_{dc}}{2} - \frac{T_r I_a}{C_{eq1}} \cdot (t - t_0) \quad (13)$$

$$v_{D_2}(t) = \frac{C_3}{(C_3 + C_4)} \cdot \frac{T_r I_a}{C_{eq1}} \cdot (t - t_0) \quad (14)$$

At $t = t_1$, v_{C_1} is charged to $\frac{V_{dc}}{2}$. The time t_1 is given as

$$t_1 = t_0 + \frac{C_{eq1}}{T_r I_a} \frac{V_{dc}}{2} \quad (15)$$

At t_1 the voltages across $S_{A_{3,A_4}}$ are-

$$v_{C_3}(t_1) = \frac{C_4}{C_3 + C_4} \frac{V_{dc}}{2} \quad (16)$$

$$v_{C_4}(t_1) = \frac{C_3}{C_3 + C_4} \frac{V_{dc}}{2} \quad (17)$$

Considering similar rating devices, the device capacitances are nearly equal or in the same order of magnitude. The device capacitances: $C_1 \simeq C_2 \simeq C_3 \simeq C_4 \simeq C$. The device voltages are given as- $v_{C_1}(t_1) = \frac{V_{dc}}{2}$, $v_{C_3}(t_1) = v_{C_4}(t_1) = v_{D_2}(t_1) = \frac{V_{dc}}{4}$ and $v_{D_1}(t_1) = 0$

3) Mode 3: (Fig. 3c, $t_1 < t < t_2$): At $t = t_1$ the diode D_1 is forward biased. The switch S_{A_2} and the diode D_1 carry the primary current i_{p_a}. This applies a zero voltage across the transformer primary. There is no active power flow from DC to AC side during this interval. The secondary side current flows through D_{a_1} and Q_{a_1}. At the end of this interval S_{A_2} is turned OFF. The capacitance across S_{A_2} ensures zero voltage turn OFF of S_{A_2} as the voltage across the capacitor can not change instantaneously.

4) Mode 4: (Fig. 3d, $t_2 < t < t_3$): At the beginning of this interval the primary current i_{p_a} starts falling and it starts charging the device capacitance of S_{A_2} and discharging the capacitances of $S_{A_{3,A_4}}$. A negative voltage is applied across the transformer primary AN. For this reason the secondary diode D_{a_2} is forward biased. The governing circuit equations are given as-

$$i_{D_{a_1}} + i_{D_{a_2}} = I_a \quad (18)$$

$$i_{p_a} = T_r(i_{D_{a_1}} - i_{D_{a_2}}) \quad (19)$$

$$C_2 \frac{dv_{C_2}}{dt} = C_3 \frac{dv_{C_3}}{dt} + i_{p_a} \quad (20)$$

$$\frac{dv_{C_2}}{dt} = -(\frac{dv_{C_3}}{dt} + \frac{dv_{C_4}}{dt}) \quad (21)$$

$$C_3 \frac{dv_{C_3}}{dt} = C_4 \frac{dv_{C_4}}{dt} \quad (22)$$

$$v_{C_2} + L_A \frac{di_{p_a}}{dt} = 0 \quad (23)$$

where L_A is leakage inductance of the HFT seen from primary. Using equations (18)-(23) device voltages and currents are expressed as-

$$i_{p_a}(t) = T_r I_a \cos \frac{t}{\sqrt{L_A C_{eq2}}} \quad (24)$$

$$v_{C_2}(t) = T_r I_a \sqrt{\frac{L_A}{C_{eq2}}} \sin \frac{t}{\sqrt{L_A C_{eq2}}} \quad (25)$$

$$v_{C_3}(t) = v_{C_3}(t_2) - \frac{C_4 \cdot T_r I_a}{C_3 + C_4} \sqrt{\frac{L_A}{C_{eq2}}} \sin \frac{t}{\sqrt{L_A C_{eq2}}} \quad (26)$$

$$v_{C_4}(t) = v_{C_4}(t_2) - \frac{C_3 \cdot T_r I_a}{C_3 + C_4} \sqrt{\frac{L_A}{C_{eq2}}} \sin \frac{t}{\sqrt{L_A C_{eq2}}} \quad (27)$$

$$v_{D_2}(t) = \frac{V_{dc}}{4} + \frac{C_3 \cdot T_r I_a}{C_3 + C_4}\sqrt{\frac{L_A}{C_{eq2}}}\sin\frac{t}{\sqrt{L_A C_{eq2}}} \quad (28)$$

$$i_{D_{a_1}}(t) = \frac{I_a}{2}\left(1 + \cos\frac{t}{\sqrt{L_A C_{eq2}}}\right) \quad (29)$$

$$i_{D_{a_2}}(t) = \frac{I_a}{2}\left(1 - \cos\frac{t}{\sqrt{L_A C_{eq2}}}\right) \quad (30)$$

where C_{eq2} is given as $\frac{C_2C_3 + C_2C_4 + C_3C_4}{C_3 + C_4}$. Considering equal device capacitances, at $t = t_3$, v_{C_3} and v_{C_4} become zero and C_2 charges to $\frac{V_{dc}}{2}$.

5) Mode 5: (Fig. 3e, $t_3 < t < t_4$): v_{C_3} and v_{C_4} can not become negative due to anti parallel diodes of the devices. In this interval the anti parallel diodes of S_{A_3,A_4} are conducting the primary current. A negative voltage $-\frac{V_{dc}}{2}$ across the transformer primary causes the primary current to fall linearly. The primary current i_{p_a} can be expressed as-

$$i_{p_a}(t) = i_{p_a}(t_3) - \frac{V_{dc}}{2L_A}(t - t_3) \quad (31)$$

The secondary diode currents are given as-

$$i_{D_{a_1}}(t) = \frac{I_a}{2} + \frac{i_{p_a}(t_3)}{2T_r} - \frac{V_{dc}}{2T_r L_A}(t - t_3) \quad (32)$$

$$i_{D_{a_2}}(t) = \frac{I_a}{2} - \frac{i_{p_a}(t_3)}{2T_r} + \frac{V_{dc}}{2T_r L_A}(t - t_3) \quad (33)$$

S_{A_3,A_4} are turned ON during this interval to achieve zero current zero voltage switching (ZCZVS) as anti-parallel diodes are conducting. At $t = t_4$, i_{p_a} becomes zero and the secondary side current $i_{D_{a_1}} = i_{D_{a_2}}$. Conditions to achieve ZVS of S_{A_3,A_4} are given as-

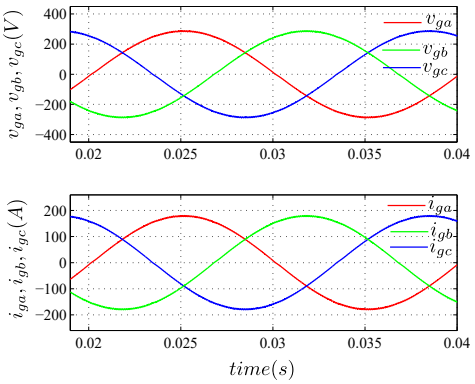
$$I_a > \frac{V_{dc}}{2T_r}\sqrt{\frac{C_{eq2}}{L_A}} \quad (34)$$

$$(t_3 - t_2) < DT < (t_4 - t_2) \quad (35)$$

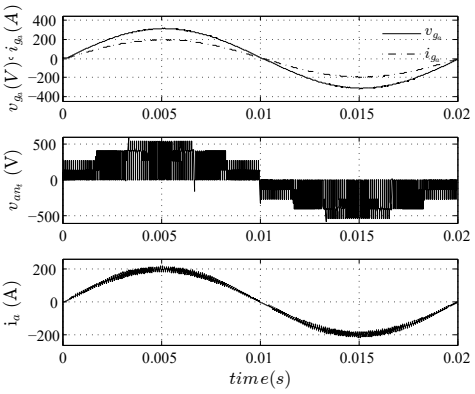
where, DT is the dead time between S_{A_2} and S_{A_3,A_4}.

6) Mode 6: (Fig. 3f, $t_4 < t < t_5$): In this interval switches S_{A_3,A_4} start conducting and the primary current is negative. The primary and secondary currents keep changing with the same slopes as in last interval. At $t = t_5$, the primary current has reached steady state value $-T_r I_a$ and the diode currents are $i_{D_{a_1}} = 0$, $i_{D_{a_2}} = I_a$.

7) Mode 7: (Fig. 3g, $t > t_5$): In primary side, S_{A_3,A_4} and in secondary side D_{a_2}, Q_{a_1} are conducting. A negative voltage is applied across the transformer primary and the transformer primary current polarity is also negative. So, active power is flowing from DC to AC side. This is a similar switching state like Mode 1.



(a)



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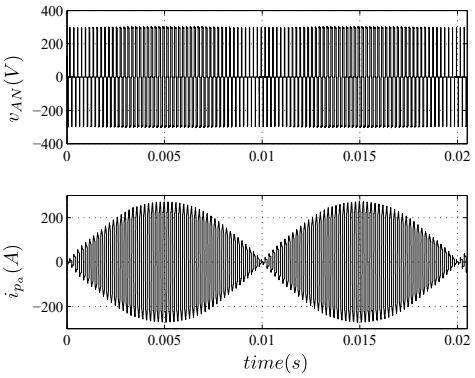

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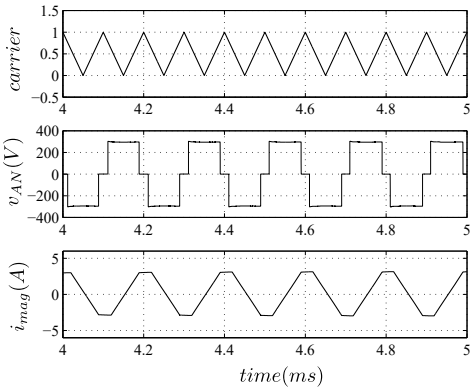

(d)

Fig. 5: Simulated waveforms- (a) 3ϕ grid voltage and current, (b) Converter output voltage and current of phase a, (c) Primary voltage and current of HFT, (d) flux balance of HFT in high frequency switching cycles.

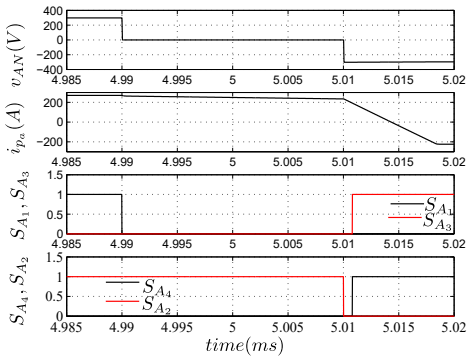

Fig. 6: Simulated soft-switching waveforms.

TABLE I: Simulation Parameters

Parameter	Value
Input DC bus voltage (V_{dc})	600 V
Peak modulation index (M)	0.8
Grid voltage per phase $v_{g_a}(RMS)$	230 V
Grid frequency (f)	50 Hz
Output power (P_a)	100 kW
Carrier frequency ($\frac{1}{T_S}$)	10 kHz
Transformer turns ratio ($N_1 : N_2$)	$25 : 34$
Filter inductance (0.5 p.u at 50 Hz)	$255\mu H$
Leakage inductance of HFT (0.5 p.u at 5 kHz)	$5.5\mu H$
Device parasitic capacitance	$10nF$
Dead time of HF inverter	$1\mu S$

III. Simulation Results

The proposed converter is simulated in MATLAB simulink with 600 V DC bus and 400 V, 50 Hz grid supplying 100 kW power. The simulation results are verified with the theoretical analysis. The simulation parameters are shown in Table I. Balanced 3ϕ output voltage and current waveforms of the inverter at grid end are shown in Fig. 5a. The converter supplies the output power at unity power factor. The a phase output voltage (v_{an_t}) and current (i_a) waveforms of the converter before the filter inductor are shown in Fig. 5b. i_a contains high frequency switching ripples and it is also in phase with the fundamental component of (v_{an_t}). The HFT primary voltage (v_{AN}) and current (i_{p_a}) waveforms are shown in Fig. 5c. The applied primary voltage (v_{AN}) has three states- $\pm$300V and zero. The primary current (i_{p_a}) does not contain any DC component. Fig. 5d shows the flux balance of the HFT in a switching cycle. i_{mag} is magnetising current of the HFT. Net volt-second over a switching cycle ($2T_S$) is zero. Transition of v_{AN} from +300V to -300 V through zero is shown in Fig. 6. The turn OFF of S_{A_1} and S_{A_2} are soft considering the device capacitances. Where as zero voltage turn ON of S_{A_3} and S_{A_4} are ensured as the body diodes of the corresponding switches are conducting when the gating signals are applied.

IV. Conclusion

A novel three phase three level high frequency link soft-switched unidirectional inverter is proposed for grid connected systems. The proposed topology has following features: (a) primary side HF inverter has similar structure of diode clamped three level converter, (b) single stage with unidirectional power flow, (c) galvanic isolation using compact and high power density high frequency transformer which reduces the overall size of the system, (d) partially soft-switched primary side HF inverter improves the converter efficiency, (e) line frequency switched secondary side converter reduces the converter switching loss. The modulation strategy and soft-switching principle are discussed in details. The simulation waveforms verify the theoretical analysis. The proposed converter can be popular for low power applications like- power electronic interface of rooftop solar or residential fuel cell with high system efficiency. This topology can also be a promising solution for high power application like direct integration of renewable energy sources (utility scale PV) with medium voltage AC grid as high voltage blocking and inherently slow semiconductor devices can be used in the secondary side line frequency switched converter.

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