# A Unidirectional Snubber Less Partially Soft-switched High Frequency Link Three Phase Inverter 

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#### Abstract

This paper presents a unidirectional three phase inverter with a high frequency link. This topology can be used for the grid integration of renewable energy sources like photovoltaic, fuel cell etc, where power flow is unidirectional. The use of high frequency transformer (HFT) results in reduction of cost with improved power density. The switches in the proposed converter are either zero voltage switched or switched only at line frequency leading to negligible switching loss. Use of additional snubber circuits are also avoided for commutation of leakage energy of the HFT. The proposed converter with small shunt active filter ensures unity power factor operation. The operation of the proposed converter is analysed in detail. Key simulation results are shown to demonstrate the effectiveness of the proposed topology.


Index Terms- SPWM inverter, high frequency link, phase shifted full bridge, soft-switching, reactive compensation, grid integration.

## I. Introduction

In recent years, issues like stringent restriction on green house gas emission, depletion of fossil fuel and concern of energy security for sustainable development are the main drives behind electricity generation using renewable energy sources. Among various available renewable energy sources solar/ photovoltaic (PV) is proven to be very promising by so far. According to the report of SolarPower Europe [1], world wide cumulative solar installed capacity is 178 GW till the end of 2014. The electric power grid all over the world is experiencing major integration of utility scale photovoltaic sources. Currently a hard switched three phase voltage source inverter (several of them in parallel) with a line frequency transformer (LFT) connects solar PV to grid. The LFT is required for voltage magnification, to ensure safety and to stop leakage current. It is also one of the most expensive and largest component in the system. An alternative approach is high frequency link inverter based grid integration. In literature, the HF transformer based inverters are broadly classified as: multi-stage and single stage. Multi-stage topology uses intermediate bulky DC link capacitor [2] between isolated DC-DC and DC to line frequency AC stage, facing long term reliability issues. The primary side HF inverter is usually hard switched and the grid/load side inverter is sine triangle pulse width (SPWM) modulated. Additional active or passive snubber circuit is required to commute the leakage energy of the HFT. The single stage high frequency link (HFL) inverter can be classified as: rectifier type HFL (RHFL) and cyclo-converter type HFL (CHFL). The RHFL topology [3]-[5] is similar
to multi-stage topology except the intermediate stage DC link filter. The CHFL topology [6]-[8] uses AC to AC cyclo-converter in the secondary of the HFL. Modulation strategies with additional snubber circuit are employed for soft switching of RHFL and CHFL topology. In [9] a source based commutation technique is used to eliminate the additional snubber circuit. In [10] a primary side push-pull based soft switched HF link inverter is proposed which uses the leakage energy of the HFT for soft switching. Generally, the grid side converter of a single stage HF link inverter is high frequency switched. In [11], [12] a modulation strategy is used for two third reduction of high frequency switching of the grid/load side inverter.

This paper presents a novel high frequency link (HFL) three phase inverter as shown in Fig. 1. The proposed topology with suggested control scheme has the following advantages - (i) soft-switching of the primary side converter (PC), (ii) line frequency switched secondary side converter (SC), so no switching loss and for high voltage grid integration this implies possible implementation with low frequency high voltage switches, (iii) reduced size and cost due to HFT and (iv) a shunt compensator with much lower power rating ( $4.5 \%$ ) ensures unity power factor operation. This paper is organised as follows. Section II presents the steady state operation and analysis of the converter. The key simulation results are shown in Section III.

## II. Steady State Operation and Analysis

This section presents the steady state operation of the proposed converter. The analysis is divided into three subsections-(a) Generation of three phase PWM line frequency AC, (b) Soft switching technique of the primary side high frequency converter and (c) Reactive power compensation scheme.

## A. Modulation Strategy

The switching strategy for the generation of PWM AC voltages at the grid end is similar for all three phases. What follows is a detail description of the modulation strategy for the generation of $a$ phase voltage. The modulation scheme is shown in Fig. 2 and 3. Switches $S_{A_{1}}-S_{A_{4}}$ in Fig. 1 are modulated to generate high frequency $\frac{1}{2 T_{s}}$ PWM square wave. The resulting voltage waveform across the transformer primary $v_{A_{1} A_{2}}$ can be seen in Fig. 2b. This high frequency inversion results in flux ( $\phi$ ) balance over a period of $2 T_{s}$ (see Fig. 3). The secondary side diode bridge


Fig. 1: Proposed grid connected 3-phase HF link inverter


Fig. 2: Switching scheme (a) grid side inverter (b) over all scheme for phase $a$
$D_{a_{1}}-D_{a_{4}}$ rectifies the high frequency AC. The switches $Q_{a_{1}}$ and $Q_{a_{2}}$ are line frequency switched and turned on based on the direction of $i_{a}(t)$ (see Fig. 2b). This results in the generation of a line frequency PWM AC voltage waveform, $v_{a N}$.


Fig. 3: Modulation scheme of primary side HF inverter

The switches $S_{A_{1}}$ and $S_{A_{2}}$ are complementary switched. For $k^{t h}$ switching cycle, the gating signal of $S_{A_{1}}$ can be given as-

$$
G_{S_{A_{1}}}= \begin{cases}1, & 2(k-1) T_{S} \leq t \leq(2 k-1) T_{S}  \tag{1}\\ 0, & (2 k-1) T_{S} \leq t \leq 2 k T_{S}\end{cases}
$$

The controller given reference signal is in phase with the line current waveform $i_{a}(t)$. Modulus of reference signal, $d_{a}(t)$ is used to generate the gating signal of switches $S_{A_{3}}$ and $S_{A_{4}}$. $d_{a}(t)$ is expressed as-

$$
\begin{equation*}
d_{a}(t)=|M \cdot \sin (2 \pi f t)| \tag{2}
\end{equation*}
$$

where, $M$ is the peak modulation index and $f$ is the grid frequency. $d_{a}(t)$ is compared with a unipolar saw tooth
carrier $C$ to generate an intermediate signal $X$.

$$
X(t)= \begin{cases}1, & d_{a}(t) \geq C(t)  \tag{3}\\ 0, & \text { otherwise }\end{cases}
$$

$S_{A_{3}}$ and $S_{A_{4}}$ are complementary switched. The gating signal of $S_{A_{3}}$ is derived as-

$$
\begin{equation*}
G_{S_{A_{3}}}=G_{S_{A_{1}}} \oplus X \tag{4}
\end{equation*}
$$

The average secondary side rectified PWM voltage over one switching cycle is expressed as-

$$
\begin{equation*}
\bar{v}_{R_{a_{1,2}} N}(t)=\frac{n V_{d c} d_{a}(t) T_{S}}{T_{S}}=n M V_{d c}|\sin (2 \pi f t)| \tag{5}
\end{equation*}
$$

where $n=\frac{N_{2}}{N_{1}}$ is turns ratio of the HFT. These rectified PWM pulses are line frequency inverted by $Q_{a_{1}, a_{2}}$ to generate PWM AC voltage $v_{a N}$. The average line frequency component of $v_{a N}$ is expressed as-

$$
\begin{equation*}
\bar{v}_{a N}=n M V_{d c} \sin (2 \pi f t) \tag{6}
\end{equation*}
$$

## B. Soft-switching scheme of the primary side HF inverters

Secondary side devices $Q_{a_{1}, a_{2}}, Q_{b_{1}, b_{2}}$ and $Q_{c_{1}, c_{2}}$ are switched at line frequency (in Fig. 2a) resulting in negligible switching loss. The primary side switches are soft switched for most part of the line current considering the leakage inductance of the HFT and the parasitic capacitance across the switches in the primary side converter. As the softswitching mechanism is similar in all three phases, detailed description of the process is given for phase $a$. Depending on the direction of the line current $i_{a}$, there are two cases. The case when $i_{a}$ is positive and $Q_{a_{1}}$ is on, is described in details. The soft-switching mechanism is similar when $i_{a}$ is negative. The slowly varying line current $i_{a}$ is modelled as constant current source in a switching cycle $\left(\frac{1}{2 T_{S}}\right)$. Over one flux balance cycle of period $2 T_{s}$ (see Fig 3) it can be seen that, the primary voltage $v_{A_{1} A_{2}}$ has three levels: positive, negative and zero. Power transfer happens during the active states when $v_{A_{1} A_{2}}$ is non zero. The switching transitions of primary side HF inverters can be classified in two types active state to zero state and zero state to active state. The detailed switching waveform is shown in Fig. 4. The circuit configuration of different modes of operation between two consecutive power transfer stages over a flux balance cycle (with positive $v_{A_{1} A_{2}}$ in Fig. 5a to negative $v_{A_{1} A_{2}}$ in Fig. 5 g ) is given in Fig. 5. Applying KCL at the HFT winding-

$$
\begin{align*}
i_{p_{a}} & =n\left(i_{D_{a_{1}}}-i_{D_{a_{2}}}\right)  \tag{7}\\
i_{a} & =\left(i_{D_{a_{1}}}+i_{D_{a_{2}}}\right) \tag{8}
\end{align*}
$$

1) Active to zero transition: The switches $S_{A_{3}}$ and $S_{A_{4}}$ are switched during this transition. The transition from $S_{A_{4}}$ to $S_{A_{3}}$ is similar with the transition from $S_{A_{3}}$ to $S_{A_{4}}$ except the direction of the HFT primary current. Hence, $S_{A_{4}}$ to $S_{A_{3}}$ transition is discussed in detail.


Fig. 4: Switching waveforms illustrating ZVS operation of HF inverter
a) Sub-interval: (see Fig. $5 b, t_{0}<t<t_{1}$ ): Before the beginning of this interval ( $t<t_{0}$ ) a positive voltage was applied at the HFT primary $A_{1} A_{2}$. $S_{A_{1}}$ and $S_{A_{4}}$ were conducting (see Fig. 5a). At $t=t_{0}, S_{A_{4}}$ is turned OFF. As the voltage across $S_{A_{4}}$ can not change immediately due to device parasitic capacitance, this is a zero voltage soft turn OFF. The circuit conditions at $t=t_{0}$ are given as: $v_{S_{A_{3}}}\left(t_{0}\right)=V_{d c}, v_{S_{A_{4}}}\left(t_{0}\right)=0, v_{A_{1} B_{1}}\left(t_{0}\right)=V_{d c}$, $v_{L_{A}}\left(t_{0}\right)=0, i_{p_{a}}\left(t_{0}\right)=n i_{a}, i_{D_{a_{1}}}\left(t_{0}\right)=i_{a}, i_{D_{a_{2}}}\left(t_{0}\right)=0$. During this interval the primary current of the HFT is remain same as before (see Fig. 4) as the applied voltage across the HFT leakage inductance $\left(L_{A}\right)$ is zero. The primary current ( $i_{p_{a}}$ ) starts charging the device parasitic capacitance of $S_{A_{4}}$ and discharge the capacitance of $S_{A_{3}}$ (see Fig.5b). Circuit equations are given as-

$$
\begin{equation*}
-C_{3} \frac{d v_{c_{3}}(t)}{d t}+C_{4} \frac{d v_{c_{4}}(t)}{d t}=i_{p_{a}}(t) \tag{9}
\end{equation*}
$$


(a)

(b)

(c)

(d)

(e)

(f)

(g)

Fig. 5: Circuit diagram during- (a) $t<t_{0}$ (b) $t_{0}<t<t_{1}$ (c) $t_{1}<t<t_{2}$ (d) $t_{2}<t<t_{3}$ (e) $t_{3}<t<t_{4}$ (f) $t_{4}<t<t_{5}$ (g) $t>t_{5}$
where $C_{3}$ and $C_{4}$ are the device parasitic capacitances of $S_{A_{3}}$ and $S_{A_{4}}$ respectively.

$$
\begin{equation*}
v_{c_{3}}(t)+v_{c_{4}}(t)=V_{d c} \tag{10}
\end{equation*}
$$

Solving equations (9) and (10) it can be shown that the capacitor voltage ( $v_{C_{3}}$ ) falls linearly with a slope $\frac{n i_{a}}{C_{3}+C_{4}}$ and $v_{C_{3}}$ is given by-

$$
\begin{equation*}
v_{c_{3}}(t)=-n i_{a} \frac{t}{C_{3}+C_{4}}+V_{d c} \tag{11}
\end{equation*}
$$

At $t=t_{1}, C_{3}$ discharges to zero. Due to diode $D_{3}$ the capacitor voltage can not be negative. $D_{3}$ is forward biased and starts conducting. To achieve ZVS of the switch $S_{A_{3}}$, gating pulse is applied after $t_{1}$, when the diode $D_{3}$ is conducting. So, the dead time between the gating signals of $S_{A_{3}}$ and $S_{A_{4}}$ should be greater than $\left(t_{1}-t_{0}\right)$ where $\left(t_{1}-t_{0}\right)$ can be expressed as-

$$
\begin{equation*}
t_{1}-t_{0}=\frac{V_{d c}\left(C_{3}+C_{4}\right)}{n i_{a}} \tag{12}
\end{equation*}
$$

At the end of this interval the switch $S_{A_{1}}$ and the diode $D_{3}$ is free-wheeling the primary current as shown in Fig. 5c. This applies a zero voltage at the HFT primary. The circuit will remain in this state until the switch $S_{A_{1}}$ is turned off at the time instant $t_{2}$.
2) Zero to active transition: In this case the switches $S_{A_{1}}$ and $S_{A_{2}}$ are switched. The circuit equations for these two transitions ( $S_{A_{1}} \leftrightarrows S_{A_{2}}$ ) are similar. Hence, only $S_{A_{1}}$ $\rightarrow S_{A_{2}}$ transition is described in details.
a) Sub-interval: (see Fig. 5d, $t_{2}<t<t_{3}$ ): This interval starts at the instant when the switch $S_{A_{1}}$ is turned OFF at $t_{2}$. This is again a device capacitance assisted zero voltage turn OFF, similarly like $S_{A_{4}}$. At the beginning of this interval the circuit conditions are given as- $v_{S_{A_{1}}}\left(t_{2}\right)=$ $0, v_{S_{A_{2}}}\left(t_{2}\right)=V_{d c}, v_{A_{1} A_{2}}\left(t_{2}\right)=0, v_{L_{A}}\left(t_{2}\right)=0, i_{P_{a}}\left(t_{2}\right)=$ $n i_{a}, i_{D_{a_{1}}}\left(t_{2}\right)=i_{a}, i_{D_{a_{2}}}\left(t_{2}\right)=0$. As a negative voltage is appeared across $A_{1} A_{2}$, the primary current starts falling in this interval (see Fig.4). Applying KCL at node $A_{1}$ in Fig. 5d-

$$
\begin{equation*}
C_{1} \frac{d v_{c_{1}}}{d t}=C_{2} \frac{d v_{c_{2}}}{d t}+i_{p_{a}} \tag{13}
\end{equation*}
$$

where $C_{1}$ and $C_{2}$ are device capacitances of $S_{A_{1}}$ and $S_{A_{2}}$ respectively. Applying KVL,

$$
\begin{gather*}
v_{c_{1}}+v_{c_{2}}=V_{d c}  \tag{14}\\
v_{c_{1}}+v_{L_{A}}=0  \tag{15}\\
v_{L_{A}}=L_{A} \frac{d i_{p_{a}}}{d t} \tag{16}
\end{gather*}
$$

Using equations (13)-(16), the primary current $i_{p_{a}}$ is expressed as-

$$
\begin{equation*}
i_{p_{a}}(t)=n i_{a} \cdot \cos \left(\frac{t}{\sqrt{\left(L_{A}\left(C_{1}+C_{2}\right)\right)}}\right) \tag{17}
\end{equation*}
$$

The capacitor voltage $v_{C_{1}}$ is given as-

$$
\begin{equation*}
v_{C_{1}}(t)=n i_{a} \cdot \sqrt{\frac{L_{A}}{C_{1}+C_{2}}} \cdot \sin \left(\frac{t}{\sqrt{L_{A}\left(C_{1}+C_{2}\right)}}\right) \tag{18}
\end{equation*}
$$

Solving equations (7), (8) and (17), the rectifier diode currents can be expressed as-

$$
\begin{align*}
& i_{D_{a_{1}}}(t)=\frac{i_{a}}{2}+\frac{i_{a}}{2} \cdot \cos \left(\frac{t}{\sqrt{L_{A}\left(C_{1}+C_{2}\right)}}\right)  \tag{19}\\
& i_{D_{a_{2}}}(t)=\frac{i_{a}}{2}-\frac{i_{a}}{2} \cdot \cos \left(\frac{t}{\sqrt{L_{A}\left(C_{1}+C_{2}\right)}}\right) \tag{20}
\end{align*}
$$

At $t=t_{3}, v_{C_{1}}$ is charged to $V_{d c}$ and $v_{C_{2}}$ is discharged to zero. The diode $D_{2}$ starts conducting. The new circuit configuration is shown in Fig. 5e.
b) Sub-interval: (see Fig. 5e, $t_{3}<t<t_{4}$ ): In this interval, the body diodes of $S_{A_{2}}$ and $S_{A_{3}}$ are conducting. So, a negative voltage is applied across the leakage inductance $\left(L_{A}\right)$. The primary current falls linearly. Applying KVL,

$$
\begin{equation*}
L_{A} \cdot \frac{d i_{p_{a}}}{d t}+V_{d c}=0 \tag{21}
\end{equation*}
$$

Solving (21), the primary current is given as-

$$
\begin{equation*}
i_{p_{a}}(t)=-\frac{V_{d c}}{L_{A}}\left(t-t_{3}\right)+i_{p_{a}}\left(t_{3}\right) \tag{22}
\end{equation*}
$$

The rectifier diode currents during this interval can be expressed as-

$$
\begin{align*}
& i_{D_{a_{1}}}(t)=\frac{i_{a}}{2}+\frac{i_{p_{a}}\left(t_{3}\right)}{2 n}-\frac{V_{d c}}{2 n L_{A}}\left(t-t_{3}\right)  \tag{23}\\
& i_{D_{a_{2}}}(t)=\frac{i_{a}}{2}-\frac{i_{p_{a}}\left(t_{3}\right)}{2 n}+\frac{V_{d c}}{2 n L_{A}}\left(t-t_{3}\right) \tag{24}
\end{align*}
$$

The primary current becomes zero at $t_{4}$ and this interval ends.

$$
\begin{equation*}
t_{4}=\frac{L_{A}}{V_{d c}} \cdot i_{p_{a}}\left(t_{3}\right)+t_{3} \tag{25}
\end{equation*}
$$

At $t=t_{4}, i_{D_{a_{1}}}=i_{D_{a_{2}}}=\frac{i_{a}}{2}$. In between $t_{3}<t<t_{4}$ the body diode $D_{2}$ is conducting. To achieve zero voltage turn ON of $S_{A_{2}}$, the gating pulse is applied within this interval. So, the dead time ( $D T_{A_{1,2}}$ ) between the switches $S_{A_{1}}$ and $S_{A_{2}}$ should be-

$$
\begin{equation*}
\left(t_{3}-t_{2}\right)<D T_{A_{1,2}}<\left(t_{4}-t_{2}\right) \tag{26}
\end{equation*}
$$

Again to achieve soft turn ON of $S_{A_{2}}$, stored leakage energy in $L_{A}$ should be sufficient enough to completely discharge the device capacitance $\left(C_{2}\right)$, so that the body diode starts conducting before the gating pulse is applied. Hence, with the given leakage inductance and device capacitances, zero voltage turn ON is not possible at low load current $\left(i_{a}\right)$. From (18) the condition is expressed as-

$$
\begin{equation*}
n i_{a} \cdot \sqrt{\frac{L_{A}}{C_{1}+C_{2}}}>V_{d c} \tag{27}
\end{equation*}
$$

c) Sub-interval: (see Fig. $5 f, t_{4}<t<t_{5}$ ): In this interval, the primary current becomes negative and falls linearly with the same slope $-\frac{V_{d c}}{L_{A}}$. The diode currents $i_{D_{a_{1}}}$ decreases and $i_{D_{a_{2}}}$ increases linearly with the same slope as in the last interval. The devices $S_{A_{2}}$ and $S_{A_{3}}$ are conducting in this interval. At $t=t_{5}$ the primary current reaches $-n i_{a}$ and stays there. The rectifier diode currents are $i_{D_{a_{1}}}\left(t_{5}\right)=0$ and $i_{D_{a_{2}}}\left(t_{5}\right)=i_{a}$. The instant $t_{5}$ is given as-

$$
\begin{equation*}
t_{5}=\frac{L_{A}}{V_{d c}} \cdot\left(n i_{a}\right)+t_{4} \tag{28}
\end{equation*}
$$

Zero to active transition ends at $t_{5}$. Then $\left(t>t_{5}\right)$ the inverter is again in an active state as shown in Fig. 5g.

## C. Reactive power compensation

The proposed three phase inverter is unidirectional and the modulation strategy requires unity power factor operation of the grid side converter. Hence, the reactive drop due to line and filter reactance is compensated by a shunt compensator (a $3 \phi$ VSI) at the grid end as in Fig. 1. As this inverter will only meet the reactive power demand by the line reactance, the size of the line frequency transformer (LFT) as well as the inverter is small.

The reactive power supplied by the shunt compensator are estimated as follows. The equivalent circuit diagram is shown in Fig. 6a. The phasor diagram is shown in Fig. 6b.


Fig. 6: (a) Reactive power compensation scheme (b) Phasor diagram

The active power drawn by the grid at UPF is given as-

$$
\begin{equation*}
P=3 V_{g_{a}} I_{g_{a}} \tag{29}
\end{equation*}
$$

where $V_{g_{a}}$ and $I_{g_{a}}$ are rms line to neutral voltage and rms current of the grid respectively. The active power supplied by the converter-

$$
\begin{equation*}
3 V_{a n_{t}} I_{a}=P \tag{30}
\end{equation*}
$$

where $V_{a n_{t}}$ and $I_{a}$ are the rms value of the line frequency component of converter output voltage and current respectively. From the phasor diagram-

$$
\begin{equation*}
V_{a n_{t}}=V_{g_{a}}+j\left(2 \pi f L_{a}\right) I_{g_{a}} \tag{31}
\end{equation*}
$$

where $L_{a}$ is combined line and filter inductance. For simplicity of computation, say $V_{g_{a}}=1$ p.u. and $I_{g_{a}}=1$ p.u.. Then the active power requirement by the grid is $P=3$ p.u.. The line inductive reactance is considered 0.05 p.u. Using equations (29)-(31) following quantities are estimated- $V_{a n_{t}}=0.9987$ p.u., $I_{a}=1.001$ p.u. and $I_{s h_{a}}=0.045$ p.u., where $I_{s h_{a}}$ is the rms current supplied by

TABLE I: Simulation Parameters

| Parameter | Value |
| :---: | :---: |
| $V_{d c}(V)$ | 600 |
| $v_{\text {grid }}(V)(L-L)$ | 400 |
| $f_{\text {grid }}(H z)$ | 50 |
| HF inverter switching frequency | 5 kHz |
| Power $(\mathrm{kW})$ | 100 |
| peak modulation index $(M)$ | 0.8 |
| HFT turns ratio | $25: 16$ |
| Line impedance (at 50 Hz) | $0.5 \mathrm{p} . \mathrm{u}(25.5 \mu H)$ |
| HFT leakage impedance (at 5kHz) | $0.5 \mathrm{p} . \mathrm{u}(5.5 \mu H)$ |
| Capacitance across the primary switches | 40 nF |
| Dead time of HF inverter | $1 \mu \mathrm{~S}$ |

the shunt compensator. So the total reactive power supplied by the shunt compensator- $Q_{c o m p}=3 V_{g_{a}} I_{s h_{a}}=0.135 \mathrm{p} . \mathrm{u}$ or $4.5 \%$ of the total power rating of the converter.

## III. Simulation Results

The proposed HF link inverter with the shunt compensator is simulated in MATLAB simulink with 600 V DC bus and $400 \mathrm{~V}, 50 \mathrm{~Hz}$ grid supplying 100 kW power. The simulation parameters are presented in table I. Simulated $3 \phi$ grid voltages and grid currents are shown in Fig. 7a. The grid voltages and currents are balanced and power is injected at unity power factor. The peak value of grid phase voltage and grid currents are- 320 V and 198A respectively. The PWM output voltage $\left(v_{a n_{t}}\right)$ and the current $\left(i_{a}\right)$ of phase $a$ of the converter are shown in Fig. 7b. The fundamental component of the output voltage and the current of the converter are also in same phase. $i_{a}$ contains switching frequency ripples. The fundamental component of converter output voltage $\left(v_{a n_{t}}\right)$ leads the grid voltage ( $v_{g_{a}}$ ) by a small angle. The converter output voltage w.r.t HFT neutral ( $v_{a N}$ ) and grid neutral $\left(v_{a n_{t}}\right)$ point are shown in Fig. 7c. The PWM high frequency AC applied at primary of the HFT $v_{A_{1} A_{2}}$ and the primary current $i_{P_{a}}$ of phase $a$ is shown in Fig. 7d. Flux balance waveform of the HFT is shown in Fig. 7e. The average value of primary voltage and magnetising current $\left(i_{m a g}\right)$ over one switching cycle are zero. With the leakage inductance and the device capacitance considered in this simulation, the soft-switching of the HF inverter is achieved for the following range of load current angle ( $w t$ ): $\frac{\pi}{6} \leq w t \leq \frac{5 \pi}{6}$ and $\frac{7 \pi}{6} \leq w t \leq \frac{11 \pi}{6}$, where $w=2 \pi f$ and $f$ is the grid frequency. The transition from $S_{A_{4}}$ to $S_{A_{3}}$ and $S_{A_{1}}$ to $S_{A_{2}}$ is shown in Fig. 7f. The gating pulse of $S_{A_{3}}$ is applied when the device capacitance is completely discharged and the body diode of $S_{A_{3}}$ is conducting. $S_{A_{2}}$ is turned ON when $i_{P_{a}}$ is negative and the body diode of $S_{A_{2}}$ is conducting (follow the red mark). This validates the theoretical analysis of soft switching of primary side HF inverter.

## IV. CONCLUSION

In this paper, a three phase high frequency link softswitched unidirectional single stage inverter is proposed for grid connected photovoltaic system. The proposed topology has following features: (a) single stage with unidirectional power flow, (b) galvanic isolation using compact and high power density high frequency transformer, (c) partially soft-switched primary side HF inverter, (d) line frequency
switched secondary side inverter, (e) a small size VSI is used to compensate reactive loss due to filter and line inductor. This topology can be used for medium voltage (611 kV ) grid integration with high voltage blocking switches at the secondary. The modulation scheme and soft-switched operation principle is discussed in detail. The simulation waveforms are presented to verify the theoretical analysis. Practical implementation of the proposed topology will be done in future.

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Fig. 7: Simulated waveforms- (a) $3 \phi$ grid voltages and currents, (b) grid voltage and current with converter o/p voltage and current of phase $a$, (c) converter $\mathrm{o} / \mathrm{p}$ voltage waveform w.r.t grid and HFT neutral point, (d) primary voltage and current of HFT, (e) flux balance waveform of HFT, (f) Soft-switching waveforms (Transitions: $S_{A_{4}} \rightarrow S_{A_{3}}$ and $S_{A_{1}} \rightarrow S_{A_{2}}$ ) (see Fig. 4).

