A Carrier-Based Implementation of a Nearest Three Space-Vector PWM Strategy of Three-Level Inverter

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***Abstract*—PWM techniques of neutral-point-clamped three-level inverters (NPC-TLI) aim at equally distributing the DC bus voltage among two split capacitors along with the generation of the average three-phase voltage. The virtual space vector class of PWM (VPWM) can make the ripple in the capacitor voltage zero at every switching cycle by ensuring that the carrier cycle average of the neutral point current is zero. The nearest three space-vector PWM (NPWM) synthesizes the average output voltage with better quality and at a lower switching frequency when compared with VPWM. With NPWM, it is not possible to achieve zero average neutral point current over a carrier cycle at all operating conditions. But by adjusting the distribution of dwell time among two redundant states through a feedback controller, it is possible to minimize the ripple in the capacitor voltage. This also ensures dynamic balancing of average voltage. Hence, this NPWM with the voltage balancing scheme is a popular choice and termed as general NPWM (GNPWM) in this work. The space vector implementation of GNPWM involves complex computation. This paper presents a carrier-based algorithm for implementing GNPWM that does not require sector identification etc. It obtains the duty ratios of six independent switches of TLI directly from the three reference output voltage signals through minimal computation. The proposed algorithm is validated through MATLAB simulation and experiment on a 2.5 kW hardware prototype.**

***Index Terms*—Three level inverter, Nearest three space-vector PWM, Carrier-based implementation**

I. Introduction

THREE-PHASE (3ϕ) neutral-point-clamped (NPC) three-level inverter (TLI) is a promising candidate in high, medium, and low voltage applications due to its several advantages over two-level inverter, like, higher voltage handling capability, reduced dv/dt stress, lower high-frequency voltage ripple and hence, smaller filter size and higher efficiency, [1]. One of the major difficulties in the broader adaptation of this converter is higher control complexity. It has more devices and requires additional neutral-point voltage balancing than a conventional two-level inverter. Hence, it involves complex pulse-width modulation (PWM) scheme with a substantial computation burden. This paper aims to reduce the computation for implementing one of the important PWM schemes of 3ϕ TLI.

In TLI, two identical capacitors provide a split DC supply from a single DC source in most applications. The average voltage across these two capacitors must be maintained to half of the DC source voltage through a closed-loop control scheme to keep the voltage ripple as small as possible. A set of switching schemes, like, Virtual space-vector PWM (VPWM), Special three space-vector PWM (S3PWM), are proposed in the literature, [2], [3], that ensures that the ripple in the capacitor voltage disappears at carrier frequency by injecting zero average neutral-point currents. In these schemes, virtual space vectors are used to synthesize the reference voltage vector. Virtual vectors consist of more than one switching state whose combined effect on the average neutral-point current is zero. Another set of modulation strategies that apply the nearest three vectors are called NPWM [4], [5]. One among the three nearest vectors can be realized with two redundant states. Equal distribution of dwell time among these two states results in so-called Conventional NPWM (CNPWM), [6]. CNPWM doesn't satisfy the above two objectives of neutral-point voltage balancing. But, by optimally distributing the dwell time through feedback control scheme, it is possible to minimize the capacitor voltage ripple and to achieve dynamic average voltage distribution, [7], [8]. This scheme is termed as General NPWM (GNPWM) in this paper. VPWM and S3PWM schemes do not apply the nearest available voltage vectors and employ more than one switching state to realize a virtual vector. Hence, these schemes result in higher total harmonic distortion (THD) and higher switching frequency when compared with NPWM, [8]. Due to their relative advantages, several hybrid PWM techniques are proposed which combine both VPWM and GNPWM, [3], [8]. Note, the only limitation of GNPWM is the requirement of a slightly higher amount of capacitance as it is not possible to make the average neutral-point current zero over a carrier cycle at all operating conditions. Nevertheless, GNPWM has emerged as one of the most popular schemes deployed in the field due to other advantages. This paper focuses on the implementation of GNPWM.

In a carrier-based implementation, switching signals are generated by comparing the so-called modulation signals with triangular carrier waveforms. The objective of any carrier-based PWM scheme is to generate these modulation signals from the reference output voltage signals through a reduced number of computation steps. For example, the carrier-based implementation of the most popular Conventional Space Vector PWM (CSVPWM) of two-level inverter generates the modulation signal of a particular phase by simply adding the

TABLE I: Definition of Switching States

Switching State	S_{XP}	S'_{XN}	S'_{XP}	S_{XN}	v_{XZ}
P	ON	ON	OFF	OFF	$+0.5V_{dc}$
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	$-0.5V_{dc}$

middle value of the three reference signals with the reference signal of that specific phase, [9]. Thus, it avoids some of the calculation-intensive steps of space-vector (SV) implementation, like, a) Clark's transformation for computation of reference voltage vector from reference signals; b) sector identification that requires inverse trigonometric operation; c) computation of duty cycle of each vector through trigonometric computation; and then finally d) generation of switching signals through a lookup table approach, [10]–[12]. So, there is a drastic reduction of the computational burden that is important in real-time implementation and conceptual simplicity. Carrier-based implementation of SVPWM techniques has been widely discussed in literature: [13] for matrix converters, [14] for multi-phase inverters and, [1], [6], [15]–[17] for three-level inverters. Recently, a carrier-based implementation of CNPWM based on the center-aligned modulation concept is presented in [18]. But no carrier-based implementation for GNPWM is known in the literature. Therefore, this paper presents carrier-based implementation of GNPWM.

The organization of the rest of the paper is as follows- Section II elaborates the conventional analysis part of 3ϕ TLI; Section III highlights the proposed algorithm; Section IV validates the proposed algorithm through both simulation and experimental results. Finally, Section V concludes the paper.

II. Analysis

A. Modeling of three-phase three-level Inverter

The basic structure of a three-phase (3ϕ) neutral point-clamped (NPC) 3-level Inverter (TLI) is shown in Fig. 1a. It has two DC-link capacitors, C_u and C_l, between positive bus ($D+$) and negative bus ($D-$), connected at DC-bus midpoint Z. Each leg of the TLI has 3 switches, .viz, S_{XP}, S_{XO}, S_{XN}, and X denotes the pole point of a leg; where $X \in \{A, B, C\}$. There are three permissible switching states corresponding to each leg of TLI, which are denoted by 'P', 'O' and 'N', respectively. Each leg of TLI can be realized either through diode-clamped structure (shown in Fig. 1b) or through T-type (shown in Fig. 1c). Table I shows the 'ON' and 'OFF' conditions of the switches and the corresponding pole-voltages, v_{XZ}, for the above three states of a leg. From this table, it can further be observed that two pairs of switches, (S_{XP} and S'_{XP}) and (S_{XN} and S'_{XN}) are switched in a complementary manner.

As each of the three legs has three states, the total number of possible switching states of this converter is $3^3 = 27$. Each of these states is denoted by a specific combination of $\{P, O, N\}$, where each alphabetic notation represents the states of leg A, leg B, and leg C, respectively. The 27 switching states of 3ϕ TLI can be mapped into $\alpha - \beta$ plane after plugging the respective pole voltages in (1b), which is $3\phi-2\phi$ Clarke's transformation. Three of these switching states, .viz OOO, PPP and NNN, are mapped into same zero-vector. Remaining 24 states give 18 distinct non-zero active voltage vectors of three different magnitudes-$\frac{V_{dc}}{3}$, $\frac{V_{dc}}{\sqrt{3}}$ and $\frac{2V_{dc}}{3}$. Each of six large and six medium vectors are associated with one unique state, but each of six small vectors has two redundant switching states. These states constitute six sectors in $\alpha - \beta$ plane and Fig. 2 shows the states corresponding to one of the sectors, named as sector-I which spans from 0° to 60° in α-β plane.

$$v_\alpha + jv_\beta = \frac{2}{3}(v_{An} + v_{Bn} \cdot e^{j\frac{2\pi}{3}} + v_{Cn} \cdot e^{-j\frac{2\pi}{3}}) \quad (1a)$$

$$= \frac{2}{3}(v_{AZ} + v_{BZ} \cdot e^{j\frac{2\pi}{3}} + v_{CZ} \cdot e^{-j\frac{2\pi}{3}}) \quad (1b)$$

When Clarke transformation is applied on the average line-neutral voltages, $\bar{v}_{An}$, $\bar{v}_{Bn}$, $\bar{v}_{Cn}$, where $\bar{v}_{Xn}$ is the average of v_{Xn} over a carrier period T_s, the reference voltage vector $\overrightarrow{V}_{ref}$ is obtained as shown in (2a). Normalizing (2a) by V_{dc}, (2b) is obtained where, $\overrightarrow{m}_{ref} = \frac{\overrightarrow{V}_{ref}}{V_{dc}}$, and $m_X = \frac{\bar{v}_{XN}}{V_{dc}}$.

$$\overrightarrow{V}_{ref} = \frac{2}{3}(\bar{v}_{An} + \bar{v}_{Bn} \cdot e^{j\frac{2\pi}{3}} + \bar{v}_{Cn} \cdot e^{-j\frac{2\pi}{3}}) \quad (2a)$$

$$\implies \overrightarrow{m}_{ref} \triangleq m_\alpha + jm_\beta = \frac{2}{3}(m_A + m_B e^{j\frac{2\pi}{3}} + m_C e^{-j\frac{2\pi}{3}}) \quad (2b)$$

To synthesize this $\overrightarrow{m}_{ref}$ using available switching states, several choices can be made among which nearest three space-vector PWM (NPWM) is one of the most popular techniques, [6].

B. NPWM Modulation Strategy

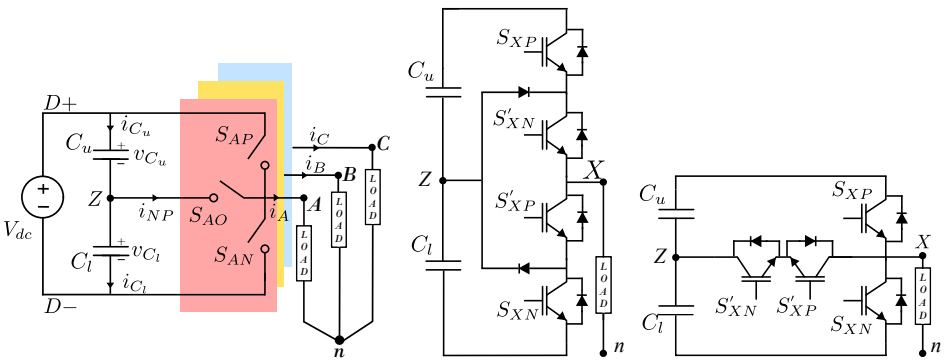
As the name suggests, this strategy synthesizes $\overrightarrow{m}_{ref}$, over a carrier cycle, using nearest three voltage vectors (NTV) around it. From Fig. 2 it can be seen that the choices of NTVs can be different depending upon the position of the tip of $\overrightarrow{m}_{ref}$ in sector-I. According to this, each sector can be segregated into four 'sub-sector's (.viz 1, 2, 3, 4). Let $\overrightarrow{V}_1$, $\overrightarrow{V}_2$, $\overrightarrow{V}_3$ are the nearest three voltage vectors and d_1, d_2, d_3 are the dwell times for which these vectors are to be applied. These dwell times of the NTVs can be obtained after solving (3).

$$d_1\overrightarrow{V}_1 + d_2\overrightarrow{V}_2 + d_3\overrightarrow{V}_3 = \overrightarrow{m}_{ref} \quad (3a) \qquad d_1 + d_2 + d_3 = 1 \quad (3b)$$

After the selection of NTVs and calculation of corresponding dwell times, it is important to design the switching sequence. The sequence design is guided by two rules:

- Transition from one-state to another is accompanied by transition in one leg only.
- Pole voltage (v_{XZ}) waveform of each leg should be unipolar within a period of T_s i.e each leg can use either (P and O) states or (O and N) states within T_s.

Every sub-sector has at least one small vector which belongs to the group of NTVs of that particular sub-sector. As each small vector has two redundant states, one can use these redundant states in the sequence. For each of sub-sectors 3 and 4 in sector-I, the above two criteria can be ensured only by one and unique switching sequence as given in Table. II. Fig. 3 shows the sequence and the corresponding pole voltage waveforms over one T_s when tip of $\overrightarrow{m}_{ref}$ is in sub-sector 3 of sector-I. As both sub-sector-1 and sub-sector-2 have two small vectors belonging to NTV group, two sequences are possible for each of these two sub-sectors, as shown in Table



(a) General 3ϕ NPC TLI (b) Diode-clamped Type (c) T-Type

Fig. 1: 3ϕ TLI Structure

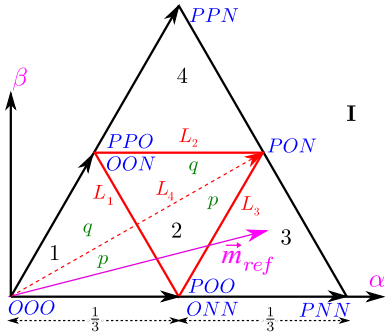


Fig. 2: Voltage vectors of sector-I

TABLE II: Switching sequences in sub-sectors of sector-I

Sub sector	Switching Sequence
1_p	*ONN-OON-OOO-POO-OOO-OON-ONN*
1_q	*OON-OOO-POO-PPO-POO-OOO-OON*
2_p	*ONN-OON-PON-POO-PON-OON-ONN*
2_q	*OON-PON-POO-PPO-POO-PON-OON*
3	*ONN-PNN-PON-POO-PON-PNN-ONN*
4	*OON-PON-PPN-PPO-PPN-PON-OON*

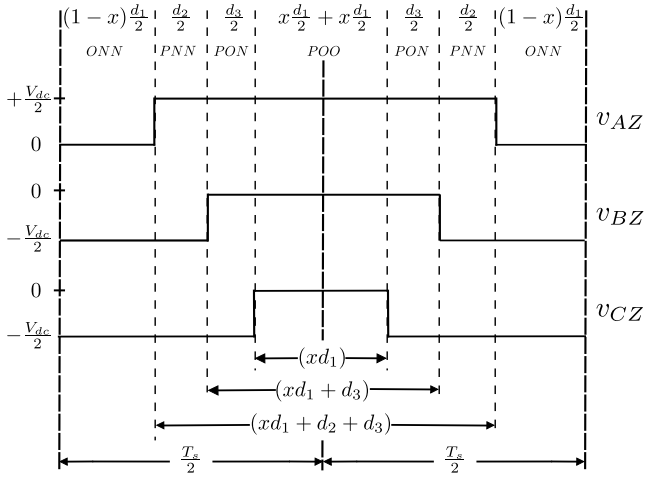


Fig. 3: Pole Voltage Pulses in sub-sector 3 of sector I

II, which conform with the two rules mentioned earlier. Thus each of these two sub-sectors can be further divided into two 'sub-sub-sectors', p and q, [6], as per the choice of switching sequence.

The duty-ratio of the small vector can be distributed between the redundant states of the above sequences in an infinite number of ways. For example, in sub-sector 3, $\vec{V}_{POO}$ can be applied for xd_1 duration and $\vec{V}_{ONN}$ can be applied for $(1-x)d_1$ duration, where $x \in [0,1]$ can be any arbitrary positive fraction. In Conventional NPWM technique (CNPWM), $x = 0.5$ [6]. This choice of x causes significant voltage unbalance between the top and bottom capacitor of the DC-bus; and predominantly has a frequency component of 3 times that of line-cycle frequency, [2], [7]. It has been shown in [19] that proper choice of x can reduce the magnitude of this voltage unbalance. Therefore, this paper proposes a carrier-based implementation strategy for any generalized value of x, and the technique is further referred as Generalized NPWM or GNPWM.

C. Effect of GNPWM on capacitor voltage

Equation (4) shows that the change in bottom capacitor voltage, v_{C_l}, is caused by the neutral point current, i_{NP}, flows out of the DC-bus midpoint, as shown in Fig. 1a. While integrating both sides over one T_s, (5) is obtained. This implies change in v_{C_l} over one carrier cycle, $\Delta\bar{v}_{C_{l_{T_s}}}$, is directly proportional to the carrier-cycle average neutral point current, $\bar{i}_{NP_{T_s}}$. Therefore, non-zero $\bar{i}_{NP_{T_s}}$ will cause non-zero $\Delta\bar{v}_{C_{l_{T_s}}}$. As the sum of voltage across top and bottom capacitor is constant, there will be change in voltage across the top capacitor, v_{C_p}, as well. Change in voltages will also cause ripple in pole voltage, v_{XZ}, and line-neutral voltage, v_{Xn}.

$$i_{NP} = i_{C_u} - i_{C_l} = C_u \cdot \frac{\mathrm{d}v_{C_u}}{\mathrm{d}t} - C_l \cdot \frac{\mathrm{d}v_{C_l}}{\mathrm{d}t} = -(C_u + C_l) \cdot \frac{\mathrm{d}v_{C_l}}{\mathrm{d}t}$$
$$(as, v_{C_u} + v_{C_l} = V_{dc}, \frac{\mathrm{d}v_{C_u}}{\mathrm{d}t} = -\frac{\mathrm{d}v_{C_l}}{\mathrm{d}t}) \quad (4)$$

$$(C_u + C_l) \underbrace{\int_{v_{C_u}(0)}^{v_{C_l}(T_s)} \mathrm{d}v_{C_l}}_{\Delta\bar{v}_{C_{l_{T_s}}}} = \underbrace{\int_{T_s}^{0} i_{NP}\mathrm{d}t}_{\bar{i}_{NP_{T_s}}} \implies \Delta\bar{v}_{C_{l_{T_s}}} = \frac{-\bar{i}_{NP_{T_s}}}{(C_u + C_l)} \quad (5)$$

It is possible to show that instantaneous i_{NP} due to large vectors and the zero vector is zero, whereas application of medium and small vectors result into non-zero i_{NP} to flow. i_{NP} caused by the redundant states corresponding to small vectors are of same magnitude but opposite polarity. These observations lead to the fact that $\bar{i}_{NP_{T_s}}$ of (5), which causes $\Delta\bar{v}_{C_{n_{T_s}}}$, depends on the modulation strategy and position of $\vec{m}_{ref}$. For example, when the tip of $\vec{m}_{ref}$ is lying in sub-sector 3 of sector-I, magnitudes of i_{NP} due to the switching states ONN, POO, PON are i_A, $-i_A$ and i_B, respectively. Equation (6) derives $\bar{i}_{NP_{T_s}}$ as a function of x for this case.

$$\bar{i}_{NP_{T_s}} = i_B d_3 + i_A(1-x)d_1 - i_A x d_1 = i_B d_3 - i_A(2x-1)d_1 \quad (6)$$

In CNPWM, ONN and POO are applied for equal duration of time, as $x = 0.5$. Therefore, their effects on $\bar{i}_{NP_{T_s}}$ are nullified. But the effect of medium voltage vector PON, $i_B \cdot d_3$ in (6), results in non zero value of $\bar{i}_{NP_{T_s}}$ which in-turn causes ripple in v_{C_l}. This ripple predominantly has a frequency component of 3 times that of line-cycle frequency, [2], [5],

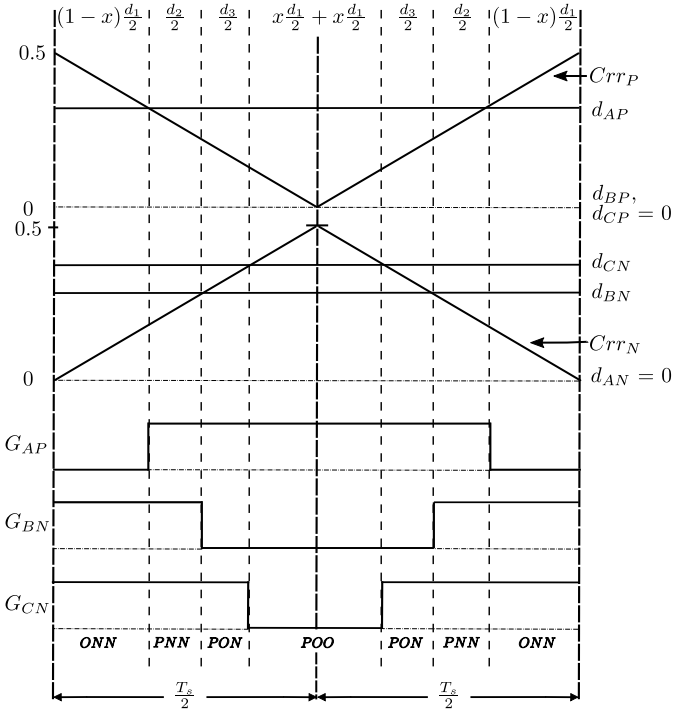


Fig. 4: Switching Pulses in sub-sector 3 of sector-I

[7]. It can be further observed from (6) that by making proper choice of x, magnitude of $\bar{i}_{NP_{T_s}}$ can be minimized, [19].

III. Proposed Algorithm For Carrier Based Implementation of GNPWM

As already mentioned before, S'_{XP} and S'_{XN} are switched in a complementary fashion to S_{XP} and S_{XN}, respectively. Therefore, implementation of GNPWM strategy requires generating the gating pulses of S_{XP} and S_{XN}, where $X \in \{A, B, C\}$, which are denoted by G_{XP} and G_{XN}, respectively. To generate G_{XP} and G_{XN}, the duty-ratios of switches S_{XP} and S_{XN}, d_{XP} and d_{XN}, should be compared with two 180° phase-shifted triangular carrier-waves, Crr_P and Crr_N, respectively, as shown in Fig. 4. Due to unipolar nature of v_{XZ}, either d_{XP} or d_{XN} will be zero.

It can be observed from Table I that the pole voltage, v_{XZ}, due to states P, O, N is $+\frac{V_{dc}}{2}$, 0 or $-\frac{V_{dc}}{2}$, respectively. Therefore, the average pole voltage over T_s, $\bar{v}_{XZ}$, can be written as given in (7b). Applying KVL over the loop formed by Z, X and n in Fig. 1, the carrier cycle average voltage equation of (7a) is obtained. Equating right-hand sides of both (7b) and (7a) and dividing both sides by V_{dc}, (7c) is obtained. Here, m^*_X and m_{cm} are termed as modulating signal and common-mode signal, respectively. The adopted NPWM scheme is an unipolar strategy. This means if the average pole voltage, $\bar{v}_{XZ}$, is greater than zero, switches S_{XP} and S_{XO} of Fig. 1a will be turned-on and off to synthesize the desired voltage, whereas S_{XN} will remain always turned-off. Hence, the duty ratios can be calculated using (8).

$$\bar{v}_{XZ} = \bar{v}_{Xn} + \bar{v}_{nZ} \tag{7a}$$

$$= \frac{V_{dc}}{2} d_{XP} + 0 \cdot d_{XO} - \frac{V_{dc}}{2} d_{XN} = \frac{V_{dc}}{2}(d_{XP} - d_{XN}) \tag{7b}$$

$$d_{XP} - d_{XN} = 2(m_X + m_{cm}) \triangleq m^*_X; \text{ where } m_{cm} \triangleq \frac{\bar{v}_{nZ}}{V_{dc}} \tag{7c}$$

$$d_{XP} = \begin{cases} m^*_X; m^*_X \geq 0 \\ 0; O.W. \end{cases} \quad d_{XN} = \begin{cases} 0; m^*_X \geq 0 \\ -m^*_X; O.W. \end{cases} \tag{8}$$

It can be seen from (8) that for the given reference signals m_A, m_B and m_C, the six duty-ratios (d_{AP}, d_{BP}, d_{CP} and d_{AN}, d_{BN}, d_{CN}) can be determined if m_{cm} is known. Therefore, a simplified algorithm to determine m_{cm} is discussed in the next sub-section.

A. Determination of common-mode signal (m_{cm})

When summation is taken on both sides of (7a) over all three phases, m_{cm} expression is obtained as (9). For a balanced 3ϕ load with isolated neutral point, n, as shown in Fig. 1a, $\sum_{X=A,B,C} \bar{v}_{Xn} = 0$ or $m_A + m_B + m_C = 0$. Using (9), one can determine m_{cm} expressions for each sub-sector or sub-sub-sectors from the knowledge of the dwell-times of each switching states of Table II. For example, it can be observed from Fig. 4 that for sub-sector 3 of sector-I, $\bar{v}_{AZ} = \frac{V_{dc}}{2}[xd_1 + d_3 + d_2]$, $\bar{v}_{BZ} = -\frac{V_{dc}}{2}[(1-x)d_1 + d_2]$, $\bar{v}_{CZ} = \frac{V_{dc}}{2}[(1-x)d_1 + d_3 + d_2]$. After solving d_1, d_2 and d_3 for sub-sector 3 from (3) and using (9), m_{cm} expression of sub-sector 3 of sector-I can be written as a function of m_A, m_B, m_C and x, as shown in (10).

$$\sum_{X=A}^{C} \bar{v}_{XZ} = \underbrace{\sum_{X=A}^{C} \bar{v}_{Xn}}_{=0} + 3\bar{v}_{nZ} \implies m_{cm} = \frac{\sum_{X=A}^{C} \bar{v}_{XZ}}{3V_{dc}} \tag{9}$$

$$m_{cm} = -(0.5 - x) - x \cdot m_A - (1 - x) \cdot m_C \tag{10}$$

Similarly, the expression of m_{cm} for all other sub-sectors can also be determined with the knowledge of which redundant switching state is to be used for x and which one is to be used for $(1 - x)$ duration, as given in Table IV. The second column of Table III shows m_{cm} expressions for all sub-sectors of sector-I. After performing similar exercise in all six sectors based on the conventions of Table IV, it is observed that the m_{cm} expression can be generalized in terms of m_{max}, m_{mid}, m_{min}, where $m_{max} \triangleq maximum(m_A, m_B, m_C)$, $m_{min} \triangleq minimum(m_A, m_B, m_C)$ and $m_{mid} = -(m_{max} + m_{min})$.

B. Sub-sector & sub-sub-sector identification

From Table III it can be observed m_{cm} expression depends upon sub-sector and sub-sub-sector information. The sub-sector and sub-sub-sector identification can be done from the position of the tip of $\overrightarrow{m}_{ref}$ with respect to lines L_1, L_2, L_3, L_4 shown in Fig. 2 [6]. The equations of these lines in sector-I, lying on $\alpha - \beta$ plane, can be expressed in terms of α and β. For example, L_1 (in sector-I) passes through $(\frac{1}{3}, 0)$ with an angle of 120° as shown in Fig. 2. Thus, it's equation can be written as $\sqrt{3}\alpha + \beta = \frac{1}{\sqrt{3}}$. At a particular time instant, when $\sqrt{3}m_\alpha + m_\beta = \frac{1}{\sqrt{3}}$, $\overrightarrow{m}_{ref}$ will lie on L_1. It can be observed that tip of $\overrightarrow{m}_{ref}$ lies in sub-sub-sector 1_p or 1_q, when $\sqrt{3}m_\alpha + m_\beta < \frac{1}{2}$ or $> \frac{1}{2}$, respectively. Likewise, equations of other three lines can be found which will give sets of inequalities from where exact position of tip of $\overrightarrow{m}_{ref}$ can be found at any given time. Using (2b), these inequalities can

TABLE III: Expressions of m_{cm} in different sub-sectors and sub-sub-sectors

sub-sector	sector-I	Generalized expression
1_p	$-(1-x)\cdot m_A - x\cdot m_B$	$-(1-x)\cdot m_{max} - x\cdot m_{mid}$
1_q	$-(1-x)\cdot m_B - x\cdot m_C$	$-(1-x)\cdot m_{mid} - x\cdot m_{min}$
2_p	$-0.5\cdot(1-x) - x\cdot m_B - (1-x)\cdot m_C$	$-0.5\cdot(1-x) - x\cdot m_{mid} - (1-x)\cdot m_{min}$
2_q	$-0.5\cdot x - x\cdot m_A - (1-x)\cdot m_B$	$-0.5\cdot x - x\cdot m_{max} - (1-x)\cdot m_{mid}$
3	$-(0.5-x) - x\cdot m_A - (1-x)\cdot m_C$	$-(0.5-x) - x\cdot m_{max} - (1-x)\cdot m_{min}$
4	$-(0.5-x) - x\cdot m_A - (1-x)\cdot m_C$	$-(0.5-x) - x\cdot m_{max} - (1-x)\cdot m_{min}$

TABLE IV: Duration of Switching States

x fraction	$(1-x)$ fraction
POO	ONN
PPO	OON
OPO	NON
OPP	NOO
OOP	NNO
POP	ONO

TABLE V: Condition for sub/sub-sub-sect. identification

if/else	sector-I	General	sub/sub-sub-sect.
if	$m_a - m_c \le \frac{1}{2}$	$m_{max} - m_{min} \le \frac{1}{2}$	1
else if	$m_a - m_b \ge \frac{1}{2}$	$m_{max} - m_{mid} \ge \frac{1}{2}$	3
else if	$m_b - m_c \ge \frac{1}{2}$	$m_{mid} - m_{min} \ge \frac{1}{2}$	4
else	-	-	2
if	$m_b \le 0$	$m_{mid} \le 0$	p
else	-	-	q

TABLE VI: Operating conditions

Quantity	Value	Quantity	Value
V_{dc}	400 V	R	17.5 Ω
C_u, C_l	56 μF	L	12 mH
ω	100π rad/sec	M_I	0.45
f_s	10 kHz	P_{out}	2.5 kW

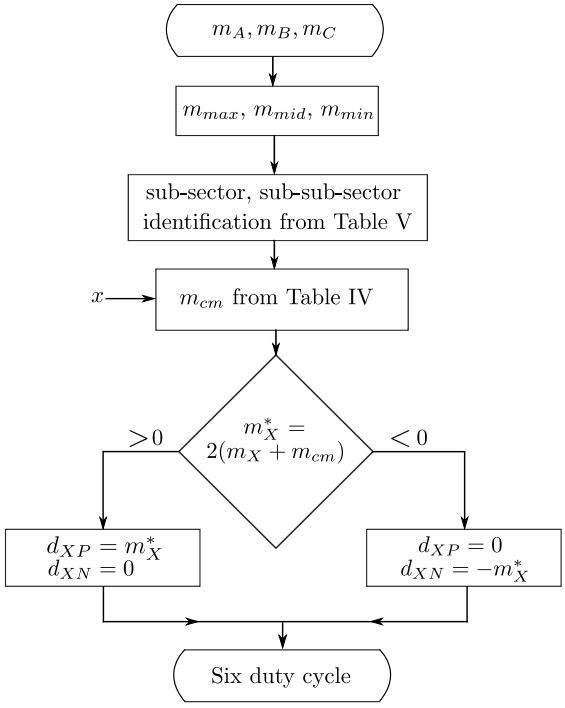


Fig. 5: Flowchart of the proposed algorithm

be written in terms of m_A, m_B, m_C as shown in the second column of Table. V. Similarly, this process can be repeated for all other sectors and general expressions of these inequalities can be derived in terms of m_{max}, m_{mid}, m_{min}, as shown in the second column of Table. V, to find position of tip of $\overrightarrow{m}_{ref}$ at any sector.

Therefore, from the given m_A, m_B, m_C and x, one can determine the duty-ratios after- 1) finding m_{max}, m_{mid}, and m_{min}, 2) determine m_{cm} using Table III, 3) then find six duty values using (8). After comparing d_{XP} and d_{XN} with Crr_P and Crr_N, respectively, gating pulses of S_{XP} and S_{XN} are obtained. The flowchart of the proposed algorithm is shown in Fig. 5.

IV. Validation through simulation and experiment

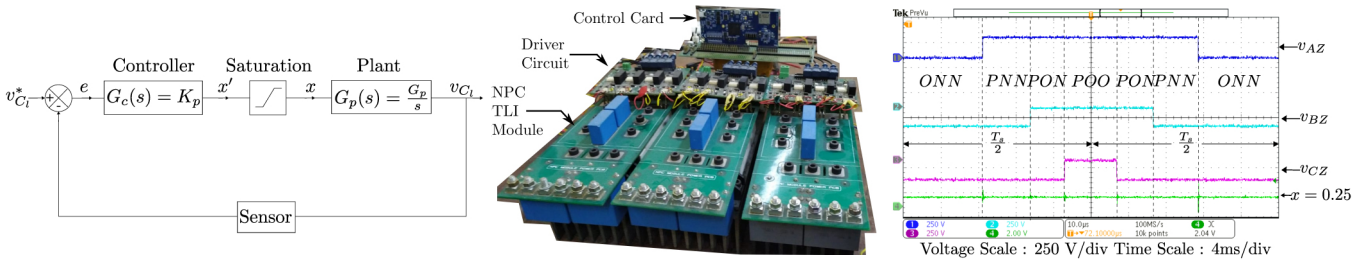
To validate the proposed algorithm through experiment, a 2.5 kW NPC-TIL prototype has been fabricated using SKM75GB123D half-bridge IGBT module and MEE 75-12 DA diodes and ACPL-339J gate drivers. Texas Instrument's delfino series micro-controller, TMS320F28379D, is used as the control card. Fig.6b shows the experimental set-up. R-L network is used as load. Simulations are performed in MATLAB Simulink. All of the internal signals inside the controller, like, x, m_{cm}, m_A^*, and $v_{Cl}* = \frac{V_{ref}}{2}$, corresponding to experimental results are shown through the digital-analog converter (DAC) of the controller card after proper scaling and biasing. Therefore, these signals are unipolar, although the actual variables might be bipolar. The operating conditions, for which the experimental and simulation results are shown here, are given in Table VI. The modulation index, M_I, is defined as the ratio of the peak of the fundamental line-neutral voltage and DC-bus voltage.

A. Verification of the proposed implementation strategy

Fig. 6d, 6e show the experimental waveforms of m_A^*, m_{cm} and v_{AZ} for $x = 0.25, 0.75$. During this verification, two split DC sources, each of 200 V, have been used as input and closed-loop control was disabled. One can see the change in both experimental and simulated m_{cm} waveforms as x changes from 0.25 to 0.75. Fig. 6c and 6f show the experimental pole voltage waveforms, v_{AZ}, v_{BZ}, v_{CZ}, over one carrier cycle for $\overrightarrow{m}_{ref} = 0.45e^{j7.5^\circ}$, i.e., tip of $\overrightarrow{m}_{ref}$ lies within sub-sector 3 of sector-I at $x = 0.25$ and $x = 0.75$, respectively. From this figure, one can determine the switching sequence, which is *ONN-PNN-PON-POO-PON-PNN-ONN* and this sequence matches with the theoretical one, as shown in Fig. 3. As x increases, the dwell-time of state POO (xd_1) increases whereas dwell-time of ONN ($(1-x)d_1$) decreases, as can be seen from Fig. 6c and 6f. From Fig. 6d and 6e, one should also note that instantaneous $v_{AZ} > 0$ when $m_A^* > 0$; and $v_{AZ} < 0$ for $m_A^* < 0$. These results verify the correctness of the implemented strategy and the unipolar operation of TLI.

B. Effectiveness of x in neutral-point voltage balancing

To validate the effectiveness of x to reduce the neutral-point average current and corresponding voltage-ripple and transient voltage recovery ability, the control strategy as proposed by [7] has been adopted. It has been shown in [7] that small-signal transfer function between change in voltage across bottom

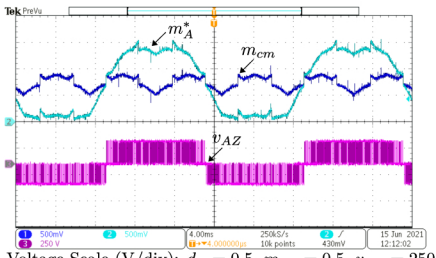


(a) Closed-Loop Control

(b) Experimental set-up

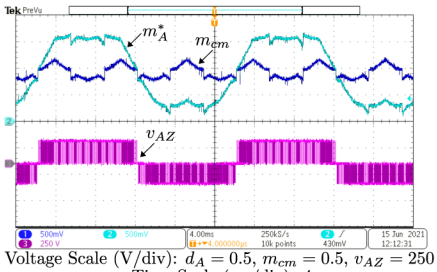
Voltage Scale : 250 V/div Time Scale : 4ms/div

(c) Switching sequence for $x = 0.25$



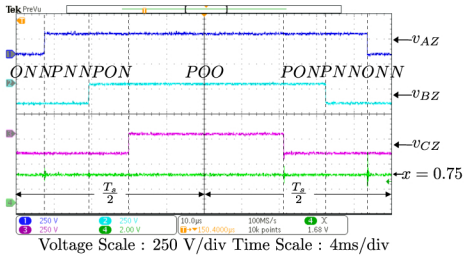
Voltage Scale (V/div): $d_A = 0.5$, $m_{cm} = 0.5$, $v_{AZ} = 250$
Time Scale (ms/div): 4

(d) Experimental result for $x = 0.25$



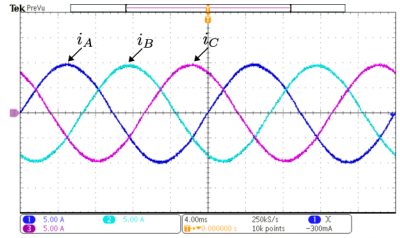
Voltage Scale (V/div): $d_A = 0.5$, $m_{cm} = 0.5$, $v_{AZ} = 250$
Time Scale (ms/div): 4

(e) Experimental result for $x = 0.75$



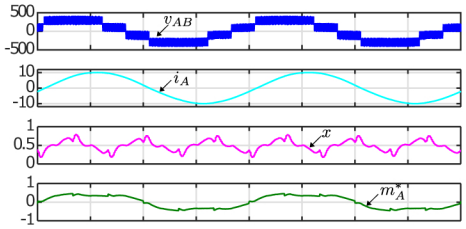
Voltage Scale : 250 V/div Time Scale : 4ms/div

(f) Switching sequence for $x = 0.75$

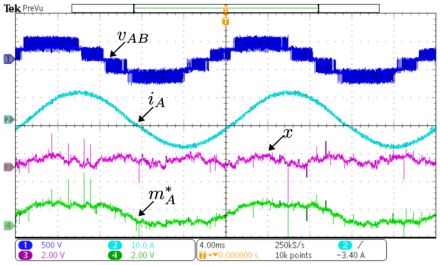


Current Scale : 5 A/div Time Scale : 4 ms/div

(g) Line current waveform

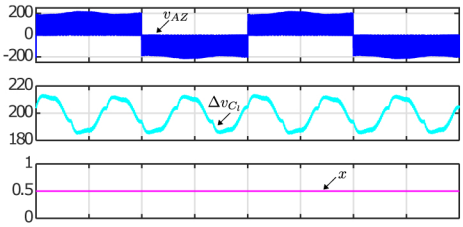


(h) Simulated line voltage, line current, x and m_A^* for GNPWM

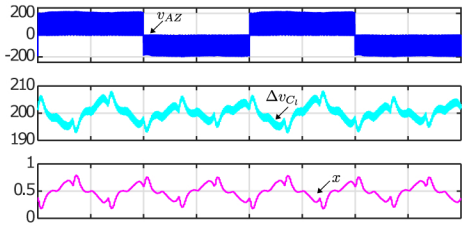


Voltage Scale (V/div): $v_{AZ} = 250$, $x = 1$, $m_A^* = 1$
Current Scale (A/div): $i_A = 5$ Time Scale (ms/div): 4

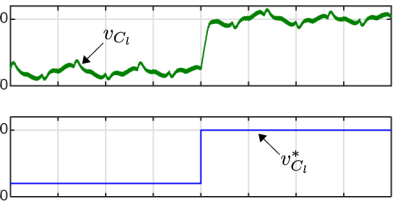
(i) Experimental line voltage, line current, x and m_A^* for GNPWM



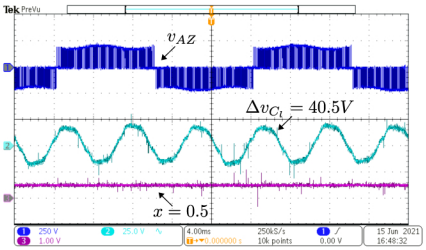
(j) Simulated pole voltage, capacitor voltage ripple and x for CNPWM



(k) Simulated pole voltage, capacitor voltage ripple and x for GNPWM

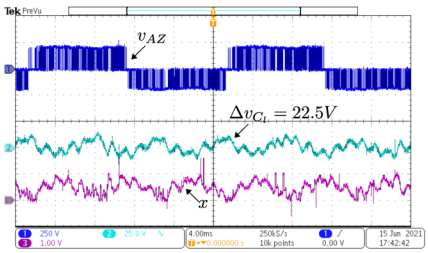


(l) Simulated reference tracking result



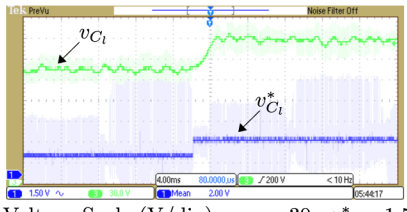
Voltage Scale (V/div): $v_{AZ} = 250$, $\Delta v_{c_n} = 25$, $x = 1$
Time Scale (ms/div): 4

(m) Experimental pole voltage, capacitor voltage ripple and x for CNPWM



Voltage Scale (V/div): $v_{AZ} = 250$, $\Delta v_{c_n} = 25$, $x = 1$
Time Scale (ms/div): 4

(n) Experimental pole voltage, capacitor voltage ripple and x for GNPWM



Voltage Scale (V/div): $v_{C_l} = 30$, $v_{C_l}^* = 1.5$
Time Scale (ms/div): 4

(o) Experimental reference tracking result

Fig. 6: Simulation and experimental results

capacitor (Δv_{C_l}) and x behaves like a integrator with a gain, i.e., plant model is $G_p(s) = \frac{G_p}{s}$. Here, G_p is a function of load power-factor and modulation index, M_I, where M_I is defined as the ratio of peak line-neutral voltage and DC-bus voltage. Therefore, a closed-loop control can be implemented to determine x, as shown in Fig. 6a. As the plant is an integrator, a simple proportional compensator is used. Finally, the output of the controller is passed through a saturation block so that $x \in [0, 1]$ criterion is satisfied. One should note here that although this paper adopts the proposed control algorithm of [7] to determine x, the distribution factor x can come from other control techniques as well, like, model-predictive control or hysteresis control.

With a single DC-source and open-loop $x = 0.5$, i.e., CNPWM technique, Fig. 6j and 6m show the simulated and experimental low-frequency voltage ripples across the bottom capacitor, Δv_{C_l}, and its effect can also be seen in the envelop of pole voltage v_{AZ}. But, if x is obtained through closed-loop and implemented through the proposed carrier-comparison way, 45% reduction (40.5 V to 22.5 V) is seen in Δv_{C_l} in both simulation and experiment, as shown in Fig. 6k and 6n. The effect of this reduction is also reflected in v_{AZ} waveforms. Fig. 6h and 6i show the simulated and experimental waveforms of v_{AB}, i_A, x and m_A^* with x control. The theoretical peak values of the fundamental line-line voltage and current should be $V_{dc} \times M_I \times \sqrt{3} = 311.8$ V and $\frac{V_{dc} \times M_I}{\sqrt{R^2+(\omega L)^2}} = 10.055$ A; the values obtained after applying Fourier series on the experimental waveforms are 307.22 V, 9.78 A, respectively. It shows the fundamental operation remains unchanged with x control. The experimentally obtained 120° phase-shifted three-phase line-currents, i_A, i_B and i_C, are shown in Fig. 6g.

To show the transient voltage recovery ability of the closed-loop system, initially the reference voltage of v_{C_l}, i.e., $v_{C_l}*$, was given as 160 V and then a step change was given in the reference to make it 200 V. Fig. 6l and 6o show experimental and simulated $v_{C_l}*$ and v_{C_l}, from where it can be observed that system is able to settle down to its new steady-state value.

V. Conclusion

The carrier-comparison-based implementation of the popular GNPWM technique is proposed in this work. The proposed algorithm expresses the common-mode signal, m_{cm}, as a function of dwell-time distribution factor of redundant switching states, x, and the maximum (max), middle (mid), and minimum (min) values of the given 3ϕ reference signals. The six duty-ratios of the top and bottom switches of three legs are calculated using this m_{cm} value and given 3ϕ reference signals. Then the corresponding duty-ratio signals are compared with two 180° phase-shifted triangular carriers to get the gating signals of top and bottom switches. The correctness of the implemented strategy and the effectiveness of GNPWM in neutral-point voltage ripple reduction is validated through simulation and experiment on a 2.5 kW hardware prototype.

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