Analytical Switching Transient Model of TO-247-4 Packaged SiC MOSFETs and Comparison with TO-247-3 Devices

Manish Mandal
Dept. of Electrical Engineering
Indian Institute of Science
Bangalore, India
manishmandal@iisc.ac.in

Shamibrota Kishore Roy
Dept. of Electrical Engineering
Indian Institute of Science
Bangalore, India
shamibrotar@iisc.ac.in

Kaushik Basu
Dept. of Electrical Engineering
Indian Institute of Science
Bangalore, India
kbasu@iisc.ac.in

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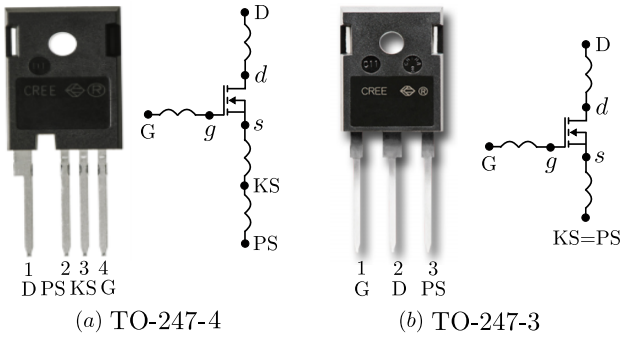
***Abstract*—SiC MOSFETs in TO-247-4 package (Kelvin-source configuration) offers the advantages of faster switching transients and lower switching losses compared to TO-247-3 packaged (common-source configuration) SiC MOSFETs. Due to small value of the common-source inductance in TO-247-4 package, switching dynamics of SiC MOSFETs can be significantly different. This paper presents a detailed analytical switching transient model of TO-247-4 packaged SiC MOSFETs where SiC Schottky diode (SBD) is used as a freewheeling diode. The model considers detailed nonlinear device characteristics of both SiC MOSFET and SiC SBD along with the effect of the external circuit parasitics. The proposed model is validated through behavioral simulation and experiment for a 1.2kV TO-247-4 packaged SiC MOSFET and SBD pair for a range of operating conditions. In addition, switching loss, (di/dt) and (dv/dt) obtained for the TO-247-4 packaged SiC MOSFET are compared with TO-247-3 packaged device.**

***Index Terms*— switching transient, SiC MOSFETs, kelvin-source, common-source**

I. Introduction

SiC MOSFETs are wide-bandgap power semiconductor devices and are commonly used in the voltage segment of 900-1700V. They are superior to similarly rated silicon (Si) insulated gate bipolar junction transistor (IGBT) due to their electrical and thermal performances [1]. These MOSFETs are commercially available in three discrete packages: TO-247-3, TO-247-4, and TO-263-7. Among these packages, TO-247-3 and TO-247-4 are through-hole packages, and are suitable for high-power designs. (see Fig. 1).

SiC MOSFETs in the TO-247-3 package (common-source configuration) have been widely used in power electronic converters. These devices have a significant amount of common-source inductance, which limits the maximum achievable switching speed and minimum achievable switching loss [2]. Kelvin-source configured (TO-247-4 packaged) SiC MOSFETs overcome the above limitations of the TO-247-3 packaged devices. By providing two separate connections; Kelvin-source (KS) for the gate input signal and the power-source (PS) for the connection in the power circuit, the amount of common-source inductance (L_s) coupling the gate and the power loop can be dramatically reduced. As a result, these devices can achieve faster switching transients and smaller switching losses compared to the TO-247-3 devices.



(a) TO-247-4 (b) TO-247-3

Fig. 1: SiC MOSFETs in TO-247-4 and TO-247-3 Packages

Switching loss estimation methods in the literature can be classified as simulation, experiment, and analytical methods. Among the three methods, analytical methods are usually preferred in designing power electronic converters. This method is superior to the simulation-based methods such as the behavioral model (i.e., Spice simulation), as it is free from convergence issues [3] and provides insight into the switching process [4].

Analytical method has been adopted by some earlier works [4], [5] to study the switching transient of SiC MOSFET and to estimate the switching loss as well as (di/dt) and (dv/dt). However, all these works are targeted at TO-247-3 packaged devices. Due to the presence of insignificant L_s (0.2-1 nH), the switching transitions of TO-247-4 devices can be significantly different. A recent work [6] has provided a qualitative discussion of the switching transient of TO-247-4 and TO-247-3 devices. However, it ignores the impact of external parasitic capacitances, and it also does not provide any analytical model for the computation of the important switching transient quantities such as loss, (di/dt) and (dv/dt).

This work presents a detailed analytical model to study the switching transients of the TO-247-4 packaged SiC MOSFETs and SiC SBD pair. It considers non-linear nature of the

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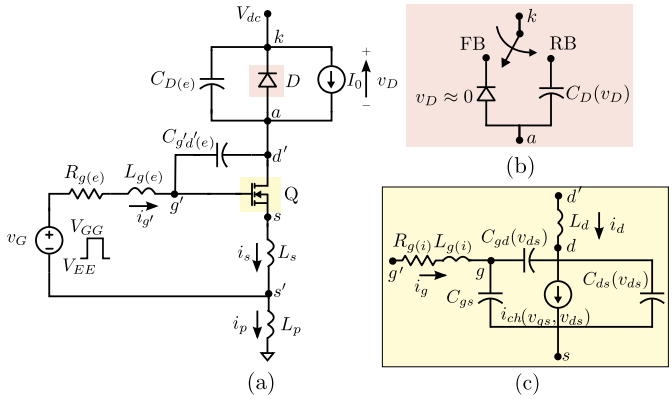


Fig. 2: Circuit configuration for switching transient analysis: (a) buck chopper configuration, (b) SiC SBD model, (c) SiC MOSFET model

channel current and functional dependence of device parasitic capacitances on their terminal voltages, along with the effect of external circuit parasitics. The proposed analytical model estimates switching loss, (di/dt) and (dv/dt), and it is validated through behavioral simulation and experiment for a 1.2kV TO-247-4 device and an SBD pair. Also, a comparison of switching losses, (di/dt) and (dv/dt) of SiC MOSFETS in TO-247-3 and TO-247-4 package is presented. This work also provides additional important observations (compared to [6]) such as: 1) for low gate resistance, a significant difference between the drain and channel current exists, and drain-source voltage reduces throughout the current-rise period (turn-on transition), and 2) during the voltage-rise period (turn-off transition), the channel current collapses to zero for most of the operating conditions. As a result, both turn-on and turn-off losses are reduced substantially.

II. Behavioural Modeling

To study the hard switching dynamics of the SiC MOSFET in TO-247-4 package, a buck-chopper circuit is considered, as shown in Fig. 2(a). A SiC Schottky diode (SBD) is used as freewheeling diode. The input of the buck chopper is connected to an ideal DC voltage source (V_{dc}). An inductive load is connected at the output of the buck circuit, which during the switching transitions is modeled as a constant current sink I_0.

The behavioral model of the SiC MOSFET (Q) is shown in Fig. 2(c). It is modeled as a three-terminal device with external terminals g', d' and s', respectively. For the switching transient analysis, lead inductances associated with the Kelvin-source (KS) and the power-source (PS) pins are clubbed with gate loop trace inductance $L_{g(e)}$ and power loop trace inductance L_p respectively. Hence, total gate loop inductance increases for the Kelvin-source configured SiC MOSFETs. Channel current of Q is modeled as a voltage-dependent current source $i_{ch}(v_{gs}, v_{ds})$. Both the transfer characteristic (i_d vs v_{gs}) and the output characterisitics (i_d vs v_{ds}) given in the datasheet of the SiC MOSFET is used for accurate representation of i_{ch} throughout the range of the gate-source voltage (v_{gs}) and

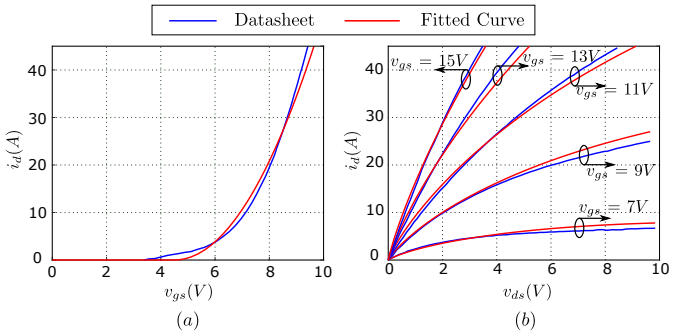


Fig. 3: Curve fitting (a) Transfer Characteristics (b) Output Characteristics

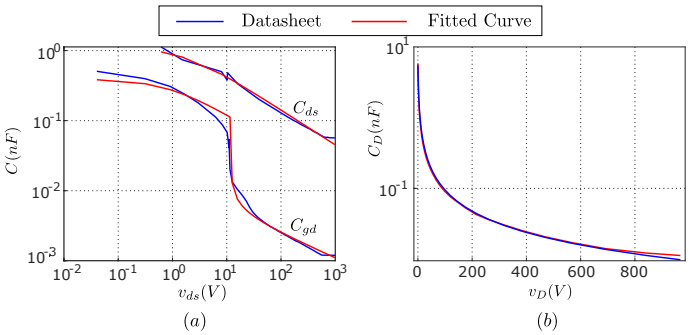


Fig. 4: Capacitance Curve fitting (a) C3M0075120K SiC MOSFET (b) C4D10120A SiC SBD

the drain-source voltage (v_{ds}). Fig. 3(a) and Fig. 3(b) shows the application of (1) in fitting the transfer and the ouput characterisitics given in the datasheet. L_d is the drain-lead inductance, and L_s is the common source inductance of Q. Unlike TO-247-3 packaged SiC MOSFETs, the value of L_s is small in TO-247-4 package due to Kelvin source connection [4] (i.e., L_s is typically around 5-10 nH for TO-247-3 package, whereas it is around 0.2-1 nH for TO-247-4 package). This makes the switching dynamics of these devices different from its TO-247-3 counterpart. $R_{g(i)}$ and $L_{g(i)}$ are the internal gate resistance and inductance of Q respectively.

$$C_{gd}(v_{dg}) = \begin{cases} C_{ox} = \dfrac{k_1}{k_3} & v_{dg} < 0 \quad \text{(2a)} \\ \dfrac{k_1}{\left(1 + \dfrac{v_{dg}}{k_2}\right)^{0.5} + k_3} & 0 \le v_{dg} \le V_T \quad \text{(2b)} \\ \dfrac{k_4}{\left(1 + \dfrac{v_{dg} - V_T}{k_5}\right)^{0.35}} & v_{dg} \ge V_T \quad \text{(2c)} \end{cases}$$

$$C_{ds}(v_{ds}) = \frac{k_6}{\left(1 + \dfrac{v_{ds}}{k_7}\right)^{0.5}} \quad (3)$$

Gate-source capacitance (C_{gs}), gate-drain capacitance (C_{gd}) and drain-source capacitance (C_{ds}) are internal capacitance of the SiC MOSFET. Whereas $C_{gs} \approx C_{iss}(V_{dc})$ is assumed

$$i_{ch} = \begin{cases} 0 & v_{gs} < V_{th} \quad (1a) \\ \dfrac{K_p K_f \left((v_{gs} - V_{th})\, v_{ds} - \left(P_{vf}^{y-1}/y \right) (v_{gs} - V_{th})^{2-y}\, v_{ds}^{y} \right)}{(1 + \theta(v_{gs} - V_{th}))}, & v_{ds} < (v_{gs} - V_{th})/P_{vf},\ v_{gs} > V_{th} \quad (1b) \\ \dfrac{K_p\, (v_{gs} - V_{th})^2}{2(1 + \theta(v_{gs} - V_{th}))}, & v_{ds} > (v_{gs} - V_{th})/P_{vf},\ v_{gs} > V_{th} \quad (1c) \end{cases}$$

to be a constant capacitance, C_{gd} and C_{ds} are non-linear functions of their terminal voltages v_{dg} and v_{ds}, respectively (see [4]). The variation of these capacitances with voltages can be obtained from the capacitance vs v_{ds} plot provided in the datasheet using the relations; $C_{gd} = C_{rss}$ and $C_{ds} = C_{oss} - C_{rss}$. It is be noted that for negative values of v_{dg}, C_{gd} is a large capacitance equal to the capacitance of the gate oxide layer C_{ox} [4]. (2) and (3) denotes the non-linear function form used for the capacitances C_{gd} and C_{ds} respectively. Fig. 4(a) shows the effectiveness of the capacitance in fitting the datasheet curves.

$$C_D(v_D) = \frac{k_8}{\left(1 + \frac{v_D}{k_9}\right)^{0.5}} \quad (4)$$

The behavioral model for SiC Schottky diode (D) is also shown in Fig. 2(b). The diode is modeled as an ideal diode with zero voltage drop in forward-biased condition. In reverse-biased condition, it is modeled as a voltage-dependent capacitor $C_D(v_D)$ where v_D is the reverse voltage acroos the diode. $C_D(v_D)$ can be obtained from the datasheet of the SiC SBD. (4) is used for modeling this reverse-biased capacitance of the diode and it is plotted in Fig. 4(b).

The SiC MOSFET is driven with the gate drive voltage v_G. While the positive level V_{GG} is used to drive the MOSFET at recommended on-state resistance and sufficient switching speed, negative voltage level V_{EE} is used to prevent the device against false turn-on events. $R_{g(e)}$ is the external gate resistance which includes the driver internal resistance.

Fast switching transitions of SiC MOSFETs excites external circuit parasitics such as $L_{g(e)}$, L_p, $C_{g'd'(e)}$, $C_{d's'(e)}$ and $C_{D(e)}$. $L_{g(e)}$ represents the external gate inductance. It is contributed by the gate driver IC pin inductance, inductance of KS pin and the PCB trace inductance connecting the gate and source pins of the SiC MOSFET to the gate driver. L_p represents the total power loop inductance, and it is the summation of DC bus inductance (contributed by layout of DC bus and ESL of DC bus capacitor), lead inductances of D and connection inductances of Q and D. $C_{g'd'(e)}$ and $C_{d's'(e)}$ are external capacitances across g', d' nodes and d', s' nodes of the SiC MOSFET and these are contributed by PCB layout. $C_{D(e)}$ is the external parasitic capacitance across a, k nodes of D and it is the summation of layout capacitance and high-frequency parasitic capacitance of the inductive load.

The time evolution of gate-source voltage $v_{gs}(t)$, drain-source voltage $v_{ds}(t)$ and channel current $i_{ch}(t)$ during switching transitions are the key waveforms related to switching dynamics study and switching loss estimation. Due to the presence of internal device and circuit parasitics, it is not possible to measure these waveforms experimentally. The measurable waveforms are $v_{g's'}(t)$, $v_{d's'}(t)$ and $i_p(t)$ (Fig. 2). The actual switching loss (E) in the MOSFET is given by (5) and the apparent loss (E') is given by (6) where T is the switching transition time. Note, E' can be obtained from double pulse test based experimental measurement. Kindly also note that $v_{gs}(t)$, $v_{ds}(t)$ and $i_{ch}(t)$ are obtained from the simulation of the behavioral model is MATLAB/Simulink.

$$E = \int_0^T v_{ds}(\tau) i_{ch}(\tau)\ d\tau \quad (5)$$

$$E' = \int_0^T v_{d's'}(\tau) i_p(\tau)\ d\tau \quad (6)$$

III. Analytical Modeling of Switching Dynamics

This section aims to analyse the turn-on and turn-off switching dynamics of the TO-247-4 packaged SiC MOSFET and SBD pair. It also estimates the actual switching loss (E), and (dv/dt) and (di/dt) rates for a given operating condition (V_{dc}, I_0) and gate driver parameters (V_{EE}, V_{GG}, $R_{g(e)}$). The device-related parameters (C_{gs}, $C_{gd}(v_{dg})$, $C_{ds}(v_{ds})$, V_{th}, K_p, K_f, θ, $R_{g(i)}$ and $C_D(v_D)$) are obtained from the datasheets and the external circuit parasitics (L_s, L_p, $C_{g'd'(e)}$, $C_{d's'(e)}$ and $C_{D(e)}$) can be approximately estimated from electromagnetic simulation [7] or experimental measurements [8]. Note: effect of $L_{g(i)}$ and $L_{g(e)}$ are negligible in switching dynamics other than initial delay period and hence, it is not considered in the analysis.

A. Turn-on analytical model

Turn-on switching dynamics of the TO-247-4 packaged SiC MOSFET can be divided into four stages: Stage I (turn-on delay period), Stage II (current-rise period), Stage III (intermediate period) and Stage IV (voltage-fall period) as shown in Fig. 5(a)). Note: divisions of these stages are similar to TO-247-3 packaged SiC MOSFET [9]. t_I, t_{II}, t_{III} and t_{IV} denote the time period of these modes respectively.

1) Stage I - Turn-on delay period : The turn-on switching dynamics begins when a positive gate pulse V_{GG} is applied and the MOSFET enters into Stage I. Gate-source voltage v_{gs} increases exponentially with time constant $\tau = (R_{g(e)} + R_{g(i)})C_{gs}$. i_{ch} remains zero throughout this period, and the entire load current I_0 freewheels through the diode. MOSFET blocks the entire dc bus voltage V_{dc} (see Fig. 5(a)). This stage ends when v_{gs} reaches V_{th}. Switching loss incurred in this stage E_I is zero.

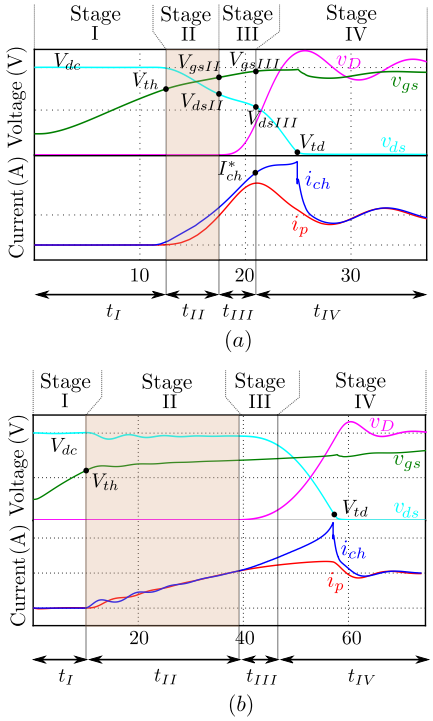


Fig. 5: Turn-on Simulation Waveforms (a) TO-247-4 Packaged SiC MOSFET (b) TO-247-3 Packaged SiC MOSFET

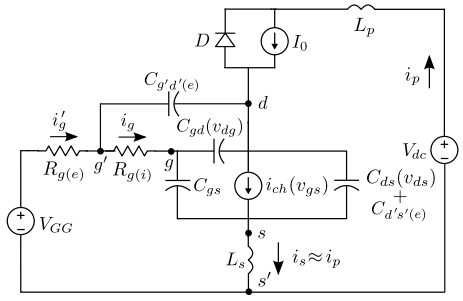


Fig. 6: Stage II Equivalent circuit

2) Stage II - Current-rise period: After v_{gs} exceeds V_{th}, i_{ch} starts to increase. In this stage, SiC MOSFET is in the saturation region, so i_{ch} is a non-linear function of v_{gs} (see (1c)). The diode D is in the forward biased condition and $v_D \approx 0$. Unlike the TO-247-3 packaged SiC MOSFET, i_p lags behind i_{ch} for the entire duration of Stage II and as a consequence, the drain-source voltage v_{ds} experiences fall in its value and does not remain constant (see Fig. 5(a) and Fig. 5(b) for TO-247-4 and TO-247-3 package devices respectively). Due to significant change in the value of v_{ds}, currents ($C_{gd}dv_{dg}/dt$ and $C_{g'd'(e)}dv_{dg'}/dt$) are induced in the gate circuit. This results in the coupled dynamics of the gate and the power loop. Note: [6] considers $i_p \approx i_{ch}$ and hence dynamics of gate and power circuit can be decoupled.

The equivalent circuit of Stage II is shown in Fig. 6. Applying KCL at node g and KVL in gate loop alongwith the approximation $(dv_{d'g'}/dt) \approx (dv_{dg}/dt)$, we get (7) where $\tau_1 = \left(R_g\left(C_{gs} + C_{gd}(v_{dg})\right) + R_{g(e)}C_{g'd'(e)}\right)$ and

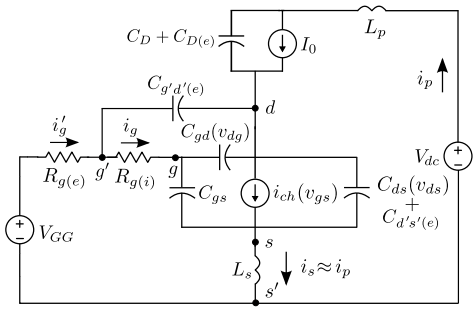


Fig. 7: Stage III Equivalent circuit

$\tau_2 = \left(R_gC_{gd}(v_{dg}) + R_{g(e)}C_{g'd'(e)}\right)$. KVL in the power loop with approximation $i_d \approx i_s \approx i_p$, (8) can be obtained. Also, applying KCL at node d with approximation $(dv_{d'g'}/dt) \approx (dv_{dg}/dt)$, (9) can be obtained.

$$V_{GG} \approx \tau_1 \frac{dv_{gs}}{dt} + v_{gs} + L_s\frac{di_p}{dt} - \tau_2\frac{dv_{ds}}{dt} \tag{7}$$

$$v_{ds} = V_{dc} - (L_p + L_d + L_s)\frac{di_p}{dt} \tag{8}$$

$$\begin{aligned}(i_d - i_{ch}) &\approx \left(C_{ds}(v_{ds}) + C_{gd}(v_{dg}) + C_{g'd'(e)} + C_{d's'(e)}\right)\frac{dv_{ds}}{dt} \\ &\approx \left(C_{oss(eq)}(v_{dg}, v_{ds})\right)\frac{dv_{ds}}{dt}\end{aligned} \tag{9}$$

Equations (7), (8) and (9) together describe the dynamics of Stage II with v_{gs}, v_{ds} and i_p being the state variables. Finite difference method (FDM) is employed to solve the coulpled dynamics. This stage ends when i_p reaches the load current I_0. t_{II} and E_{II} (given by (5)) denotes the time period and actual energy loss during this mode,. At the end of Stage II, $v_{gs} = V_{gsII}$, $i_p = I_0$ and $v_{ds} = V_{dsII}$.

3) Stage III (Intermediate period): After i_d reaches I_0, the SiC Schottky diode becomes reverse-biased and its voltage v_D begins to increase (see Stage III in Fig. 5(a)). v_{ds} drops from its initial value V_{dsII}. SiC MOSFET is in the saturation region and i_{ch} evolves according to (1c). All the state variables start changing appreciably, and the gate and the power loop are fully coupled.

The equivalent circuit of this stage is shown in Fig. 7. (7)-(9) together with (10) approximately describe the dynamics of this stage. These form a set of coupled nonlinear differential equations in the state variables v_{gs}, v_{ds}, v_D and i_p and hence, solved using FDM. This stage ends when i_p reaches its peak or $(di_p/dt) = 0$. E_{III} represents the switching loss incurred in this mode. At the end of Stage III, $v_{gs} = V_{gsIII}$ and $v_{ds} = V_{dsIII}$.

$$i_p = I_0 + (C_D(v_D) + C_{D(e)})\frac{dv_D}{dt} \tag{10}$$

4) Stage IV (Voltage-fall period): During this stage, v_{gs} remains almost constant to V_{gsIII}. The MOSFET Q still operates in the saturation and i_{ch} which follows (1c) also stays constant at I^*_{ch}. v_{ds} starts to fall sharply from its initial value V_{dsIII} (see Stage IV in Fig. 5(a)). In this stage, $i'_g \ll i_p$ and $v_D \approx V_{ds} - v_{ds}$ as the drop across the inductances L_d, L_s and

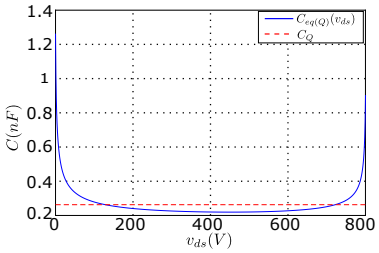


Fig. 8: $C_{eq(Q)}$ vs v_{ds} and C_Q

L_p are small compared to v_{ds} and v_D. Also, $v_{dg}, v_{dg'} \approx v_{ds}$ as v_{ds} is significantly higher than v_{gs}.

$$I_0 \approx I^*_{ch} + C_{eq(Q)}(v_{ds})\frac{dv_{ds}}{dt} \tag{11}$$

$$C_Q = \frac{1}{(V_{dsIII} - V_T)}\int_{V_T}^{V_{dsIII}} C_{eq(Q)}(v_{ds})dv_{ds} \tag{12}$$

Fig. 7 also shows the equivalent circuit of Stage IV. Using the aforementioned approximations in (9) and (10), we obtain (11) where $C_{eq(Q)}(v_{ds}) = \left(C_{oss(eq)}(v_{dg}, v_{ds}) + C_D(V_{dc} - v_{ds}) + C_{D(e)})\right)$. Note: $C_{eq(Q)}(v_{ds})$ remains constant most of this mode's duration (see Fig. 8) and hence, it can replaced by an equivalent charge related capacitance C_Q which is defined as (12). As a result of these approximations, closed form expressions of $v_{ds}(t)$, t_{IV} and hence, E_{IV} (loss incurred in this stage) can be obtained (see (13), (14) and (15) respectively). This stage ends when the SiC MOSFET enters into ohmic region.

$$v_{ds} \approx V_{dsIII} + \frac{I_0 - I^*_{ch}}{C_Q} \tag{13}$$

$$t_{IV} \approx \left(\frac{V_{dsIII} - V_T}{I^*_{ch} - I_0}\right) C_Q \tag{14}$$

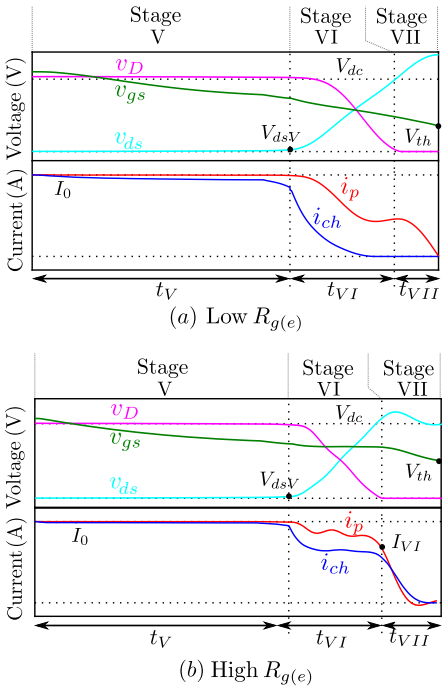
$$E_{IV} \approx \frac{1}{2}\left(V_{dsIII} + V_T\right) I^*_{ch} t_{IV} \tag{15}$$

Total switching energy loss during the turn-on switching transition is given as $E_{on} = (E_{II} + E_{III} + E_{IV})$. (di/dt) and (dv/dt) are calculated using (I_0/t_{II}) and (V_{dsIII}/t_{IV}), respectively.

B. Turn-off analytical model

Similar to the turn-on switching transition, turn-off switching transient can be divided into three stage: 1) Stage V (turn-off delay period), 2) Stage VI (Voltage-rise period) and 3) Stage VII (Current-fall period) as shown in Fig. 9.

1) Stage V - Turn-off delay period: Turn-off switching transient begins when negative gate signal of strength V_{EE} is applied to the MOSFET and it enters into Stage V. v_{gs} reduces from its initial value of V_{GG}. The MOSFET is in the ohmic region and i_{ch} has non-linear functional dependence on v_{gs} and v_{ds} (see (1b)). In this stage, power loop state variables v_D and i_p are assumed to remain constant at their respective initial values $(V_{dc} - v_{ds(on)})$ and I_0. A coupled dynamics of the gate and the power loop is considered to obtain the accurate initial conditions for the following stages [4]. Effect of L_s is neglected.



(a) Low $R_{g(e)}$

(b) High $R_{g(e)}$

Fig. 9: Turn-off Simulation waveforms

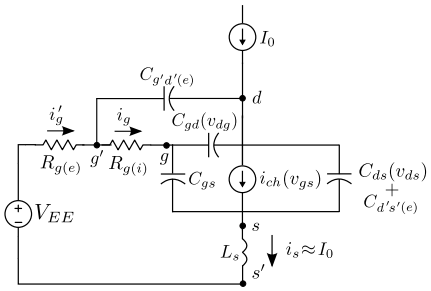


Fig. 10: Stage V Equivalent Circuit

Fig. 10 shows the equivalent circuit of this stage. $v_{dg} < 0$ for the most of the Stage V and C_{gd} is given by (2a). Applying KCL at the nodes g and d and by using the approximation that $(dv_{dg'}/dt) \approx (dv_{dg}/dt)$, we obtain the equations (16) and (17). Here, $\tau_1 = \left(R_g\left(C_{gs} + C_{gd}(v_{dg})\right) + R_{g(e)}C_{g'd'(e)}\right)$, $\tau_2 = \left(R_g C_{gd}(v_{dg}) + R_{g(e)}C_{g'd'(e)}\right)$, $\left(C_{oss(eq)}\right) = C_{ds}(v_{ds}) + C_{gd}(v_{dg}) + C_{g'd'(e)} + C_{d's'(e)}$ and $C_{gd(eq)} = C_{gd}(v_{dg}) + C_{g'd'(e)}$. The dynamics of this stage is approximately governed by two state variables v_{gs} and v_{ds}. Finite difference method is used for solving this stage. Stage V ends when the SiC MOSFET enters the saturation region.

$$V_{GG} \approx \tau_1\frac{dv_{gs}}{dt} + v_{gs} - \tau_2\frac{dv_{ds}}{dt} \tag{16}$$

$$(i_d - i_{ch}) \approx \left(C_{oss(eq)}\right)\frac{dv_{ds}}{dt} - C_{gd(eq)}\frac{dv_{gs}}{dt} \tag{17}$$

2) Stage VI - Voltage-rise period: This stage starts when the MOSFET enters saturation region. i_{ch} solely depends on v_{gs} during this stage and it falls sharply. Gate and power circuit are fully coupled. Similar to Stage III, Fig. 7 also represents the equivalent circuit of this stage. Coupled non-linear equations

TABLE I: Extracted parameter values of SiC MOSFET (C3M0075120K) and SBD (C4D10120A) pair

V_{th} (V)	K_p (A/V^2)	K_f	θ (1/V)	P_{vf}	$R_{g(i)}$ (Ω)	C_{gs} (nF)	k_1 (nF)	k_2 (V)	k_3	V_T (V)	k_4 (nF)	k_5 (V)	k_6 (nF)	k_7 (V)	k_{10} (nF)	k_{11} (V)
4.5	3.4	2.0588	0.00	0.2	9	1.39	0.55	0.6	0.4	12	0.22	0.25	1.1281	1.6	0.7535	1.7

containing state variables v_{gs}, v_{ds}, v_D and i_p approximately represents the time evolution of this stage (see (7)-(10)). Based on the values of I_0 and $R_{g(e)}$, two different scenarios can occur. For low values of I_0 and/or $R_{g(e)}$, i_{ch} collapses to zero during Stage VI (voltage rise period) (see Fig. 9(a)), whereas for high I_0 and/or $R_{g(e)}$, i_{ch} sustains during Stage VI (see Fig. 9(b)). However, the first scenario is common for TO-247-4 packaged devices due to the small value of L_s. As a result, turn-off switching losses reduces significantly.

3) Stage VII - Current-fall period: As stated in the previous subsection, this stage exists when I_0 and/or $R_{g(e)}$ are sufficiently high. The diode D is forward-biased and both i_{ch} and i_p start falling sharply. Similar to the current-rise period (Stage II), gate and power circuit are fully coupled during this stage and the (7)-(9) governs this stage's dynamics. This stage ends when v_{gs} reaches V_{th} and the SiC MOSFET enters into cut-off region. E_{VII} denotes the switching loss of this stage.

Total switching energy loss during the turn-off switching transition is given as $E_{off} = (E_V + E_{VI} + E_{VII})$. (di/dt) and (dv/dt) are calculated as (I_{VI}/t_{VII}) and (V_{dsV}/t_{VI}), respectively.

IV. Simulation and Experimental Results

Double pulse test (DPT) based experiments are performed to obtain the switching dynamics of the TO-247-4 packaged SiC MOSFET and SBD pair. Fig. 11 shows the experimental setup for the DPT. C3M0075120K (1200V, 32A) and C4D10120A (1200V, 33A) from Wolfspeed/CREE was used as the SiC MOSFET and SiC SBD respectively. The device-related parameters of the SiC MOSFET and SiC SBD extracted from their respective datasheets are provided in Table I. Gate driver voltage levels are $V_{GG} = 15V$ and $V_{EE} = -5V$. External circuit parasitics were obtained from measurement [8] and are given as $L_d = 10nH$, $L_s = 0.25nH$, $L_p = 25nH$, $C_{g'd'(e)} = 9pF$, $C_{d's'(e)} = 60pF$ and $C_{D(e)} = 40pF$. DPT experiments were conducted at $V_{dc} = 800V$ and for three values of $R_{g(e)}$ (2.5Ω, 7.5Ω, 15Ω) and three values of I_0 (10A, 20A, 30A). Note: The devices were tested at room temperature ($\approx 25^{\circ}C$).

$v_{g's'}(t)$, $v_{d's'}(t)$, and $i_p(t)$ are important waveforms for the characterization of the switching dynamics. Passive probe TPP1000 (10x, 1GHz), high voltage probe P5100A (100x, 500 MHz) and coaxial current shunt SSDN-414-10 (100mΩ, 2GHz) were used for the measurement of $v_{g's'}(t)$, $v_{d's'}(t)$, and $i_p(t)$ respectively. Mixed Signal Oscilloscope MDO3104 (1GHz, 5Gs/s) was used to capture the signals. Deskew and calibration fixture (067-1686-00) was used to match the propagation delay between the voltage and current probes before the experiment.

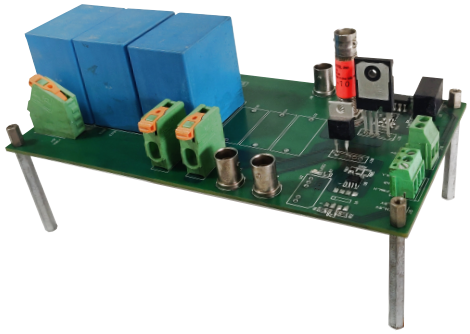


Fig. 11: DPT setup

A. Validation of Behavioral Model

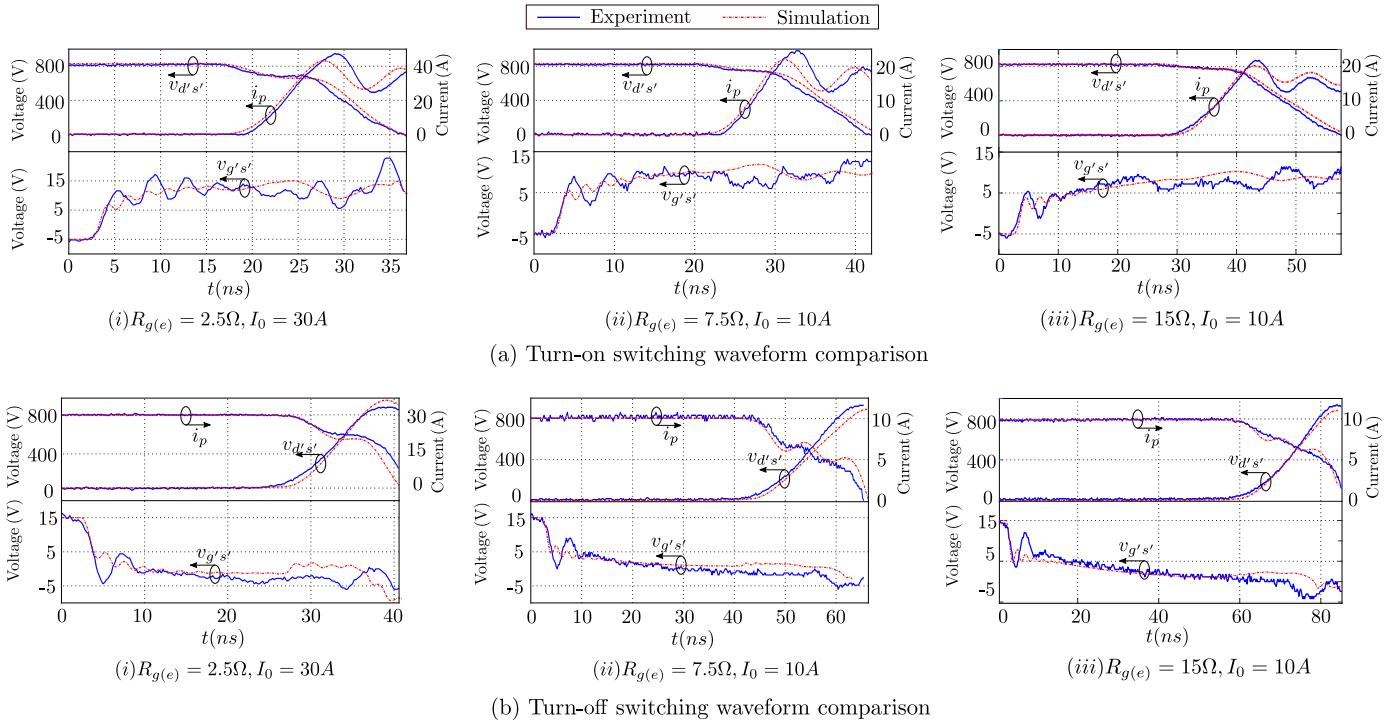
The behavioral model presented in Section II is validated through the DPT results in this subsection. The model was implemented in MATLAB/Simulink using the Simscape library. In Fig. 12(a), $v_{d's'}$, i_p and $v_{g's'}$ waveforms obtained from the DPT and simulation of the behavioral model are superimposed for the turn-on switching transitions. Similarly, Fig. 12(b) shows the comparison for the turn-off switching transition. A close agrement between the simulation and experiment are observed. The same observation also holds true for other operating conditions. This validates our behavioral model and also verifies the correctness of the parameters used in the simulation.

B. Verification of the Proposed Analytical Model

In this section, the analytical model presented in Section III is verified by using the validated behavioral model as the benchmark.

1) Actual Loss Comparison: In fig. 13(a) actual turn-on switching energy loss (E_{on}) obtained from the analytical model and the behavioral model are compared. Comparison of the actual turn-off switching energy loss (E_{off}) is presented in Fig.13(b). It can be observed that analytical model can predict the actual switching loss with good accuracy. Also, turn-on switching loss for TO-247-4 packaged devices can be observed to be significantly higher than the turn-off switching loss.

2) Switching loss comparison among DPT, simulation and analytical methods: Experimental loss (6) obtained from DPT is compared with the actual loss obtained from behavioral and the analytical methods. The validated behavioral model is taken as the benchmark as it can give the actual loss (5). The switching losses during the turn-on and the turn-off transitions obtained from the three methods are plotted against the load current I_0 in Fig. 14 (a) and (c) respectively. Their percentage error plot is given in Fig. 14(b) and (d) respectively. It can be observed that both analytical model and DPT has similar performance. Whereas analytical model results in slight over-esstimation of the turn-on loss, DPT slightly underestimates



(a) Turn-on switching waveform comparison

(b) Turn-off switching waveform comparison

Fig. 12: Comparison of behavioral model with experiment - (a) Turn-on Switching dynamics (b) Turn-off Switching dynamics

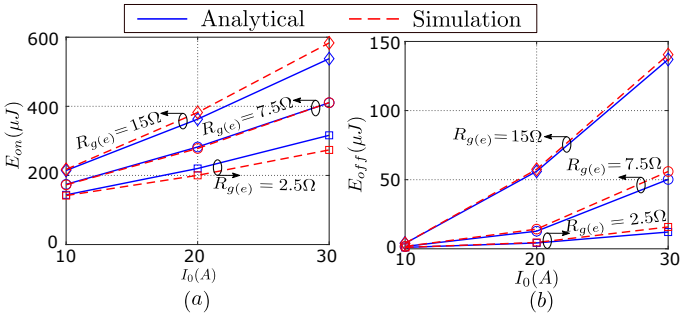


Fig. 13: Analytical model validation - Actual switching Energy Loss Comparison

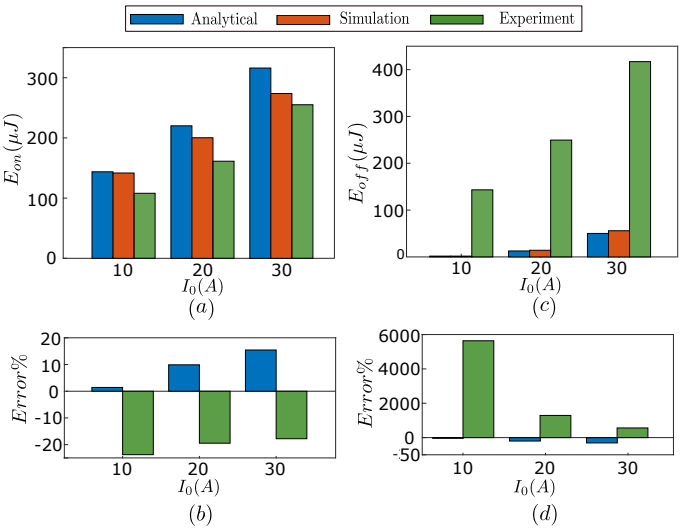


Fig. 14: Illustration on the error in switching loss estimation from DPT

it. On the other hand, high discrepancy is observed in the estimation of the turn-off switching loss by the DPT. This is due collapse of the channel current to during Mode VI (voltage-rise period) which cannot be accounted in the DPT.

3) (di/dt) and (dv/dt) comparison: Turn-on and turn-off (di/dt) obtained using behavioural simulation, analytical model and experiment are compared in Fig. 15(a) and (b), respectively. Whereas, the turn-on (di/dt) is observed to have strong correlation with the external gate resistance $R_{g(e)}$, turn-off (di/dt) shows a weak dependence on $R_{g(e)}$. This is due to the collapse of i_{ch} during the voltage-rise period (turn-off transition) for most of the operating conditions for TO-247-4 packaged devices. As a result, switching speed of the SiC MOSFET is no longer controlled by the gate circuit.

Fig. 15(c) and (d) presents a comparison of the turn-on and the turn-off (dv/dt) obtained using behavioural simulation, analytical model and experiment. It can be observed that both the turn-on and the turn-off (dv/dt) has a weak dependence on $R_{g(e)}$. Also, turn on (dv/dt) remains almost invariant with I_0 whereas the turn-off (dv/dt) increases with I_0.

V. Comparison of TO-247-4 and TO-247-3 Devices

Experimental comparison of the SiC MOSFET in TO-247-4 package (C3M0075120K) and in TO-247-3 package (C3M0075120D) is presented in this section. Fig. 16(a) and (b) respectively shows the comparison of the turn-on switching loss E_{on} and turn-off switching loss E_{off}. It can be observed that both E_{on} and E_{off} of TO-247-4 packaged devices are smaller than their TO-247-3 packaged counterpart and the difference increase with higher gate resistance. Comparison of (di/dt) and (dv/dt) rates during the turn-on and turn-

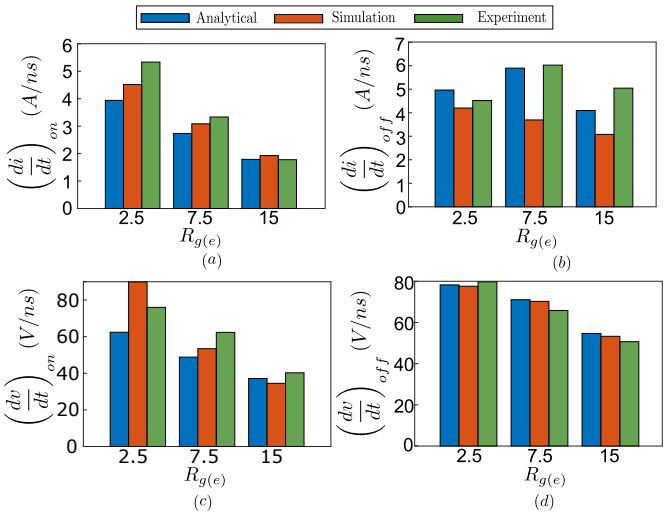


Fig. 15: Analytical model validation - Comparison of di/dt and dv/dt $[V_{dc} = 800V, I_0 = 20A]$

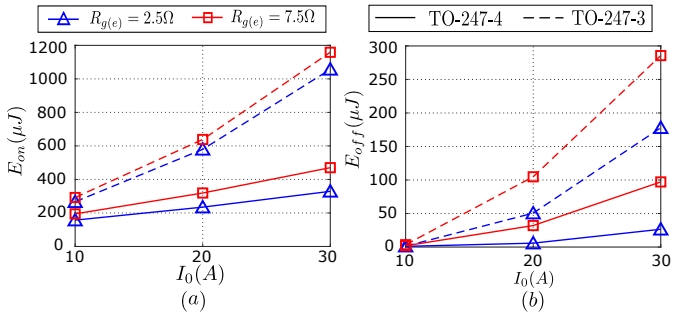


Fig. 16: Comparison of TO-247-3 and TO-247-4 devices: (a) E_{on} (b) E_{off}

off transitions are shown in Fig. 17. It can be observed that both the turn-on and the turn-off (di/dt) and (dv/dt) of TO-247-4 packaged devices are significantly higher than the TO-247-3 counterpart. Also, difference in turn-on (di/dt) and (dv/dt) between the two packages is observed to reduce with external gate resistance. It is worthwhile to note that switching dynamics of TO-247-3 packaged devices approach their TO-247-3 counterpart with the increase in gate resistance due to slower switching transitions.

VI. Conclusion

In this paper, an analytical switching transient model of terminal SiC MOSFET (TO-247-4 package) and SBD pair using datasheet parameters and external circuit parasitics is presented. This model is derived from the behavioral model. The proposed model considers the nonlinearity in the device current and capacitance characteristics and estimates (dv/dt), (di/dt), and actual switching loss. The behavioral simulation and experiment for 1.2kV SiC MOSFET and SBD pair validates the proposed model.

Unlike TO-247-3 packaged SiC MOSFETs, there can be significant difference between drain and channel current during current-rise period (Stage II) of TO-247-4 packaged devices. As a result, substantial drop in the drain-source voltage of

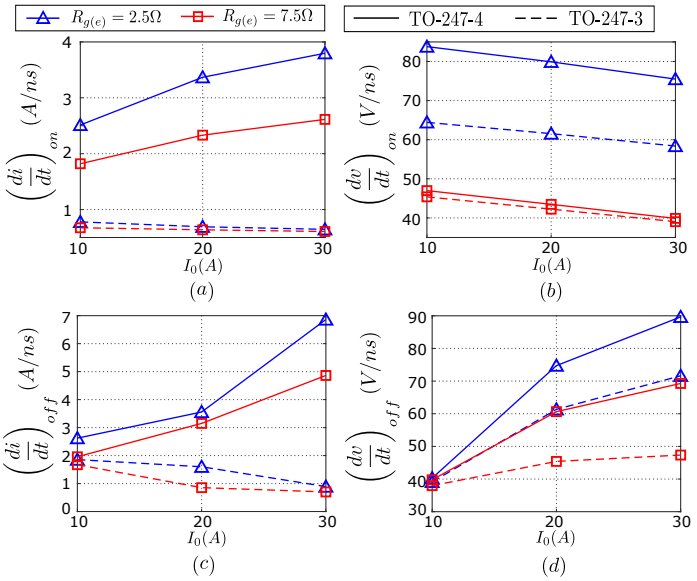


Fig. 17: Comparison of TO-247-3 and TO-247-4 devices: (a) $(di/dt)_{on}$ (b) $(dv/dt)_{on}$ (c) $(di/dt)_{off}$ (d) $(dv/dt)_{off}$

the SiC MOSFET is observed and the gate and the power loop becomes fully coupled. Also, during turn-off, channel current collapses to zero during voltage-rise period for most of the operating conditions resulting in significantly lower turn-off switching losses. Moreover, TO-247-4 devices have lower switching loss compared to similarly rated TO-247-3 device and faster (dv/dt) and (di/dt) rates due to reduced value of common source inductance in case of TO-247-4 devices.

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