An Energy based Approach to Calculate Actual Switching Loss for SiC MOSFET from Experimental Measurement

Shamibrota Kishore Roy
Electrical Engineering Department
IISc Bangalore
Bangalore, India
shamibrotar@iisc.ac.in

Kaushik Basu

Electrical Engineering Department

IISc Bangalore

Bangalore, India

kbasu@iisc.ac.in

Abstract: It is well known for SiC MOSFET that the integration of the product of experimentally measured drain current and drain-source voltage results in inaccurate estimation of switching loss. This paper presents an alternative energy based approach to accurately compute switching loss from experimentally measured waveforms. This indirect but relatively simple method requires device parameters available in data-sheet. It is derived from the behavioural model through approximations. Detailed non-linear capacitance model of the SiC MOSFET is used that results in accurate estimation of actual turn on and turn off losses. It has been verified through behavioural simulation and experiment for a SiC MOSFET and schottky barrier diode (SBD) pair for a wide range of operating conditions.

Index Terms—Hard switching, Soft switching, dead-time, Double pulse test, Modelling, SiC MOSFET

I. INTRODUCTION

SiC MOSFETs are widely used nowadays due to its superior switching, conduction and thermal performance [1]. This MOSFETs are commercially available in the voltage range of 600-1700V and try to penetrate the Si IGBT market in this voltage range.

Estimation of switching loss is important to decide the switching frequency of a power electronic converter and it is also an input to the thermal design. Experimental switching loss measurement technique such as double pulse test (DPT) is generally used to estimate the switching loss where drain current and drain-source voltage are measured in a double pulse test (DPT) and then multiplied and integrated over switching period to estimate switching loss. However, it is not possible to measure the actual switching loss using this method [2] as the device and external circuit parasitics play a significant role during switching transient of SiC MOSFET. There are different simulation based techniques like physics based simulation [3] or behavioural simulation [4], that are used to estimate the actual switching loss. However, it requires domain knowledge and expensive softwares. Analytical model proposed in some of the existing works [2], [5], [6] can

be used to estimate the actual switching loss. However, it is less accurate compared to simulation based approaches due to the approximations used. Energy based switching loss calculation technique is proposed for hard switching condition in [7] where two step approximation of the non-linear device capacitance is used. However, this will result in inaccurate estimation of actual switching loss as the device parasitic capacitances of SiC MOSFET are highly non-linear [2]. Also, the expression for estimating soft turn off switching loss is not provided.

In this paper, a energy based approach is presented where the actual turn on and turn off losses can be estimated from the experimentally measured waveforms and using the values of device and external circuit parasitics obtained from device datasheet and/or measurement. Detailed non-linear model of device capacitances are used to increase the accuracy of the proposed method. There are two different switching conditions have been studied in this paper: a) hard turn on and turn off for SiC MOSFET and Schottky diode pair, b) Soft turn off of SiC MOSFET in a bridge leg configuration. This method is derived from the behavioural model of the switching transient. It has been verified through behavioural simulation and experiment for a SiC MOSFET and SBD for a wide range of operating conditions.

The rest of the paper is arranged in the following way. First, a behavioural model to study hard and soft switching dynamics of SiC MOSFET is described in Section II. Then the proposed energy based technique is derived in section III. Details of experimental measurement set-up and results are given in Section IV. Section V draws the conclusion.

II. BEHAVIOURAL MODEL

The behavioural model for hard switching conditions is given in Fig. 1(a). This model is presented in [2] and used in this work to derive the energy based method for actual loss measurement. A buck chopper configuration is considered with Q_B as the active SiC MOSFET and SiC SBD diode D_T is the free-wheeling SiC SBD. V_{dc} is the input DC bus voltage and I_0 is the load current. Q_B is modelled as a three terminal device

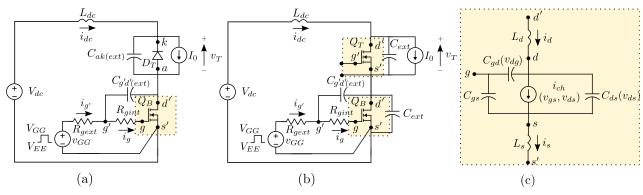


Figure 1: Circuit configuration for switching transient analysis: (a) Hard switching transient, (b) Soft switching transient, (c) Equivalent model of SiC MOSFET

$$i_{ch}(v_{gs}, v_{ds}) = \begin{cases} 0, & v_{gs} < V_{th} \\ \frac{K_p K_f \left((v_{gs} - V_{th}) v_{ds} - \left(\frac{P_{vf}^{y-1}}{y} \right) (v_{gs} - V_{th})^{2-y} v_{ds}^y \right)}{(1 + \theta(v_{gs} - V_{th}))}, & v_{gs} \ge V_{th} \quad v_{ds} < (v_{gs} - V_{th})/P_{vf} \\ \frac{K_p (v_{gs} - V_{th})^2}{2(1 + \theta(v_{gs} - V_{th}))} & v_{gs} \ge V_{th} \quad v_{ds} > (v_{gs} - V_{th})/P_{vf} \end{cases}$$

$$(1)$$

with terminals g', d' and s' as given in Fig. 1(c). Similarly D_T is modelled as two terminal device with terminals a and k.

 v_{GG} is the gate input voltage and it has two levels, V_{GG} and V_{EE} respectively. R_{gint} and R_{gext} are the internal and external gate resistances. R_{gext} is controllable and takes into account the internal resistance of gate driver IC. The SiC MOSFET is modelled as a voltage controlled current source along-with high frequency parasitic capacitances. Channel current i_{ch} is a function of gate source (v_{gs}) and drain source (v_{ds}) voltage and is given by (2) [2].

 C_{gs} , C_{gd} and C_{ds} are the gate-source, gate-drain and drain-source parasitic capacitances. C_{gs} is a constant capacitance whereas C_{gd} and C_{ds} are functions of v_{dg} and v_{ds} respectively ((2) and (3)). Diode D_T is modelled as a ideal diode in forward bias condition whereas in reverse biased condition, it is modelled as a non-linear capacitance C_D (4). Experimentally measured C_{gd} and $C_{oss} = (C_{gd} + C_{ds})$ as a function of v_{ds} are given in device datasheet. So the parameters of (2) and (3) are obtained by fitting respective equations to the experimentally measured datasheet plots. Non-linear voltage dependant capacitance C(v) can be replaced with equivalent energy related capacitance $C_{er}(V_1, V_2)$ in the voltage interval $v \in (V_1, V_2)$ given by (5).

$$C_{gd} = \begin{cases} C_{oxd} = k_1/k_3, & v_{dg} \in (-\infty, 0) \\ \frac{k_1}{\left(1 + \frac{v_{dg}}{k_2}\right)^{1/2}}, & v_{dg} \in [0, V_{td}) \\ \frac{k_1}{\left(1 + \frac{v_{dg}}{k_2}\right)^{1/2}} + k_3 & v_{dg} \in [V_{td}, \infty) \end{cases}$$

$$(2)$$

$$C_{ds}(v_{ds}) = \frac{k_6}{\left(1 + \frac{v_{ds}}{k_7}\right)^{1/2}} \tag{3}$$

$$C_D(v_D) = \frac{k_8}{\left(1 + \frac{v_D}{k_9}\right)^{1/2}} \tag{4}$$

$$C_{er}(V_1, V_2) = \frac{2}{V_2^2 - V_1^2} \int_{V_1}^{V_2} vC(v) \ dv \tag{5}$$

 L_d and L_s are the drain and source lead inductances of Q_B . L_{dc} is the power loop inductance which is contributed by the lead inductance of D_T , DC bus inductance, ESL of DC bus capacitor and the connection inductance of D_T and Q_B (it excludes L_d and L_s). $C_{g'd'(ext)}$ and $C_{ak(ext)}$ are the external parasitic capacitances across g', d' node and a, k node respectively which is solely contributed by the PCB layout. The parasitic capacitance $C_{d's'(ext)}$ is neglected as the minimum value of C_{ds} is high compared to measured $C_{d's'(ext)}$.

For capacitor assisted soft switching study, D_T is replaced with a SiC MOSFET Q_T which is similar to Q_B (see Fig. 1(b)) [8]. During dead-time, the load current free-wheels through the body diode of Q_T . The body diode of Q_T is considered as ideal in forward biased condition. When reverse biased, output capacitance (C_{oss}) of Q_T influences the switching transition and it is modelled with similar function as (4). C_{ext} is the external snubber capacitance connected across d' and s' nodes of both Q_T and Q_B . $C_{ak(ext)}$ comes in parallel with C_{ext} and its value is small compared to C_{ext} and hence neglected for capacitor assisted turn off soft switching transient study. Using experimental measurement, $v_{q's'}(t)$, $v_{d's'}(t)$ and $i_{dc}(t)$

$$E = \int_{0}^{T} v_{ds}(\tau) \left(i_{dc}(\tau) - \left(C_{gd}(v_{dg}) + C_{g'd'(ext)} \right) \frac{dv_{dg}}{d\tau} - C_{ds}(v_{ds}) \frac{dv_{ds}}{d\tau} \right) d\tau$$

$$\approx \int_{0}^{T} v_{ds}(\tau) i_{dc}(\tau) d\tau - \int_{0}^{T} \left(C_{gd}(v_{dg}) + C_{g'd'(ext)} \right) v_{dg} dv_{dg} - \int_{0}^{T} C_{ds}(v_{ds}) v_{ds} dv_{ds}$$
(6)

$$E \approx \underbrace{\int_{0}^{T} v_{d's'}(\tau) i_{dc}(\tau) \ d\tau}_{E'} - (L_d + L_s) \int_{I_1}^{I_2} i_{dc}(\tau) \ di_{dc}(\tau) - \int_{V_1}^{V_2} \left(C_{gd}(v_{dg}) + C_{g'd'(ext)} \right) v_{dg} \ dv_{dg} - \int_{V_1}^{V_2} C_{ds}(v_{ds}) v_{ds} \ dv_{ds}$$
 (7)

$$E \approx \underbrace{\int_{0}^{T} v_{d's'}(\tau) i_{dc}(\tau) \ d\tau}_{-\frac{1}{2}} - \frac{1}{2} (L_d + L_s) \left(I_2^2 - I_1^2 \right) - \frac{1}{2} \left(C_{gd(er)}(V_1, V_2) + C_{ds(er)}(V_1, V_2) + C_{g'd'(ext)} \right) \left(V_2^2 - V_1^2 \right)$$
(8)

$$E_{on} \approx \underbrace{\int_{0}^{T_{on}} v_{d's'}(\tau) i_{dc}(\tau) d\tau}_{E'.} - \frac{1}{2} (L_d + L_s) I_0^2 + \frac{1}{2} \left(C_{gd(er)}(0, V_{dc}) + C_{ds(er)}(0, V_{dc}) + C_{g'd'(ext)} \right) V_{dc}^2$$
(9)

$$E_{off} \approx \underbrace{\int_{0}^{T_{off}} v_{d's'}(\tau) i_d(\tau) d\tau}_{E'_{off}} + \frac{1}{2} (L_d + L_s) I_0^2 - \frac{1}{2} \left(C_{gd(er)}(0, V^*) + C_{ds(er)}(0, V^*) + C_{g'd'(ext)} \right) V^{*2}$$
(10)

$$E_{off(sft)} \approx \underbrace{\int_{0}^{T_{off}} v_{d's'}(\tau) i_{dc}(\tau) d\tau}_{E'_{off(sft)}} + \frac{1}{2} (L_d + L_s) I_0^2 - \frac{1}{2} \left(C_{g'd'(ext)} + C_{ext} + C_{gd(er)}(0, V^*) + C_{ds(er)}(0, V^*) \right) V^{*2}$$
(11)

are measured as it is not possible to access device internal nodes g, d and s. In conventional loss measurement using DPT, switching loss is calculated using the expression given in (12) where T is the switching transition time. On the other hand, the actual switching loss happens inside the MOSFET channel during switching transition. So the actual switching loss is given as (13) which requires time evolution of i_{ch} and v_{ds} . Due to fast switching transient of SiC MOSFET, impact of parasitics are significant. So i_{ch} and v_{ds} can not me measured experimentally and there can be significant difference between E and E'.

$$E' = \int_0^T v_{d's'}(\tau) i_{dc}(\tau) d\tau$$
 (12)

$$E = \int_0^T v_{ds}(\tau) i_{ch}(\tau) d\tau \tag{13}$$

III. ENERGY BASED METHOD FOR ACTUAL SWITCHING LOSS ESTIMATION

The objective of this section is to estimate the actual switching loss (E) using experimentally measured E' for both hard switched and soft turn off conditions. The estimation technique requires values of L_d , L_s , $C_{gd}(v_{dg})$ and $C_{ds}(v_{ds})$. Values of $C_{gd}(v_{dg})$ and $C_{ds}(v_{ds})$ can be obtained from device datasheet whereas L_d ans L_s is given in Spice model of the device or can be experimentally measured [9]. Actual loss estimation for hard switching and turn off soft switching are discussed separately.

A. Actual loss estimation for hard switched SiC MOSFET and SBD pair

In this subsection, the method for calculating actual hard switching loss from the experimental measurement is proposed. Applying KCL at node d' and d of Fig. 1 and add these two equations, we get (14), which can be approximated as (15) as $v_{g'd'} \approx v_{gd}$. Applying KCL at s' node, we get $i_s = (i_{dc} + i_{g'})$. As $i_{g'} \ll i_{dc}$, $i_{dc} \approx i_s$. Similarly, $i_s = (i_d + i_g)$ and $i_g \ll i_d$, so $i_d \approx i_s \approx i_{dc}$. Applying KVL across d', d, s and s' nodes of Q_B with approximation $i_d \approx i_s \approx i_{dc}$, we get (16).

$$(i_{dc} - i_{ch}) = C_{ds}(v_{ds}) \frac{dv_{ds}}{dt} + C_{gd}(v_{dg}) \frac{dv_{dg}}{dt} + C_{g'd'(ext)} \frac{dv_{d'g'}}{dt}$$
(14)

$$(i_{dc} - i_{ch}) \approx C_{ds}(v_{ds}) \frac{dv_{ds}}{dt} + (C_{gd}(v_{dg}) + C_{g'd'(ext)}) \frac{dv_{dg}}{dt}$$
 (15)

$$v_{d's'} \approx v_{ds} + (L_d + L_s) \frac{di_{dc}}{dt} \tag{16}$$

Now, replacing the expressions for i_{ch} (15) to (13), the expression for actual loss E can be written as (6). Now replacing the expression of v_{ds} from (16), (6) is reduced to (7) where $i \in (I_1, I_2)$ and $v_{dg}, v_{ds} \in (V_1, V_2)$ for $t \in (0, T)$. Using (5), (7) can be written as (8) where $C_{gd(er)}$ and $C_{ds(er)}$ are the energy related capacitances in $v \in (V_1, V_2)$. Time evolution of $v_{d's'}$ and i_{dc} during switching transient is obtained through experimental measurement. The initial and final conditions for hard turn on and turn off conditions are different. So the expressions of actual turn on and turn off losses (E_{on}) and E_{off} are given below separately.

V_{th} (V)	K_p (A/V ²)	K_f	θ (1/V)	P_{vf}	$R_{gint} \ (\Omega)$	C_{gs} (nF)	k ₁ (nF)	k ₂ (V)	k_3	V_{td} (V)	k ₄ (nF)	k ₅ (V)	k ₆ (nF)	k ₇ (V)	k ₈ (nF)	(V)
5.6	1.6	2.19	0.4	0.01	4.6	0.95	0.95	0.35	0.71	12	0.12	0.025	0.79	5.5	0.75	1.7

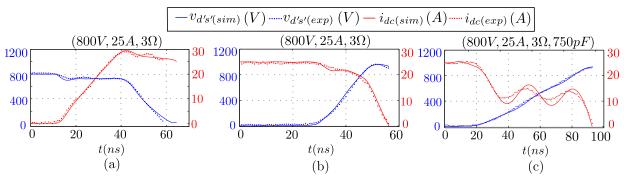


Figure 2: Simulation vs experimental waveforms, (a) Hard Turn-on, (b) Hard Turn-off, (c) Soft Turn-off

- 1) Hard Turn on switching loss calculation: Initial Condition: $t=0,\ i_{dc}=0,\ v_{ds}\approx v_{dg}=V_{dc}$. Final condition: $t=T_{on},\ i_{dc}=I_0,\ v_{ds}\approx v_{dg}=0$. Using these initial and final conditions, (8) can be simplified to (9).
- 2) Hard turn off switching loss calculation: Initial Condition: $t=0,\ i_d=I_0,\ v_{ds}\approx v_{dg}=0$. Final condition: $t=T_{off},\ i_{dc}=0,\ v_{ds}\approx v_{dg}=V^*.\ V^*$ is close to V_{dc} and $v_{d's'}(t=T_{off})$ obtained from experimental measurement is used as V^* . Using these initial and final conditions, (8) can be simplified to (10).

B. Actual turn off loss estimation for soft switched SiC MOS-FET

In zero voltage switching (ZVS) converters, turn on loss is negligible and switching loss is mostly contributed by the turn off loss [10]. Through C_{ext} , turn off switching loss can be significantly reduced. Similar to hard turn off loss, the actual switching loss for soft turn off condition can be calculated using (11).

IV. EXPERIMENTAL SET-UP AND RESULTS



Figure 3: Experimental Set-up

Double pulse test (DPT) is used to experimentally measure $v_{d's'}$ and i_{dc} (see Fig. 3). DPT set-up is rated for 800V DC bus voltage and 30A load current. SiC MOSFET C2M0080120D

(1200V, 36A) and SiC SBD C4D10120A (1200V, 33A) are used for experiment (both devices are from Wolfspeed). The device related parameters are extracted from device datasheet and it is given in Table I.

Opto-isolator IX3180GS followed by a current booster IXDN609SI is used to drive the gate of the SiC MOSFET. Gate driver parameters: $V_{CC}=-5V$, $V_{GG}=20V$, $R_{gext}=3,5,9\Omega$; external circuit parasitics required for actual loss calculations: $L_d=6nH$ $L_s=7nH$, $L_{dc}=45nH$ and $C_{g'd'(ext)}=15pF$. Operating conditions are $V_{dc}=800V$ and $I_0=5-25A$ in steps of 5 amperes. $C_{ext}=750pF$ is used for turn off soft switching study.

Experimentally measured signals are $v_{g's'}(t)$, $v_{d's'}(t)$ and $i_{dc}(t)$. Oscilloscope MDO3104 from Tektronix with 1 GHz bandwidth is used for measurement. $v_{g's'}(t)$ measurement is done using a passive probe from Tektronix with 1 GHz bandwidth (TPP1000). A high voltage single ended probe from Tektronix (P5100A) with 500 MHz bandwidth is used for $v_{d's'}(t)$ measurement. Current $i_{dc}(t)$ is measured using a AC/DC current probe from Tektronix (TCP0030A) with 120 MHz bandwidth and 50A peak current measurement capability. Matching of propagation delay between voltage and current signals are done using a delay matching instrument available from Tektronix (067-1686-00, Power Measurement De-skew and Calibration Fixture).

MATLAB/Simulink[®] is used to simulate the behavioural model. All the experiments are performed at room temperature ($\approx 25^{\circ}$ C).

In Fig. 2, $v_{d's'}(t)$ and $i_{dc}(t)$ obtained from behavioural simulation (using MATLAB/Simulink®) and experiment are plotted for three different conditions (hard turn on, turn off and soft turn off). Similarly, experimentally obtained E' (E'_{exp}) and E' obtained using behavioural simulation (E'_{sim}) are compared in TABLE III for hard turn on, turn off and soft turn off conditions. There are close match observed between simulated and experimental results. This verifies that the

Table II: E_{off} calculation using (10) for $V_{dc}=800V$, $I_0=20A$ and $R_{gext}=3\Omega$

$\overline{I_0}$ (A)	$E'_{off} (\mu J)$	V* (V)	$(L_d + L_s)$ (nH)	$C_{g'd'(ext)}$ (pF)	$C_{gd(er)}(0,V^*)$ (pF)	$C_{ds(er)}(0,V^*)$ (pF)	$E_{off} (\mu J)$
20	108.3	980	13	15	9.84	77.8	62.03

behavioural simulation can accurately capture the switching transition for both hard and soft switching conditions.

Table III: Comparison of E'

I_0		Hard Swit	Soft Turn-off (μJ)				
(A)	Tur	n on	Tur	n off	$(C_{ext} = 750pF)$		
	E'_{exp}	E'_{sim}	E'_{exp}	E'_{sim}	$\mid E'_{exp} \mid$	E'_{sim}	
5	67	72.7	42	39	297	261	
15	202	212	69.4	65	347.3	312	
25	322	311	134.7	153.42	402	383	

Table IV: Comparison of E

I_0	ŀ	Hard Switch	Soft Turn-off (μJ)				
(A)	Turi	n on	Turi	n off	$(C_{ext} = 750pF)$		
	E_{sim}	E_{on}	E_{sim}	E_{off}	$\mid E_{sim} \mid$	E_{sft}	
10	167.22	161.41	0.8	15.52	1	2.7	
15	245.9	236.1	20.66	25.76	3	10.9	
20	343.3	354.49	63.5	62.03	7	25.5	

In TABLE IV, E obtained using the proposed energy based method (E_{on}, E_{off}) and E_{sft} for hard turn on, turn off and soft turn off conditions respectively) are compared with the E obtained from behavioural simulation (E_{sim}) . It can be observed from the results that the actual loss numbers obtained from proposed method matches with behavioural simulation well except for the hard turn off loss for low current $(I_0 = 10A)$. Also, the soft turn off loss numbers estimated using the proposed method is high compared to the actual loss numbers obtained from behavioural simulation. A sample calculation of estimating E_{off} using (10) is shown in TABLE II.

V. CONCLUSION

A method to estimate the actual switching loss for SiC MOSFET and Schottky diode pair for hard switching condition and soft turn off loss for SiC MOSFET in a half bridge configuration is proposed in this paper. The proposed technique uses the experimentally measured drain-source voltage and drain current waveforms along-with the device parasitic inductances and non-linear voltage dependent capacitances as inputs. It has been validated using behavioural simulation for a 1200V SiC MOSFET and schottky diode pair for a wide range of operating conditions.

It can be observed that the proposed technique can estimate the hard turn on switching loss quite accurately. For low load currents, hard turn off loss is small and the proposed technique somewhat overestimates the loss. Similar thing has be observed for soft turn off loss for the entire current range.

REFERENCES

- C. D. Fuentes, S. Kouro, and S. Bernet, "Comparison of 1700-v sic-mosfet and si-igbt modules under identical test setup conditions," *IEEE Transactions on Industry Applications*, vol. 55, no. 6, pp. 7765–7775, 2019
- [2] s. k. roy and K. Basu, "Analytical model to study hard turn off switching dynamics of sic mosfet and schottky diode pair," *IEEE Transactions on Power Electronics*, pp. 1–1, 2020.
- [3] X. Li, X. Li, P. Liu, S. Guo, L. Zhang, A. Q. Huang, X. Deng, and B. Zhang, "Achieving zero switching loss in silicon carbide mosfet," *IEEE Transactions on Power Electronics*, vol. 34, no. 12, pp. 12193– 12199, 2019.
- [4] Z. Duan, T. Fan, X. Wen, and D. Zhang, "Improved sic power mosfet model considering nonlinear junction capacitances," *IEEE Transactions* on *Power Electronics*, vol. 33, no. 3, pp. 2509–2517, 2018.
- [5] S. K. Roy and K. Basu, "Analytical estimation of turn on switching loss of sic mosfet and schottky diode pair from datasheet parameters," *IEEE Transactions on Power Electronics*, vol. 34, no. 9, pp. 9118–9130, 2019.
- [6] D. Christen and J. Biela, "Analytical switching loss modeling based on datasheet parameters for mosfets in a half-bridge," *IEEE Transactions* on *Power Electronics*, vol. 34, no. 4, pp. 3700–3710, 2019.
- [7] X. Wang, Z. Zhao, K. Li, Y. Zhu, and K. Chen, "Analytical methodology for loss calculation of sic mosfets," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 1, pp. 71–83, 2019.
- [8] S. k. Roy and K. Basu, "Analytical model to study turn off soft switching dynamics of sic mosfet in a half-bridge configuration," *IEEE Transactions on Power Electronics*, pp. 1–1, 2021.
- [9] S. K. Roy and K. Basu, "Measurement of important circuit parasitics for switching transient analysis of sic mosfet and schottky diode pair," in 2019 IEEE Energy Conversion Congress and Exposition (ECCE), 2019, pp. 1948–1952.
- [10] B. Liu, P. Davari, and F. Blaabjerg, "An optimized hybrid modulation scheme for reducing conduction losses in dual active bridge converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2019.