# Effects of Parasitics on An Active Clamp Assisted Phase Shifted Full Bridge Converter Operation 

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#### Abstract

The phase-shifted full bridge (PSFB) converter is widely used for isolated DC-DC applications due to simple control and zero voltage switching (ZVS) capability. The ZVS is achieved with the help of primary bridge device capacitances and transformer leakage inductance. The secondary diode parasitic capacitances cause high voltage stress and affect the converter voltage gain. In literature, several snubber circuits are presented to clamp the voltage overshoot, but the change in voltage gain due to secondary diode capacitances is ignored. In this paper the operation of PSFB with an active clamp is analysed considering all circuit parasitics including transformer leakage inductance, primary device and secondary diode capacitances. A closed form expression of the voltage gain is analytically derived. It is observed that the voltage gain is independent of snubber clamp voltage. Other than the known duty cycle loss due to leakage inductance, the output voltage has a duty cycle gain due to secondary diode capacitance. The paper also presents an estimation technique of key parasitics through experiment. These findings are essential for the design of a PSFB particularly for high-step-up application. A prototype of 1.5 kW with input 400 V and output 1.25 kV is built and tested. Key experimental results are shown to verify the presented analysis of PSFB considering all parasitics.


Index Terms-Phase-shifted full bridge, parasitics, leakage inductance, device output capacitance, active clamp, ZVS.

## I. Introduction

The phase shifted full bridge (PSFB) converter is widely popular for medium power isolated DC-DC applications [1][8]. Active and zero are the two operational states of PSFB [9]. In the active state, power is transferred from input to output port whereas power free-wheels in zero state. The PSFB has some attractive features like- simple duty-cycle control, zero voltage switched primary bridge without additional snubber and linear relationship of the steady-state voltage gain with duty ratio. Ideally for a given dc bus, the gain is independent of load and can be controlled linearly by varying duty-ratio. The transformer leakage inductance and device capacitances help to achieve ZVS of the converter.

But the PSFB has few major limitations. The ZVS depends on load current. Secondary diodes experience high voltage stress at the end of zero to active state transition due to parasitic resonance. In literature, several active [10], [11] and passive [12], [13] snubber circuits are given to limit the voltage stress. Additionally in zero to active state transition due to transformer leakage inductance, the rectifier output voltage remains zero during the diode bridge current commutation.

This results in significant duty cycle loss. These effects of the parasitics were analysed in details in the existing PSFB literature [9], [10]. The zero voltage (ZVS) transitions considering primary device capacitances and transformer leakage inductance were investigated.

In the existing analysis, the effects of secondary diode capacitances are either ignored or only considered to explain the secondary voltage overshoot phenomena [9], [12]. It is observed that the PSFB voltage gain is affected by the secondary diode capacitances. Additionally, due to the secondary diode capacitances the primary current falls significantly during active to zero state transition which otherwise is assumed to remain constant in ideal operation. The reduced current in zero state further affects soft-switching. The above effects are dominant in a step-up PSFB due to large leakage inductance and large reflected diode capacitances. Hence the existing analysis is incomplete and the PSFB operation with all dominant parasitics needs to be explored.


Fig. 1. PSFB converter with circuit parasitics and active snubber.
This paper presents a detailed circuit analysis of PSFB operation considering all dominant parasitics including transformer leakage inductance, primary device and secondary diode capacitances. A commonly used active snubber [10] is employed at the secondary. The major contributions and key observations are as follows. (i) A closed form expression of average output voltage is derived. (ii) Other than the wellknown duty cycle loss in the average output voltage due to transformer leakage inductance, a duty cycle gain due to secondary parasitic capacitances is observed. (iii) The average output voltage is independent of the active clamp voltage. (iv) An analytical expression of primary current in zero state is provided. This helps to properly select the dead-time for soft-
switching. (v) The paper also presents an estimation technique of key parasitics through experiment. The mode by mode converter operation is verified experimentally with a 1.5 kW , $400 \mathrm{~V}-1.25 \mathrm{kV}$ PSFB prototype. The expressions derived in this paper helps in optimally design the converter.

The paper is organised as follows. The converter operation considering parasitics is presented in Section II. In Section III an analytical closed form expression of the output voltage is given. Estimation methods of the converter parasitics are discussed in section IV. Key experimental results are presented in section V to verify the converter operation.

## II. Circuit operation and DC analysis

In Fig. 1, a PSFB converter is shown. Fig. 2a presents the ideal waveforms of the converter (without considering any parasitic). $v_{p}$ and $i_{p}$ are transformer primary voltage and current respectively. $v_{l}$ is the diode bridge output voltage. An active clamp circuit with clamp voltage $V_{C}$ is employed after the diode bridge. The snubber capacitor is large enough so that it can be modelled as a voltage source $V_{C}$. The snubber device $\left(S_{s n b}\right)$ is switched at low frequency to maintain charge balance of the snubber capacitor. In a normal switching cycle $S_{s n b}$ is kept OFF. The design of the snubber is given in [14]. The parasitics considered in the analysis are given as follows- primary device capacitance $\left(C_{C E}\right)$, secondary diode capacitance $\left(C_{D}\right)$, transformer leakage inductance referred to primary $(L)$ and snubber device parasitic capacitance $\left(C_{s n b}\right)$. The snubber branch has effective capacitance $C_{s n b}$ as the snubber capacitance is relatively large. Over a transformer flux balance cycle $\left(T_{s}\right)$, the PSFB has two active and two zero states. The converter operation is symmetrical over $T_{s} / 2$ and has 9 modes. The primary switches have gating signals $\left(G_{1}-G_{4}\right)$ with period $T_{s}$ and $50 \%$ duty ratio. Key waveforms over $T_{s} / 2$ are shown in Fig. 2b. The output filter inductor current is modelled as a constant sink, $I_{o}$ with negligible ripple.


Fig. 2. Waveforms- (a) considering ideal operation of PSFB, (b) considering circuit parasitics

The converter is in zero state when $t<t_{0}$ (Fig. 2b) as $S_{2}$ and $D_{4}$ are in conduction, shorting the transformer primary terminals $\left(v_{p}=0\right)$. In secondary all four diodes are conducting. The primary current is given as $i_{p}(t) \approx-\left(n I_{o}-\frac{V_{d c}}{\sqrt{L / C_{S}}}\right)$ and is derived in Mode 8. where $C_{S}=n^{2}\left(2 C_{D}+C_{s n b}\right)$ and $n$ is the transformer secondary to primary turns ratio.

## A. Mode 1: $t_{0}<t<t_{1}$

This mode starts when $S_{2}$ is turned off at $t=t_{0}$. Due to presence of switch capacitance $C_{C E}$, voltage across the device cannot change immediately. Channel current through the device falls first and then the device drain to source voltage starts rising. So, turn OFF of $S_{2}$ is a zero voltage switching (ZVS) transition. As the magnitude of $i_{p}$ is lower than load current $n I_{o}$ (see Fig. 2b), all four diodes of the secondary rectifier are in conduction, shorting the transformer secondary. The equivalent circuit during this mode is shown in Fig. 3a. $C_{P}=2 C_{C E}$ is the effective primary side capacitance. Solving


Fig. 3. Equivalent Circuits in (a) Mode 1, (b) Mode 2
the $L-C$ dynamics with initial conditions- $i_{p}\left(t_{0}\right) \approx-n I_{o}+$ $\frac{V_{d c}}{\sqrt{L / C_{S}}}$ and $v_{p}\left(t_{0}\right)=0, i_{p}$ and $v_{p}$ are given in (1).

$$
\begin{align*}
& i_{p}(t) \approx\left(-n I_{o}+\frac{V_{d c}}{\sqrt{L / C_{S}}}\right) \cos \left(\omega_{1}\left(t-t_{0}\right)\right) \\
& v_{p}(t) \approx\left(n I_{o}-\frac{V_{d c}}{\sqrt{L / C_{S}}}\right) \sqrt{\frac{L}{C_{P}}} \sin \left(\omega_{1}\left(t-t_{0}\right)\right)  \tag{1}\\
& t_{I}=\left(t_{1}-t_{0}\right)=\sqrt{L C_{P}} \sin ^{-1}\left(\frac{\frac{V_{d c}}{\sqrt{L / C_{P}}}}{n I_{o}-\frac{V_{d c}}{\sqrt{L / C_{S}}}}\right)
\end{align*}
$$

where $\omega_{1}=\frac{1}{\sqrt{L C_{P}}}$. The device voltages are given as $v_{S_{1}}=$ $\left(V_{d c}-v_{p}\right)$ and $v_{S_{2}}=v_{p}$. This mode ends at $t_{1}$ when $v_{p}$ reaches $V_{d c}$ and anti-parallel diode of $S_{1}$ is forward biased. The time interval for Mode $1\left(t_{I}\right)$ is given in (1). This mode will end if $\frac{V_{d c}}{\sqrt{\frac{L}{C_{P}}}\left(n I_{o}-\frac{V_{d c}}{\sqrt{L / C_{S}}}\right)}<1$ (using (1)). The above condition can further be simplified as $\frac{V_{d c}}{n I_{o}} \frac{\sqrt{C_{P}}+\sqrt{C_{S}}}{\sqrt{L}}<1$. In case of a step-up PSFB with large $L$, typically at rated load, $\frac{V_{d c}}{n I_{o}} \frac{\sqrt{C_{P}}+\sqrt{C_{S}}}{\sqrt{L}} \ll 1$. And hence following approximations are made. $t_{I} \approx \frac{V_{d c} C_{P}}{n I_{o}}$ and $i_{p}\left(t_{1}\right) \approx-n I_{o}+\frac{V_{d c}}{\sqrt{L / C_{S}}}$. Meaning, $i_{p}$ remains almost same, leading to a linear change in the capacitor voltage ( $v_{p}$ ).

## B. Mode 2: $t_{1}<t<t_{2}$

In this mode the anti-parallel diodes of $S_{1}$ and $S_{4}$ ( $D_{1}$ and $D_{4}$ ) are in conduction. As the applied voltage $v_{p}$ is against the direction of $i_{p}$, it falls linearly. Equivalent circuit during
this mode is shown in Figure 3b. The primary current is given as in (2).

$$
\begin{equation*}
i_{p}(t) \approx-n I_{o}+\frac{V_{d c}}{\sqrt{L / C_{S}}}+\frac{V_{d c}}{L}\left(t-t_{1}\right) \tag{2}
\end{equation*}
$$

To ensure ZVS turn ON, the gating pulse of $S_{1}$ is applied in this mode when the anti-parallel diode is in conduction. At the end of this mode $i_{p}$ becomes zero and changes the direction. The interval of this mode can be estimated solving (2) and is given as $t_{I I}=t_{2}-t_{1} \approx\left(n I_{o}-\frac{V_{d c}}{\sqrt{L / C_{S}}}\right) \frac{L}{V_{d c}}$. The ZVS turn ON of $S_{1}-S_{2}$ can be ensured when the dead time $(D T)$ is $t_{I} \leq D T \leq\left(t_{I}+t_{I I}\right)$.

## C. Mode 3: $t_{2}<t<t_{3}$

In this mode, $S_{1}$ and $S_{4}$ are conducting and $i_{p}$ changes linearly with same slope as in the previous mode. Equivalent circuit during this mode is shown in Figure 3b. The primary current $i_{p}(t)$ is given as $i_{p}(t)=\frac{V_{d c}}{L}\left(t-t_{2}\right)$. In secondary, the current is transferred linearly from $D_{6}, D_{7}$ to $D_{5}, D_{8}$. This mode ends at $t_{3}$ when $i_{p}$ reaches $n I_{o}$ and $D_{6}$ and $D_{7}$ are reverse biased. The time interval is given as $t_{I I I}=t_{3}-t_{2}=$ $\frac{n L I_{o}}{V_{d c}}$.

## D. Mode 4: $t_{3}<t<t_{4}$

As $D_{5}, D_{8}$ are conducting, the capacitances across reverse biased diodes $D_{6}, D_{7}$ are in parallel with the series combination of $C$ and $C_{s n b}$ (see Fig. 1). As $C \gg C_{s n b}$, $\frac{C C_{s n b}}{C+C_{\text {snb }}} \simeq C_{s n b}$. Hence the effective capacitance seen from primary is $C_{S}=n^{2}\left(2 C_{D}+C_{s n b}\right)$. The transformer leakage inductance $(L)$ and $C_{S}$ form a resonating circuit as shown in Figure 4a. The initial values of $i_{p}$ and $v_{l}^{\prime}$ are $i_{p}\left(t_{3}\right)=n I_{o}$ and


Fig. 4. Equivalent Circuits in (a) Mode 4, (b) Mode 5
$v_{l}^{\prime}\left(t_{3}\right)=0$. where $v_{l}^{\prime}$ is the rectifier output voltage referred to primary and $n v_{l}^{\prime}=v_{l} . i_{p}(t)$ and $v_{l}^{\prime}(t)$ are given as

$$
\begin{align*}
i_{p}(t) & =n I_{o}+\frac{V_{d c}}{\sqrt{L / C_{S}}} \sin \left(\omega_{2}\left(t-t_{3}\right)\right)  \tag{3}\\
v_{l}^{\prime}(t) & =V_{d c}\left[1-\cos \left(\omega_{2}\left(t-t_{3}\right)\right)\right]
\end{align*}
$$

where $\omega_{2}=\frac{1}{\sqrt{L C_{S}}}$. At $t=t_{4}^{\prime}, v_{l}$ reaches $n V_{d c}$. The duration $t_{4}^{\prime}-t_{3}=\frac{\pi \sqrt{L C_{S}}}{2}$. This mode ends at $t=t_{4}$ when $v_{l}$ reaches $V_{C}$ and $D_{s n b}$ is forward biased. Solving (3), the duration of Mode 4 is given as $t_{I V}=t_{4}-t_{3}=$ $\sqrt{L C_{S}} \cos ^{-1}\left(1-\frac{V_{C}}{n V_{d c}}\right)$. And $i_{p}$ at the end of this mode is given as $i_{p}\left(t_{4}\right)=n I_{o}+\sqrt{\frac{V_{C}}{n}\left(2 V_{d c}-\frac{V_{C}}{n}\right) \frac{C_{S}}{L}}$. Due to the
active snubber $V_{C} \simeq V_{d c}$. Hence $t_{I V}$ can be approximated as $\frac{\pi \sqrt{L C_{S}}}{2}$.
E. Mode 5: $t_{4}<t<t_{5}$

In this mode the active clamp circuit is in operation as $D_{s n b}$ is forward biased. $v_{l}$ is clamped to $V_{C}$. Equivalent circuit during this mode is shown in Fig. 4b. In this duration $i_{p}$ and $v_{l}^{\prime}$ are given as

$$
\begin{align*}
i_{p}(t) & =i_{p}\left(t_{4}\right)-\frac{V_{C} / n-V_{d c}}{L}\left(t-t_{4}\right)  \tag{4}\\
v_{l}^{\prime}(t) & =V_{C} / n
\end{align*}
$$

$i_{p}$ falls linearly. This mode ends at $t=t_{5}$ when $i_{p}(t)$ reaches $n I_{o}$ and current through $D_{\text {snb }}$ becomes zero. Using (4), the time interval $t_{V}$ is given as

$$
\begin{equation*}
t_{V}=t_{5}-t_{4}=\frac{\sqrt{V_{C}\left(2 n V_{d c}-V_{C}\right)}}{V_{C}-n V_{d c}} \sqrt{L C_{S}} \tag{5}
\end{equation*}
$$

As the active snubber is used to reduce the voltage stress, it is desired to operate $V_{C}$ close to $n V_{d c}$. Hence $\left(V_{C}-n V_{d c}\right)^{2} \ll$ $\left(n V_{d c}\right)^{2}$. So (5) can be approximated as $t_{V} \approx \frac{n V_{d c} \sqrt{L C_{S}}}{V_{C}-n V_{d c}}$.

## F. Mode 6: $t_{5}<t<t_{6}$

This is an active power transfer mode. Equivalent circuit during this mode is shown in Fig. 5a. In this mode $i_{p}$ and $v_{l}^{\prime}$


Fig. 5. Equivalent Circuits in (a) Mode 6, (b) Mode 7
can be expressed as

$$
\begin{align*}
i_{p}(t) & =n I_{o}-\frac{\left(V_{C} / n-V_{d c}\right)}{\sqrt{L / C_{S}}} \sin \left(\omega_{2}\left(t-t_{5}\right)\right)  \tag{6}\\
v_{l}^{\prime}(t) & =V_{d c}+\left(V_{C} / n-V_{d c}\right) \cos \left(\omega_{2}\left(t-t_{5}\right)\right)
\end{align*}
$$

Here power transfer happens with the DC components $n I_{o}$ and $V_{d c}$. The link voltage, $v_{l}(t)=n v_{l}^{\prime}(t)$ oscillates around $n V_{d c}$ with an amplitude of $V_{C}-n V_{d c}$. Due to lossy elements of the practical circuit, the oscillation dies down and $v_{l}$ and $i_{p}$ settle to $n V_{d C}$ and $n I_{o}$ respectively. This mode ends at $t_{6}$ when $S_{4}$ is turned OFF. The duration, $t_{V I}$ is given as$t_{V I}=\left(t_{6}-t_{5}\right)=d T_{s} / 2-t_{I}-t_{I I}-t_{I I I}-t_{I V}-t_{V}$ where $\frac{d T_{s}}{2}$ is the duration of active power transfer (see Fig. 2a) and $d$ is the duty ratio. Here it is defined as the time between turn OFF of $S_{2}$ to turn OFF of $S_{4}$.

## G. Mode 7: $t_{6}<t<t_{7}$

After $S_{4}$ is turned OFF at $t=t_{6}$, the voltage across it cannot change immediately due to switch capacitance $C_{C E}$. Channel current through the device falls before any change in device drain to source voltage which results in ZVS turn OFF of $S_{4}$. Equivalent circuit in this mode is shown in Fig. 5b. The
voltage across the devices are $v_{S_{3}}=v_{p}$ and $v_{S_{4}}=V_{d c}-v_{p}$. In this mode $i_{p}(t), v_{p}(t)$ and $v_{l}^{\prime}(t)$ are given as
$i_{p}(t)=\frac{n I_{o}}{C_{P}+C_{S}}\left[C_{P}+C_{S} \cos \left(\omega_{3}\left(t-t_{6}\right)\right)\right]$
$v_{p}(t)=V_{d c}-\frac{n I_{o}}{\left(C_{P}+C_{S}\right)}\left[\left(t-t_{6}\right)+\frac{1}{\omega_{3}}\left(\frac{C_{S}}{C_{P}}\right) \sin \left(\omega_{3}\left(t-t_{6}\right)\right)\right]$
$v_{l}^{\prime}(t)=V_{d c}-\frac{n I_{o}}{C_{P}+C_{S}}\left[\left(t-t_{6}\right)-\frac{1}{\omega_{3}} \sin \left(\omega_{3}\left(t-t_{6}\right)\right)\right]$
where $\omega_{3}=\frac{1}{\sqrt{L\left(C_{P} C_{S} /\left(C_{P}+C_{S}\right)\right)}}$. Third order dynamics are observed in the expressions of $v_{p}$ and $v_{l}^{\prime}$. This mode ends at $t=t_{7}$ when $v_{p}$ reaches 0 and $D_{3}$ is forward biased. It is observed that with large leakage and at rated load, the fast dynamics of $C_{P}$ and $L$ leads to a shorter interval of mode 7 i.e $\omega_{3}\left(t_{7}-t_{6}\right) \ll 1$, which leads to following approximations$i_{p}(t) \approx n I_{o}, v_{p}(t) \approx V_{d c}-\frac{n I_{o}}{C_{P}}\left(t-t_{6}\right), v_{l}^{\prime}(t) \approx V_{d c}$ and $t_{V I I}=t_{7}-t_{6} \approx \frac{V_{d c} C_{P}}{n I_{o}}$. The condition for this approximation is given as $\left(\frac{V_{d c}}{n I_{o}} \sqrt{\frac{C_{P}}{L}} \sqrt{1+\frac{C_{P}}{C_{S}}}\right) \ll 1$. This actually implies that $i_{p}$ and $v_{l}^{\prime}$ remain constant and $v_{p}$ falls linearly (as known in existing literature).

## H. Mode 8: $t_{7}<t<t_{8}$

In this mode $S_{1}$ and the anti-parallel diode of $S_{3}$ are conducting and thus shorting the primary winding of the transformer. Equivalent circuit in this mode is shown in Fig. 6a. The gating signal of $S_{3}$ can be applied now to ensure ZVS turn ON. Hence, the minimum required dead time ( $D T$ ) of $S_{3}-S_{4}$ is given as $D T \geq t_{V I I} . i_{p}$ and $v_{l}^{\prime}$ are given as

(a)

(b)

Fig. 6. Equivalent Circuits in (a) Mode 8, (b) Mode 9

$$
\begin{align*}
& i_{p}(t) \approx n I_{o}-\frac{V_{d c}}{\sqrt{L / C_{S}}} \sin \left(\omega_{2}\left(t-t_{7}\right)\right)  \tag{8}\\
& v_{l}^{\prime}(t) \approx V_{d c} \cos \left(\omega_{2}\left(t-t_{7}\right)\right)
\end{align*}
$$

The link voltage $v_{l}(t)=n v_{l}^{\prime}(t)$. This mode ends at $t=t_{8}$ when $v_{l}^{\prime}$ reaches zero and $D_{6}, D_{7}$ are forward biased. The time interval $t_{V I I I}$ is estimated solving (8).

$$
\begin{align*}
& t_{V I I I}=t_{8}-t_{7}=\frac{\pi \sqrt{L C_{S}}}{2}  \tag{9}\\
& i_{p}\left(t_{8}\right) \approx n I_{o}-\frac{V_{d c}}{\sqrt{L / C_{S}}}
\end{align*}
$$

Due to periodic nature of the waveform with half-wave symmetry, the magnitude of $i_{p}$ derived in this mode is used as initial condition in Mode 1.

## I. Mode 9: $t>t_{8}$

In this mode, both $v_{p}$ and $v_{l}$ are clamped to zero. The converter is in free-wheeling state. Equivalent circuit in this mode is shown in Fig. 6b. The primary current is given as $i_{p}(t)=n I_{o}-\frac{V_{d c}}{\sqrt{L / C_{S}}}$. All four diodes of secondary rectifier are conducting. To achieve ZVS turn ON of $S_{3}$, gating pulse is applied in this mode. The mode ends when $S_{1}$ is turned OFF and the circuit enters into a similar mode as Mode 1. The duration of the mode is given as in (10).

$$
\begin{equation*}
t_{I X}=\frac{(1-d) T_{s}}{2}-t_{V I I}-t_{V I I I} \tag{10}
\end{equation*}
$$

In the next half of the flux balance cycle $\left(T_{s}\right)$ the circuit evolves through similar modes as discussed above.

## III. Computation of Output voltage

$$
\begin{aligned}
& V_{o}=\frac{2}{T_{s}} \int_{0}^{T_{s} / 2} v_{l}(t) d t \\
&=\frac{2}{T_{s}}\left[\int_{t_{3}}^{t_{4}} n V_{d c}\left[1-\cos \left(\omega_{2}\left(t-t_{3}\right)\right)\right] d t+V_{C} t_{V}\right. \\
&\left.+n V_{d c}\left(t_{V I}+t_{V I I}\right)+\int_{t_{7}}^{t_{8}} n V_{d c} \cos \left(\omega_{2}\left(t-t_{7}\right)\right) d t\right] \\
&=\frac{2}{T_{s}}\left[n V_{d c} t_{I V}+V_{C} t_{V}+n V_{d c}\left(t_{V I}+t_{V I I}\right)\right] \\
&=\frac{2}{T_{s}}\left[n V_{d c} t_{I V}+\left(V_{C}-n V_{d c}\right) t_{V}+n V_{d c}\left(t_{V}+t_{V I}+t_{V I I}\right)\right] \\
&=d n V_{d c}-\frac{4 n^{2} L I_{o}}{T_{s}}+\frac{2 n V_{d c}}{\pi} \frac{\omega_{s}}{\omega_{2}}=n V_{d c}\left(d+\frac{2}{\pi} \frac{\omega_{s}}{\omega_{2}}\right)-R_{o} I_{o} \\
&(11)
\end{aligned}
$$

Considering ideal operation of the converter, the output voltage is $V_{o}=n d V_{d c}$. But the profile of the link voltage $v_{l}$ and duration of active states are changed due to parasitics and active snubber clamp (see Fig. 2b). Considering all non idealities, a closed form expression of $V_{o}$ is presented here. The average output voltage can be given as in (11), where $\omega_{s}=\frac{2 \pi}{T_{s}}$ and $R_{o}=4 n^{2} L / T_{s}$. In the above derivation we have considered $t_{I} \approx t_{V I I}$ and $t_{I V} \approx t_{V I I I}$. The expressions of the time intervals of different modes derived in the last section are used here. As seen in (11), in the expression of $V_{o}$ there is an increase in duty cycle, $\frac{2 \omega_{s}}{\pi \omega_{2}}$ along with the wellknown duty-cycle loss due to leakage inductance. When $\omega_{2}$ is comparable with $\omega_{s}$, the effect of secondary capacitance (duty cycle increase) can not be ignored. Another important observation is that the expression of $V_{o}$ is independent of active snubber clamp voltage $V_{C}$.

## IV. Estimation of parasitics

To estimate the output voltage $\left(V_{o}\right)$, the values of parasitics, $L$ and $C_{s}$ are required (see (11)). What follows is a method of estimation of these parasitics from experimental waveforms.

## A. Estimation of $L$

From the experimental waveform of $i_{p}$, the current slope $\left(K_{1}\right)$ can be evaluated in Mode 2 and 3 . Then $L$ can be given as $L=\frac{V_{d c}}{K_{1}}$. Again, in Mode 5, the slope of $i_{p}$ is estimated as $K_{2} . L$ is given as $L=\frac{V_{C} / n-V_{d c}}{K_{2}}$.

## B. Estimation of $C_{s}$

From the experimental waveform of $v_{l}$, the period of oscillation $T_{\text {osc }}$ can be estimated in Mode 6. The effective capacitance $C_{S}=\left(\frac{T_{o s c}}{2 \pi}\right)^{2} \frac{1}{L}$. It can also be estimated from the duration of Mode 4 as follows $C_{s}=\frac{t_{I V}^{2}}{L\left(\cos ^{-1}\left[1-\frac{V_{C}}{n V_{d c}}\right]\right)^{2}}$.

## V. Experimental verification



Fig. 7. Hardware prototype
A PSFB is designed to experimentally validate the converter operation. The specifications of the prototype are listed in Table I. The setup is shown in Fig. 7. The primary bridge is

TABLE I
Specifications of The setup

| Parameter | Value |
| :---: | :---: |
| Input Voltage $\left(V_{d c}\right)$ | 400 V |
| Duty $(d)$ | 0.85 |
| Turns Ratio $(n)$ | 4 |
| Switching Frequency $\left(f_{s}\right)$ | 20 kHz |
| Load current $\left(I_{o}\right)$ | 1.2 A |
| Output Power $(P)$ | 1.5 kW |
| Clamp voltage $\left(V_{C}\right)$ | 1870 V |

implemented with Semikron IGBT modules SKM50GB12T4. The secondary rectifier is implemented with 3 kV SiC Schottky diodes GAP3SLT33-214. EPCOS ferrite E cores E80/38/20 are used for the high frequency transformer. The key experimental waveforms of $v_{p}, v_{l}$ and $i_{p}$ are shown in Fig. 8. In the figure, the modes of operation and durations are marked. The experimental result closely matches with the analytical waveforms shown in Fig. 2b. Observed clamp voltage $V_{C}$ is 1870 V . The parasitics $L$ and $C_{S}$ are estimated following the procedure stated in the last section from the experimental waveform and are tabulated in Table II. The estimated values are $L=141.6 \mu H$ and $C_{S}=4.56 n F$. For the given operating condition in Table I and measured values of parasitics, using (11) the output voltage ( $V_{o}$ ) is analytically estimated as


Fig. 8. Experimental waveforms of the converter

TABLE II
Estimation of parasitics

| Parameter | Method of estimation or measurement | value |
| :---: | :---: | :---: |
| $L$ | Mode $2\left(K_{1}=2840909 \mathrm{~A} / \mathrm{s}\right)$ | $140.8 \mu \mathrm{H}$ |
|  | Mode $5\left(K_{2}=468720 \mathrm{~A} / \mathrm{s}\right)$ | $142.4 \mu \mathrm{H}$ |
| $C_{S}$ | Mode $6\left(T_{o s c}=5.03 \mu \mathrm{~s}\right)$ | 4.56 nF |
|  | Mode $4\left(t_{I V}=1.4 \mu \mathrm{~s}\right)$ | 4.57 nF |

1244.9 V . The actual measured output voltage is 1240 V (see Table III). The error in analytical estimation is $0.4 \%$. Fig. 9 shows the ZVS turn ON of $S_{2}$ and $S_{3}$ respectively. From the figures it is seen that, the gate voltages ( $G_{2}$ and $G_{3}$ ) rise above threshold when the voltage across the devices $\left(v_{S_{2}}\right.$ and $\left.v_{S_{3}}\right)$ becomes zero. This confirms the ZVS turn ON as discussed in Mode 2.

## VI. Conclusion

The steady state operation of the phase shifted full bridge converter is analysed considering device and diode output capacitances and transformer leakage inductance. A commonly employed single-switch active clamp is considered to limit the voltage stress of the rectifier diodes. It is observed that the rectifier output of a PSFB deviates significantly from ideal waveform due to dominant effects of the parasitics. Due to

TABLE III
Estimated and observed output voltage ( $V_{o}$ )

| Analytically estimated using (11) |  |  |  | Experimentally measured |
| :---: | :---: | :---: | :---: | :---: |
| $n d V_{d c}$ | $2 n V_{d c} \omega_{s} /\left(\pi \omega_{2}\right)$ | $R_{o} I_{o}$ | $V_{o}$ |  |
| 1360 V | 102.4 V | 217.5 V | 1244.9 V | 1240 V |



Fig. 9. ZVS turn ON of $S_{2}$ and $S_{3}$
secondary diode parasitic capacitances, the circulating current during zero state is lower than the reflected load current leading to reduction in ZVS range. The analysis provides an expression for this current which will help in dead-time design to achieve ZVS. A closed form expression of the output voltage is analytically derived and experimentally verified. It is observed that other than the known duty cycle loss due to leakage inductance, there is a duty cycle gain in output voltage due to secondary diode capacitances. These effects of the secondary diode capacitance are generally ignored in the existing analysis of PSFB. It is observed that the output voltage is independent of the snubber clamp voltage. A laboratory prototype of $1.5 \mathrm{~kW}, 400 \mathrm{~V}$ to 1.25 kV PSFB is built. The mode by mode converter operation is experimentally verified. The analytical waveforms are closely matched with the experimental results and clearly show the effects of parasitics on the PSFB operation. The paper also presents an estimation technique to find the values of key parasitics. Presented analysis and estimation technique will be valuable in proper design and control of this widely used isolated DCDC converter.

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