Optimal Design of a Dual Active Bridge based Single-stage DC-AC Converter

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***Abstract*—This paper presents a design and operation strategy for a single-phase single-stage Dual active bridge (DAB) based AC-DC converter. Conventional AC-DC power conversion happens in two stages, an active front end converter followed by an isolated DC-DC conversion stage. Conversion with multiple stages lead to lower efficiency and power density due to presence of an intermediate DC link capacitor and hard-switched rectifier. This paper utilizes a single stage conversion topology where the grid side converter is switched only twice in a line cycle resulting in reduced switching losses. A modulation strategy is discussed which results in unity power factor operation and soft switching. Two separate design strategies are proposed which lead to minimization of the DAB rms and peak of inductor current. Simulation results are presented for a 2.5 kW converter which verify the effectiveness of the design technique.**

***Index Terms*—Dual active bridge, soft switching, optimal design, line frequency unfolding**

I. Introduction

Single phase AC-DC power conversion with power factor correction have several applications such as hybrid electric vehicle chargers [1], uninterrupted power supply systems, inverters for photo-voltaic systems, etc. Several of these applications require bidirectional power flow such as V2G [1].

Commercial AC-DC power conversion systems have two stages [1]. The active front-end converter consisting of an H-bridge is high frequency switched and draws/injects sinusoidal current. The intermediate DC link filters the second harmonic ripple to produce a constant DC link voltage. An isolated DC-DC converter is then placed between the intermediate DC link and the output for isolation and voltage matching. This converter may be a dual active bridge (DAB) or a resonant converter (LLC/SRC). Multiple stages of power conversion result in larger losses and reduction of efficiency. Moreover the intermediate DC link usually consists of a large electrolytic capacitor which is bulky and has reliability issues. Several single stage power conversion strategies are proposed in literature to take care of these issues [2]–[9].

Dual active bridge DC-DC power conversion have several advantages such as isolation, bidirectional power flow capability and soft-switching [10]. Several single stage converter solutions based on DAB principle are proposed in literature [6]. A modulation strategy with line frequency unfolding and achieving zero voltage switching over the entire line cycle is discussed in [4]. The proposed strategy however leads to increased current stresses since the choice of design parameters is suboptimal. A modulation strategy using phase shift and variable frequency for achieving soft-switching is discussed in [11]. A DAB modulation strategy for achieving lower value of inductor rms currents is discussed in [12]. However, it results in low frequency harmonics in the grid current waveform which increases the filtering requirement. A trapezoidal current modulation scheme for achieving sinusoidal line currents is discussed in [9]. Although, it results in lower line total harmonic distortion (THD), the power transfer becomes a complicated function of modulation variable which results in complicated control. A matrix converter based single stage power conversion through DAB principle is proposed in [13]. The modulation strategy results in unity power factor operation and soft switching. Although several efforts have been made in literature for determining an optimal modulation scheme, a systematic design procedure for deciding the design parameters (transformer turns ratio and DAB inductance) is not discussed.

This paper presents a method for selecting the two key design parameters i.e. the transformer turns ratio and leakage inductance of an AC-DC power converter based on DAB principle. Line frequency unfolding strategy is used to minimise switching losses in the grid side converter. A modulation strategy is discussed which leads to unity power factor operation and soft switching of the DAB converter [13]. Based on this modulation strategy, two optimization problems are formulated for minimizing the rms and peak of inductor current. Analytical solution of the problem leads to two design strategies, one resulting in minimum rms current and other resulting in minimum peak current. It is observed that the design strategy used to achieve minimum inductor rms current also leads to near optimal value of peak current. Simulation results verify the theoretical analysis.

The rest of the paper is organized as follows. Section II provides the detailed analysis of the converter and the formulation of the rms and peak current minimization problem. The analytical solution of the problem along-with a step-by-step design procedure is discussed. Section III presents the simulation results. Section IV concludes the paper.

II. Analysis

This section describes the modulation and design strategy of the single-stage DC-AC converter based on dual active bridge (DAB) principle. The single-stage converter topology is shown in Fig.1. The topology is similar to the conventional two stage topology consisting of active front-end converter followed by an isolated DC-DC converter. However, the front-end converter referred to as unfolder in this case switches only twice in the line cycle. On the DC side, H-bridge converter formed by switches S_1-S_4 generates a high frequency duty modulated square waveform v_p which is applied to a transformer with turns ratio $n_p/n_s = n$ connected in series with an inductor L. The H-bridge converter formed by switches S_5-S_8 similarly converts the rectified voltage v_{uv} to a high frequency square waveform. A phase shift is introduced between v_p and v_s for power transfer. A typical waveform showing v_p and v_s during a switching cycle is given in Fig.2a. The magnetising inductance is neglected and ideal operation of the switches are considered in the analysis. With these assumptions, the DAB converter can be represented by the equivalent circuit shown in Fig.2b.

A. Problem Description

Consider the converter with a power rating P, DC voltage V_1, AC voltage with peak V_2 and frequency f and switching frequency f_s. Design of the converter involves determination of transformer turns ratio n (n_p/n_s) and the inductance value L. Once the design parameters are fixed, the modulation parameters d_1, d_2 and δ need to be determined. The design and modulation of the converter should be carried out to ensure the converter operates in an optimal manner.

Based on the utility grid specifications, the AC current should be having low total harmonic distortion and current should be drawn at or close to unity power factor. The converter operation should ensure lossless switching transitions (Zero current or Zero voltage switching) and lower value of conduction losses which will lead to improvement of efficiency and power density. For the converter topology in Fig.1, the unfolder is switched only twice in a line cycle leading to negligible amount of switching losses. It has been identified in literature that the minimisation of the rms or peak of the inductor current while ensuring soft switching results in loss minimisation [14], [15].

The unfolder modulation strategy is discussed in the subsequent section. Based on the unfolder strategy, the DAB modelling and the optimal design strategy is proposed.

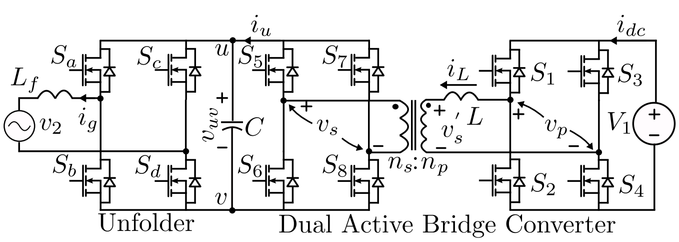

Fig. 1. Topology of the single stage DAB based DC-AC converter

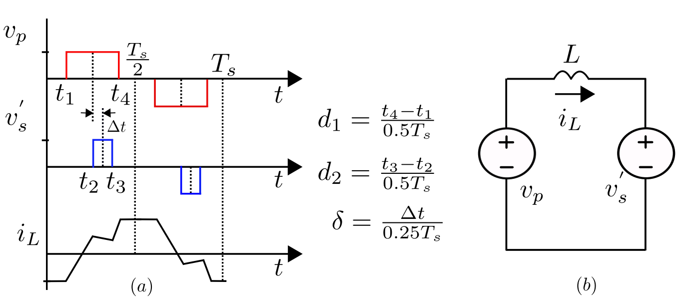

Fig. 2. (a) Typical waveforms in DAB converter (b) Equivalent Circuit

B. Unfolder Modulation

Consider the utility voltage defined as,

$$v_2(t) = V_2 \sin(\omega t) \tag{1}$$

where V_2 is the peak value of line-neutral voltage and $\omega = 2\pi f$. The unfolder is switched twice in a line cycle with the switching states as shown in Fig.3. The modulation of the unfolder results in a rectified sinusoidal voltage v_{uv} as shown in Fig.3.

$$v_{uv}(t) = V_2 |\sin(\omega t)| \tag{2}$$

All the unfolder switches S_a-S_d always need to block unipolar voltage and carry bidirectional currents. An H-Bridge converter is thus suitable for line frequency unfolding.

C. Modelling of DAB converter

Considering ideal converter operation, the inductor current i_L is described using the following equation.

$$L\frac{di_L}{dt} = v_p - nv_s \tag{3}$$

Since, the unfolder modulation strategy generates a rectified sinusoidal voltage across uv of peak V_2 and V_1 is known, the inductor applied voltage is completely determined for any given choice of d_1, d_2 and δ. Several modulation strategies exist in literature which aims towards achieving soft switching while eliminating low frequency harmonics in the current waveform [5], [13], [16]. The modulation stratgy described in [13] is chosen in the present analysis because of its several advantages.

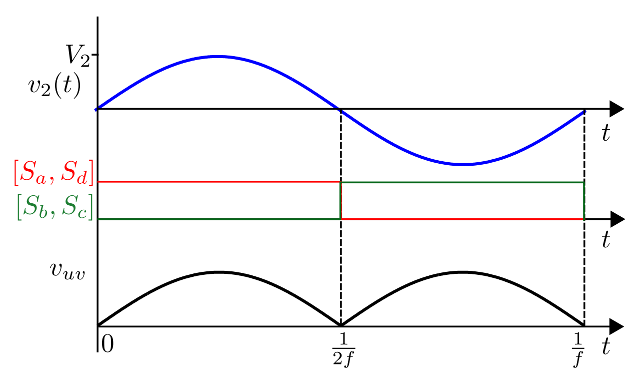

Fig. 3. Waveforms showing unfolder operation

- Modulation strategy in [13] results in unity power factor operation.
- The power becomes a linear function of phase shift angle.
- The modulation results in zero current switching (ZCS) of S_5-S_8 and zero voltage switching (ZVS) of S_1-S_4 in the entire line cycle.
- The strategy results in elimination of all low frequency harmonics in the current waveform. Thus the filter capacitor C needs to filter only switching ripple making it much smaller in size.

The primary side converter (S_1-S_4) applies a voltage pulse whose width is decided by $d_1(t)$. The H-bridge converter on the secondary side (S_5-S_8) is switched two times in a switching cycle to generate a square waveform with $d_2 = 1$ as shown in Fig.4. Since the switching frequency is much higher than the line frequency, the voltage v_{uv} can be assumed to be constant during the switching cycle. The voltage v_s is phase shifted by $\delta T_s/4$ for power transfer. Subsequent analysis is carried out for $\delta > 0$ i.e. power transfer from DC to AC side. Similar analysis can be carried out for $\delta < 0$.

The duty cycle $d_1(t)$ is chosen such that the volt seconds applied across inductor is zero over each half cycle or $T_s/2$ of v_s. This gives,

$$d_1(t) = \frac{nV_2|\sin(\omega t)|}{V_1} = M|\sin(\omega t)| \tag{4}$$

where $M := nV_2/V_1$. The phase shift δ is chosen such that the positive pulse of v_p remains inside the positive section of the secondary pulse as shown in Fig.4. This happens when $d_1(t) + \delta \leq 1$ [13] which is always satisfied if $M + \delta \leq 1$. This mode of operation is hereafter referred to as *inner mode*. Since the volt-seconds applied across the inductor is zero for $t \in (t_1, t_4)$, $i_L(t_1) = i_L(t_4)$ in Fig.4. Moreover from half-wave symmetry of the inductor current, since $t_4 = t_1 + T_s/2$, $i_L(t_1) = -i_L(t_4)$. These conditions can be simultaneously satisfied only if $i_L(t_1) = i_L(t_4) = 0$. This implies that the secondary bridge is always switched at zero current. Thus the current at instants t_2 and t_3 can be determined using (3) and given in (5) and (6).

$$i_2 = \frac{nv_{uv}}{4f_sL}\left(d_1(t) + \delta - 1\right) \tag{5}$$

$$i_3 = \frac{nv_{uv}}{4f_sL}\left(1 - d_1(t) + \delta\right) \tag{6}$$

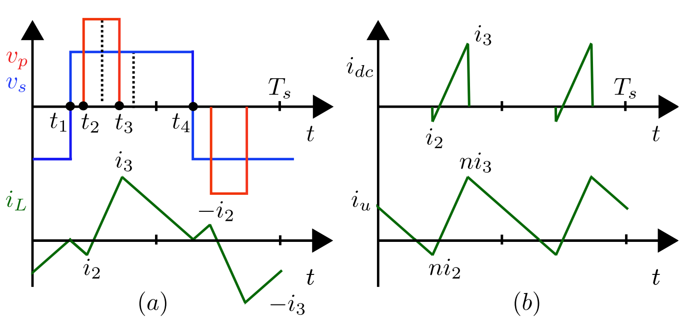

Fig. 4. DAB waveforms (a) v_p, v_s and i_L (b) i_{dc} and i_u

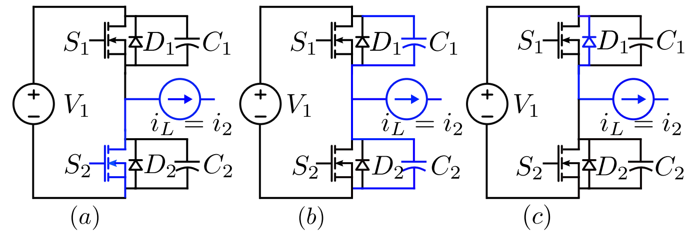

Fig. 5. ZVS switching transition of S_2 and S_1

ZVS of primary bridge: Consider the switching transition at $t = t_2$ where switch S_2 is turned off and S_1 is turned on after dead time. The current i_2 is negative at this instant and hence switch S_2 is conducting (Fig.5a). On turning off S_2, the current i_2 has to flow through the capacitors C_1 and C_2 discharging and charging them respectively (Fig.5b). Since the channel current of S_2 quickly drops before the voltage across capacitor C_2 can rise, S_2 experiences zero voltage turn-off. Once the voltage across C_1 reaches zero, the diode D_1 starts conducting (Fig.5c). Switch S_1 turned on after this instant is turned on at zero voltage.

It can be seen that i_2 is negative and i_3 is positive over the entire line cycle. These polarity of currents facilitate capacitor assisted zero voltage switching (ZVS) of the switches S_1-S_4 participating in the switching transitions [17].

The average power transferred over a switching cycle p_s can be calculated using the following expression.

$$p_s = \frac{2}{T_s}\int_{t_1}^{t_4} v_{uv} i_u dt = \frac{nV_1 v_{uv}}{4f_sL} d_1\delta \tag{7}$$

The current $\bar{i}_u$ which is average of i_u (DC side current of H-bridge formed by S_5-S_8 in Fig.1) in one switching cycle is,

$$\bar{i}_u = \frac{nV_1}{4f_sL} d_1\delta = \frac{n^2 V_2 \delta}{4f_sL}|\sin(\omega t)| \tag{8}$$

The current is in phase with the voltage waveform and is free from low frequency harmonics. Finally, the average power transmitted over a line cycle is given by,

$$P = \frac{2}{T}\int_0^{T/2} \frac{nV_1 v_{uv}}{4f_sL} d_1\delta dt = \frac{M^2 V_1^2 \delta}{8f_sL} \tag{9}$$

where $T = 1/f$. This power is proportional to δ.

1) Inductor RMS current: The inductor rms current over line cycle can be evaluated by the following expression [13].

$$\langle i_{Lrms}\rangle_T^2 = \frac{1}{T}\int_0^T i_L^2 dt \tag{10}$$

This integral is evaluated in two steps. The rms current in each switching cycle is given by

$$\langle i_{Lrms}\rangle_{T_s}^2 = \frac{V_1^2}{48f_s^2L^2} d_1^2\left[d_1^2 - 2d_1 + 1 + 3\delta^2\right] \tag{11}$$

Integrating (11) over line cycle, the rms current is given by (12).

$$i_{Lrms} = \frac{MV_1}{24f_sL}\left[6 + 18\delta^2 - \frac{32}{\pi}M + \frac{9}{2}M^2\right]^{\frac{1}{2}} \tag{12}$$

Replacing the f_sL product from the power expression (9) in (12), we obtain (13).

$$i_{Lrms} = \frac{P}{3V_1} \underbrace{\left[\frac{1}{\delta^2} \left(\frac{6}{M^2} - \frac{32}{\pi M} + \frac{9}{2} \right) + \frac{18}{M^2} \right]^{\frac{1}{2}}}_{\Psi(M,\delta)} \quad (13)$$

2) Inductor Current Stress: Since inductor current has half wave symmetry for $t \in [0, T_s]$, it is sufficient to determine the maximum value of $|i_L|$ for $t \in [t_1, t_4]$. Note that $i_L(t_1) = i_L(t_4) = 0$. Moreover $i_2 < 0$ and $i_3 > 0$. The value of $i_2 + i_3$ can be evaluated from (5) and (6).

$$i_2 + i_3 = \frac{n v_{uv}}{2 f_s L} \delta \quad (14)$$

which is always positive. This implies $i_3 > -i_2$ and thus $max\, |i_L| = i_3$. Since v_{uv} and d_1 vary over line cycle, the magnitude of the peak i_3 changes. This variation can be given by the following equation.

$$i_3(t) = \frac{V_1 M |\sin(\omega t)|}{4 f_s L} \left(1 - M |\sin(\omega t)| + \frac{8 f_s L P}{M^2 V_1^2} \right) \quad (15)$$

The value of t where i_3 is maximum can be determined by equating the derivative of (15) w.r.t time t to zero. For $P < \frac{n^2 V_2^2}{8 f_s L} (2M - 1)$, the maximum value of i_3 occurs at $\omega t = \sin^{-1} [(1 + \delta)/2M]$. Otherwise the peak value occurs at $\omega t = \pi/2$. The peak current expression is given by (16).

$$i_{Lpk} = \begin{cases} \frac{n V_2}{4 f_s L} (1 - M + \delta) & \text{if } P \geq \frac{n^2 V_2^2}{8 f_s L} (2M - 1) \\ \frac{V_1}{16 f_s L} (1 + \delta)^2 & \text{otherwise} \end{cases} \quad (16)$$

Replacing the f_sL product from the power expression (9) in (16), we obtain (17).

$$i_{Lpk} = \frac{P}{V_1} \times \underbrace{\begin{cases} 2 \left(\frac{1}{M\delta} - \frac{1}{\delta} + \frac{1}{M} \right) & \text{if } \delta \geq (2M - 1) \\ \frac{1}{2M^2 \delta} (1 + \delta)^2 & \text{otherwise} \end{cases}}_{\Phi(M,\delta)} \quad (17)$$

So one needs to determine L, M and δ so that the current stress (either RMS/peak) is minimised. M and δ can be found by solving the optimisation problem (18). The value of L can be found using (9).

$$\min_{\substack{M,\delta \\ M,\delta \in [0,1],\ M+\delta \leq 1}} \quad f(M, \delta) \quad (18)$$

where $f = \Psi(M, \delta)$ for rms current problem and $f = \Phi(M, \delta)$ for peak current problem.

D. Design problem solution

Consider the DAB converter which needs to operate with the modulation strategy described in Section II-C for a fixed P, V_1, V_2, f_s and f. The design problem involves determining n and L such that the converter operates the most efficient manner. Note that M is same as n for a fixed V_1 and V_2.

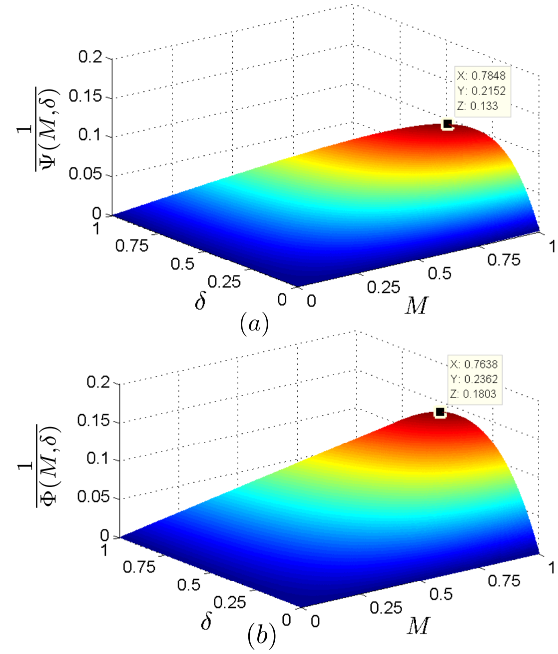

Fig. 6. Plot showing the functions (a) $1/\Psi(M, \delta)$ and (b) $1/\Phi(M, \delta)$

1) Solution of rms current problem: Minimisation of rms current is same as minimisation of $\Psi(M, \delta)$. For all $M \in [0, 1]$, $\Psi(M, \delta)$ is strictly decreasing in δ. Minimum is obtained when δ is maximum i.e. $\delta = (1 - M)$. Substituting this value in (13), Ψ becomes a function of M. Evaluating the first order necessary condition, the following cubic equation in M is obtained.

$$(90\pi) M^3 - (216\pi + 192) M^2 + (264\pi + 64) M - 96\pi = 0 \quad (19)$$

Solution of (19) leads to $M = 0.7848$. Thus, the turns ratio $n = 0.7848 V_1/V_2$. The value of δ is 0.2152. The value of inductance can be determined using (9), $L = 0.0166 \frac{V_1^2}{f_s P}$. Putting these values in the (13), the optimal value of rms current $i_{Lrms} = 2.503 \frac{P}{V_1}$.

2) Solution of peak current problem: Minimisation of peak current is same as minimisation of $\Phi(M, \delta)$. The piecewise function $\Phi(M, \delta)$ is strictly decreasing in δ for all $M \in [0, 1]$. Minima occurs when $\delta = (1 - M)$. Putting this value and simplifying, we obtain the following piecewise defined function in M.

$$\Phi(M, 1 - M) = \begin{cases} \frac{4}{M} & \text{if } 0 \leq M < 2/3 \\ \frac{(2-M)^2}{2M^2(1-M)} & \text{if } 2/3 \leq M \leq 1 \end{cases} \quad (20)$$

Evaluating the first order necessary condition, the following equation in M is obtained.

$$(M - 2) \left(M^2 - 6M + 4 \right) = 0 \quad (21)$$

The feasible solution of the equation is $M = 3 - \sqrt{5} = 0.7638$. Thus, $n = 0.7638 V_1/V_2$. The value of δ is 0.2362. The value

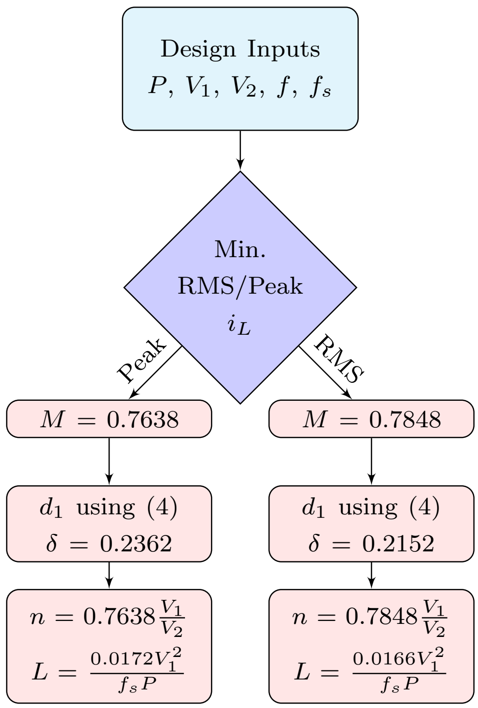

Fig. 7. Flowchart showing the design steps

TABLE I
CONVERTER SPECIFICATIONS

V_1	V_2	f	f_s	P	C	L_f
400V	250V	50Hz	100kHz	2.5kW	$5\mu F$	$50\mu H$

of $L = 0.0172\frac{V_1^2}{f_sP}$ and the optimal value of peak current is $i_{Lpk} = 5.545\frac{P}{V_1}$.

Fig.6 shows the graphical plot of the functions $1/\Psi(M,\delta)$ and $1/\Phi(M,\delta)$ for various M and δ. The inverse functions are plotted since both Ψ and Φ become infinite as M and δ approach zero. It can be seen from Fig.6a that $1/\Psi$ attains maximum value (which means Ψ attains minimum value) for $M = 0.7848$ and $\delta = 0.2152$. This matches with the theoretically obtained values. Fig. 6b similarly shows the graphical plot of the function $1/\Phi(M,\delta)$. It can be seen that the maximum of $1/\Phi$ occurs for $M = 0.7638$ and $\delta = 0.2362$ which matches with the theoretically obtained values.

Fig.7 shows a flowchart detailing the step by step procedure for design and operation considering rms or peak current minimisation as the design objective.

III. Simulation Results

For verifying the converter design and operation strategy, simulation results are presented for an AC-DC converter with the specifications in Table I. Following design strategy for rms current minimisation in Fig.7, $n = 1.25$, $L = 10.6\mu H$ and $\delta = 0.215$ is obtained. Fig.8a shows the voltages v_p, v_s and the inductor current in a given switching cycle. The inductor current is is zero at instants t_1 and t_4 marked on the figure and hence the secondary bridge achieves zero current switching. i_2 is negative and i_3 is positive which results in zero voltage switching of primary bridge. Fig.8b shows the input voltage $v_2(t)$ an the current $i_g(t)$. It can be seen that the capacitor C and L_f filter the switching ripple and thus the current is free from harmonics. Moreover, the converter operates at unity power factor with i_g in phase with v_2. The current waveform has a very low THD (2.07%) which is

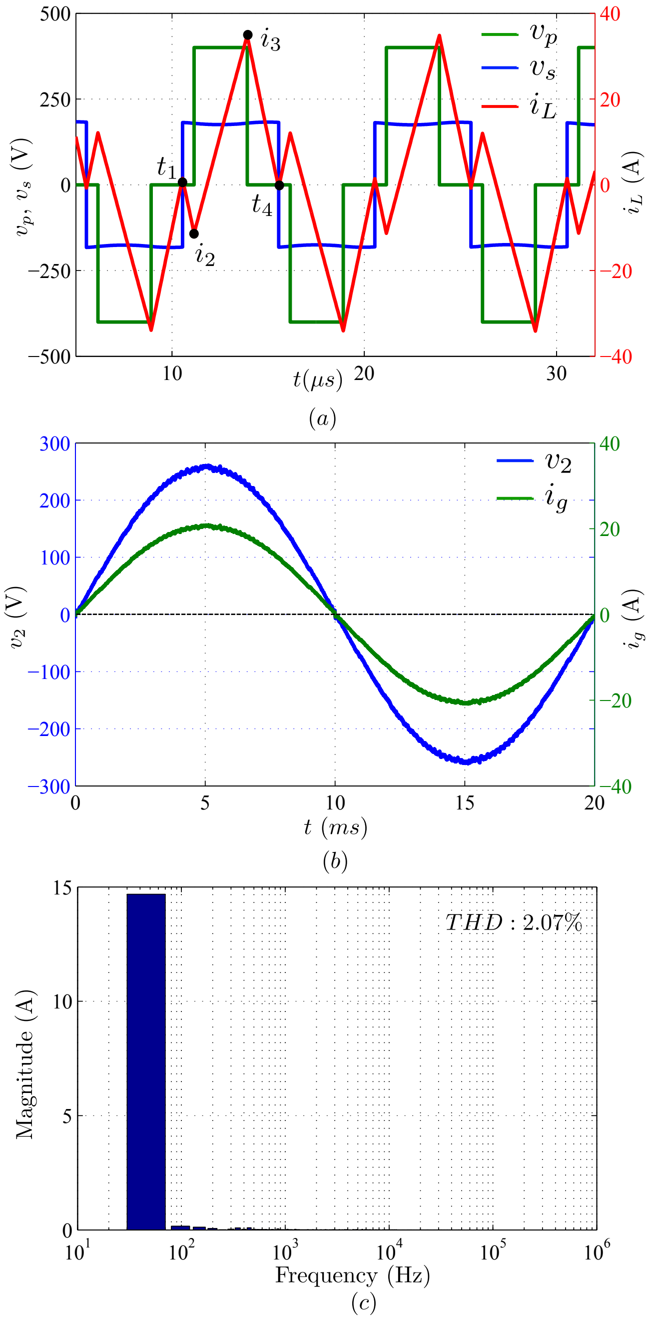

Fig. 8. Simulation results for optimum rms design. (a) Switching cycle waveforms (b) Line voltage V_2 and line current i_g (c) Frequency Spectrum of Grid Current

TABLE II
COMPARISON AT RMS AND PEAK OPTIMISED DESIGN STRATEGIES

	i_{Lpk} (th.)	i_{Lpk} (Sim.)	i_{Lrms} (th.)	i_{Lrms} (Sim.)
Design with min. RMS	34.81	35.50	15.64	15.76
Design with min. Peak	34.65	34.80	15.70	15.82

in accordance with the grid connection standards. Following the design strategy for peak current minimisation, the design parameters are $n = 1.22$, $L = 11\mu H$ and $\delta = 0.236$. Similar results for switching cycle and line cycle are obtained with this strategy. A comparative study of the two design strategies is provided in Table II. It can be seen that with the optimal rms strategy, the peak currents obtained are very close to the optimum peak current (see first column of Table II). Same is the case for rms currents with optimal peak strategy. Thus rms and peak current minimisation problem for the *inner mode* modulation strategy is closely related.

IV. CONCLUSION

This paper presented an optimal design strategy for a single stage DAB based AC-DC converter. Line frequency unfolding results in lower switching losses in the grid side H-bridge converter. The chosen modulation strategy results in unity power factor operation without low frequency harmonics in line current and soft switching of all devices. A design methodology considering this modulation strategy is proposed for minimisation of the rms or peak of the DAB inductor current resulting in lower conduction loss. By solving an optimisation problem, the paper shows how to compute two key design parameters, transformer turns ratio and series inductance value. It is observed both peak and rms current minimization results in similar design. Simulation results verify the theoretical analysis.

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