Turn on Switching Transient Analysis of SiC MOSFET and Schottky Diode Pair

Shamibrota Kishore Roy
Electrical Engineering Department
IISc Bangalore
Bangalore, India
shamibrotar@iisc.ac.in

Kaushik Basu
Electrical Engineering Department
IISc Bangalore
Bangalore, India
kbasu@iisc.ac.in

Abstract: A detailed model to study turn on switching dynamics of SiC MOSFET and SiC schottky diode (SBD) pair is presented. This study takes the non-linear effect of channel current along with the non-linear voltage dependence of depletion capacitances into account. Also the effect of external gate to drain and anode to cathode parasitic capacitances is incorporated in the analysis. External gate to drain parasitic capacitance has a predominant effect on switching dynamics at high value of external gate resistance. It's effect has not been considered in the existing literature. Proposed model estimates turn on (di/dt), (dv/dt) and loss incurred. The simulation and experimental results confirm the accuracy of the presented method over a range of operating conditions for a 1.2-kV discrete SiC MOSFET and SBD pair.

I. Introduction

SiC MOSFETs are wide band gap (WBG) power devices and promised to replace Si IGBTs to achieve better efficiency and power density [1]. Switching loss estimation is important in selection of switching frequency and is an input to the thermal design. For SiC MOSFETs, the turn on switching loss is predominant over turn off loss [2], [3]. Fast turn on switching transient of SiC MOSFET may lead to high (di/dt), (dv/dt) and spurious turn on etc [1]. This paper concerns with the turn on switching dynamics of SiC MOSFET and schottky diode pair.

Experimental approach to study switching transient is time consuming and requires expensive measurement equipments. On the other hand, physics based simulation requires sophisticated software and internal device parameters not available in device datasheet. Behavioural model based approach does not provide insight to the switching process and often suffers from convergence problem. Analytical model is simple and fast and derived from the behavioural model through approximations. It also provides insight into the switching process. In this paper, an analytical approach is adopted which uses parameters extracted from device datasheet and external circuit parasitics as input.

Analytical approach to study the switching transient for low voltage Si MOSFET [4] is not applicable for high voltage SiC MOSFETs because of there non-linear device characteristics [5] and the predominant effect of external circuit parasitics [6]. Analytical modelling approach for SiC MOSFET has been adopted by some earlier work [1], [6]–[9]. Except [6], a linear approximation or a modified linear approximation of channel current is considered. Also piecewise constant approximation of some of the non-linear device capacitances are considered in [7]–[9]. In [1], [6], non-linear voltage dependent capacitance are modelled accurately but the effect of external gate-drain parasitic capacitance is ignored, which has a significant impact during voltage fall period [10].

This paper makes the following improvements over the previous work [6]: a) the effect of external gate drain parasitic capacitance is incorporated in the analytical model. It helps in estimating actual turn on loss and (dv/dt) rate accurately for higher external gate resistance. Note, in [6], analytical loss estimation technique performs poorly for high values of external gate resistance, b) a simplified analysis compared to [6] during voltage fall period is proposed, c) a detailed model of miller capacitance is taken into account. Non-linear channel current dependence over gate source voltage is considered along with the non-linear voltage dependence of device internal capacitances. This proposed analytical model estimates turn on (di/dt), (dv/dt) and actual turn on switching loss.

II. Behavioural Model

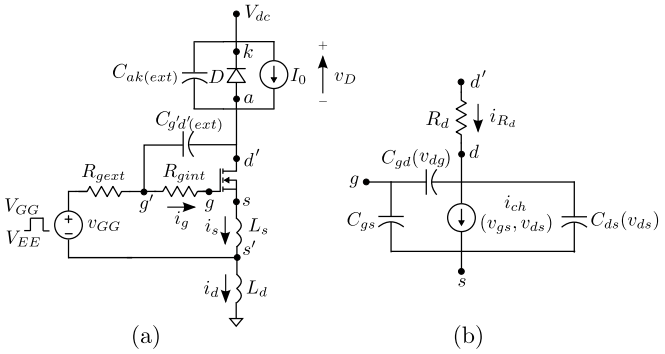

Figure 1: Circuit configuration for switching transient analysis

Hard turn on dynamics of SiC MOSFET and schottky diode pair is analysed using a buck-chopper configuration as shown in Fig. 6(a). V_{dc} is the DC bus voltage and I_0 is the load current. SiC MOSFET and SBD are modelled as three

terminals gate (g), drain (d) and source (s) and two terminals anode (a) and cathode (k) respectively (Fig. 6(a)). v_{GG} is the applied gate driver voltage with high and low voltage levels V_{GG} and V_{EE} respectively. R_{gint} and R_{gext} are the internal and external gate resistance respectively.

The equivalent circuit model or behavioural model of the SiC power MOSFET is shown in Fig. 6(b). Channel current in saturation (i_{ch}) is modelle as described in [5] and single channel approximation is considered. For most part of the turn on switching transition, SiC MOSFET traverses through cut off and saturation region. MOSFET is in cut-off region for $v_{gs} < V_{th}$ and i_{ch} is equal to zero, V_{th} is the threshold voltage of the MOSFET. In ohmic region, $v_{gs} > V_{th}$, $v_{ds} < (v_{gs} - V_{th})/P_{vf}$, so i_{ch} is given by (1). The condition for MOSFET being in saturation region is $v_{ds} > (v_{gs} - V_{th})/P_{vf}$, $v_{gs} > V_{th}$ and i_{ch} is given by (2). Here long channel approximation of the SiC MOSFET is considered. K_p is saturation region transconductance. K_f is ohmic region transconductance factor defined as the ratio of extracted ohmic region transconductance to saturation region transconductance. θ represents the transverse electric field parameter. P_{vf} is the pinch-off voltage parameter which defines how sharp the transition from ohmic region to saturation region happens. R_d represents the drift region resistance. Device parameter variation with temperature is not considered in this model. K_p, K_f, V_{th}, θ, P_{vf} and R_d are obtained from the transfer characteristics (in saturation region) (Fig. 2) and output characteristics (in ohmic region) of the SiC MOSFET given in the data-sheet at 25^oC through curve fitting.

$$i_{ch} = \frac{K_p K_f \left((v_{gs} - V_{th})\, v_{ds} - \dfrac{P_{vf}^{y-1} (v_{gs} - V_{th})^{2-y} v_{ds}^{y}}{y} \right)}{(1 + \theta(v_{gs} - V_{th}))} \tag{1}$$

$$i_{ch} = \frac{K_p (v_{gs} - V_{th})^2}{2(1 + \theta(v_{gs} - V_{th}))} \tag{2}$$

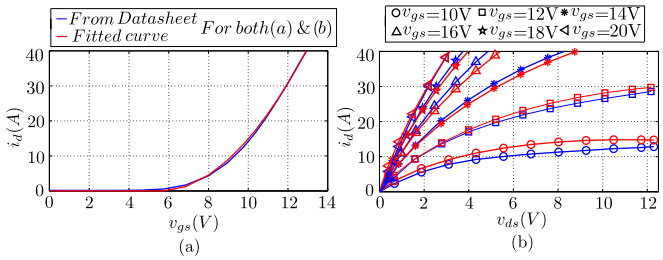

Figure 2: i_d vs. v_{gs} and i_d vs. v_{ds} curve for C2M0080120D

C_{gs}, C_{gd} and C_{ds} are the gate to source, gate to drain and the drain to source device parasitic capacitances respectively. Input capacitance $C_{iss} = (C_{gs} + C_{gd})$, transfer capacitance $C_{rss} = C_{dg}$ and output capacitance $C_{oss} = (C_{dg} + C_{ds})$. In data-sheet, C_{iss}, C_{rss} and C_{oss} are plotted as a function of drain source voltage (v_{ds}). C_{gs} is modelled as a constant capacitance and it is approximately equal to C_{iss} for high value of v_{ds}. C_{gd} is a non-linear capacitance, depends on v_{gd}. For $v_{dg} < 0$, $C_{gd} \approx C_{oxd}$. When $v_{dg} > 0$, C_{oxd} will be in series with the gate drain depletion capacitance. As v_{dg} increases, there are two distinct decay rate of C_{gd} can be observed in SiC MOSFET [11]. Also for high v_{dg}, effect of C_{oxd} is negligible and C_{gd} solely depends on the gate to drain depletion capacitance. So C_{gd} can be represented by the the set of equations given in (3). Similarly, C_{ds} is also a depletion capacitance depends upon v_{ds} and modelled as (4). Extraction of parameters k_1 to k_7 and V_{td} are done by fitting (3) and (4) to the corresponding plots given in the data-sheet. Fig. 3 shows one such example.

$$C_{gd} = \begin{cases} C_{oxd} = k_1/k_3, & v_{dg} \in (-\infty, 0) \\ \dfrac{k_1}{\left(1 + \dfrac{v_{dg}}{k_2}\right)^{1/2} + k_3}, & v_{dg} \in [0, V_{td}) \\ \dfrac{k_4}{\left(1 + \dfrac{v_{dg} - V_{td}}{k_5}\right)^{1/4}}, & v_{dg} \in [V_{td}, \infty) \end{cases} \tag{3}$$

$$C_{ds}(v_{ds}) = \frac{k_6}{\left(1 + \dfrac{v_{ds}}{k_7}\right)^{1/2}} \tag{4}$$

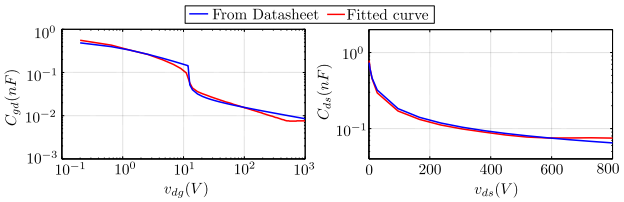

Figure 3: C_{gd} vs v_{dg} and C_{ds} vs v_{ds} plot for C2M0080120D

Diode is considered as ideal with zero voltage drop across it during forward biased condition ($v_D \approx 0$). In reverse bias, diode is modelled as a capacitance C_D, which is also non-linear function of voltage (v_D) across the diode (5).

$$C_D(v_D) = \frac{k_8}{\left(1 + \dfrac{v_D}{k_9}\right)^{1/2}} \tag{5}$$

Fast switching transition of SiC MOSFET excites external circuit parasitics. External circuit parasitics which have been considered are the common source inductance (L_s), power loop inductance (L_d), external gate to drain capacitance ($C_{g'd(ext)}$) and external anode to cathode capacitance ($C_{ak(ext)}$). Effect of external drain to source parasitic capacitance effect is neglected as it is small compared to the minimum value of $C_{ds}(v_{ds})$. L_s is the parasitic inductance that is common to both gate and power circuit loop whereas L_d is only part of power circuit loop. L_d is the summation of the DC bus inductance, the lead inductances of the MOSFET and the diode and connection inductance between the MOSFET and the diode.

The time evolution of gate source ($v_{gs}(t)$) and drain source ($v_{d's}(t)$) voltage and the channel current ($i_{ch}(t)$) during

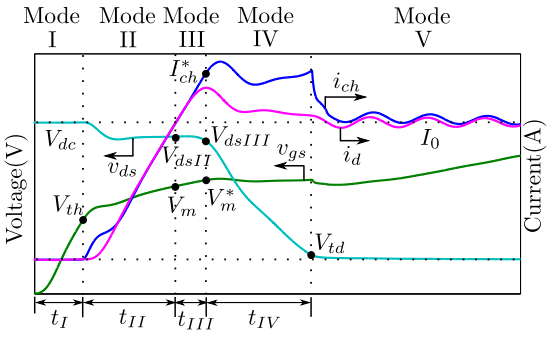

Figure 4: Simulation waveforms

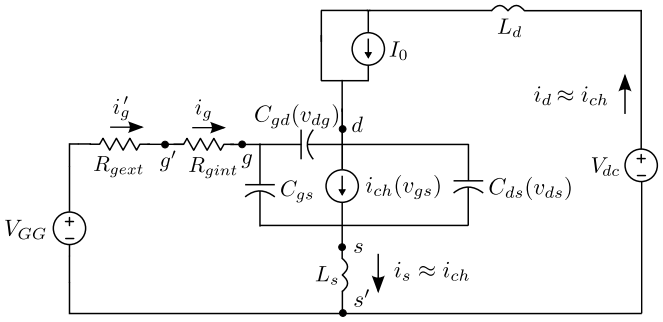

Figure 5: Equivalent circuit model for Mode II

switching transitions are the key waveforms related to switching dynamics study and switching loss estimation. Due to the presence of internal device parasitics, circuit parasitics and R_{gint}, it is not possible to measure these waveforms experimentally. The measurable waveforms are $v_{g's'}(t)$, $v_{d's'}(t)$ and $i_d(t)$ (Fig. 4). The actual switching loss in the MOSFET is given by (6) and the measured loss is given by (7) where T_{on} is the turn on switching transition time..

$$E = \int_0^{T_{on}} \left(v_{ds}(\tau) i_{ch}(\tau) + i^2_{R_d} R_d\right)\ d\tau \tag{6}$$

$$E' = \int_0^{T_{on}} v_{d's'}(\tau) i_d(\tau)\ d\tau \tag{7}$$

III. Analytical Model

The objective of this section is to analyse the turn on switching dynamics of SiC MOSFET and Schottky barrier diode pair and estimate actual switching loss, (di/dt), (dv/dt) rates for a given operating condition using values of device and gate driver parameters and external circuit parasitics. R_d is neglected as it has negligible impact in switching dynamics. Hard switching turn on transient of SiC MOSFET can be divided into five modes, Mode I to Mode V (Fig. 4).

A. Mode I

Mode I is the turn on delay period when positive gate pulse V_{GG} is applied and v_{gs} changes from V_{EE} to V_{th}. Channel current remains zero throughout this period and the entire load current I_0 free-wheel through the diode. The voltage across the MOSFET is V_{dc} (Mode I in Fig. 4). As switching loss during this mode is zero, this mode has not been analysed in this paper.

B. Mode II

After v_{gs} crosses V_{th}, channel current i_{ch} starts increasing. During this mode, the SiC MOSFET is in saturation region. As $(v_{gs} - V_{th})$ is small and $\theta \ll 1$, i_{ch} can be approximately represented as $i_{ch} \approx (K_p/2)(v_{gs} - V_{th})^2$. Diode is forward biased, $v_D \approx 0$. i_d follows i_{ch} and v_{ds} remains almost constant except for the initial portion (Mode II in Fig. 4). Effect of $C_{g'd(ext)}$ can be neglected as change in v_{ds} is small. i_d follows i_{ch} and v_{ds} remains almost constant except for the initial portion (Mode II in Fig. 4). Fig. 5 represents the equivalent circuit of Mode II.

Applying KVL in the gate loop and using the approximations $(dv_{ds}/dt) \approx 0$, $C_{gd}(v_{dg}) \ll C_{gs}$ and $i_d \approx i_s \approx i_{ch}$, we get (8). Here $R_g = (R_{gext} + R_{gint})$. Also KVL in power loop with the approximation $i_d \approx i_s \approx i_{ch}$ gives (9).

$$V_{GG} \approx R_g C_{gs} \frac{dv_{gs}}{dt} + v_{gs} + \left(\frac{K_p L_s}{2}\right) \frac{d}{dt}\left(v_{gs} - V_{th}\right)^2 \tag{8}$$

$$\begin{aligned} v_{ds} &\approx V_{dc} - (L_d + L_s)\frac{di_{ch}}{dt} \\ &\approx V_{dc} - \left(\frac{K_p}{2}\right)(L_d + L_s)\frac{d}{dt}\left(v_{gs} - V_{th}\right)^2 \end{aligned} \tag{9}$$

This mode has been solved in [6] with initial condition $v_{gs}(t = 0) = V_{th}$ and final condition $v_{gs}(t_{II}) = (2I_0/K_p)^{1/2} + V_{th} = V_m$ and closed form expressions of both time duration (t_{II}) (10), loss incurred (E_{II})[1] (11) and drain-source voltage at the end of this mode (V_{dsII}) (12) was provided. At the end of Mode II $v_{gs} = V_m$, $i_d \approx i_{ch} \approx I_0$ and $v_{ds} = V_{dsII}$. (di/dt) can be estimated as (I_0/t_{II}).

C. Mode III

After i_d reaches I_0, diode becomes reversed biased and diode voltage v_D starts to increase. Fig. 6 represents the equivalent circuit of this mode. SiC MOSFET is still in saturation region. v_{gs} starts increasing from it's initial value V_m. Effect of $C_{g'd'(ext)}$ is considered as v_{ds} starts reducing during this period. All the state variables start changing noticeably and the gate and the power loop are fully coupled.

Functional form of internal MOSFET capacitances $C_{gd}(v_{dg})$ and $C_{ds}(v_{ds})$ are defined in third expression of (3) (as $v_{dg} > V_{td}$) and (4) respectively. $v_{dg} \approx v_{ds}$($v_{ds} \gg v_{gs}$) and $((v_{ds} - V_{td})/k_5) \gg 1$ throughout this mode makes $C_{gd}(v_{ds}) \approx \left(\alpha_1/\sqrt[4]{v_{ds} - V_{td}}\right)$ where $\alpha_1 = \left(k_4 \sqrt[4]{k_5}\right)$. Similarly $C_{ds}(v_{ds}) \approx \left(\alpha_2/\sqrt{v_{ds}}\right)$, $\alpha_2 = \left(k_6\sqrt{k_7}\right)$. $C_D(v_D)$ is defined in (5).

KVL in the power loop (Fig. 6) with the approximation $i_s \approx i_d$ gives (13). Applying KCL at d node, we get (14). $v_{dg'} = (v_{dg} - v_{g'g})$ and drop $v_{g'g} = R_{gint} i_g \ll V_{dg}$ makes $v_{dg'} \approx v_{dg}$. $v_{ds} = (v_{dg} - v_{gs})$ and change in v_{ds} is high

[1] $d_1 = -(R_g C_{gs} + K_p L_s (V_{GG} - V_{th}))$, $d_2 = -K_p L_s (V_{GG} - V_{th})$ and $d_3 = \left(\frac{V_m - V_{th}}{V_{GG} - V_{th}}\right)$

$$t_{II} = -\left(R_g C_{gs} + K_p L_s \left(V_{GG} - V_{th}\right)\right) \ln\left(1 - \frac{V_m - V_{th}}{V_{GG} - V_{th}}\right) - K_p L_s (V_m - V_{th}) \tag{10}$$

$$E_2 = \frac{\beta V_{dc}}{2} \left(V_{GG} - V_{th}\right)^2 \left(d_1 \left(d_3 + \frac{d_3^2}{2} + \ln\left(1 - d_3\right)\right) + \frac{d_2 d_3^3}{3}\right) - \frac{\beta^2 \left(L_d + L_s\right)}{8} \left(V_{GG} - V_{th}\right)^4 d_3^4 \tag{11}$$

$$V_{dsII} = V_{dc} - \frac{K_p \left(L_d + L_s\right) \left(V_m - V_{th}\right) \left(V_{GG} - V_m\right)}{R_g C_{gs} + K_p L_s \left(V_m - V_{th}\right)} \tag{12}$$

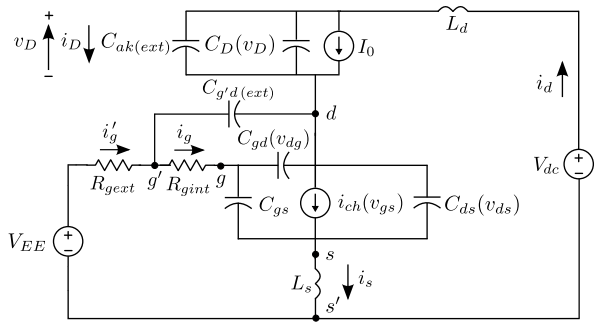

Figure 6: Circuit configuration for switching transient analysis

compared to v_{gs}, so $(dv_{dg}/dt) \approx (dv_{ds}/dt)$. KCL at d node with these approximations give (15). KVL in gate loop with approximations $i_g \ll i_d$ and $v_{dg'} \approx v_{dg}$ gives (16) where $i_g \approx C_{gs}(dv_{gs}/dt) + C_{gd}(v_{ds})(dv_{gd}/dt)$. These set of equations (13), (14), (15) and (16) along with channel current expression (2) form a set of coupled nonlinear differential equations and finite difference method is employed.

$$v_{ds} \approx V_{dc} - v_D - \left(L_d + L_s\right) \frac{di_d}{dt} \tag{13}$$

$$i_d = I_0 + \left(C_D(v_D) + C_{ak(ext)}\right) \frac{dv_D}{dt} \tag{14}$$

$$\left(i_d - i_{ch}\right) \approx \left(C_{gd}(v_{ds}) + C_{ds}(v_{ds}) + C_{g'd(ext)}\right) \frac{dv_{ds}}{dt} \tag{15}$$

$$V_{GG} \approx \left(R_{gext} + R_{gint}\right) i_g + R_{gext} C_{g'd(ext)} \frac{dv_{gd}}{dt} + v_{gs} + L_s \frac{di_d}{dt} \tag{16}$$

Mode III ends when i_d reaches its local maxima or $(di_d/dt) = 0$. t_{III} is the time period of this mode and E_{III} represents the actual switching loss and can be computed using $v_{ds}(t)$ and $i_{ch}(t)$ over this time interval. At the end of this mode $v_{ds} = V_{dsIII}$, $v_{gs} = V_m^*$, $v_D = V_{DIII}$ and $i_d = I_{dIII}$.

D. Mode IV

After the end of Mode III, v_{ds} falls sharply and both miller feedback (through $C_{gd}(v_{dg})$ and $C_{g'd(ext)}$) and feedback through L_s maintains the v_{gs} voltage almost constant to V_m^*. The SiC MOSFET is in saturation and i_{ch} is also constant to $I_{ch}^* = \frac{K_p \left(V_m^* - V_{th}\right)^2}{2(1 + \theta(V_m^* - V_{th}))}$. Governing equations of this mode is same as Mode III. As $i'_g \ll i_d$ and $\left(L_d + L_s\right)(di_d/dt)$ is small compared to v_{ds} and v_D, then $v_D \approx (V_{dc} - v_{ds})$. From (14), (15) and previously stated assumption, we get (17). Note for most of this mode $v_{gs} \ll v_{ds}$ and $v_{dg} \approx v_{ds}$. This mode ends when $v_{dg} \approx v_{ds} = V_{td}$. $\left(C_{D(eq)}(v_D) + C_{oss(eq)}(v_{dg}, v_{ds})\right)$ is plotted with respect to v_{ds} in Fig. 7 in the range of $v_{ds} \in (V_{td}, V_{dsIII})$. It can be observed that $\left(C_{D(eq)}(v_D) + C_{oss(eq)}(v_{dg}, v_{ds})\right)$ remains almost constant for most of the range. Similar observation for half bridge configuration has been reported in [9]. Non-linear voltage dependant capacitance can be replaced with equivalent charge related capacitance C_Q in the voltage interval $v \in (V_1, V_2)$ given by (18). Here $V_1 = V_{td}$ and $V_2 = V_{dsIII}$. $v_{ds}(t)$ can be given by (20). t_{IV} and E_{IV} represent the total time period and switching loss of this mode and given by (19) and (21) respectively. (dv/dt) is given by $\left(V_{dsIII} - V_{td}\right)/t_{IV}$.

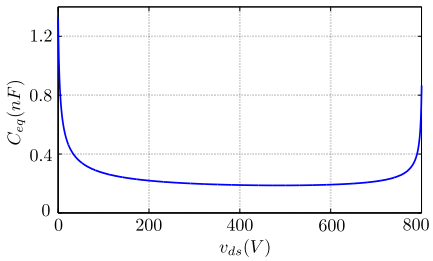

Figure 7: C_{eq} vs v_{ds} plot for C2M0080120D SiC MOSFET and C4D10120A SBD pair

$$C_Q = \frac{1}{V_2 - V_1} \int_{V_1}^{V_2} C_{eq}(v)\, dv \tag{18}$$

$$t_{IV} = \left(\frac{V_{dsIII} - V_{td}}{I_{ch}^* - I_0}\right) C_Q \tag{19}$$

$$v_{ds}(t) = V_{dsIII} + \left(\frac{I_0 - I_{ch}^*}{C_Q}\right) t \tag{20}$$

$$E_{IV} = 0.5 \left(V_{td} + V_{dsIII}\right) I_{ch}^* t_{IV} \tag{21}$$

E. Mode V

During this mode v_{ds} reduces from it's initial value V_{td}. As v_{ds} is very small, switching loss is insignificant. So Mode V has not been analysed. Total turn on switching loss $E = (E_{II} + E_{III} + E_{IV})$.

IV. Simulation and Experimental Result

Double pulse test has been carried out to validate the the proposed analytical model. C2M0080120D SiC MOSFET

$$(I_0 - I^*_{ch}) \approx \underbrace{\left(C_{gd}(v_{ds}) + C_{ds}(v_{ds}) + C_{g'd(ext)} + C_D(v_D) + C_{ak(ext)}\right)}_{C_{eq}(v_{ds}, v_D \approx (V_{dc} - v_{ds}))} \frac{dv_{ds}}{dt} \tag{17}$$

Table I: Device parameters of C2M0080120D SiC MOSFET and C4D10120A SBD pair extracted from data-sheet

V_{th} (V)	K_p (A/V^2)	K_f	θ (1/V)	P_{vf}	R_d (Ω)	R_{gint} (Ω)	C_{gs} (nF)	k_1 (nF)	k_2 (V)	k_3	V_{td} (V)	k_4 (nF)	k_5 (V)	k_6 (nF)	k_7 (V)	k_8 (nF)	k_9 (V)
5.6	1.6	2.19	0.01	0.4	0.01	4.6	0.95	0.95	0.35	0.71	12	0.12	0.025	0.79	5.5	0.75	1.7

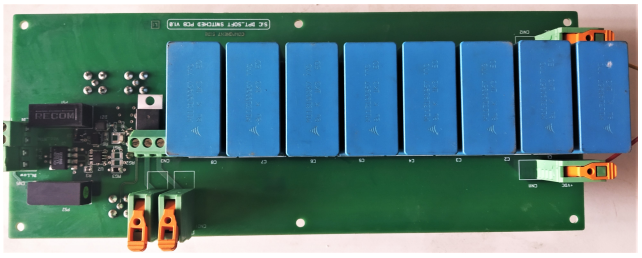

Figure 8: Experimental setup

(1200V, 36A) along with C4D10120A SBD (1200V, 33A) (both from Wolfspeed) is used for experiment. Device parameters are given in Table I. gate driver parameters are given in Table II and external circuit parasitics are given in Table III. $L_d = 65nH$, $L_s = 7.5nH$, $C_{g'd(ext)} = 10pF$, $C_{ak(ext)} = 15pF$. Operating conditions are $V_{dc} = 800V$ and $I_0 = 5 - 25A$ in steps of 5 amperes. This implies total 15 different operating conditions.

Table II: Driver parameters

V_{CC} (V)	V_{GG} (V)	R_{gext} (Ω)
-5	20	3.5, 5.5, 9.5

Table III: External circuit parameters

L_d (nH)	L_s (nH)	$C_{g'd'(ext)}$ (pF)	$C_{ak(ext)}$ (pF)
65	7.5	10	15

A. Validation of behavioural simulation through experiment

The behavioural model used for the development of analytical model is validated through experiment. In Fig. 9, $v_{d's'}(t)$ and $i_d(t)$ obtained from behavioural simulation and experiment are plotted for two different operating conditions and a close match is observed. Similarly experimentally obtained loss (E'_{exp}), measured and actual loss computed using behavioural model (E'_{sim} and E_{sim} respectively) are compared in Fig. 10 for $V_{dc} = 800V$, $R_{gext} = 3.5\Omega$ and $I_0 = 5 - 25A$. A closed agreement is observed between E'_{exp} and E'_{sim}. This verifies the correctness of the behavioural model and the parameters used. Note, there is a significant difference between E_{sim} (actual loss obtained from behavioural simulation using (6)) and E'_{exp} (experimentally measured loss obtained using using (7)) [6].

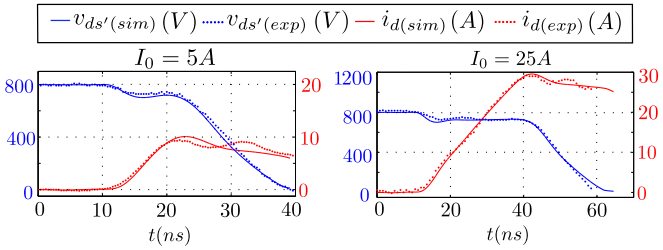

Figure 9: Simulation vs experimental waveforms, Operating condition: [800V, 9.5Ω]

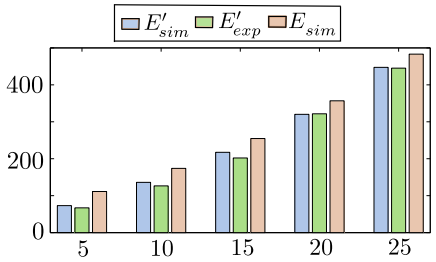

Figure 10: Comparison: E'_{sim}, E'_{exp} and E_{sim} (in μJ) for [800V, 3.5Ω]

B. Actual loss obtained using behavioural simulation (E_{sim}) and proposed analytical model (E_{anly})

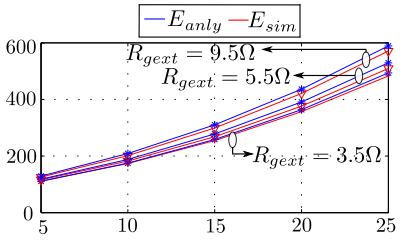

Figure 11: Comparison: E_{sim} vs E_{anly} (in μJ)

Actual loss obtained from the behavioural simulation (E_{sim}) is compared with the loss estimated from the proposed analytical model (E_{anly}) in Fig. 11. A close aggremet is observed. As mentioned before, there is a significant difference between actual loss and experimentally measured loss and the proposed

analytical model predicts the actual switching loss. Unlike [6], good match is observed for high values of R_{gext}.

C. (di/dt) obtained using behavioural simulation ($(di/dt)_{sim}$), proposed analytical model ($(di/dt)_{anly}$) and experiment ($(di/dt)_{exp}$)

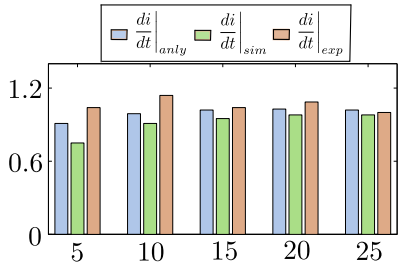

Figure 12: Comparison: $(di/dt)_{anly}$, $(di/dt)_{sim}$ and $(di/dt)_{exp}$ (in A/ns) for [800V, 9.5Ω]

Table IV: Comparison of (di/dt) (A/ns)

(800V, 25A, 3.5Ω)			(800V, 25A, 9.5Ω)		
Anly	Sim	Exp	Anly	Sim	Exp
1.156	1.6	1.28	1.02	0.98	1.0

(di/dt) obtained from proposed analytical model, behavioural simulation and experiment are plotted in Fig. 12 for $V_{dc} = 800V$, $R_{gext} = 9.5\Omega$ and $I_0 = 5 - 25A$. A close agreement is observed. For a fixed V_{dc} and R_{get}, (di/dt) remains almost constant with I_0. From Table IV it can be observed that, for a fixed V_{dc} and I_0, (di/dt) reduces as R_{gext} increases but they are weakly correlated. It is noteworthy that the turn on (di/dt) is heavily dictated by the common source inductance L_s and it can not be controlled properly by varying R_{gext}.

D. (dv/dt) obtained using behavioural simulation ($(dv/dt)_{sim}$), proposed analytical model ($(dv/dt)_{anly}$) and experiment ($(dv/dt)_{exp}$)

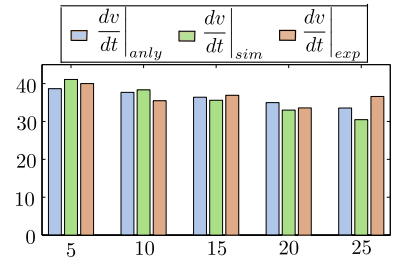

Figure 13: Comparison: $(dv/dt)_{anly}$, $(dv/dt)_{sim}$ and $(dv/dt)_{exp}$ (in V/ns) for [800V, 9.5Ω]

(dv/dt) obtained from proposed analytical model, behavioural simulation and experiment are plotted in Fig. 13 and results are closely matching. Unlike turn off switching transient of SiC MOSFET and schottky diode pair, (dv/dt) does not vary noticeably as I_0 changes for a fixed V_{dc} and R_{gext}. This is because of the fact that i_{ch} is higher than I_0 during voltage fall period (Mode IV) and difference between i_{ch} and I_0 remains almost constant with the change in I_0. Also for a fixed V_{dc} and I_0, (dv/dt) reduces with the increase in R_{gext} as can be seen from Table V and unlike (di/dt), R_{gext} has strong control over turn on (dv/dt).

Table V: Comparison of (dv/dt) (V/ns)

(800V, 25A, 3.5Ω)			(800V, 25A, 9.5Ω)		
Anly	Sim	Exp	Anly	Sim	Exp
50.38	55.57	51.67	33.55	30.47	38.22

V. Conclusion

An analytical model to study the turn on switching dynamics of SiC MOSFET and schottky diode pair using datasheet parameters and external circuit parasitics is presented in this paper. This model is derived from the behavioural model. Proposed analytical model estimates (di/dt), (dv/dt) and actual turn on switching loss. Effect of external gate to drain parasitic capacitance is taken into account which results in better estimation of (dv/dt) and loss incurred for high value of external gate resistance. Also a simplified analysis during voltage fall period is proposed. It has been validated through behavioural simulation and experiment for a 1.2kV SiC MOSFEET and schottky diode pair.

It has been observed that there is a significant difference between the experimentally obtained loss and the actual switching loss and the proposed analytical model estimates the actual switching loss. Turn on (di/dt) and (dv/dt) does not vary noticeably with load current for a fixed DC bus voltage and external gate resistance. On the other hand, (dv/dt) is highly correlated with external gate resistance for a fixed DC bus voltage and load current whereas (di/dt) has weak correlation.

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