# Design and Implementation of 1.5 kW Half Bridge Bidirectional DC-DC Converter based on Gallium Nitride devices

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***Abstract*—Use of wide band gap devices such as SiC MOSFET and GaN HEMT in a converter results in high power density and high efficiency as compared to state of the art Si switches. The objective of this work is to build a 350V DC (input), 1.5kW buck converter with switching frequency 100kHz. Commercially available GaN devices are compared based on performance in terms of package, conduction and switching losses. The module achieves more than 97% efficiency at all values of the current.**

***Index Terms*—Gallium nitride (GaN), little box challenge (LBC), high electron mobility transistor (HEMT), silicon carbide (SiC), two dimensional electron gas (2DEG).**

## I. Introduction

GaN high electron mobility transistors (HEMT) belong to the category of wide band gap (WBG) power devices and it is gaining attraction due to its superior switching performance and lower on state voltage drop. GaN HEMTs are available in the voltage range of 15-650V and current ranging from 0.5-90A. Power electronic converters are nowadays widely used in applications like rooftop solar, EV charging, data center power supplies, UPS etc. where achieving high efficiency and power density is of primary focus. Commonly used two stage architecture consist of AC-DC stage followed by an isolated DC-DC stage. AC side is connected to 230V, single phase AC and the intermediate DC bus is regulated approximately at 400V. So the power devices of AC-DC stage and primary side of DC-DC has to withstand voltage greater than 400V. Generally, devices of 600-650V is used. GaN HEMTs available in this voltage range are of two types: enhancement mode GaN (e-GaN) and cascode GaN. In this voltage range, Si super junction (SJ) MOSFETs are also widely used in state-of-the-art converters. On state drain source resistance $R_{DS(ON)}$, rise time $t_r$ and fall time $t_f$ of e-GaN and SJ MOSFET are in the same range (see $Q_{rr}$ in Table I). One of the main shortcomings of SJ MOSFET is its poor body diode performance which leads to large reverse recovery loss in hard switched converters as given in Table I. So, the converter efficiency will get reduced (AC-DC stage in these applications). One may argue that in case of soft switched converters, effect of reverse recovery will not be present and zero switching loss can be achieved which increases the efficiency and power density, but it is well established in the literature that due to hysteresis effect of the output capacitor, almost 50% of the stored energy gets lost in one charge discharge cycle [1]. So using SJ MOSFETs are not advantageous also for soft switching converters. Reverse recovery effect is not present in GaN HEMTs. Also very small hysteresis effect of the output capacitance of the device makes it attractive for both hard and soft switched converters [1].

TABLE I: Important parameters of GaN and SJ MOSFET.

| Parameter | e-GaN (GS66508T) | SJ MOSFET (IPZ60R125P6) |
|---|---|---|
| Gate - source resistance $R_{DS(ON)}(m\Omega)$ (for $T_j$=25°$C$) | 50 | 56 |
| Gate - source resistance $R_{DS(ON)}(m\Omega)$ (for $T_j$=150°$C$) | 129 | 125 |
| Maximum junction temperature $T_{j(max)}(^\circ C)$ | 150 | 150 |
| Gate charge $Q_G(nC)$ | 5.8 | 68 |
| Reverse recovery charge $Q_{rr}(nC)$ | 0 | 6000 |
| Rise time $t_r(nsec)$ | 3.7 | 5 |
| Fall time $t_f(nsec)$ | 5.2 | 3.5 |
| Device package | SMD | SMD |

Although several benefits are offered by the GaN devices but very fast switching transient and lower threshold voltage make it sensitive to circuit parasitics. Some of the detrimental effects due to fast switching transients like Miller turn on, dead time oscillation etc. are common for GaN HEMTs [2]. So one of the main challenges is to design optimum layout to reduce circuit parasitics. Due to highly dense packaging and small thermal relief pads, there is possibility of failure due to formation of local hot spots. Hence, thermal design also needs careful attention. Half bridge leg is the basic building block of AC-DC and DC-DC stage. Here we have studied the performance of a GaN HEMT based half bridge leg where two enhancement mode GaN HEMTs are connected in series. Half bridge is operated as a synchronous buck converter.

Section II describes the characteristics of different types of GaN devices available in the market. In section III, loss estimations for e-GaN and cascode GaN are shown which is required to select the device. Section IV and V show the various important points considered during the designing of the module. Section VI shows the experimental results with module operated as a buck converter.

## II. GaN HEMT characteristics, comparison and applications

High power density is required in many applications including electric vehicles and renewable energy systems [3]. For these applications, wide band gap devices are extensively

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being used due to their better performance in medium power range converters. “Google Little Box Challenge (LBC)” sponsored by Google was held in 2014-2015 to design a high power density 2kVA converter [4]. In this competition, many GaN devices were used due to their superior performance. Different commercially available GaN devices are shown in Table II.

TABLE II: Commercially available HV GaN devices.

| Manufacturer | Voltage Range ($V$) | Current Range ($A$) | Gate Source Voltage ($V$) | Device Structure |
|---|---|---|---|---|
| GaN systems | 650 | 5-60 | 0 to 6 / -3 to 6 | e-GaN |
| Transphorm | 600 | 6-70 | 0 to 8 | Cascode GaN |
| Panasonic | 600 | 10-26 | 5 to 4 | e-GaN |
| EPC | 200 | 5-48 | 0 to 5 | e-GaN |
| Texas instruments | 600 | 12 | - | Half bridge module |
| Infineon | 600 | 12-31 | 0 to 4 | e-GaN |

The cascode, e-GaN and direct drive GaN devices have different structures as shown in Fig. 1.

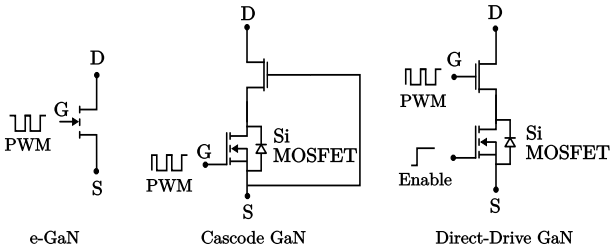


Fig. 1: Circuit diagram of different GaN HEMTs.

### A. e-GaN

e-GaN is an enhancement mode device, which is normally off when no gate-source voltage $V_{GS}$ is applied. Fig. 2 shows the output characteristics of e-GaN at different working states. Similar to a MOSFET, the device offers same $R_{DS(ON)}$ in forward and reverse direction during on state [5]. There is no body diode, but the 2DEG channel conducts during off state. The resistance offered by channel during off state $R_{DS(REV)}$ is different than $R_{DS(ON)}$. The voltage drop during reverse conduction (with $V_{GS} \leqslant 0$) is dependent on the threshold voltage and negative $V_{GS}$ applied. Hence, dead time losses will be higher if more negative $V_{GS}$ is applied during turn off state [5]. Threshold voltage and maximum/minimum transient $V_{GS}$ limit is less in case of GaN devices, these put strict limit on operating $V_{GS}$. Reverse recovery effect will not be seen in e-GaN as it is a majority carrier device.

### B. Cascode GaN

Cascode GaN comprises of a depletion mode GaN and a low voltage Si MOSFET connected in cascode configuration. Fig. 3 shows the output characteristics of Cascode GaN. Gate pulses are given to the low voltage Si MOSFET. $V_{DS}$ of the low voltage Si MOSFET directly drives $V_{GS}$ of the normally on GaN HEMT ($V_{DS(Si)}$ = -$V_{GS(GaN)}$). During forward conduction, $R_{DS(ON)}$ of Si MOSFET comes in series with

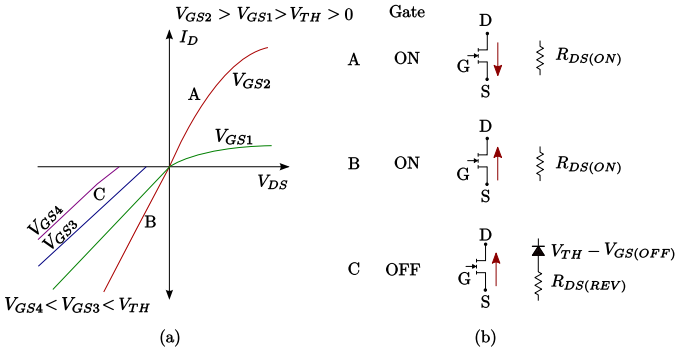


Fig. 2: (a) Static characteristics of e-GaN, (b) equivalent circuits during on and off states.

the $R_{DS(ON)}$ of normally on GaN HEMT. Also, it can be seen from Fig. 3 that the forward characteristics of cascode GaN does not depend on applied $V_{GS}$. This is because with the applied $V_{GS}$ (across the gate source of Si MOSFET), change in $V_{DS(Si)}$ = -$V_{GS(GaN)}$ is small. So, $R_{DS(ON)}$ of normally on GaN HEMT, which has more contribution to forward on state resistance, does not change much with the change in applied $V_{GS}$. During reverse conduction when $V_{GS} > V_{th}$, same static behavior can be observed. During dead time, $V_{GS}$ applied to the Si MOSFET is less than zero and the current is flowing in the reverse direction. So the Si MOSFET channel is off and the current flows through the body diode of Si MOSFET and a small positive voltage is applied across the gate source of normally on GaN HEMT (as $V_{DS(Si)}$ = -$V_{GS(GaN)}$). So, during off state the reverse characteristic of cascode GaN can be represented by a body diode of Si MOSFET in series with $R_{DS(ON)}$ of normally of GaN HEMT. Because of this, dead time losses are less as compared to e-GaN, since diode drop of low voltage Si MOSFET is low. Also there is small amount of reverse recovery present in cascode GaN due to the body diode of low voltage Si MOSFET.

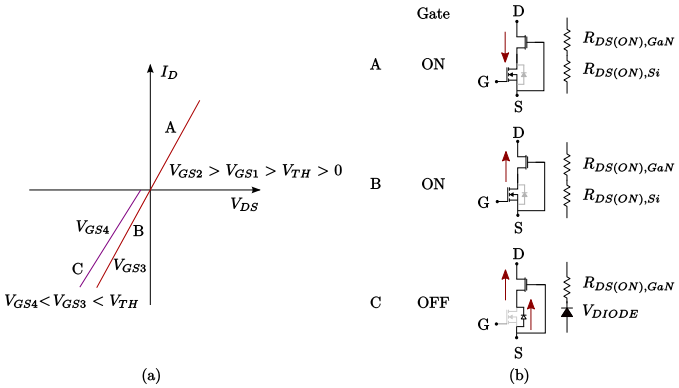


Fig. 3: (a) Static characteristics of cascode GaN, (b) equivalent circuits during on and off states.

$R_{DS(ON)}$ for depletion mode devices are lower as compared to enhancement devices. However, the total $R_{DS(ON)}$ for cascode structure is the addition of $R_{DS(ON)}$ of depletion

mode device and that of low voltage Si MOSFET which becomes comparable to e-GaN as shown Table III. Since the $V_{GS}$ is applied to the Si MOSFET, operating gate source voltage range is higher for cascode GaN.

### C. Direct drive GaN

Direct drive GaN is a series configuration of normally on GaN and a low voltage Si MOSFET. Conduction is controlled by giving pulses to low voltage Si MOSFET. Static characteristics of direct drive GaN is similar as e-GaN, only difference is that the low voltage Si MOSFET resistance comes in series with normally on GaN HEMT during both forward and reverse conduction as shown in Fig. 4. Also, during off state and reverse conduction $V_{DS}$ drop is little higher compared to e-GaN as normally on GaN HEMT has negative threshold voltage. No reverse recovery is present in direct drive GaN.

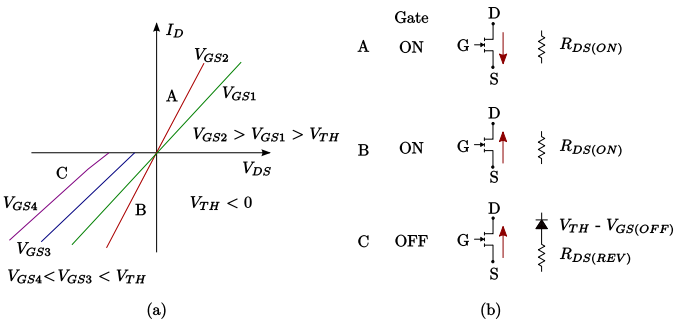


Fig. 4: (a) Static characteristics of direct drive GaN, (b) equivalent circuits during on and off states.

Various static and switching parameters for the following three GaN devices are shown in Table III and Table IV.

1) e-GaN - GS66508T, GaN Systems (650V, 30A).
2) Cascode GaN - TPH3205WSB, Transphorm (600V, 35A).
3) Direct drive GaN half bridge module - LMG3410R070, Texas Instruments (600V, 12A).

TABLE III: Static parameters of different GaN devices.

| Parameter | e-GaN | Cascode | Direct drive GaN |
|---|---|---|---|
| $V_{GSH}$/ $V_{GSL}(V)$ | 7/-10 | 18/-18 | |
| Gate threshold voltage $V_{TH}(V)$ | 1.7 | 2.1 | - |
| On state drain source resistance $R_{DS(ON)}$(mΩ) ($T_j$=25°$C$) | 50 | 50 | 70 |
| On state drain source resistance $R_{DS(ON)}$(mΩ) ($T_j$=150°$C$) | 129 | 120 | 110 |
| Dead time drain source voltage $V_{DT}(V)$ | 6 | 1.5 | - |

From the above comparison we observe that, e-GaN has lowest on state resistance, rise and fall time and no reverse recovery but the voltage drop during dead time is high. Whereas cascode GaN has almost similar $R_{DS(ON)}$ as e-GaN, lower dead time losses but high reverse recovery loss and higher output charge.

## III. Device Loss Estimation

Conduction and switching losses in e-GaN and cascode GaN are calculated and compared. Losses are calculated using two methods given below.

TABLE IV: Switching parameters of different GaN devices.

| Parameter | e-GaN | Cascode | Direct drive GaN |
|---|---|---|---|
| Reverse recovery charge $Q_{rr}(nC)$ | 0 | 136 ($i_D$ = 22 A, $V_{DD}$ = 400 V, $di/dt$ = 1000 A/$\mu$s) | 0 |
| Reverse recovery time $t_{rr}(nsec)$ | 0 | 40 | - |
| Output charge $Q_{oss}(nC)$ | 57 | 107 | - |
| Rise time $t_r(nsec)$ | 3.7 | 7.6 | - |
| Fall time $t_f(nsec)$ | 5.2 | 8.6 | - |

### A. Switching loss estimation using gate charge method

Gate charge method is a conventional method to calculate the switching energy losses for a buck converter configuration as shown in Fig. 5. Here, $V_{DC}$ is the DC bus voltage and $I_o$ is the load current. Gate charges during different switching transitions are taken from the gate charge characteristics of the device for a given $V_{DC}$ and $I_o$. The parameters taken from the datasheet of e-GaN and cascode GaN are given in Table V and external circuit conditions are in Table VI. For all other values of $V_{DC}$ and $I_o$, gate charges and corresponding energy losses are calculated by equations given in [6]. This is plotted in Fig. 6 and Fig. 7 for e-GaN and cascode GaN respectively with $L_s$ = $L_{loop}$ = 0.

TABLE V: Values taken from the datasheet gate charge curve

| Parameter | e-GaN ($V_{DC}$ 400$V$, $I_o$ 15$A$) | Cascode GaN ($V_{DC}$ 400$V$, $I_o$ 22$A$) |
|---|---|---|
| Gate charge I $Q_{GS1}(nC)$ | 0.7692 | 4 |
| Gate charge II $Q_{GS2}(nC)$ | 1.0638 | 5.1 |
| Gate drain charge $Q_{GD}(nC)$ | 2.013 | 8.9 |
| Average gate drain capacitance $C_{GDav}(pF)$ | 6.6875 | 42.1875 |
| Input capacitance $C_{iss}(pF)$ | 275 | 2250 |
| Miller plateau voltage $V_{GP}(V)$ | 3 | 2.8 |
| Internal gate resistance $R_{Gint}(\Omega)$ | 1.5 | 1.5 |
| Gate threshold voltage $V_{TH}(V)$ | 1.7 | 2.1 |
| $V_{GSH}(V)$ | 6 | 6 |

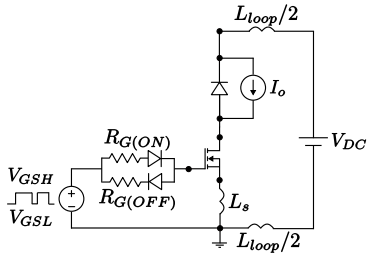


Fig. 5: PSPICE simulation circuit for loss estimation.

### B. Switching loss estimation using PSPICE simulation

PSPICE models for the two devices have been taken from the manufacturer website and the circuit shown in Fig. 5 is simulated in PSPICE software with conditions given in Table

VI. Diodes are taken as ideal diode with no reverse recovery. Fig. 6 and Fig. 7 shows the total energy loss $E_{on} + E_{off}$ for current $I_o$ varying from $1A$ to $20A$ with $L_s$ = $L_{loop}$ = 0 for e-GaN and cascode GaN respectively. Fig. 8 shows the same for e-GaN with inclusion of parasitic inductances.

TABLE VI: Circuit conditions for switching loss calculations.

| Parameter | Value |
|---|---|
| $V_{GSH}$/ $V_{GSL}(V)$ | $6/-3V$ |
| $R_{G(ON)}(\Omega)$ | $10\Omega$ |
| $R_{G(OFF)}(\Omega)$ | $1\Omega$ |
| Common source inductance $L_s$ $(nH)$ | $2nH$ |
| Loop inductance $L_{loop}$ $(nH)$ | $10nH$ |
| Current $I_o(A)$ | $1A$ - $20A$ |
| DC input voltage $V_{DC}(V)$ | $400V$ |

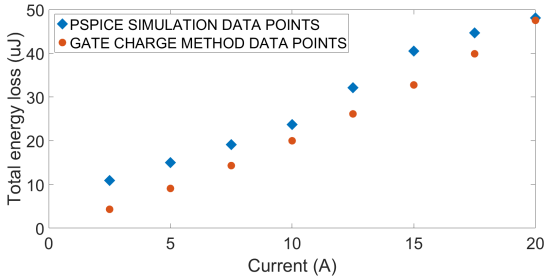


Fig. 6: Switching energy loss v/s current for GS66508T without including parasitic inductance effects.

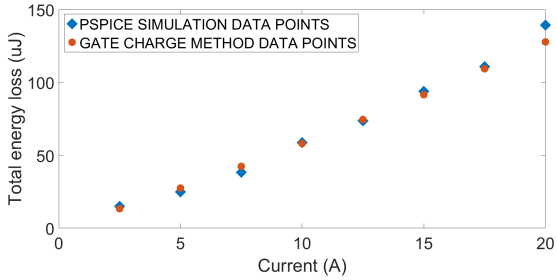


Fig. 7: Switching energy loss v/s current for TPH3205WSB without including parasitic inductance effects.

### C. Total loss in a buck converter

The total loss for buck converter operation is given by,

$$P_{loss(sw)} = I_{DS}^2 \times R_{DS(ON)} \times d + (E_{on} + E_{off}) \times f$$

For e-GaN, the total loss for 100kHz, 0.5 duty ratio and 1.5kW output power is 33.08Watt. For cascode GaN, total loss is 36.39Watt. This difference further increases with higher switching frequency. From Section II and III, we observe that e-GaN offers slight better performance than cascode GaN. Also, e-GaN offers more challenging design due to its critical device parameters. Hence e-GaN is chosen as operating device.

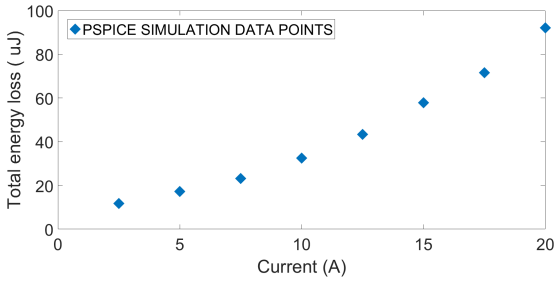


Fig. 8: Switching energy loss v/s current for GS66508T (including parasitic inductance effects).

## IV. Gate driver and power circuit design

### A. Gate driver selection

For selection of gate driver,points considered are below.

1) Gate driver isolation voltage should be greater than maximum DC bus voltage with some margin for voltage appearing across parasitic inductance. For DC bus voltage of 350V, it should be greater than 600V.
2) Since the switching time are in nano seconds for e-GaN, propagation delay, rise time and fall time of gate driver should be minimum (in the order of $nsec$).
3) For $V_{GSH}$/$V_{GSL}$ of $6/-3V$ and $R_{G(ON)}/R_{G(OFF)}$ of $10\Omega/1\Omega$, Peak output current of gate driver required is $I_{Gpeak(ON)}$ =$\frac{9}{11.5}$ = $0.7826A$ and $I_{Gpeak(OFF)}$ =$\frac{9}{2.5}$ = $3.6A$ Here, internal gate resistance of GaN device $R_{G(int)}$ = $1.5\Omega$ is included.
4) CMTI rating greater than $(100-200)kV/\mu s$

TABLE VII: Important gate circuit parameters.

| Parameter/Component | Value/Part number |
|---|---|
| $V_{GSH}$/$V_{GSL}(V)$ | $6/-3V$ |
| $R_{G(ON)}(\Omega)$ | $10\Omega$ |
| $R_{G(OFF)}(\Omega)$ | $1\Omega$ |
| Dead time $(nsec)$ | greater than $(40-50)nsec$ |
| Gate driver | Si labs Si8271x |
| Isolated power supply | PES1-S5-S9-M-TR |

### B. Gate driver circuit critical points

- $V_{GS}$ applied is $6/-3V$. Although negative voltage increases the dead time losses but still it is applied to avoid miller turn on. Also, $R_{G(OFF)}$ is kept minimum to avoid gate source voltage shoot up above threshold voltage during device turn off.
- Dead time should be more than the summation of propagation delay skew, rise time/fall time delay of the device and delay due to gate driver IC.

$$t_{dead} > \Delta t_{pd} + t_d + max(t_r/t_f)$$

### C. Layout considerations

Two gate driver loops shown in Fig. 9 are compared [7]. Four layer PCB is used. In Fig. 9(a), gate driver IC and the GaN device are placed on the bottom side of PCB. In Fig. 9(b),

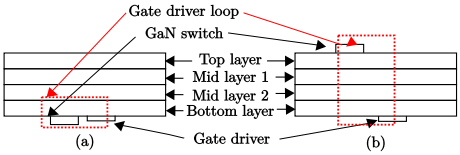


Fig. 9: Gate driver circuit layout.

gate driver is placed on top side and GaN device is placed on bottom side of PCB. Due to inductance of vias, gate driver loop inductance in Fig. 9(b) is higher. Hence layout similar to Fig. 9(a) is selected.

Power loop consists of high frequency capacitors and two

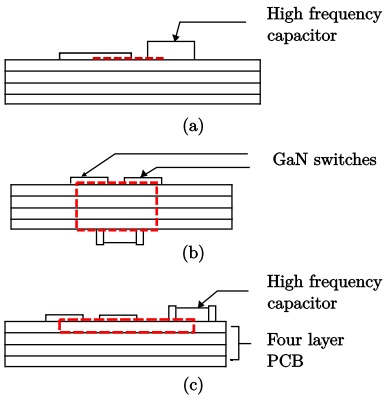


Fig. 10: Power circuit layout.

e-GaN devices. Fig. 10 shows comparison of three different layouts. In Fig. 10(a) high frequency capacitors and GaN device are placed on the same side and the return path is on the same PCB layer. Since the current return path is on the same layer, there is no flux cancelling effect in this case. In Fig. 10(b), high frequency capacitors and GaN device are placed on the opposite side of PCB which results in larger power loop inductance due to inductance of the vias. In Fig. 10(c), placement is on same side of PCB but the return path is taken from the adjacent PCB layer which minimizes the loop inductance due to flux cancelling effect. Hence layout similar to Fig. 10(c) is designed.

## V. Thermal Design

Top cooled package GS66508T is selected. In this package, the device thermal pad can be directly attached to heat sink. Due to small thermal pads in e-GaN as compared to Si MOSFET, smaller size heat sink with large number of fins and small fin gaps are required. These type of heat sinks are used for IC cooling. The heat sink chosen is ATS-FPX060060013-112-C2-R1. SIL-PAD 2000 is used as electrically insulating TIM (ITIM) and T766 phase change material is used as electrically conducting TIM (CTIM). Two heat sink assemblies I and II as shown in Fig. 11(a) and Fig. 11(b) respectively are selected for comparison. In assembly I, e-GaN device is directly connected to the heat sink using electrically insulating TIM. In assembly II, a copper bar is placed between each GaN device and the heat sink. The copper bars remain at their respective source potentials and they are separated from the heat sink using electrically insulating TIM. These two assemblies are compared by using equivalent thermal circuit model as well as by SOLIDWORKS simulation.

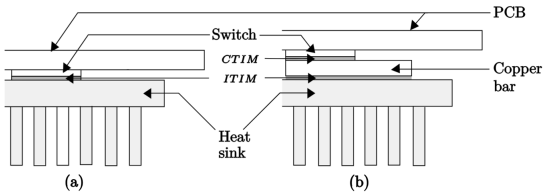


Fig. 11: Heat sink assembly diagram (a) assembly I, (b) assembly II.

### A. SOLIDWORKS simulation

SOLIDWORKS simulations for both assemblies with convection coefficient 112W/$m^2$ °C are shown in Fig. 12. Convection coefficient h is calculated with conventional method as given in [8]. For calculation simplifications of h, the air flow is considered uniform and direction is assumed in horizontal plane. Whereas in actual set up, the air flow direction is vertical plane and temperature near the axis of fan will be higher due to improper flow of air at the center. SOLIDWORKS simulations give 101°C and 74.5°C maximum heat sink temperatures for assembly I and II respectively for a power loss of 10Watt per device.

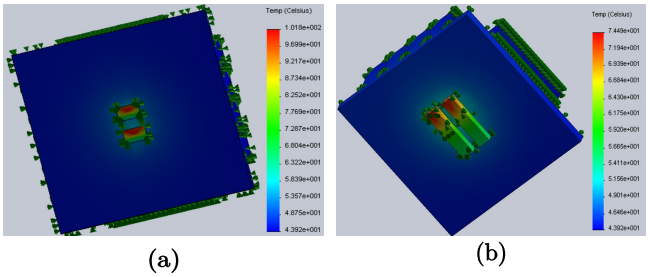


Fig. 12: SOLIDWORKS simulation results for (a) heat sink assembly I, (b) heat sink assembly II.

### B. Equivalent thermal model

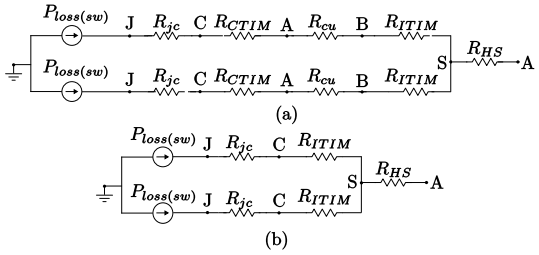


Fig. 13: Equivalent thermal circuit for (a) heat sink assembly I, (b) heat sink assembly II.

Fig. 13(a) and Fig. 13(b) show equivalent thermal circuits for heat sink assembly I and assembly II respectively. Table

VIII gives the different equivalent thermal resistances of the components. Thermal resistance of the heat sink is taken from the datasheet for unducted air flow and 700 LFM air velocity, which is also proved experimentally. Here it is to be noted that the equivalent thermal model analysis can only be used for comparative analysis since heat transfer in this case is not a one dimensional problem. So, the actual result will vary from the calculated values.

TABLE VIII: Thermal resistances in heat sink assembly I and assembly II

| Assembly | $R_{jc}$ | $R_{CTIM}$ | $R_{cu}$ | $R_{ITIM}$ | $R_{HS}$ |
|---|---|---|---|---|---|
| Assembly I | 0.5°C | - | - | 4.15°C | 1.3°C |
| Assembly II | 0.5°C | 0.62°C | 0.20°C | 0.86°C | 1.3°C |

Although there are more resistances in circuit with heat sink assembly II, but due to increase in area of insulating TIM, overall resistance of insulating TIM is reduced since the maximum thermal resistivity is offered by insulating TIM. For 10Watt power loss per device, the case temperature with assembly I and assembly II is 67.5°C and 42.8°C respectively. Hence, it is observed that heat sink assembly II shows better thermal performance.

## VI. Experimental results

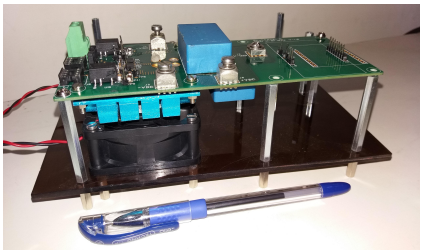

Fig. 14: PCB image of half bridge module.

### A. Buck converter operation

TABLE IX: Parameters for buck converter operation

| Parameter | Value |
|---|---|
| DC bus voltage $V_{DC}$ | 350 $V$ |
| Output current $I_o$ | 1 - 8 $A$ |
| Output inductor $L$ | 0.6 $mH$ |
| Duty cycle $d$ | 0.5 |
| Switching frequency $f_{sw}$ | 100 $kHz$ |

Fig. 14 shows one half bridge module. The circuit is operated as a buck converter to observe the losses at different currents. Table IX shows the operating conditions. Fig. 16 shows that efficiency is more than 97% for all values of current. Efficiency for 1.55kW output power is 97.6%.

## VII. Conclusion

The paper describes different types of medium voltage GaN devices available in the market along with its characteristics, static and switching parameters. Loss estimations for the e-GaN and cascode GaN switch are done based on gate charge method and PSPICE simulation. e-GaN is found to show slight better performance than cascode GaN. Different critical points for designing gate driver and power circuit with e-GaN GS66508T is given. For thermal management, a novel heat sink assembly is designed which offers efficient heat extraction as well as cost benefits. Results of buck converter operation show more than 97% efficiency at all operating currents.

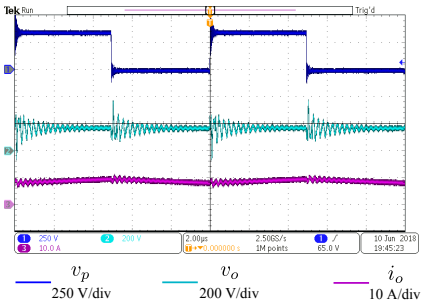


Fig. 15: Experimental waveforms for buck converter operation at 100 kHz fsw, 350V $V_{DC}$ and 8A $I_o$

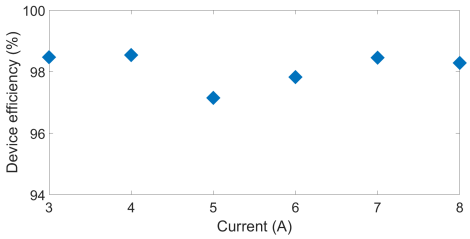


Fig. 16: Device efficiency v/s current curve for buck converter operation

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