A Partially Soft-Switched DC/AC High Frequency Link Unidirectional Converter for Medium Voltage Grid Integration

Abstract—**This paper presents a novel single stage high frequency link DC to AC converter for the integration of utility scale photovoltaic systems (> 100 kW) to the medium voltage (11 kV) electric grid. This type of converter is also gaining popularity in applications such as compact UPS, storage, hybrid vehicles and grid connection of distributed renewable generation systems The use of high frequency transformer (HFT) reduces the volume, weight and cost of overall system. For the conventional grid integration of high power photovoltaic system , galvanic isolation is necessary to ensure safety and to reduce the leakage current. The proposed topology aims at a direct connection to the medium voltage grid leading to reduced conduction loss. A direct medium voltage integration implies high voltage blocking semiconductor switches in the grid side converter. These type of switches are mostly commercially not available, require complicated gate drivers and due to inherently slow speed results in higher switching loss. Considering unidirectional nature of active power flow, this paper proposes an unidirectional grid side converter topology which is only line switched, along with a small shunt reactive power compensator. The primary side converter is soft-switched. The operation of the converter is analysed in detail. Key Simulation results are presented to confirm the operation of the proposed converter.**

Keywords—SPWM inverter, High frequency link, Phase shifted full bridge, Reactive compensation, H bridge, Medium voltage integration, Soft-switching.

I. Introduction

The electric power grid all over the world is experiencing major integration of utility scale photovoltaic resources. Due to the abundance of sunlight in many parts of the country, India is currently producing 4229.36 MW [1] from solar per year. The conventional grid integration system (in Fig. 1) uses line frequency transformers to achieve required voltage magnification as well as galvanic isolation to ensure safety and to reduce leakage current. The use of line frequency transformers increases the overall system cost and volume. An alternative option is - high frequency transformer (HFT) link based grid integration [2]. The high frequency link (HFL) provides required voltage magnification, galvanic isolation. Low volume , weight and low cost high frequency transformer link replaces conventional line frequency counterpart. The application of high frequency link converter system is not only restricted to distributed generation systems but also finds applications in naval and aerospace power supplies where compactness and reliability are essential, UPS and energy storage system, fuel cell based hybrid vehicle [3] etc.

The high frequency link inverters discussed in literature are broadly classified in two types: multi-stage and single-stage. A conventional multi-stage HFL inverter [4] has following

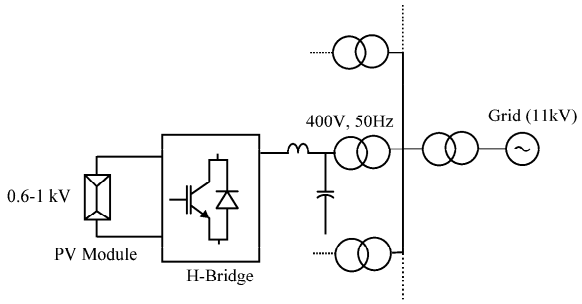

Fig. 1. State of the art utility scale PV generation

stages: DC-high frequency AC-DC-adjustable frequency AC, as shown in Fig. 2. This requires intermediate bulky DC link capacitor. The capacitor creates long term reliability issue for such a system. Usually the primary side high frequency square wave inverter is hard switched. The secondary side inverter is sine triangle pulse width (SPWM) modulated. To commute leakage energy of HFT, additional circuitry with active and passive components are required. The single stage high frequency inverter is also classified in two types: rectifier type HFL (RHFL) and cyclo-converter type HFL (CHFL). The RHFL type topology has structure similar to its multi-stage counterpart (in Fig. 3) except the intermediate stage dc link capacitor is removed [5], [6]. In this topology, additional active or passive snubber circuit is required to commute leakage energy of the HFT. In CHFL [7], [8], [9] and [10] the secondary of the HFT is directly connected to the load through an AC to AC cyclo-converter as shown in Fig. 4. The cyclo-converter first rectifies the high frequency AC and then generates line frequency PWM AC output. The cyclo-converter merges the rectifier and the voltage source inverter (VSI) of RHFL. Different modulation strategies are employed to achieve soft-switching of the cyclo-converter. Auxiliary circuits are employed to commute the leakage energy of HFT. In [11] a source based commutation technique is used which eliminates the need of additional commutation circuitry. Paper [12] has reported a combined synchronous rectifier based HFL inverter which is a derived topology from CHFL by breaking the operation of ac switches in two parts- positive synchronous rectifier (PSR) and negative synchronous rectifier (NSR) and a modulation strategy for their alternative operations in positive and negative half of the line frequency cycle. This break-up of operation reduces the conduction loss.

The grid side converter in all of the single stage HF link converters reported in literature [13], [14] switches at higher frequency. In this paper a novel topology (in Fig. 5)

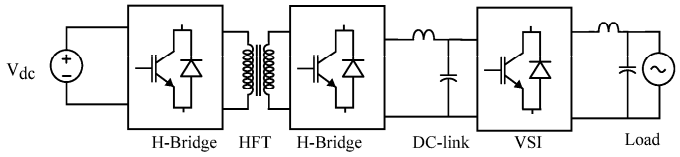

Fig. 2. Multi-stage topology

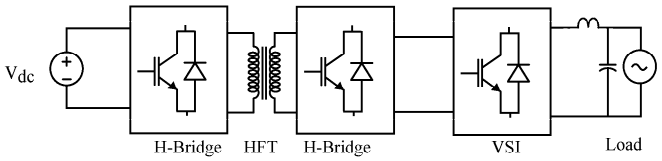

Fig. 3. RHFL topology

is reported which employs SPWM modulation of primary side HF converter and the grid side converter is line switched. The primary side converter first generates bipolar, high-frequency, pulse width modulated (PWM) square wave using sine triangle PWM which contains line frequency AC information. Then the required voltage magnification is achieved using the HFT. The amplified, PWM, bi-polar voltage pulse train is then rectified to generate unipolar PWM voltage pulses which carry the information of line frequency AC. The grid side DC-AC converter is only line switched at the zero-crossing of the output current to generate required line frequency AC voltage. The unity power factor (UPF) operation of grid side converter is implemented considering unidirectional nature of active power flow of photovoltaic grid connected systems. The required reactive power by line inductance along with the grid end filter is supplied by a shunt reactive compensator. The energy stored in leakage inductance of the HFT and parasitic capacitances of devices is used to soft-switch the primary side high frequency inverter which reduces switching loss of the HF converter. Thus requirement for any additional circuitry to commute the leakage energy of the HFT is avoided. The line frequency zero-voltage and zero current switching of the

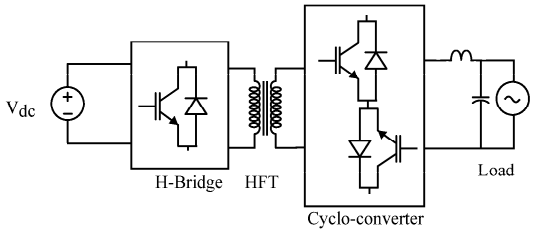

Fig. 4. CHFL topology

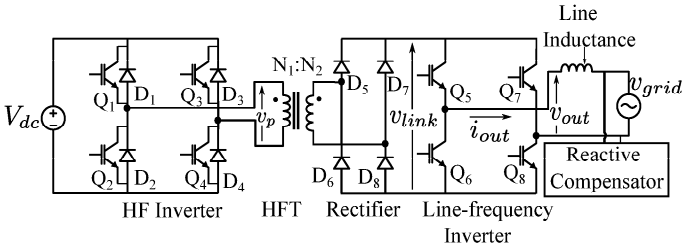

Fig. 5. Simplified circuit diagram of the proposed grid connected high-frequency link inverter

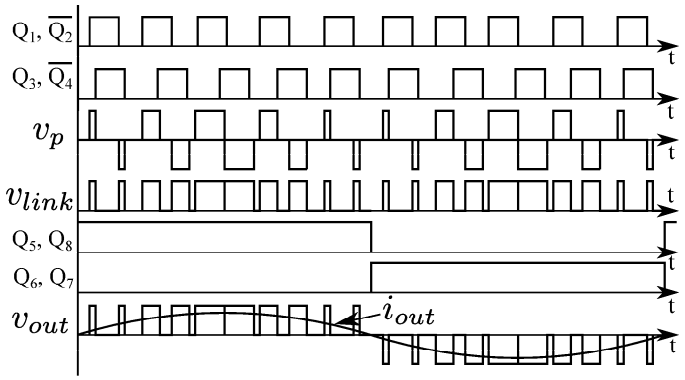

Fig. 6. Switching scheme of the proposed converter

grid side converter resolves the problem of high switching loss of the inherently slow high voltage blocking semiconductor devices and also avoids the requirement of complicated gate drive circuit to implement any modulation technique. In this paper, operation of the proposed topology and simulation results for open loop operation are presented.

The organization of this paper is as follows. Section II presents the proposed operation and analysis of the converter and is divided into three subsections- PWM modulation technique of low voltage side high frequency DC to AC inverter; soft switching of primary side converter and working principle of the shunt reactive power compensation at the grid end. Key simulation results are presented in Section III.

II. Analysis

This section presents the control of the proposed converter. the analysis is divided into three subsection-(a) generation of PWM line frequency AC, (b) soft-switching of the primary side HF converter and (c) unity power factor operation.

A. Modulation technique

The modulation strategy of the proposed converter is shown in Fig. 6. The sine-triangle PWM technique is employed to control the operation of the primary side HF inverter. In a switching cycle, the operation of the HF inverter is similar to a phase shifted full bridge converter. The output of the HF inverter is fed to the primary of the high frequency transformer. To avoid transformer saturation, the average voltage applied across the transformer primary should be zero. So, to achieve flux balance per switching cycle, a control signal F is considered with 50% duty ratio and switching frequency $\frac{1}{2T_s}$ as shown in the Fig. 7. The positive slope unipolar saw-tooth carrier C at a frequency $f_s = \frac{1}{T_s}$ is compared with a modulation signal $d(t)$ and generate the signal X as shown in Fig. 7. The modulation signal $d(t)$ is expressed as-

$$d(t) = |M \cdot sin(2\pi ft)| \tag{1}$$

where, M is the peak value of the modulation signal and f is the grid frequency. The gating signals for the switches of the HF inverter are derived form F and X as follows.

$$Q_1 = F \tag{2}$$

$$Q_2 = \overline{Q_1} \tag{3}$$

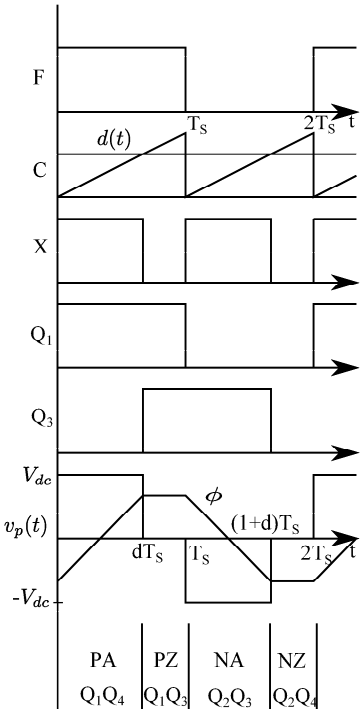

Fig. 7. Modulation scheme of primary side HF inverter

$$Q_3 = F \otimes X \tag{4}$$

$$Q_4 = \overline{Q_3} \tag{5}$$

Above switching scheme will generate active and zero states like in a phase shifted full bridge converter operation as shown in Table I. The sequence of the switching states are shown in Fig. 7. The control scheme will apply a primary voltage, v_p (in

TABLE I. STATES IN PHASE SHIFTED FULL BRIDGE CONVERTER OPERATION

Switching state	On switches
Positive Active (PA)	Q_1Q_4
Positive Zero (PZ)	Q_1Q_3
Negative Active (NA)	Q_2Q_3
Negative Zero (NZ)	Q_2Q_4

Fig. 6), at the HFT such that volt-second balance is achieved. The volt-second balance equation is given as-

$$|V_{dc} \cdot dT_S| = |-V_{dc} \cdot (T_S - (1+d)T_S)| \tag{6}$$

where, d is the duty ratio and V_{dc} is the input voltage of the converter. The secondary side average rectified PWM line frequency AC voltage is shown in Fig. 6 and is expressed as-

$$\overline{v_{link}}(t) = \frac{N_S}{N_P} \cdot M \cdot V_{dc} |sin(2\pi ft)| \tag{7}$$

where, N_P and N_S are number of primary and secondary turns of HFT respectively. The grid side inverter is line switched. The switching signals are applied at the zero crossing of the converter current. The gating signals, Q_5 - Q_8 are shown in Fig. 6. The output of the converter $v_{out}(t)$, average PWM line frequency AC is expressed as-

$$\overline{v_{out}}(t) = \frac{N_S}{N_P} \cdot M \cdot V_{dc} \cdot sin(2\pi ft) \tag{8}$$

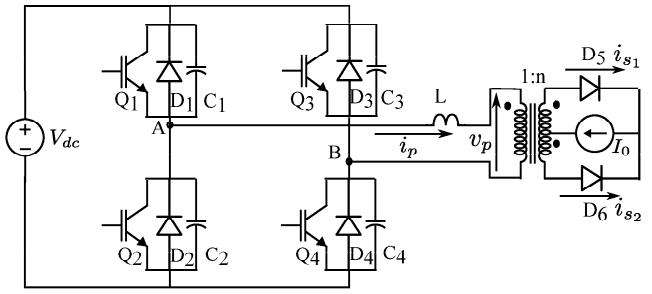

Fig. 8. Simplified circuit diagram to explain soft-switching of the HF inverter

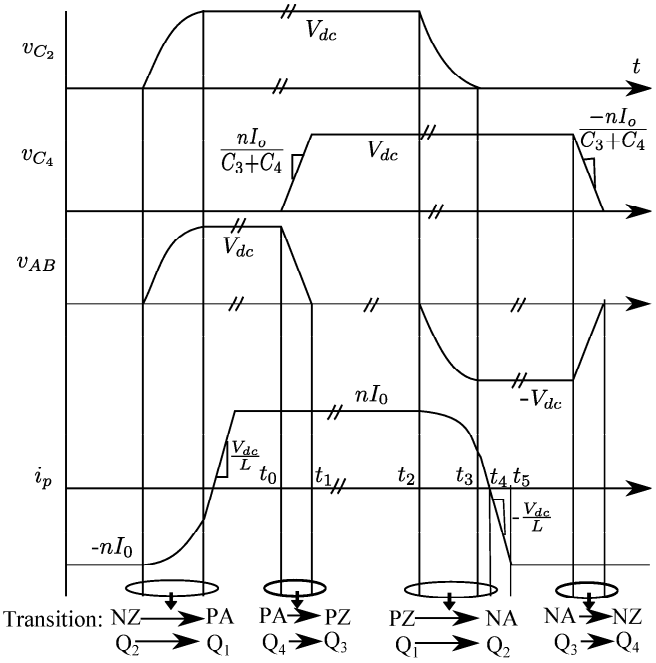

Fig. 9. Switching waveforms illustrating the zero voltage switching mechanism [15].

B. Soft-switching of the primary side high frequency converter

Using the leakage inductance of the high frequency transformer and the device parasitic capacitances, zero voltage switching of the primary side HF inverter is achievable. Like a phase shifted full bridge converter, the HF converter has two types of switching transition: active state to zero state and zero state to active state [15]. Circuit operation during these transitions are discussed in the following sections. Figure 8 shows the simplified circuit diagram to discuss the soft switching operation. For the simplification of the presentation, the secondary of the HFT with full diode bridge in Fig. 5 can be equivalently replaced with the centre tapped rectifier configuration as in Fig. 8. Switching waveforms during these transitions are presented in Fig. 9. Using KCL at the HFT winding the primary current i_p is expressed as-

$$i_p = n(i_{S1} - i_{S2}) \tag{9}$$

where n is the transformer turns ratio: $\frac{N_S}{N_P}$. The load current I_0 is given by

$$I_0 = (i_{S1} + i_{S2}) \tag{10}$$

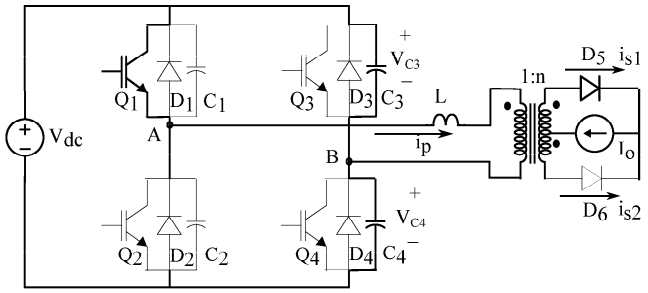

Fig. 10. Circuit diagram during subinterval: $t_0 < t < t_1$ of active to zero state transition

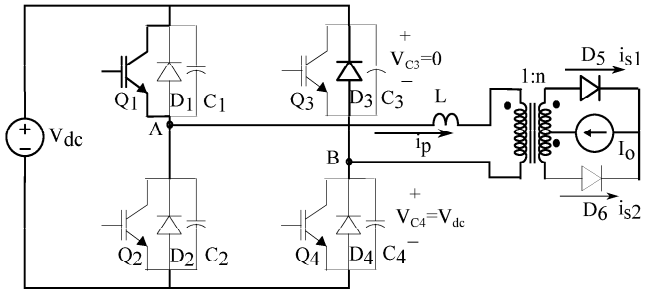

Fig. 11. Circuit diagram during subinterval: $t_1 < t < t_2$ after active to zero state transition

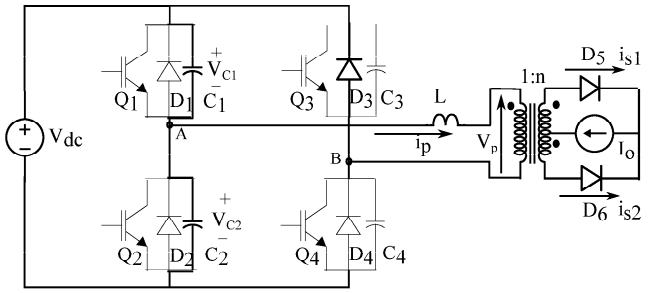

Fig. 12. Circuit diagram during subinterval: $t_2 < t < t_3$ of zero to active state transition

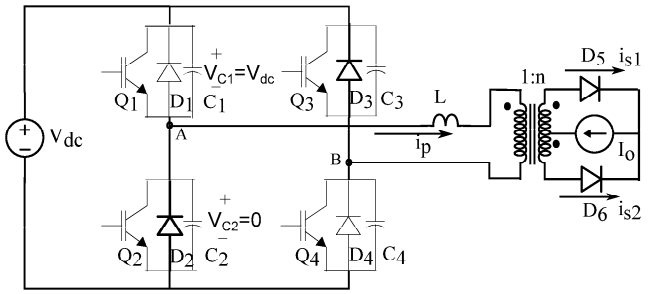

Fig. 13. Circuit diagram during subinterval: $t_3 < t < t_4$ of zero to active state transition

1) Active to zero transition: The leg B devices are switched during this transition. The transition from Q_4 to Q_3 is similar with transition from Q_3 to Q_4 except the polarity of the primary current. Hence, Q_4 to Q_3 transition is discussed here in detail. The equivalent circuit in this interval is shown in Fig. 10.

Sub-interval: $t_0 < t < t_1$

This interval starts with the turn off of the device Q_4. Initial conditions during this sub interval are: $v_{c3}(t_0) = V_{dc}$, $v_{c4}(t_0) = 0$, $v_{AB}(t_0) = V_{dc}$, $v_L(t_0) = 0$, $i_p(t_0) = nI_0$, $i_{S1}(t_0) = I_0$, $i_{S2}(t_0) = 0$. In this interval the primary current will remain constant and is nI_0 as shown in Fig. 9. So, the presence of leakage inductance (L) will not cause any LC oscillation during this switching transition. The primary current will start charging the capacitor C_4 and discharging the capacitor C_3. Applying, KCL at node B and KVL across leg B, the governing equations are derived as follows:

$$-C_3\frac{dv_{c3}(t)}{dt} + C_4\frac{dv_{c4}(t)}{dt} = i_p(t) \tag{11}$$

$$v_{c3}(t) + v_{c4}(t) = V_{dc} \tag{12}$$

Using (11) and (12), it is shown that, the voltage v_{c3} will fall linearly with a slope $\frac{nI_0}{(C_3+C_4)}$ and v_{c3} is given as

$$v_{c3}(t) = -nI_0\frac{t}{(C_3+C_4)} + V_{dc} \tag{13}$$

At t = t_1, C_3 is discharged to zero and the diode D_3 starts conducting. Due to diode D_3, v_{c3} can not go to negative. To achieve ZVS of the switch Q_3, gating pulse needs to be applied after t_1, when the diode D_3 is conducting. So, the dead time between gating signal of Q_3 and Q_4 should be greater than $(t_1 - t_0)$. And t_1 is given as-

$$t_1 = \frac{V_{dc}(C_3+C_4)}{nI_0} + t_0 \tag{14}$$

At the end of this interval, the switch Q_1 and the diode D_3 will continue to conduct the primary current as shown in Fig. 11.

2) Zero to active transition: Only leg A devices are switched in this transition. During NZ to PA state change over, Q_2 is turned off and Q_1 is turned on and during PZ to NA state change over, Q_1 is turned off and Q_2 is turned on as shown in Fig. 9. The governing equations of these two switching transitions are similar and hence transition from Q_1 to Q_2 is only discussed here. The primary voltage of the transformer v_p is zero through-out the interval.

Sub-interval: $t_2 < t < t_3$

This interval starts at the moment Q_1 is turned off. The simplified circuit diagram in this interval is shown in the Fig. 12. At the beginning of this interval, the circuit conditions are given as: $v_{c1}(t_2) = 0$, $v_{c2}(t_2) = V_{dc}$, $v_{AB}(t_2) = 0$, $v_L(t_2) = 0$, $v_p - 0$, $i_p(t_2) - nI_0$, $i_{S1}(t_2) - I_0$, $i_{S2}(t_2) - 0$. From the Fig. 9, the primary current starts falling in this interval. So, transformer leakage inductance will play a role in charging and discharging of capacitors C_1 and C_2. Applying KCL at node

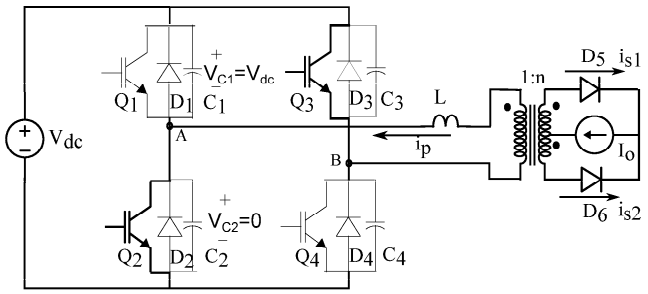

Fig. 14. Circuit diagram during (t> t_4)

A, the governing circuit equation in this interval is expressed as follows:

$$C_1\frac{dv_{c1}}{dt} = C_2\frac{dv_{c2}}{dt} + i_p \tag{15}$$

Applying KVL,

$$v_{c1} + v_{c2} = V_{dc} \tag{16}$$

$$v_{c1} + v_L + v_p = 0 \tag{17}$$

$$v_L - L\frac{di_p}{dt} \tag{18}$$

By solving (15) to (18), the primary current is expressed as-

$$i_p(t) = nI_0 \cdot cos\left(\frac{t}{\sqrt{L(C_1+C_2)}}\right) \tag{19}$$

And the voltage of the capacitor C_1 is given as-

$$v_{c1}(t) = nI_0 \cdot \sqrt{\frac{L}{C_1+C_2}} sin\left(\frac{t}{\sqrt{L(C_1+C_2)}}\right) \tag{20}$$

At $t = t_3$, v_{c1}(t) will reach V_{dc} and will remain there. v_{c2}(t) discharges to zero and the diode D_2 starts conducting. The new circuit configuration is shown in Fig 13.

Sub-interval: $t_3 < t < t_4$

As the diode D_2 and D_3 are conducting (Fig. 13), a negative voltage is applied across the leakage inductor (L) which will linearly reduce the primary current further. The voltage drop across the leakage inductor is given as-

$$L \cdot \frac{di_p}{dt} + V_{dc} = 0 \tag{21}$$

By solving (21), the primary current is expressed as-

$$i_p(t) = -\frac{V_{dc}}{L}(t - t_3) + i_p(t_3) \tag{22}$$

The primary current will reach to zero at time t_4 and this interval will end.

$$t_4 = \frac{L}{V_{dc}} \cdot i_p(t_3) + t_3 \tag{23}$$

In between $t_3 < t < t_4$ the diode D_2 will conduct. To achieve ZVS of Q_2, gating pulse should be applied within this interval. So the condition for the dead time between the gating signals of switches Q_1 and Q_2 can be expressed as: $(t_3 - t_2) <$ dead time $< (t_4 - t_2)$.

For a given leakage inductance and device capacitances, ZVS is not possible below a certain value of the primary current. The condition is given as-

$$nI_0 \cdot \sqrt{\frac{L}{C_1+C_2}} > V_{dc} \tag{24}$$

Sub-interval: $t_4 < t < t_5$

In this interval, the primary current is negative and continues to fall with same slope $-\frac{V_g}{L}$. The device Q_2 and Q_3 will conduct. The circuit diagram is shown in Fig. 14. At the time t_5 the current i_p reaches $-nI_0$. t_5 is expressed as-

$$t_5 = \frac{L}{V_{dc}} \cdot (nI_0) + t_4 \tag{25}$$

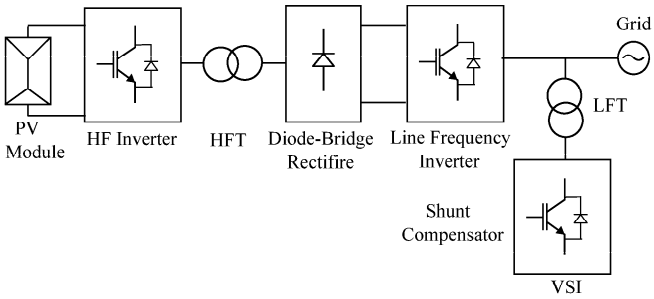

Fig. 15. Schematic diagram for reactive power compensation of line loss

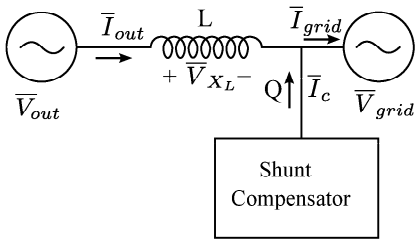

Fig. 16. Circuit diagram for shunt reactive compensation

C. Reactive power compensation

The proposed topology is unidirectional and the modulation technique ensures the unity power factor operation of the grid side converter. To compensate the reactive power requirement by line reactance a shunt compensator (a voltage source inverter) with a small line frequency transformer is connected at the grid end of the converter as shown in Fig. 15. This inverter supplies only the reactive power needed to keep the grid current at unity power factor (UPF). The size of the line frequency transformer and the power rating of the inverter will be small.

The reactive power supplied by the shunt compensator can be estimated as follows. As shown in Fig. 16, the shunt compensator is connected at the grid end. Phasor diagram associated with reactive power estimation is shown in Fig. 17. The active power drawn by the grid at UPF is given as-

$$P = |\overline{V}_{grid}| \cdot |\overline{I}_{grid}| \tag{26}$$

This active power is supplied by the converter. Power supplied by the converter-

$$|\overline{V}_{out}| \cdot |\overline{I}_{out}| = P \tag{27}$$

From the phasor diagram in Fig. 17-

$$\overline{V}_{out} = \overline{V}_{grid} + j \cdot X_L \cdot \overline{I}_{out} \tag{28}$$

The grid voltage $\overline{V}_{grid}$ and active power requirement (P) are given and are equal to 1 p.u. The line inductive reactance is

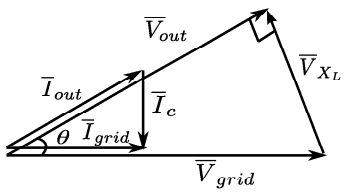

Fig. 17. Phasor diagram for shunt reactive compensation

considered 0.05 p.u. By solving (26) - (28) following quantities are estimated as- $\overline{V}_{out} = 0.9987$ p.u., $\overline{I}_{out} = 1.001$ p.u., $\overline{I}_c = 0.045$ p.u. So, the reactive power supplied by the shunt compensator- $Q = |\overline{V}_{grid}| \cdot |\overline{I}_c| = 0.045$ p.u. or 4.5% of the total power rating of the converter.

III. Simulation Results

The proposed topology is simulated and is verified with theoretical analysis. The simulation parameters are presented in Table II. Fig. 18 presents the simulated grid phase voltage

TABLE II. Simulation parameters

Parameter	Particulars
V_{dc} (V)	600
V_{grid} (V) (L-L)	400
f_{grid} (Hz)	50
Power (kW)	100
Peak modulation index (M)	0.8
HFT turns ratio	100:68
Line impedance (at 50 Hz)	0.05 p.u (0.255 mH)
Reactive compensator (X_C)	35.56 Ω
HFT leakage impedance (at 5 kHz)	0.05 p.u (5.5 μH)
Capacitance across the device	37 nF
Dead time	1.0 μs
HF inverter switching frequency	5 kHz

and line current. v_{grid} and i_{grid} are in phase. The peak values of v_{grid} and i_{grid} from simulation results are 320 V and 198 A respectively. Fig. 19 shows PWM output voltage of the converter v_{out} in phase with the converter output current i_{out}. i_{out} contains high switching ripple. Whereas v_{grid} and i_{grid} have negligible ripple content. The line inductor acts as filter and eliminate high switching ripple from the converter output voltage and current. v_{grid} and i_{grid} lags v_{grid} and i_{grid} by an angle 2.9° due to the presence of line reactance. Fig. 20 presents the rectified PWM voltage v_{link} and the link current i_{link} at the diode bridge rectifier output. i_{link} is the rectified form of i_{out} which also contains similar high frequency ripple. The simulation wave forms of HFT primary voltage v_{pri} and current i_{pri} is shown in Fig. 21. PWM with high frequency inversion is seen in the primary voltage waveform. The flux balance at the HFT is shown in Fig 22. The magnetising current (i_{mag}), primary voltage v_{pri} and carrier waveforms are presented. The average primary voltage and the average magnetising current are zero over a switching cycle. The soft switching of HF inverter is achieved for 50% of the peak value of primary current and above. The transition from Q_4 to Q_3 and Q_1 to Q_2 is shown in Fig. 23.

IV. Conclusion

In this paper, a converter topology with high frequency link dc-ac converter for a single phase grid connected photovoltaic system has been proposed. The proposed topology has the following features: (1) single stage and unidirectional power flow; (2) galvanic isolation with high power density HFT; (3) partial soft-switching primary side HF inverter; (4) line switched grid side (secondary side) high voltage inverter and (5) reactive loss compensation at grid end by a small size VSI. The converter has been analysed in detail and the simulated waveforms verify the operation. The converter topology can also be implemented as multi-level structure shown in Fig. 24. Multi-level topology is essential to connect the converter to a medium voltage grid with available relatively low voltage

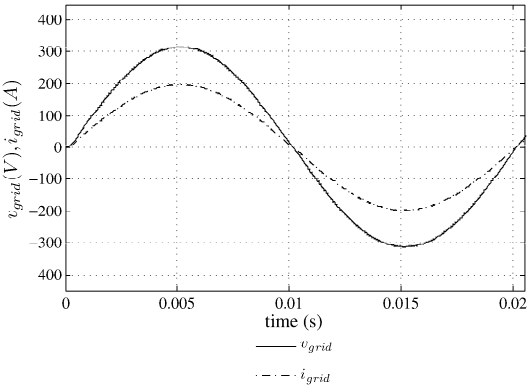

Fig. 18. Simulated voltage and current waveforms at grid end

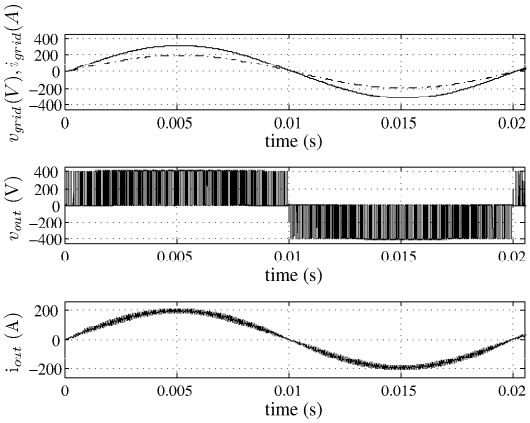

Fig. 19. Simulated waveform of the output voltage and the output current of the converter

devices in the high voltage side of the converter. This topology will be studied in future.

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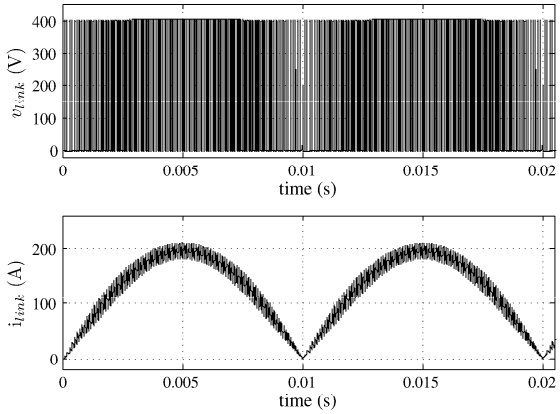

Fig. 20. Simulated waveform of the secondary side rectified link voltage and the link current

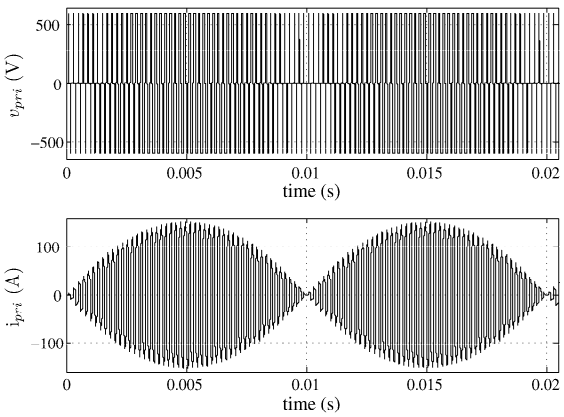

Fig. 21. Simulated waveform of the HFT primary voltage and the primary current

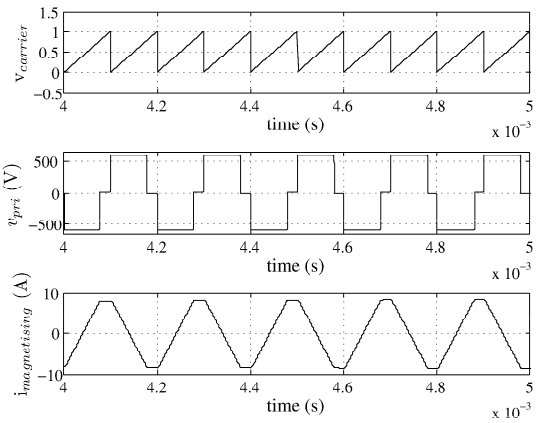

Fig. 22. Simulated waveform of the HFT primary voltage and the carrier signal

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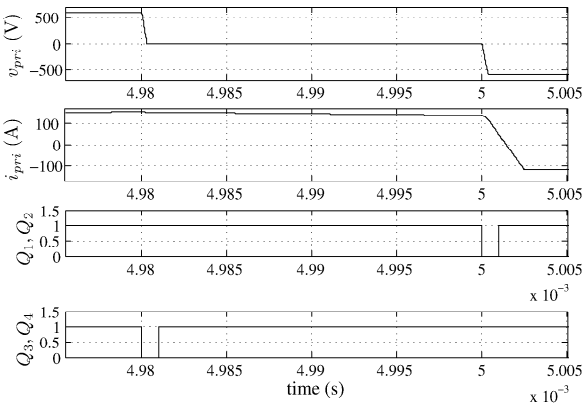

Fig. 23. Soft-switching waveforms (Z→A/Q_4→Q_3 and A→Z/Q_1→Q_2)

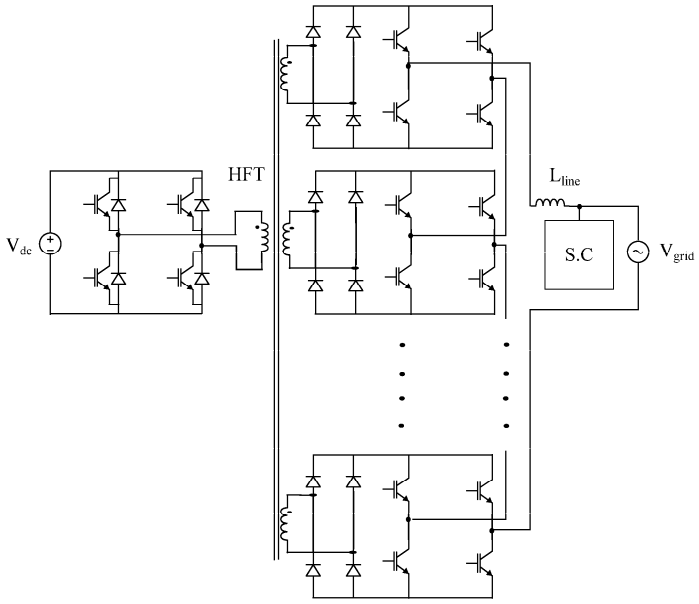

Fig. 24. Multilevel topology of the proposed converter

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