2012 IEEE International Conference on Power Electronics, Drives and Energy Systems
December16-19, 2012, Bengaluru, India

Dual two level inverter carrier SVPWM with zero common mode voltage

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***Abstract*—Conventional Space Vector PWM (CSVPWM) Voltage Source Inverters (VSI) are commonly used for adjustable speed drives. However, common mode voltage produced by these drives causes problems such as electromagnetic interference. A Space Vector PWM scheme for a dual converter has been presented in the past for eliminating common mode voltage while providing more maximum output voltage than a CSVPWM regulated VSI. In this paper, a carrier based implementation of that scheme has been presented. The algorithm does not require any square root or trigonometric calculations required by the Space Vector approach, but generates the duty ratios directly from the reference output phase voltages by simple logical operations. The paper also presents a method capable of producing switching sequence similar to CSVPWM for good output voltage quality. It requires sector determination, again from logical operations, but not the exact position of the reference output voltage space vector.**

I. INTRODUCTION

Two level voltage source inverters are one of the most widespread power electronic converters, used for dc to 3 phase ac conversion. Pulse Width Modulation or PWM is used to regulate the output voltage in these converters. Conventional Space Vector PWM (CSVPWM) [1], [2] is commonly used to modulate these converters due to high quality of the output voltage waveform. But CSPWM modulated two level VSIs apply switching common mode voltage at load terminals leading to bearing currents, failure of the shaft and conducted electromagnetic interferences [3]-[4].PWM schemes have been proposed that aim at minimizing or eliminating the common mode voltage switching [5]. It is possible to modulate the VSI without switching the common mode voltage, but such a modulation leads to poor quality of the output voltage waveform along with the reduction in the voltage gain. A dual two level inverter with a PWM scheme proposed in [6] completely eliminates the switching common mode voltage with a quality of the output voltage waveform similar to CSVPWM. The voltage gain is $\sqrt{3}$ times that of CSVPWM modulated single VSI.

A carrier based implementation of CSVPWM has been presented in [7] and [8]. It obviates the need for output voltage vector's magnitude and position determination and the subsequent calculations needed for duty ratios, thus making the implementation process simpler while giving the same output. The switching signals are obtained directly from the reference modulation signals. In this paper, a carrier based algorithm will be presented for the dual two level inverter PWM scheme in [6] that leads to common mode voltage elimination. The paper begins with an introduction to the dual two level inverter and the voltage vectors to be used in the scheme. Then the process of developing the carrier based algorithm is described. Finally, simulation results are presented to prove the functionality of the algorithm.

II. DUAL TWO LEVEL INVERTER AND ZERO COMMON MODE VOLTAGE SPACE VECTORS

A dual two level inverter drive comprises one two level inverter on each side of the three phase load [9] as shown in Fig.1.

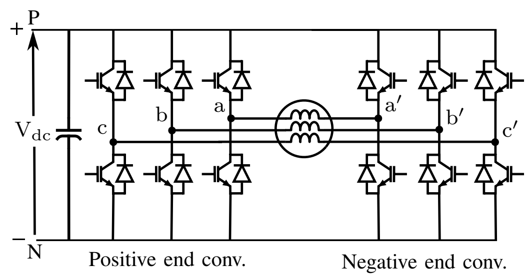

Fig. 1. Dual 2 level inverter drive

The two inverters are called positive and negative end converters. They share the same dc bus, the positive and negative terminals of which are denoted by P and N respectively. The load terminals connected to positive end and negative end converters are labeled as a, b, c and a′, b′, c′ respectively. The space vectors of positive end and negative end converters are shown in Fig 2. We observe that the vectors of the negative end converter are opposite in direction to those of the positive end converter. The voltage vector synthesized at positive end of the load is given in (1).

$$\mathbf{V_{PE}} = V_{aN} + V_{bN}e^{j\frac{2\pi}{3}} + V_{cN}e^{j\frac{4\pi}{3}} \tag{1}$$

The positive end converter has six active vectors or switching states, which are produced by the a, b, c terminals connected to either P or N. So when terminal a and b are connected to

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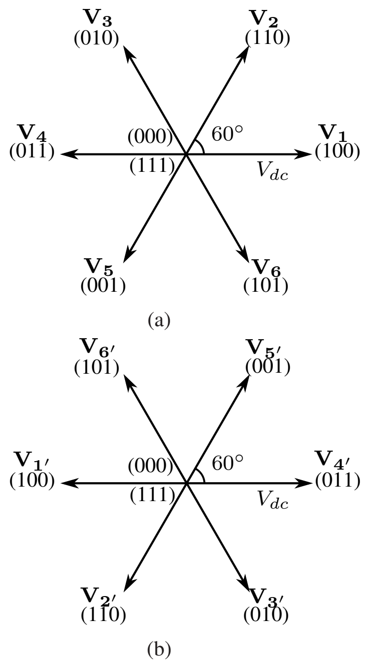


Fig. 2. Space vectors (a)Positive End conv. (b)Negative End conv.

P while c is connected to N, the voltages V_{aN} and V_{bN} are V_{dc} while the voltage V_{cN} is zero. Thus, the voltage vector V_2 is synthesized which has magnitude V_{dc} at an angle of sixty degrees. Similarly, the voltage vector synthesized by the negative end converter is given in (2).

$$\mathbf{V_{NE}} = -(V_{a'N} + V_{b'N}e^{j\frac{2\pi}{3}} + V_{c'N}e^{j\frac{4\pi}{3}}) \tag{2}$$

When terminal a' is connected to P while b' and c' are connected to N, the voltage $V_{a'N}$ is V_{dc} while the voltages $V_{b'N}$ and $V_{c'N}$ are zero. Thus, the voltage vector $V_{1'}$ is synthesized which has a magnitude of V_{dc} and is at an angle of 180 degrees. The positive end common mode voltage is defined as

$$V_{PE,com} = \frac{V_{aN} + V_{bN} + V_{cN}}{3}$$

and the negative end common mode voltage is defined as

$$V_{NE,com} = \frac{V_{a'N} + V_{b'N} + V_{c'N}}{3}$$

Based on above expressions, the vectors $\mathbf{V_1}$, $\mathbf{V_3}$ and $\mathbf{V_5}$ have equal common mode voltage viz. $V_{dc}/3$ while the vectors $\mathbf{V_2}$, $\mathbf{V_4}$ and $\mathbf{V_6}$ have equal common mode voltage viz. $2V_{dc}/3$. The common mode voltage across the three phase load is given by $V_{PE,com} - V_{NE,com}$. The zero sequence currents through the load should be zero. This implies that the common mode voltage across the load terminals should be zero at all times. In order to eliminate switching common mode voltage, either we can use $\mathbf{V_1}$, $\mathbf{V_3}$ and $\mathbf{V_5}$ from the positive end and $\mathbf{V_{1'}}$, $\mathbf{V_{3'}}$ and $\mathbf{V_{5'}}$ from the negative end converter. Alternatively, we could use the voltage vectors $\mathbf{V_2}$, $\mathbf{V_4}$ and $\mathbf{V_6}$ from the positive end converter and vectors $\mathbf{V_{2'}}$, $\mathbf{V_{4'}}$ and $\mathbf{V_{6'}}$ from the negative end converter. When either of these sets of vectors are being used, the common mode voltage across the load is zero. We will select the first set for our discussion. The six vectors in this set can be combined to produce the resultant six vectors of the dual converter as shown in Fig.3.

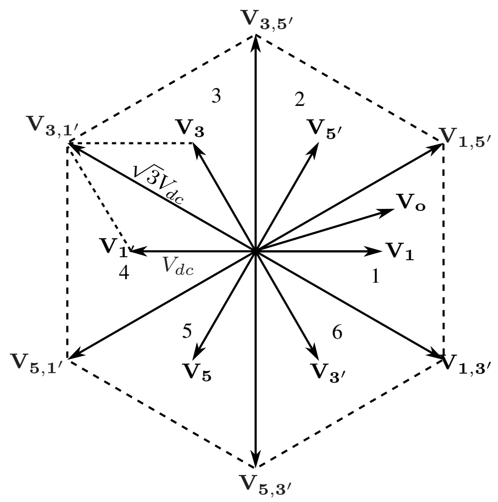


Fig. 3. Resultant and individual converter space vectors

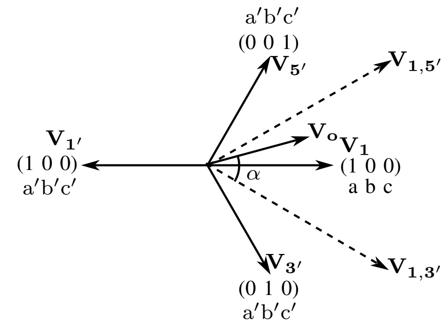
The resultant vectors are of magnitude $\sqrt{3}V_{dc}$ and are shifted by $30°$ counterclockwise with respect to the individual converter space vectors. Thus, the sectors are also shifted by the same amount. They form six sectors which are also labeled in the figure as 1 through 6. The output phase voltages to be synthesized across the load are given by (3)

$$\begin{aligned} V_{aa'} &= V_o\cos(\omega t) \\ V_{bb'} &= V_o\cos(\omega t - \frac{2\pi}{3}) \\ V_{cc'} &= V_o\cos(\omega t + \frac{2\pi}{3}) \end{aligned} \tag{3}$$

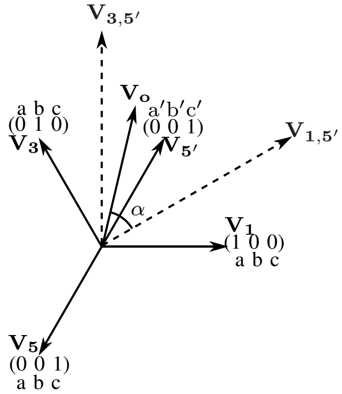
where ω is the output angular frequency and V_o is the peak of the output phase voltages. These values can be used to construct the output voltage vector as:

$$\mathbf{V}_o = V_{aa'} + V_{bb'}e^{j\frac{2\pi}{3}} + V_{cc'}e^{j\frac{4\pi}{3}} = \frac{3}{2}V_oe^{j\omega t} \tag{4}$$

So, the output voltage vector as in (4), is of magnitude $\frac{3}{2}V_o$ and rotates at an angular speed of ω in counterclockwise direction. The output voltage vector can be in any of these six sectors and once the sector is identified, the two adjacent active vectors are used to synthesize the average output voltage vector in one sampling time period. If the total time of active vectors is less than the sampling time period, a zero vector is applied for the remaining time, which is realized by vectors $\mathbf{V_{1,1'}}$, $\mathbf{V_{3,3'}}$ and $\mathbf{V_{5,5'}}$. Let us consider the case where the output voltage vector is in the first sector. This situation is shown in Fig.4(a).



(a) $\mathbf{V_o}$ in Sector 1



(b) $\mathbf{V_o}$ in Sector 2

Fig. 4. Output voltage vector $\mathbf{V_o}$ in different sectors

In sector 1, output voltage vector is synthesized by the vectors $\mathbf{V_{1,3'}}$ and $\mathbf{V_{1,5'}}$ as shown in (5).

$$d_1\mathbf{V_{1,3'}} + d_2\mathbf{V_{1,3'}} = \mathbf{V_o} \tag{5}$$

where d_1 and d_2 are the duty ratios of $\mathbf{V_{1,3'}}$ and $\mathbf{V_{1,5'}}$ respectively. This means that $\mathbf{V_{1,3'}}$ is applied for time d_1T_s and $\mathbf{V_{1,5'}}$ is applied for time d_2T_s where T_s is the sample time period. The zero vector used in this sector is $\mathbf{V_{1,1'}}$ which is applied for the remaining time period. Thus, we see that the vector $\mathbf{V_1}$ of positive end converter is applied for whole time while the vectors $\mathbf{V_{1'}}$, $\mathbf{V_{3'}}$ and $\mathbf{V_{5'}}$ of negative end converter are ON for times $(1-d_1-d_2)T_s$, d_1T_s and d_2T_s respectively.

III. Derivation of carrier based expressions for the duty ratios

In the previous sections, the vectors to be used in the modulation have been discussed. The technique to synthesize the output voltage using space vector approach requires following steps:

- Determination of the magnitude and angle of the average output voltage vector $\mathbf{V_o}$
- Determination of the sector the output voltage vector is in and the angle α made by $\mathbf{V_o}$ with the starting space vector for the determined sector
- Determination of the duty ratios d_1 and d_2 and d_z
- Determination of the switching states for both two level inverters to be applied for different fractions of sampling period.

The first step in above process requires an inverse trigonometric operation and a square root operation. The third step requires computation with trigonometric functions. In this section, we will discuss the carrier based technique that obviates the need to determine these output voltage vector characteristics and hence the subsequent computations for the duty ratios. The technique is motivated from the min. max. mid. technique used in conventional Space Vector PWM for a two level inverter [7]. We begin by stating that at any instant the reference output phase voltages across the load i.e. $V_{aa'}$, $V_{bb'}$ and $V_{cc'}$ are balanced, resulting in (6).

$$V_{aa'} + V_{bb'} + V_{cc'} = 0 \tag{6}$$

Now from Fig.4(a), we have

$$\begin{aligned}\vec{V}_{1,3'} &= \sqrt{3}V_{dc}e^{-j\frac{\pi}{6}}\text{and}\\ \vec{V}_{1,5'} &= \sqrt{3}V_{dc}e^{j\frac{\pi}{6}}\end{aligned} \tag{7}$$

Using (5), (4) and (7), we get

$$\sqrt{3}V_{dc}(d_1e^{-j\frac{\pi}{6}} + d_2e^{j\frac{\pi}{6}}) = V_{aa'} + V_{bb'}e^{j\frac{2\pi}{3}} + V_{cc'}e^{j\frac{4\pi}{3}} \tag{8}$$

Comparing real and imaginary parts in (8) and using (6), we get (9) and (10).

$$d_1 = -\frac{V_{bb'}}{V_{dc}} \tag{9}$$

$$d_2 = -\frac{V_{cc'}}{V_{dc}} \tag{10}$$

The above computation is repeated for all the six sectors and Table I is obtained.

TABLE I
Duty ratios d_1, d_2 for six sectors

Sector	d_1	d_2
1	-$m_{bb'}$	-$m_{cc'}$
2	$m_{aa'}$	$m_{bb'}$
3	-$m_{cc'}$	-$m_{aa'}$
4	$m_{bb'}$	$m_{cc'}$
5	-$m_{aa'}$	-$m_{bb'}$
6	$m_{cc'}$	$m_{aa'}$

where $m_{ii'} = V_{ii'}/V_{dc},\ i \in \{a, b, c\}$

Next, we identify a pattern in the output voltage waveforms to design an algorithm to send the duty ratios to the proper power switches. The three phase output reference voltage waveforms is shown in Fig.5.

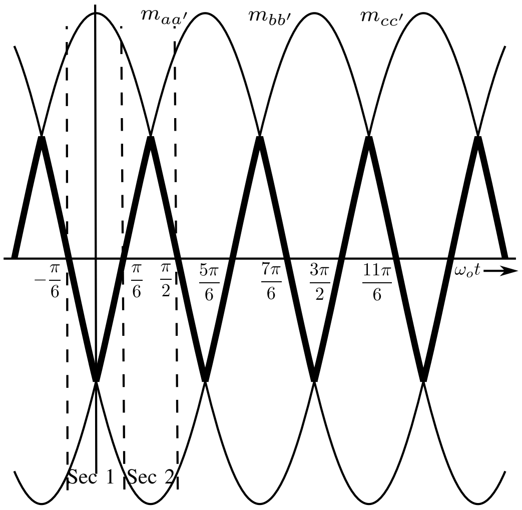


Fig. 5. 3-phase output reference voltage waveform

The waveform with medium value of the three waves is made bold. The first and second sectors, which span from $\omega t = -\frac{\pi}{6}$ to $\omega t = \frac{\pi}{6}$ and $\omega t = \frac{\pi}{6}$ to $\omega t = \frac{\pi}{2}$ respectively are marked by the vertical dashed lines and labeled **Sec 1** and **Sec 2**. We make the following observations in the first sector:

- The medium voltage is negative in sign.
- Phase a is maximum. From Fig.4(a), the positive end converter is clamped to the switching state (100). Thus, the output leg a of the positive end converter is always ON, i.e. the duty ratio d_a is 1. The other two legs are always OFF, i.e. $d_b = d_c = 0$.
- From Fig.4(a) and Table 1, the duty ratios for the legs of negative end converter corresponding to non-maximum phases i.e. $d_{b'}$ and $d_{c'}$ are equal to $-m_{bb'}$ $-m_{cc'}$ respectively.
- The duty ratio for the leg of the negative end converter corresponding the maximum phase i.e. $d_{a'}$ is $1-(-m_{bb'}-m_{cc'}) = 1 - m_{aa'}$.

In the second sector, following observations are made:

- The medium voltage is positive in sign.
- Phase c is minimum. From Fig.4(b), the negative end converter is clamped to the switching state (001). Thus, the output leg c′ of the positive end converter is always ON, i.e. the duty ratio $d_{c'}$ is 1. The other two legs are always OFF, i.e. $d_{b'} = d_{c'} = 0$.
- From Fig.4(b) and Table 1, the duty ratios for the legs of positive end converter corresponding to non-minimum phases i.e. d_a and d_b are equal to $m_{aa'}$ $m_{bb'}$ respectively.
- The duty ratio for the leg of the positive end converter corresponding the minimum phase i.e. d_a is $1-(m_{aa'} + m_{bb'}) = 1 + m_{cc'}$.

Similar observations in other four sectors give Table II.

TABLE II
PHASE DUTY RATIO BASED ON MIN MAX VALUES

Duty ratio	mid>0		mid<0	
	a is max	a isn't max	a is min	a isn't min
d_a	$1+m_{aa'}$	$m_{aa'}$	1	0
$d_{a'}$	1	0	$1-m_{aa'}$	$-m_{aa'}$
	b is max	b isn't max	b is min	b isn't min
d_b	$1+m_{bb'}$	$m_{bb'}$	1	0
$d_{b'}$	1	0	$1-m_{bb'}$	$-m_{bb'}$
	c is max	c isn't max	c is min	c isn't min
d_c	$1+m_{cc'}$	$m_{cc'}$	1	0
$d_{c'}$	1	0	$1-m_{cc'}$	$-m_{cc'}$

So, first we need to find the sign of the medium value. Once that is identified, we find which phase is minimum or maximum, depending on whether the medium voltage is positive or negative respectively. Then we can use Table II to get the duty ratios of all the six legs. This process is shown in flowchart format in Fig.6.

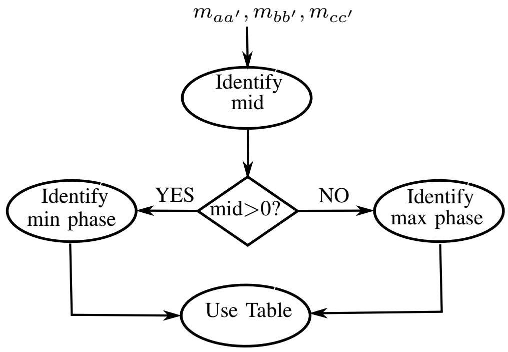


Fig. 6. Algorithm flowchart

After we have determined the duty ratios for all the six legs of both converters, we can pick duty ratios of two legs for both converters. Then we process them in the following way to produce the gate pulses for three legs:

- Add duty ratios d_a and d_b and call it d_{ab}.
- Compare d_{ab} and d_a with the carrier to produce pulses q_{ab} and q_a respectively.
- The pulse for leg b is given by q_{ab}AND (NOTq_a).
- The pulse for leg c is given by NOTq_{ab}

The above process can be repeated with $d_{a'}$ and $d_{b'}$ to produce the gate pulses for the legs of the negative end converter. This method is simple, but it fixes the order of the output phase pulses (order being cbabc in this case) and doesn't keep the zero vector centered. To get the pulses in the 0120210 order, the following method could be used:

- Determine the sign of the medium voltage.
- If medium voltage is positive, determine which phase is minimum. If medium voltage is negative, determine which phase is maximum. This gives the sector. Based on the tables II and III, get the duty ratios d_1, d_2 and d_z and which phases they are going to.
- Compare the duty ratios with a carrier to produce pulses as shown in Fig.7.

- Send the pulses based on the the information in second step to the inverter legs.

TABLE III
DUTY RATIO DISTRIBUTION BASED ON SECTOR

Mid<0 & Max phase	Sector	Inverter leg q_1 goes to	Inverter leg q_2 goes to	Inverter leg q_z goes to
A	1	b′	c′	a′
B	3	c′	a′	b′
C	5	a′	b′	c′
Mid<0 & Min phase	**Sector**	**Inverter leg q_1 goes to**	**Inverter leg q_2 goes to**	**Inverter leg q_z goes to**
A	4	b	c	a
B	6	c	a	b
C	6	a	b	c

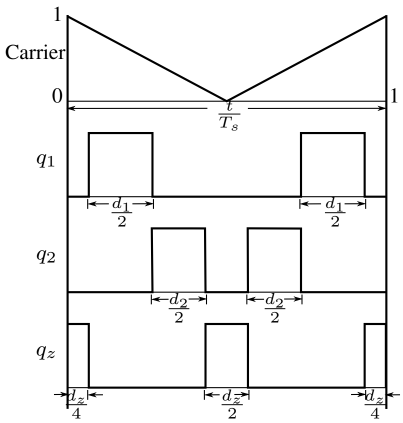


Fig. 7. Pulses with centering of zero vector

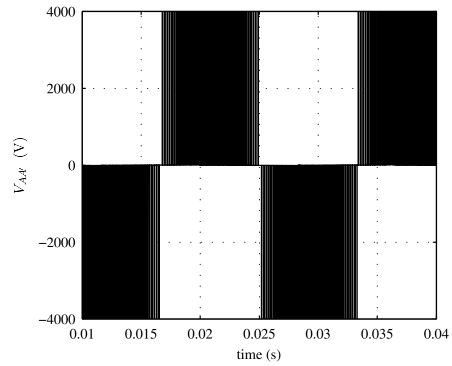
IV. SIMULATION RESULTS

The modulation scheme for the dual converter is implemented using the proposed algorithm and simulated on MATLAB Simulink. The conditions for the simulation are shown in table below:

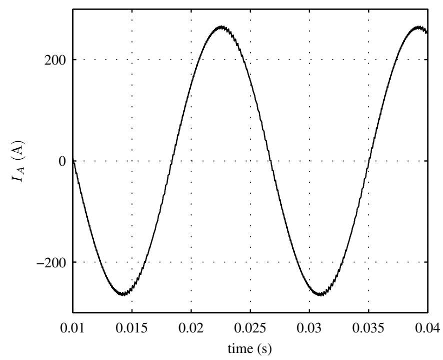
TABLE IV
SIMULATION PARAMETERS

Parameter	Value
V_{dc}	4kV
T_s	200μs
Output power	1.04MW
Power factor	0.8 lag
f	60Hz

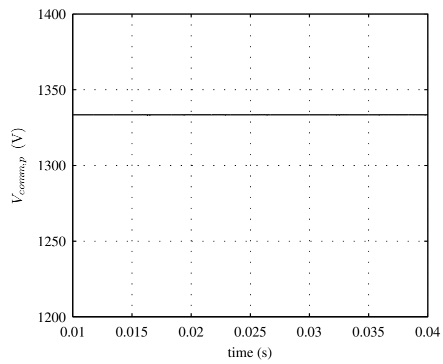
The parameter V_o is the per phase peak output voltage. The output frequency is 60Hz which corresponds to an angular frequency ω of 377rad/s. The plots resulting from the simulation are shown in Fig. 8



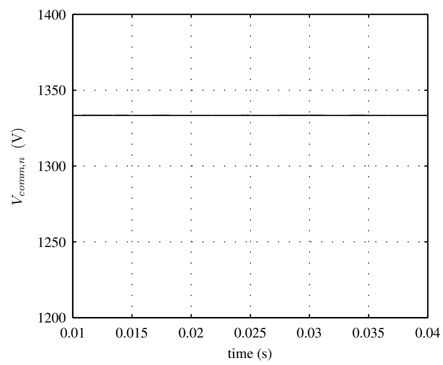
(a) Voltage across load phase a



(b) Current through output phase a

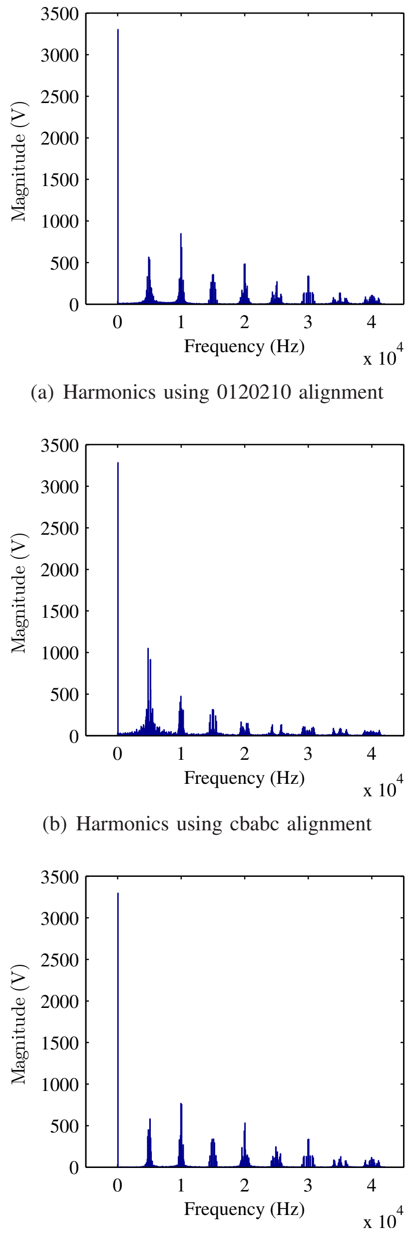


(c) Common mode voltage at positive load terminals



(d) Common mode voltage at negative load terminals

Fig. 8. Simulation results (Voltages and currents)



(a) Harmonics using 0120210 alignment

(b) Harmonics using cbabc alignment

(c) Harmonics with CSVPWM

Fig. 9. Simulation results(Harmonic spectrum of output phase voltage)

Fig.8(a) shows the switching voltage across the output phase a. Fig.8(b) shows the line current through output phase a. Its frequency is observed to be 60Hz, which is equal to the reference value, while the peak is 260A which is close to the analytical value of 263.5A. Fig.8(c) and Fig.8(d) show the positive end and the negative end common mode voltages respectively. Both the voltages are clamped at $\frac{V_{dc}}{3}$ i.e. 1666.67V. This proves that the proposed algorithm eliminates switching common mode voltages. Since the two common mode voltages are equal, they cancel out to give zero net common mode voltage across the load. This can be seen in the output current waveform as it is free from any zero sequence components. In Fig.9, the harmonic spectrum of output phase a has been shown for three PWM techniques viz. the 0120210 pulse alignment in Fig.9(a), for cbabc alignment in Fig.9(b) and for CSVPWM in Fig.9(c). The harmonics in 0120210 and CSVPWM look quite similar, while the cbabc harmonics look different, basically more harmonics in 5kHz. region, i.e. around the switching frequency.

V. Conclusion

A carrier based implementation of a Space Vector PWM scheme for a dual converter is presented. The PWM scheme is aimed at eliminating common mode voltage across the load. The implementation technique doesn't involve any square root or trigonometric calculations. It derives the phase duty ratios directly from reference output phase modulation signals by simple logical operations. A simple technique to sequence the gate pulses is presented that fixes the alignment of output phase pulses for each switching period, but doesn't require any sector information. It is also possible to apply zero vectors centered sequence same as CSVPWM in order to get high quality output voltage waveforms. Although, the application of this sequence requires sector determination, which can be again done by simple logical operations.

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