Input Filter Design of a Current Source Inverter or a Front End Rectifier : Analysis and Simulation

Kaushik Basu, Shabari Nath and Ned Mohan
Department of Electrical Engineering, University of Minnesota
Minneapolis, Minnesota 55455
Email: basux017@umn.edu

Keywords: Current source inverters, input filter design, ripple current estimation ....

Abstract

This paper presents a step by step design procedure for the input filter of a current source inverter (CSI). The design is also applicable to matrix converters. The design is based on the specifications of allowable ripple in the input voltage of the CSI and high frequency harmonic components in input grid current. Analytical techniques have been developed to estimate the ripple present in the input current and to model the converter for fundamental or grid frequency. This is essential for the analysis of input filter. The analysis and design of the input filter have been verified by simulation in MATLAB/SIMULINK environment.

1. INTRODUCTION

Current source inverter (CSI) has been in wide use for high power induction motor drives. CSI needs filters to filter the switched currents at their input. Fig. 1 shows a CSI system with input LC filters. Optimum design of these filters are required to reduce cost and size and also to meet the specifications of power quality on utility side.

A few filter design procedures have been presented in current literature. Reference [1] describes filter design in terms of selecting the break frequency in the spectrum of input current of CSI. The damping of LC resonance of input filter and its effect on closed loop control of CSI is explained in [2]. Filter design based on IEEE 519 restrictions are presented in [3]. Similar filter design procedure as in [1] is described in [4] and [5].

This paper proposes a new filter design method based on specifications of allowable ripple in the input voltage of the CSI and distortion present in the input grid current. It has been shown that this design ensures high input power factor and minimum drop in the grid voltage in the input filter. As opposed to selection of break frequency of filter, the values of L and C can be directly calculated using the expressions obtained. Section II A presents a simple carrier based modulation technique for the control of CSI [6]. In section II B an analytical method has been developed for the estimation of the ripple component present the input current of the CSI. The estimation of the ripple component of the current is essential for the filter design. This section also provides a way to model the switching converter for fundamental power flow. Section III explains the filter design procedure. Simulation results and verification of analysis is provided in section IV.

2. ANALYSIS

A simple carrier based modulation for the control of CSI has been presented. Next this modulation technique has been used to estimate the switching frequency component in the input line current and to model the converter for different frequencies.

2.1. Modulation of the CSI

Equation (1) gives the sinusoidal input voltages v_{oa}, v_{ob}, v_{oc} at the input of CSI.

$$\begin{aligned} v_{oa} &= V_o \cos \omega t \\ v_{ob} &= V_o \cos\left(\omega t - \frac{2\pi}{3}\right) \\ v_{oc} &= V_o \cos\left(\omega t + \frac{2\pi}{3}\right) \end{aligned} \tag{1}$$

where V_o is the peak and ω (normally $2\pi 60$ rad/sec) is the angular frequency of the sinusoidal input voltage.

Each leg of the CSI consists of three switches i.e. the switches in the top leg are S_{aA}, S_{bA}, S_{cA}. In any one leg no two switches can be ON simultaneously (to avoid

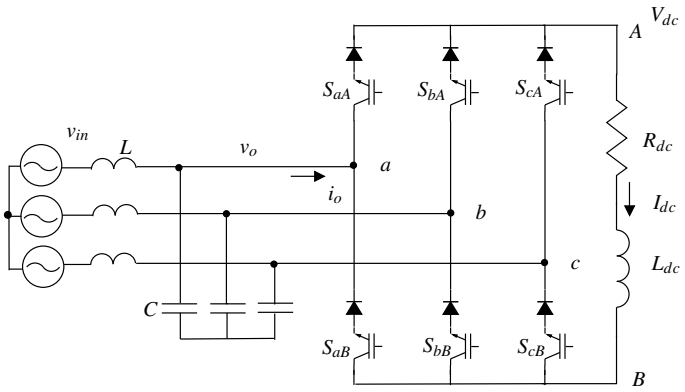

Figure 1. Circuit diagram

short circuit between the phases) and at least one switch has to be ON (to avoid open circuit of inductive dc side current). In order to satisfy the second condition the duty ratios of the switches S_{aA}, S_{bA}, S_{cA}, S_{aB}, S_{bB}, S_{cB} should satisfy (2). The first condition is met by placing the pulses according to Fig. 2.

$$d_{ai} + d_{bi} + d_{ci} = 1 \qquad i \in [A,B] \tag{2}$$

Four offset duty cycles D_a, D_b, D_c and Δ are defined as in equation (3) and (4). These duty cycles are added to fundamental component of the duty cycle (for example $m\cos\omega t$ for d_{aA}) in order to satisfy (2) and keep the final duty cycles between 0 and 1. Here m is the modulation index and can have a maximum value of 0.5.

$$\begin{aligned} D_a &= 0.5|\cos\omega t| \\ D_b &= 0.5\left|\cos\left(\omega t - \frac{2\pi}{3}\right)\right| \\ D_c &= 0.5\left|\cos\left(\omega t + \frac{2\pi}{3}\right)\right| \end{aligned} \tag{3}$$

$$\Delta = \frac{1-(D_a+D_b+D_c)}{2}$$

The duty ratios for the array of switches S_{aA}, S_{bA}, S_{cA} and of S_{aB}, S_{bB}, S_{cB} are given in (4) and (5) respectively.

$$\begin{aligned} d_{aA} &= m\cos\omega t + D_a + \Delta \\ d_{bA} &= m\cos\left(\omega t - \frac{2\pi}{3}\right) + D_b \\ d_{cA} &= m\cos\left(\omega t + \frac{2\pi}{3}\right) + D_c + \Delta \end{aligned} \tag{4}$$

$$\begin{aligned} d_{aB} &= -m\cos\omega t + D_a + \Delta \\ d_{bB} &= -m\cos\left(\omega t - \frac{2\pi}{3}\right) + D_b \\ d_{cB} &= -m\cos\left(\omega t + \frac{2\pi}{3}\right) + D_c + \Delta \end{aligned} \tag{5}$$

Fig. 2 shows the pulse generation for switches S_{aA}, S_{bA}, S_{cA}. A triangular carrier of frequency $f_s = \frac{1}{T_s}$ is used to generate the switching signals.

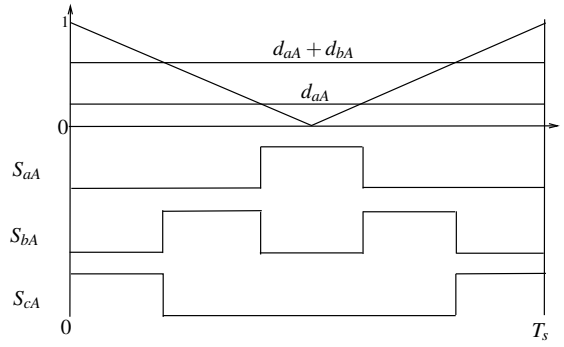

Figure 2. Pulse Generation

The average voltages produced by the two array of switches S_{aA}, S_{bA}, S_{cA} and of S_{aB}, S_{bB}, S_{cB} at A and B in Fig. 1. are given by

$$v_i = d_{ai}v_{oa} + d_{bi}v_{ob} + d_{ci}v_{oc} \qquad i \in [A,B] \tag{6}$$

Therefore, the DC link voltage, or the dc component V_{AB} is given by

$$V_{dc} = v_A - v_B = 3mV_o \tag{7}$$

Fundamental component of the current produced at the input side of CSI is given by

$$\begin{aligned} i_{oa_1} &= (d_{aA} - d_{aB})I_{dc} \\ &= 2mI_{dc}\cos\omega t \\ &= I_o\cos\omega t \end{aligned} \tag{8}$$

where I_o is the peak of fundamental component of current. Note that this results in input power factor correction i.e. the voltage v_{oa} and i_{oa1} are in the same phase.

2.2. Modelling of CSI for Filter design

The dc component of the V_{AB} voltage at steady state is given by (10), where I_{dc} is the dc component of the current in the dc side.

$$V_{dc} = R_{dc}I_{dc} \tag{9}$$

From equation (1) and (9), it is seen that v_{oa} and i_{oa1} are in phase. Therefore, for the fundamental components, the CSI can be modeled as a resistance R as defined below.

$$R = \frac{V_o}{I_o} = \frac{R_{dc}}{6m^2} \tag{10}$$

In this analysis it is assumed that the input current, i_{oa}, to the CSI has two components, first the fundamental frequency component i_{0a_1} and second the switching frequency component $i_{o_{SW}}$. All other components are neglected as they are negligible. Fig. 3 shows the instantaneous i_{oa} current over a switching cycle i.e. the k^{th} cycle. The pattern may change from cycle to cycle but the current will always have an amplitude of I_{dc} and will be flowing for $T_s 2m|\cos\omega(kT_s)|$ amount of time. So the RMS of this current over a switching cycle is given by (12). Provided $T_s << T$, the RMS of the input current over a fundamental cycle ($T = \frac{2\pi}{\omega}$) is given by (13). Using (12) and (13) we get an expression for the RMS value of the input current, (14).

$$I^2_{o_{RMS}}(kT_s) = I^2_{dc}2m|\cos\omega(kT_s)| \tag{11}$$

$$I^2_{o_{RMS}} = \frac{1}{T}\sum I^2_{o_{RMS}}(kT_s)T_s \tag{12}$$

$$I^2_{o_{RMS}} = \frac{4I^2_{dc}m}{\pi} \tag{13}$$

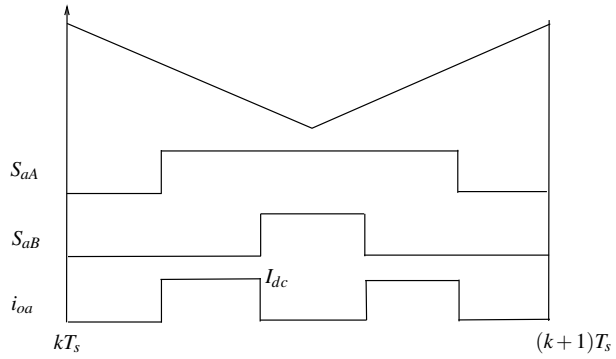

Figure 3. i_{oa} waveform over a switching cycle

The rms value of the switching frequency component of current $I_{o_{SWRMS}}$ is then given by the difference of rms values of total current and the fundamental current.

$$I^2_{o_{SWRMS}} = I^2_{o_{RMS}} - \frac{I^2_o}{2} \tag{14}$$

Solving (9) and (14), the expression for $I_{o_{SWRMS}}$ is obtained as

$$I^2_{o_{SWRMS}} = 2m\left(\frac{2}{\pi} - m\right)I^2_{dc} \tag{15}$$

3. FILTER DESIGN

The equivalent circuit at fundamental frequency after replacing CSI with resistance R is shown in Fig. 4.

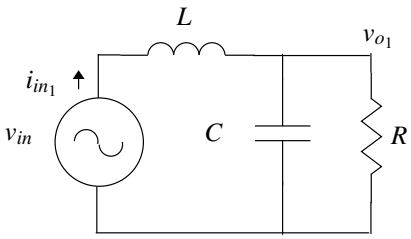

Figure 4. Per-phase equivalent circuit at fundamental frequency

After analyzing this circuit assuming sinusoidal steady state the phase difference between voltage v_{in} and current i_{in_1} is given by (17) and the relation between peak values of voltage v_{in} and v_{o_1} is given by equation (18). The filter design should be such that the angle θ representing the input power factor must be as small as possible and the ratio of $\frac{V_o}{V_{in}}$ must be close to unity.

$$\theta = \tan^{-1}\omega CR - \tan^{-1}\frac{\omega L}{R(1-\omega^2 LC)} \tag{16}$$

$$\frac{V_o}{V_{in}} = \frac{R}{\sqrt{\omega^2 L^2 - R^2(1-\omega^2 LC)^2}} \tag{17}$$

The equivalent circuit for the switching frequency component is given by Fig. 5.

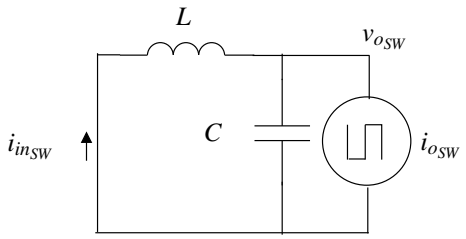

Figure 5. Per-phase equivalent circuit at switching frequency

After analysing this circuit it is possible to express the amount of RMS switching frequency ripple present in the voltage at the input of CSI (19) and current ripple present in the input grid current (20) in terms of the ripple current present in the input of the CSI.

$$V_{o_{SWRMS}} = \frac{I_{o_{SWRMS}}}{C\omega_s|1-\frac{1}{\omega_s^2 LC}|} \tag{18}$$

And the expression for switching component of capacitor current is obtained as

$$I_{in_{SWRMS}} = \frac{I_{o_{SWRMS}}}{|1-\omega_s^2 LC|} \tag{19}$$

The filter design procedure is explained as follows. The THD (total harmonic distortion) of the input grid current is given as a specification. With the knowledge of the input grid voltage amplitude V_{in} and the total amount of power for which the converter is designed for, we can get an estimate of i_{in_1}, assuming the input power factor is nearly unity. From this it is possible to obtain a specification of maximum allowable $I_{in_{SWRMS}}$. Note that $V_{o_{SWRMS}}$ must be small compared to its fundamental component V_o. Otherwise it will not be possible to do the modulation. The allowable RMS ripple in v_o as a percentage of V_{in} (as it is very close to V_o) is decided at the beginning of the design. This consideration results in a specification of $V_{o_{SWRMS}}$. Equations (19) and (20) are then solved to obtain the values of L and C. Then the effective value of the angle θ and the ratio of $\frac{V_o}{V_{in}}$ are checked using (17) and (18) respectively.

Table 1. Parameters

L_{dc}	4 mH
R_{dc}	8Ω
L	4 mH
C	75 μF
V_i	$100\sqrt{2}$V
$f_s = \frac{1}{T_s}$	5kHz
ω	$2\pi 60$
m	0.5

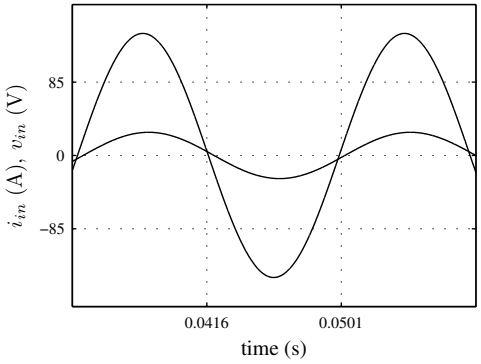

Figure 6. Simulation results: Grid voltage and current

4. SIMULATION

A CSI with the modulation strategy explained in section II is simulated in MATLAB/SIMULINK environment with the parameters shown in Table I. The values of L and C are decided such that $V_{o_{SWRMS}} = 4.12V$ and $I_{in_{SWRMS}} = 33mA$. The simulation results are shown in Fig. 6, 7, 8 and is summarized in Table II. Fig. 6 shows simulated supply voltage and supply current. Its evident that the input grid current is almost in phase with the grid voltage and more or less free of the ripple current and appears to be sinusoidal. Frequency spectrum of i_{in} confirms this observation. It turns out that in simulation the RMS ripple current present is around $31mA$ as shown in Table II. Fig. 7 shows the input voltage and current of the CSI. The frequency spectrums of these signals are shown in Fig. 8. Its clear that i_o has a considerable amount of switching frequency component. From Table II our analytical estimation for $I_{o_{SWRMS}}$ closely matches with simulation. Also the filter ensures that the ripple component of the voltage v_o is very small.

Table II shows a comparison between values of differ-

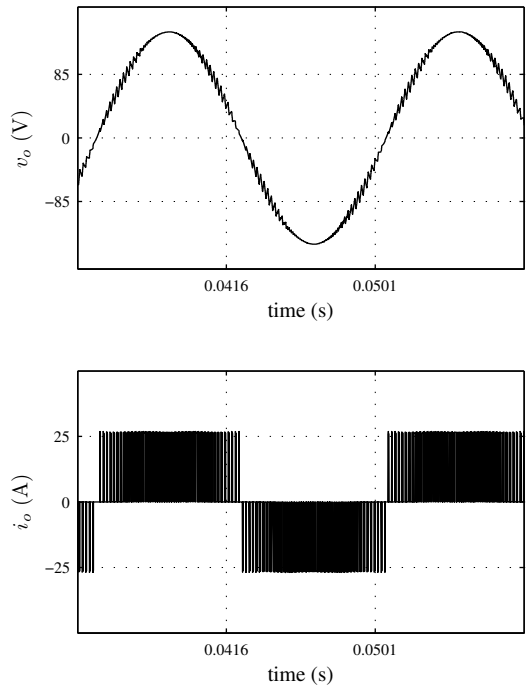

Figure 7. Simulation results: Input voltage and current

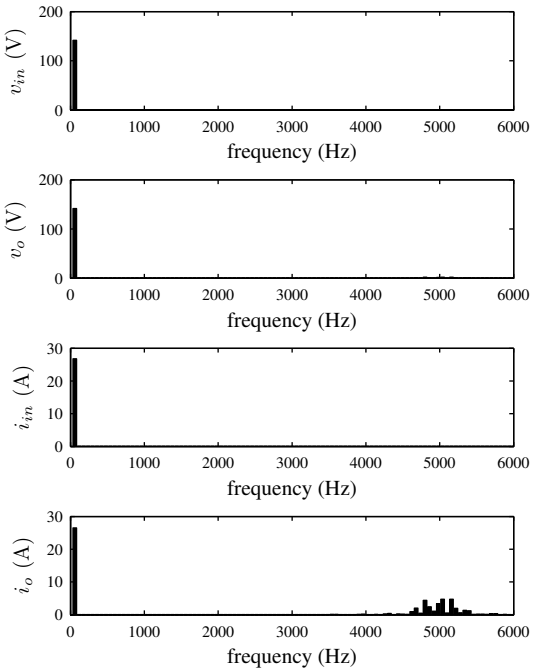

Figure 8. Simulation results: Frequency spectrum

Table 2. Simulation Results : A Comparison

VARIABLES	ANALYTICAL	SIMULATED
V_{dc}	212.50V	212.02V
I_{dc}	26.56A	26.53A
I_o	26.56A	26.48A
$I_{o_{RMS}}$	21.19A	21.14A
$I_{o_{SWRMS}}$	9.81A	9.82A
V_o	141.67V	141.63V
$V_{o_{SWRMS}}$	4.18V	3.12V
$I_{in_{SWRMS}}$	33mA	31mA
θ	-7.87^o	-8.64^o

ent variables obtained from analysis performed in section II and from the simulation. It can be seen that the values obtained from analysis very closely match with those obtained from simulation. Thus, the analysis provided in section II and filter design method explained in section III are verified.

5. CONCLUSION

A design procedure for the input filter required to filter out the switching component of the currents present in the input line currents of a current source inverter or a front end voltage source rectifier has been presented in this paper. The design is based on the specification of the THD of the input grid or supply current and the allowable ripple voltage at the input of the converter. This design procedure needs an accurate estimation of the ripple component present in the input line currents. This paper provides a analytical method to estimate this ripple. The design also ensures high input power factor and low voltage drop in the filter. A detailed simulation of the entire system confirms the analytical estimation of the input current ripple of the CSI and the proposed design. The design procedure developed in this paper is applicable to many other converters including the matrix converter.

REFERENCES

[1] G. Moschopoulos, G. Joos, and P. Ziogas, "Input characteristics of variable modulation current source inverters," in *Industrial Electronics, Control and Instrumentation, 1991. Proceedings. IECON 91., 1991*

International Conference on, 1991.

[2] Y. W. Li, ”Control and resonance damping of voltage-source and current- source converters with lc filters,”*Industrial Electronics, IEEE Transac- tions on,* vol. 56, no. 5, pp. 1511 -1521, May 2009.

[3] F. Filsecker, R. A andlvarez, and S. Bernet, ”Design and losses of pwm current source converters,” in *Industrial Technology (ICIT), 2010 IEEE International Conference on*, 2010, pp. 737 -744.

[4] G. Moschopoulos, G. Joos, and P. Ziogas, ”Input characteristics of variable modulation index controlled current source inverters,” *Industrial Electronics, IEEE Transactions on*, vol. 41, no. 2, pp. 216 -223, Apr. 1994.

[5] A. Maswood, ”A current source inverter with sinusoidal pwm switch- ing analysis, modeling and performance,” in *Energy Management and Power Delivery, 1998. Proceedings of EMPD ’98. 1998 International Conference on*, vol. 2, Mar. 1998, pp. 527 -531 vol.2.

[6] K. Basu, A. Umarikar, K. Mohapatra, and N. Mohan, ”High-frequency transformer-link three-level inverter drive with common-mode voltage elimination,” in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE,* June 2008, pp. 4413-4418.