High−Frequency Transformer−Link Three−Level Inverter Drive with Common−Mode Voltage Elimination

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***Abstract*—This paper proposes a novel topology along with a switching strategy for AC/AC conversion with a high frequency transformer link. The input side converter is a three phase to single phase direct link matrix converter switched with a simple triangle comparison based novel PWM strategy and provides input power factor correction. This PWM technique also helps to eliminate the effect of the pulsating DC bus seen by the output inverter. The high frequency transformer provides flexible voltage transfer ratio along with galvanic isolation and has much reduced size compared to the bulky line frequency transformer. The centre tapped secondary of the transformer along with a single phase rectifier provide the required voltage levels for a three level inverter. This inverter is operated as a two level inverter in order to eliminate common mode voltages at its output. A novel variable slope carrier is used for this inverter in order to nullify the effect of fluctuating DC bus. The major advantages of this scheme are a) elimination of DC bus capacitor, b) low neutral point fluctuation, c) isolation, d) input power factor correction e) flexible voltage transfer ratio and f) high power density. The proposed configuration is simulated and simulation results are presented, which verifies the operation.**

I. Introduction

In conventional adjustable speed AC drives with ßex− ible voltage transfer ratio, there is a front end recti Þer often with input power factor correction followed by a large electrolytic DC link capacitor. Then there is an inverter followed by a bulky low frequency transformer. In order to avoid the DC link capacitor and the bulky transformer, use of high frequency electronic transformer [1] [2] along with indirect matrix converter topologies has been proposed in literature [3]. In [3], a three phase to single phase direct link matrix converter has been connected to a high frequency transformer followed by a single phase recti Þer and two level voltage source inverter. This is similar to the topology proposed in this paper except in output there is a three level inverter. In this paper a novel and simple triangle comparison based PWM technique [4] is used for the front end converter that operates in synchronism with the output three level inverter in order to eliminate the effect of pulsating DC bus without any current control in a rotating reference frame [5].

Common mode voltage switching is a substantial prob− lem in high power motor drives driven by PWM inverters. Various strategies have been proposed to eliminate or to reduce this problem [6] [7] [8]. One of them is to operate a three level inverter as a two level inverter [9]. However with three level inverters, the problems like DC bus capacitor unbalance and large DC bus capacitor requirements are substantial when power and voltage ratings becomes higher. The method of common mode elimination using a three level inverter without using a DC bus capacitor is proposed in this paper. This is achieved by using a direct link matrix converter and a centered tapped high frequency transformer. The major advantages of this scheme are elimination of DC bus capacitor, isolation, ßexible voltage transfer ratio, common mode voltage elimination, high power density and inherent input power factor correction.

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II. Analysis

A. PWM Strategy for the Front End Converter

The front end converter as in Þgure (1), Þrst converts the three phase input AC voltage at the line frequency to DC by creating a virtual DC link. This is called the recti Þcation stage [10]. In the following inversion stage, it converts the virtual DC to a high frequency AC which is fed to the transformer. A three phase low frequency AC is converted into a high frequency single phase AC. This converter is basically a direct link matrix converter with a conventional recti Þcation stage followed by a single phase inverter instead of a three phase one. The line currents are also shaped to be in phase with the input voltage.

The PWM signals for the front end converter are generated using a simple triangle comparison method [4]. As the input three phases are connected to voltage sources they can not be shorted at any instant of time. Due to the inductive nature of load the output phases can not be opened. Let S_{aA} be the switching state of the switch between the input a phase and output A phase and d_{aA} be its duty ratio. S_{aA} is 0 when it is off and 1 when it is on. The above mentioned conditions translate into the fact that S_{aA}, S_{bA} and S_{cA} can not be simultaneously 1 (any

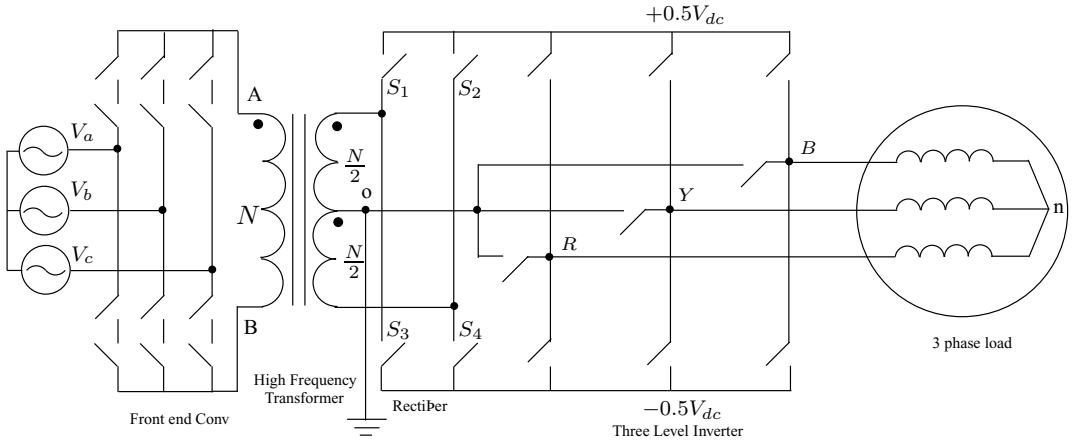

Fig. 1. Circuit diagram of the high frequency AC link

two of them or all of them). Also they can not be 0 all at a time. Figure (2) shows how the reference voltage signals are compared with a triangular carrier signal in order to meet the above mentioned requirements. The signal S_{bA} is obtained by XOR ing the signals obtained by comparing the triangular carrier with d_{aA} and $(d_{aA} + d_{bA})$.

The above requirements also implies equation (1). Another restriction on duty ratios is given by equation (2).

$$\begin{aligned} d_{aA} + d_{bA} + d_{cA} &= 1 \\ d_{aB} + d_{bB} + d_{cB} &= 1 \end{aligned} \tag{1}$$

Let us assume that input is a three phase balanced sinusoidal voltage source with peak magnitude V_i and angular frequency ω_i, equation (3).

$$\begin{aligned} 0 \leq d_{aA}, d_{bA}, d_{cA} \leq 1 \\ 0 \leq d_{aB}, d_{bB}, d_{cB} \leq 1 \end{aligned} \tag{2}$$

$$\begin{aligned} v_a(t) &= V_i \cos \omega_i t \\ v_b(t) &= V_i \cos\left(\omega_i t - \frac{2\pi}{3}\right) \\ v_c(t) &= V_i \cos\left(\omega_i t + \frac{2\pi}{3}\right) \end{aligned} \tag{3}$$

The virtual DC link voltage at the output phase A, $v_A(t)$ is synthesized on an average over a subcycle period T_s from $v_a(t)$, $v_b(t)$ and $v_c(t)$. The average voltage in the two output phases can be obtained from the equation (4).

$$\begin{aligned} v_A(t) = d_{aA} v_a + d_{bA} v_b + d_{cA} v_c \\ v_B(t) = d_{aB} v_a + d_{bB} v_b + d_{cB} v_c \end{aligned} \tag{4}$$

The choice of d_{aA} as $K_A(t) \cos \omega_i t$ and phase shifted versions of the same for d_{bA} and d_{cA} will generate an average voltage of $\frac{3}{2} K_A(t) V_i$ in phase A over a subcycle, equation (4). In order to satisfy equation (2) it is required to add a common mode component in each of these duty ratios. $D_a(t) = 0.5|\cos \omega_i(t)|$ is added in d_{aA} and d_{aB}. Similarly phase shifted versions of $D_a(t)$ is added to the corresponding duty ratios of phase b and c, equation (5). The common mode voltage generated due to this gets cancelled in the line to line voltage of V_{AB}, which is the input to the primary of the high frequency transformer. In order to maintain equation (1), it is required to inject another set of common mode duty ratios Δ_a, Δ_b and Δ_c corresponding to the phases a, b and c, equation (6). After the inversion, the high frequency AC applied to the transformer primary has three distinct levels over a subcycle. This results in a variable DC bus for the output side three level inverter. A variable slope carrier is used to average out this effect. This particular choice of common mode duty ratios is made in order to generate such a carrier for the output converter.

$$\begin{aligned} D_a(t) &= 0.5|\cos \omega_i t| \\ D_b(t) &= 0.5\left|\cos\left(\omega_i t - \frac{2\pi}{3}\right)\right| \\ D_c(t) &= 0.5\left|\cos\left(\omega_i t + \frac{2\pi}{3}\right)\right| \end{aligned} \tag{5}$$

$$\begin{aligned} \Delta_a(t) &= \frac{1 - (D_a + D_b + D_c)}{2} \\ \Delta_b(t) &= 0 \\ \Delta_c(t) &= \frac{1 - (D_a + D_b + D_c)}{2} \end{aligned} \tag{6}$$

Finally with all of these considerations, the duty ratios of all of the six switches in the front end converter are given by equations (7) and (8). This choice of duty ratios leads to an average line to line voltage, v_{AB}, over a subcycle as given by the equation (9).

$$\begin{aligned} d_{aA}(t) &= K_A(t) \cos \omega_i t + D_a + \Delta_a \\ d_{bA}(t) &= K_A(t) \cos\left(\omega_i t - \frac{2\pi}{3}\right) + D_b + \Delta_b \\ d_{cA}(t) &= K_A(t) \cos\left(\omega_i t + \frac{2\pi}{3}\right) + D_c + \Delta_c \end{aligned} \tag{7}$$

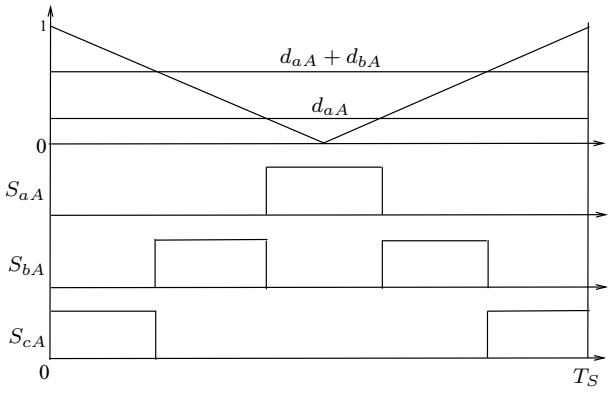

Fig. 2. Front end converter PWM generation

$$\begin{aligned} d_{aB}(t) &= K_B(t)\cos\omega_i t + D_a + \Delta_a \\ d_{bB}(t) &= K_B(t)\cos\left(\omega_i t - \frac{2\pi}{3}\right) + D_b + \Delta_b \\ d_{cB}(t) &= K_B(t)\cos\left(\omega_i t + \frac{2\pi}{3}\right) + D_c + \Delta_c \quad (8) \end{aligned}$$

$$v_{AB}(t) = \frac{3}{2}V_i\left[K_A(t) - K_B(t)\right] \quad (9)$$

In order to achieve the inverter operation, $K_A(t)$ is always chosen to be equal to the negative of $K_B(t)$ equation (10) and $K_A(t)$ is given by the equation (11). K_i is called the modulation index of the input converter and it is set to its maximum value equal to 0.5. This implies that the average line to line input voltage to the transformer primary is a square wave with amplitude $3K_iV_i$.

$$K_A(t) = -K_B(t) \quad (10)$$

$$K_A(t) = \begin{cases} +K_i & \text{for } (n-1)T_s \le t < nT_s \\ -K_i & \text{for } nT_s \le t < (n+1)T_s \end{cases} \quad (11)$$

This pulse width modulation strategy also ensures that the input line currents are in phase with the input voltage. Assuming a continuous power ßow the average current in the transformer primary is also a square wave with an amplitude I_1. The average input line current in phase a is given in equation (12) and it is in phase with the input voltage v_a. All the six switches of the front end three phase to single phase matrix converter need to be four quadrant.

$$\begin{aligned} i_a &= (S_{aA} - S_{aB})i_{AB} \\ &= 2K_iI_1\cos\omega_i t \quad (12) \end{aligned}$$

B. Isolation and Rectification

Transformer changes the voltage level of the high frequency input voltage and provides isolation. As shown in Þgure (1), the midpoint of the secondary winding is taken as the secondary ground. Other two ends of the secondary winding are connected to a single phase rectiÞer. A three level voltage source inverter is used to synthesize the three phase sinusoidal output voltage at a desired frequency and amplitude. The midpoint of the secondary winding and the two outputs of the rectiÞer provide the three voltage levels for the output inverter. The rectiÞer is synchronized with the input converter. Switches S_1 and S_4 are closed during the subcycle interval when $K_A(t)$ is K_i. In the next interval when $K_A(t)$ is $-K_i$, S_2 and S_3 is switched on.

In this analysis the turns ratio of the transformer is taken as one. An approximate equivalent circuit of one of the halves of the secondary winding is shown in Þgure (3). Let r_1 be the resistance and l_1 be the leakage inductance of the primary winding. Similarly r_2 and l_2 represent the same quantities for one half of the secondary winding. The equivalent leakage impedance turns out to be $r_e = \frac{r_1}{2} + r_2$ and $l_e = \frac{l_1}{2} + l_2$. In this analysis the effect of magnetising inductance is neglected and the currents in the two halves of the secondary winding is assumed to be equal and opposite from the symmetry arguments. Assuming the rectiÞer and the output three level inverter to be ideal and the three phase load to be inductive in nature, the load in this equivalent circuit can be represented as a pulsating current source. Due to the presence of leakage inductance it is not possible to connect the secondary directly to the switching load and a voltage port has to be created. This can be done with a capacitor that is placed at the output of the secondary winding. Presence of considerable amount of leakage inductance causes the output to be oscillatory and poorly damped and that in turn leads to a reduction in switching frequency. To provide considerable damping a resistance is put in parallel to the capacitor. This leads to a constant power loss. An active loss less solution to this problem needs to be worked out. Also in the design of the transformer it is very important to keep the leakage inductance to be at its minimum otherwise it will lead to the reduction in switching frequency and increase in the transformer size.

C. PWM strategy for the output inverter

A three level inverter produces 27 vectors as shown in the Þgure (4). Each of these vectors are denoted by a switching state. For example when voltage vector V_1 is applied the switching state is $(+0-)$. The output R phase is connected to the positive DC bus, $+0.5V_{dc}$, Y phase is shorted to the ground and B phase is connected to $-0.5V_{dc}$, Þgure (1). Out of these only six active vectors

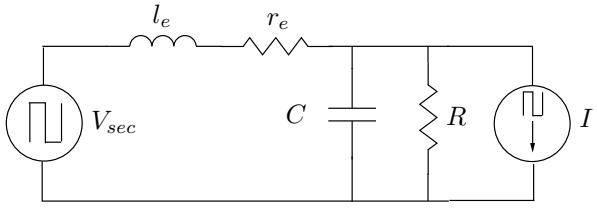

Fig. 3. Equivalent circuit of the transformer secondary

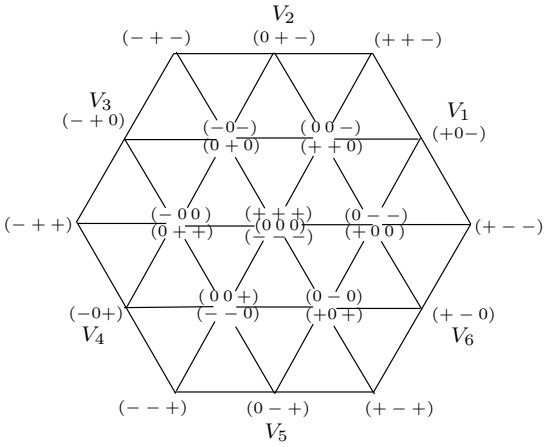

Fig. 4. Voltage vectors produced by a three level inverter

are used. These vectors are denoted by V_1 to V_6. The sum of the pole voltages are instantaneously zero when these vectors are employed. This leads to a complete elimination of common mode voltages from the output load terminals. The inverter is operated as a two level inverter with all of these six vectors . Only one zero vector is used that is when all the phases are connected to the ground as it ensures zero common mode voltage. The average DC bus voltage V_{dc} available is $3K_iV_i$. Use of above mentioned vectors leads to an effective DC bus of $\frac{\sqrt{3}}{2}V_{dc}$. This results in an under utilization of the DC bus. The modulation index K_o of the three level inverter is deÞned as the ratio of the magnitude of the synthesized output voltage vector to that of the available DC bus. The maximum limit of K_o is $\frac{\sqrt{3}}{2}$. So the peak value of the output phase voltage is given by the equation (13).

$$V_o = \sqrt{3}K_iK_oV_i \tag{13}$$

As mentioned earlier the modulation index of the front end converter is set to its maximum value of 0.5. This leads to a three level voltage waveform in a subcycle, in the transformer primary as shown in Þgure (5). One of the level is zero. Even though the average voltage remains $3K_iV_i$, the DC bus voltage for the output three level inverter is pulsating in nature. This will lead to a distortion in the fundamental component of the output voltage. In order to solve this problem a variable slope carrier is used to generate the duty ratios for the output inverter as indicated in the Þgure (5). This carrier is generated with the help of two control signals as shown in Þgure (6) and given by the equation (14). These two signals when multiplied with the subcycle time period T_s give the time periods of the two different non zero voltage levels present in the DC bus voltage waveform. The variable slope carrier ensures an average effective DC bus voltage of $3K_iV_i$.

$$\begin{aligned} u_1(t) &= \min\{D_a, D_b, D_c\} \\ u_2(t) &= \max\{D_a, D_b, D_c\} - u_1(t) \end{aligned} \tag{14}$$

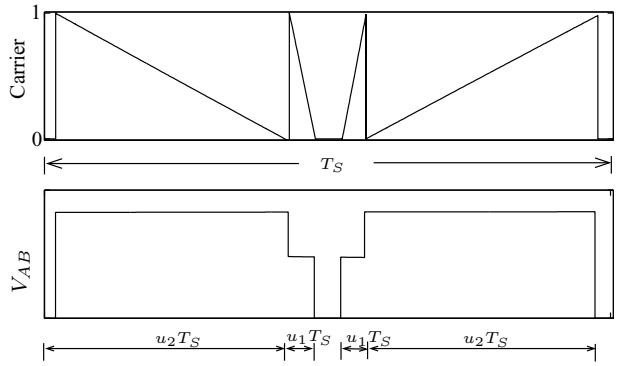

Fig. 5. Variable slope carrier and primary voltage over a subcycle

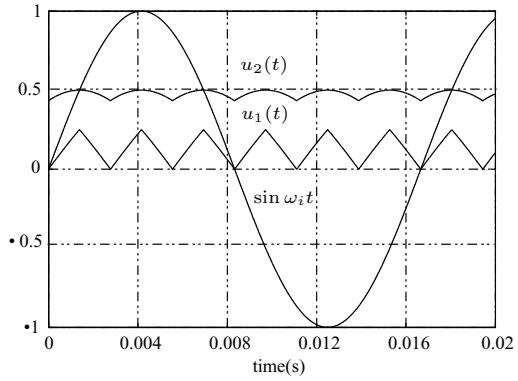

Fig. 6. Control Signals

D. Simulation results

The proposed topology has been simulated in SABER. The PWM switching signals are generated in MATLAB SIMULINK and fed into the SABER model through COSIM. The input is a three phase balanced AC voltage with peak magnitude, V_i, of 120 volts at a frequency of 60 Hz. The output is connected to a three phase balanced R−L load. The transformer parameters are given in the table (I). R_c and L_m are the core loss resistance and the magnetizing inductance as seen from the transformer primary. The frequency of the AC voltage applied to the transformer is chosen to be 2.5 kHz. As mentioned earlier K_i is set to 0.5 and the modulation index of the output inverter, K_o is chosen to be 0.8. Output voltage is generated at a frequency of 60 Hz. According to the equation (13) the peak of the output voltage is 83.14 volts resulting in a line current of 40 A peak. The Þgure (7) shows the simulated output current waveform with a peak slightly less than its analytically predicted value. This is due to the voltage drop in transformer windings. As the load is balanced and its neutral point is isolated. the voltage V_{no} gives the common mode voltage present in the pole voltages of the three level inverter. Figure (8) gives the simulated V_{no} voltage waveform. Figure (9) presents the the simulated positive DC bus voltage at the input to the output inverter. Because of the presence of leakage impedance there are spikes in the DC link voltage waveform. This also shows up in the common mode voltage waveform. The simulated input current

TABLE I
PARAMETERS

L_{load}	$3.3mH$
R_{load}	1.66Ω
l_1	$10\mu H$
r_1	$10m\Omega$
l_2	$5\mu H$
r_2	$5m\Omega$
L_m	$1mH$
R_c	100Ω

waveform (filtered) is shown in figure (10) along with the input voltage. It clearly indicates the input power factor correction.

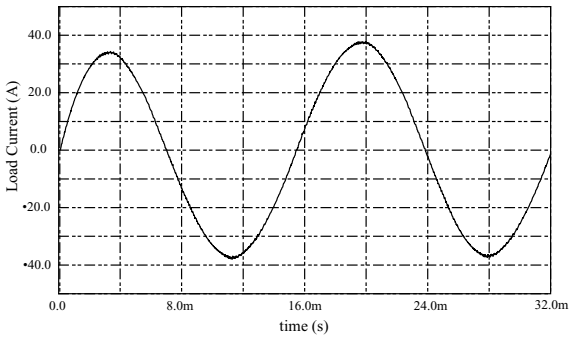

Fig. 7. Simulation result: output load current

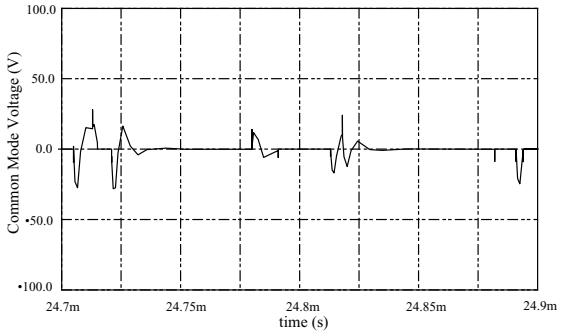

Fig. 8. Simulation result: common mode voltage

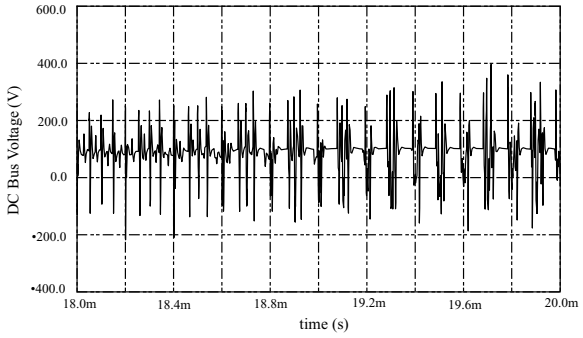

Fig. 9. Simulation result: positive DC link voltage

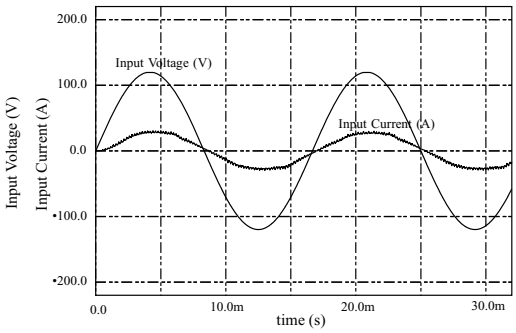

Fig. 10. Simulation result: input line current

III. CONCLUSION

A novel AC/AC converter topology along with a simple control scheme has been proposed in this paper. In this proposed configuration the front end converter is a three phase to single phase direct link matrix converter with input power factor correction. It is controlled with a simple triangle comparison based PWM technique that converts the line frequency AC to a high frequency AC applied to a high frequency reduced size transformer. The transformer provides a flexible voltage transfer ratio along with galvanic isolation. Its centre tapped secondary along with a single phase rectifier provides three voltage levels for the output inverter. The output three level inverter is operated as a two level inverter in order to provide common mode voltage elimination at the load terminals. This leads to an under utilization of the available DC bus. A variable slope carrier synchronized with the input converter is used to generate switching signals for the three level inverter. This mitigates the effect of pulsating DC bus without employing any current controller. This topology achieves high power density due to the high frequency AC link in comparison with conventional DC link systems. Important advantages of the proposed configuration are elimination of DC bus capacitor, isolation, flexible voltage transfer ratio, common mode voltage elimination and inherent input power factor correction. The disadvantage of this scheme are more number of switches and under utilization of DC bus. The entire system has been simulated and the simulation results confirm the principle of operation of the proposed topology.

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